2A Integrated Hot Swap Controller

FEATURES

- **Small Footprint**
- **33mΩ MOSFET with R_{SENSE}**
- **Wide Operating Voltage Range: 2.9V to 26.5V**
- **Adjustable, 5% Accurate Current Limit**
- Current and Temperature Monitor Outputs
- Overtemperature Protection
- Adjustable Current Limit Timer Before Fault
- Power Good and Fault Outputs
- Adjustable Inrush Current Control
- 2% Accurate Undervoltage and Overvoltage Protection
- Pin Compatible with LTC4232 (DFN Package Only)
- Available in 20-Lead TSSOP and 16-Lead 5mm × 3mm DFN Packages

APPLICATIONS

- RAID Systems, Solid State Drives
- Server I/O Cards
- Industrial

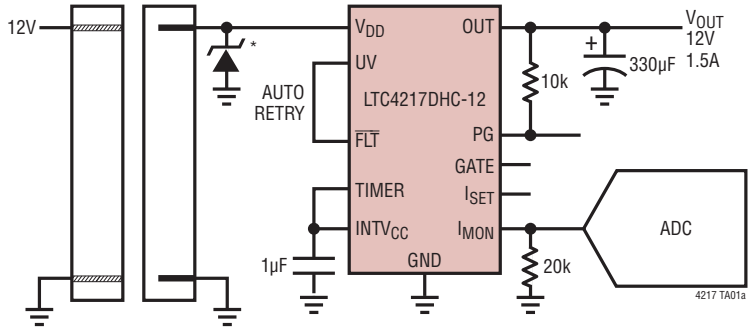
DESCRIPTION

The LTC®4217 is an integrated solution for Hot Swap applications that allows a board to be safely inserted and removed from a live backplane. The part integrates a Hot Swap controller, power MOSFET and current sense resistor in a single package for small form factor applications. A dedicated 12V version (LTC4217-12) contains preset 12V specific thresholds, while the standard LTC4217 allows adjustable thresholds.

The LTC4217 provides separate inrush current control and a 5% accurate 2A current limit with foldback current limiting. The current limit threshold can be adjusted dynamically using an external pin. Additional features include a current monitor output that amplifies the sense resistor voltage for ground referenced current sensing and a MOSFET temperature monitor output. Thermal limit, overvoltage, undervoltage and power good monitoring are also provided. For a 5A pin compatible version, see LTC4232.

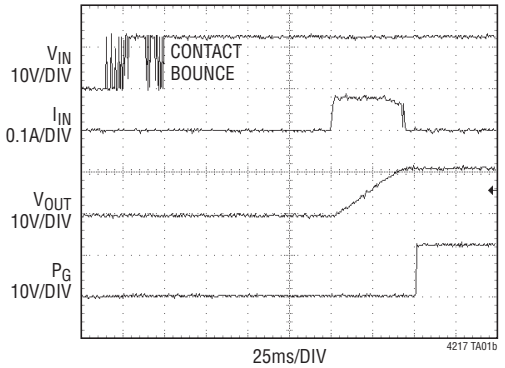
TYPICAL APPLICATION

12V, 1.5A Card Resident Application with Auto-Retry



* TVS: DIODES INC. SMAJ17A

Power-Up Waveforms



ABSOLUTE MAXIMUM RATINGS

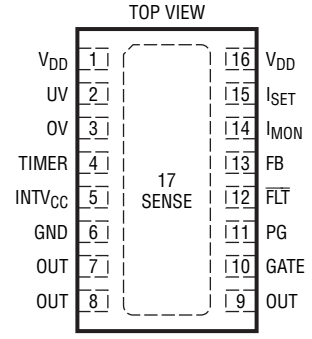
(Notes 1, 2)

Supply Voltage (V_{DD}) ..... –0.3V to 28V
Input Voltages
  FB, OV, UV ..... –0.3V to 12V
  TIMER ..... –0.3V to 3.5V
  SENSE ..... V_{DD} – 10V or – 0.3V to V_{DD}
Output Voltages
  I_{SET}, I_{MON} ..... –0.3V to 3V
  PG, $\overline{FLT}$ ..... –0.3V to 35V
  OUT ..... –0.3V to V_{DD} + 0.3V
  $INTV_{CC}$ ..... –0.3V to 3.5V
  GATE (Note 3) ..... –0.3V to 33V

Operating Ambient Temperature Range
  LTC4217C ..... 0°C to 70°C
  LTC4217I ..... –40°C to 85°C
  LTC4217H ..... –40°C to 125°C
Junction Temperature (Notes 4, 5) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  FE Package Only ..... 300°C

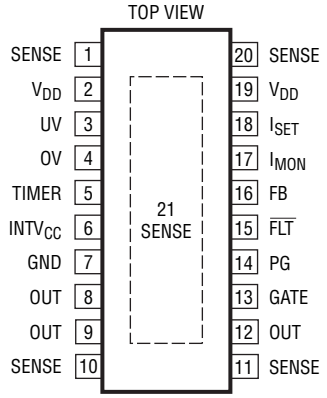
PIN CONFIGURATION

LTC4217
LTC4217-12



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS SENSE,
θ_{JA} = 43°C/W SOLDERED, OTHERWISE θ_{JA} = 140°C/W

LTC4217



FE PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS SENSE,
θ_{JA} = 38°C/W SOLDERED, OTHERWISE θ_{JA} = 130°C/W

ORDER INFORMATION (http://www.linear.com/product/LTC4217#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4217CDHC-12#PBF	LTC4217CDHC-12#TRPBF	421712	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC4217IDHC-12#PBF	LTC4217IDHC-12#TRPBF	421712	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4217CDHC#PBF	LTC4217CDHC#TRPBF	4217	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC4217IDHC#PBF	LTC4217IDHC#TRPBF	4217	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4217CFE#PBF	LTC4217CFE#TRPBF	LTC4217FE	20-Lead Plastic TSSOP	0°C to 70°C
LTC4217IFE#PBF	LTC4217IFE#TRPBF	LTC4217FE	20-Lead Plastic TSSOP	–40°C to 85°C
LTC4217HFE#PBF	LTC4217HFE#TRPBF	LTC4217FE	20-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
V_{DD}	Input Supply Range		●	2.9		26.5	V
I_{DD}	Input Supply Current	MOSFET On, No Load	●		1.6	3	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.65	2.73	2.85	V
$V_{DD(UVTH)}$	Input Supply Undervoltage Threshold	LTC4217-12, V_{DD} Rising	●	9.6	9.88	10.2	V
$\Delta V_{DD(UVHYST)}$	Input Supply Undervoltage Hysteresis	LTC4217-12	●	520	640	760	mV
$V_{DD(OVTH)}$	Input Supply Overvoltage Threshold	LTC4217-12, V_{DD} Rising	●	14.7	15.05	15.4	V
$\Delta V_{DD(OVHYST)}$	Input Supply Overvoltage Hysteresis	LTC4217-12	●	183	244	305	mV
$V_{OUT(PGTH)}$	Output Power Good Threshold	LTC4217-12, V_{OUT} Rising	●	10.2	10.5	10.8	V
$\Delta V_{OUT(PGHYST)}$	Output Power Good Hysteresis	LTC4217-12	●	127	170	213	mV
I_{OUT}	OUT Leakage Current	V_{OUT} = V_{GATE} = 0V, V_{DD} = 26.5V	●		0	±150	µA
		V_{OUT} = V_{GATE} = 12V, LTC4217	●	1	2	4	µA
		V_{OUT} = V_{GATE} = 12V, LTC4217-12	●	50	70	90	µA
		V_{OUT} = V_{GATE} = 12V, LTC4217H	●	1	2	6	µA
dV_{GATE}/dt	GATE Pin Turn-On Ramp Rate		●	0.15	0.3	0.55	V/ms
R_{ON}	MOSFET + Sense Resistor On-Resistance	C-Grade, I-Grade	●	15	33	50	mΩ
		H-Grade	●	15	33	60	mΩ
$I_{LIM(TH)}$	Current Limit Threshold	V_{FB} = 1.23V		1.9	2	2.1	A
		V_{FB} = 1.23V	●	1.85	2	2.15	A
		V_{FB} = 0V	●	0.35	0.5	0.7	A
		V_{FB} = 1.23V, R_{SET} = 20kΩ	●	0.85	1	1.17	A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Inputs							
I_{IN}	OV, UV, FB Input Current	V = 1.2V, LTC4217	●		0	±1	µA
R_{IN}	OV, UV, FB Input Resistance	LTC4217-12	●	13	18	23	kΩ
V_{TH}	OV, UV, FB Threshold Voltage	V_{PIN} Rising	●	1.21	1.235	1.26	V
$\Delta V_{OV(HYST)}$	OV Hysteresis		●	10	20	30	mV
$\Delta V_{UV(HYST)}$	UV Hysteresis		●	50	80	110	mV
$V_{UV(RTH)}$	UV Reset Threshold Voltage	V_{UV} Falling	●	0.55	0.62	0.7	V
$\Delta V_{FB(HYST)}$	FB Power Good Hysteresis		●	10	20	30	mV
R_{ISET}	I_{SET} Internal Resistor		●	19	20	21	kΩ
Outputs							
V_{OL}	PG, $\overline{FLT}$ Pin Output Low Voltage	I_{SINK} = 2mA C-Grade, I-Grade H-Grade	 ● ●		 0.4 0.4	 0.8 0.92	 V V
I_{OH}	PG, $\overline{FLT}$ Pin Input Leakage Current	30V	●		0	±10	µA
$V_{TIMER(H)}$	TIMER Pin High Threshold	V_{TIMER} Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Pin Low Threshold	V_{TIMER} Falling	●	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current	V_{TIMER} = 0V	●	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pin Pull-Down Current	V_{TIMER} = 1.2V	●	1.4	2	2.6	µA
$I_{TIMER(RATIO)}$	TIMER Pin Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	1.6	2	2.7	%
A_{IMON}	I_{MON} Pin Current Gain	I_{OUT} = 2A	●	47.5	50	52.5	µA/A
BW_{IMON}	I_{MON} Bandwidth				250		kHz
$I_{OFF(IMON)}$	I_{MON} Pin Offset Current	I_{OUT} = 132mA	●		0	±7.5	µA
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, $V_{GATE} = V_{OUT}$ = 12V	●	–19	–24	–29	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	Gate Drive Off, V_{GATE} = 18V, V_{OUT} = 12V C-Grade, I-Grade H-Grade	 ● ●	 190 164	 250 140	 400 500	 µA µA
$I_{GATE(FST)}$	Gate Fast Pull-Down Current	Fast Turn Off, V_{GATE} = 18V, V_{OUT} = 12V			140		mA
AC Characteristics							
$t_{PHL(GATE)}$	Input High (OV), Input Low (UV) to Gate Low Propagation Delay	V_{GATE} < 16.5V Falling	●		8	10	µs
$t_{PHL(ILIM)}$	Short-Circuit to Gate Low	V_{FB} = 0, Step I_{SENSE} to 1.2A, V_{GATE} < 16.5V Falling	●		1	5	µs
$t_{D(ON)}$	Turn-On Delay	Step V_{UV} to 2V, V_{GATE} > 13V	●	50	100	150	ms
$t_{D(FAULT)}$	UV Low to Clear Fault Latch Delay				1		µs
$t_{D(CB)}$	Circuit Breaker Filter Delay Time (Internal)	V_{FB} = 0V, Step I_{SENSE} to 1.2A C-Grade, I-Grade H-Grade	 ● ●	 1.5 1.4	 2 2	 2.7 2.7	 ms ms
$t_{D(AUTO-RETRY)}$	Auto-Retry Turn-On Delay (Internal)		●	50	100	150	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a maximum of 6.5V above OUT. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the formula:

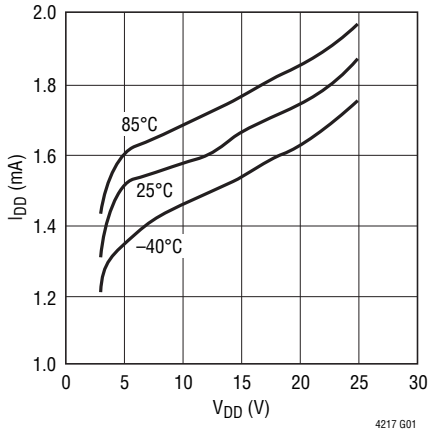
LTC4217DHC, LTC4217DHC-12: $T_J = T_A + (P_D \bullet 43°C/W)$

LTC4217FE: $T_J = T_A + (P_D \bullet 38°C/W)$

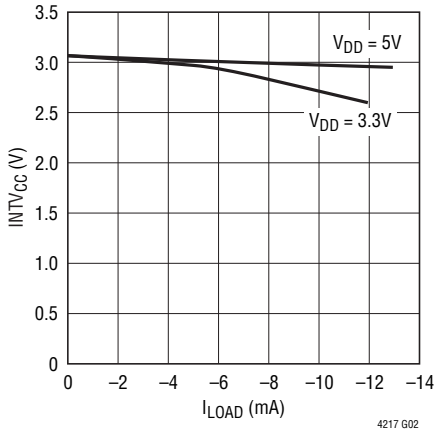
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

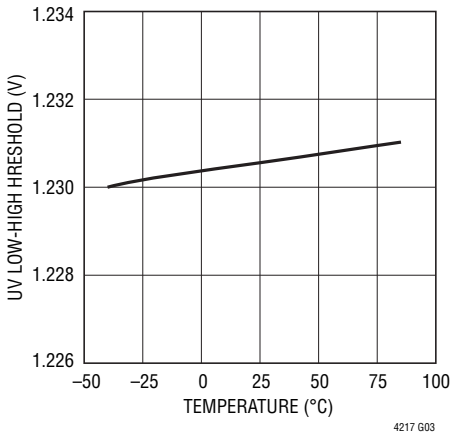
I_{DD} vs V_{DD}



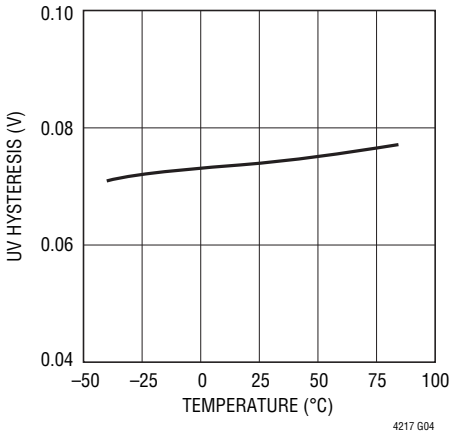
$INTV_{CC}$ Load Regulation



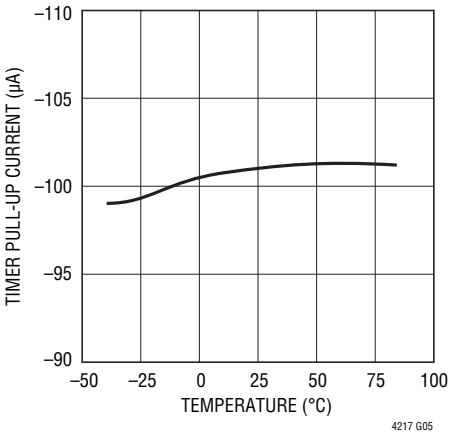
UV Low-High Threshold vs Temperature



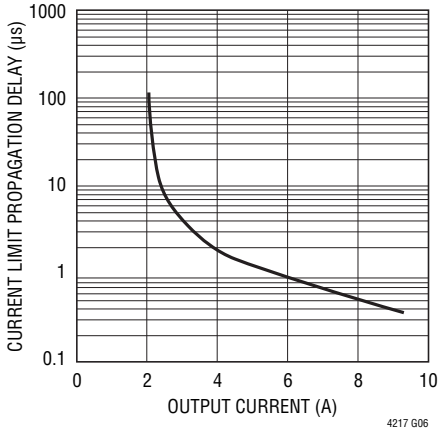
UV Hysteresis vs Temperature



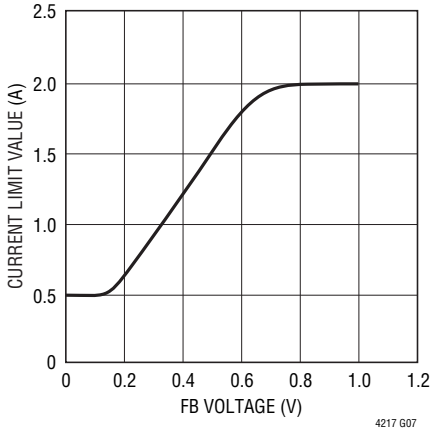
Timer Pull-Up Current vs Temperature



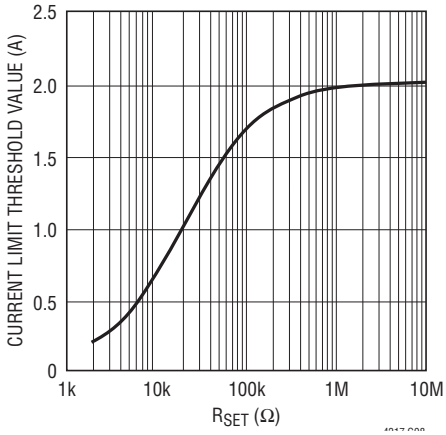
Current Limit Delay ($t_{PHL(ILIM)}$ vs Overdrive)



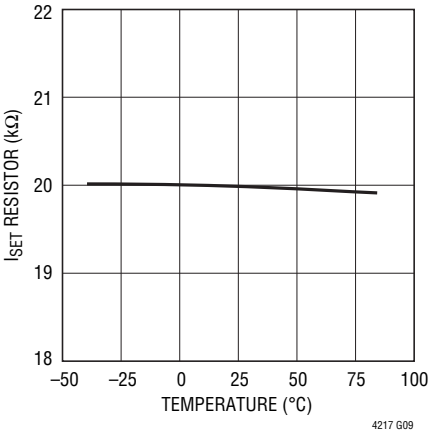
Current Limit Threshold Foldback



Current Limit Adjustment (I_{OUT} vs R_{SET})

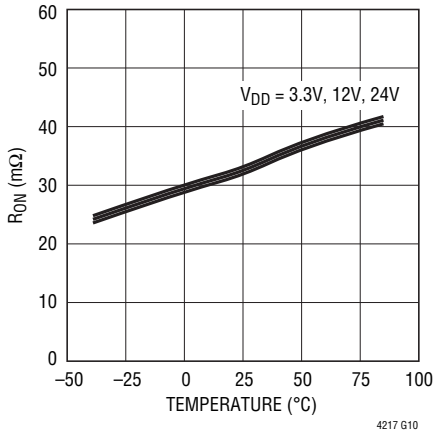


Internal I_{SET} Resistor (R_{ISET})

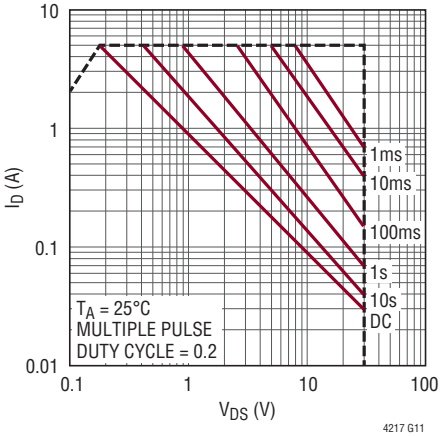


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = 12V unless otherwise noted.

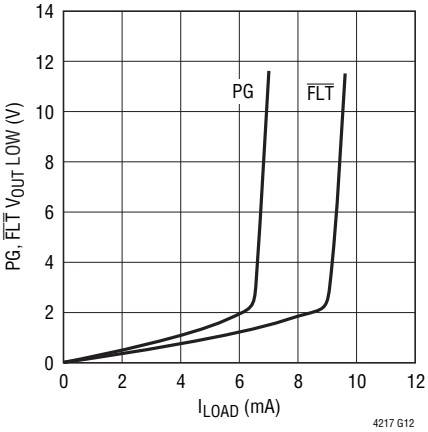
R_{ON} vs V_{DD} and Temperature



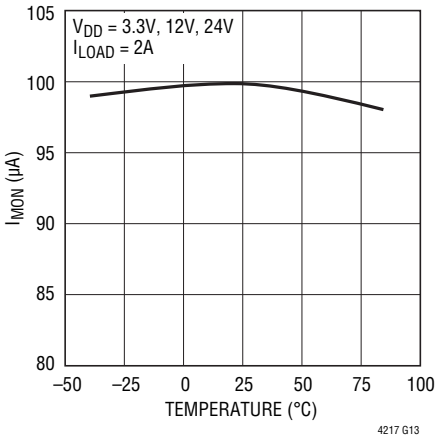
MOSFET SOA Curve



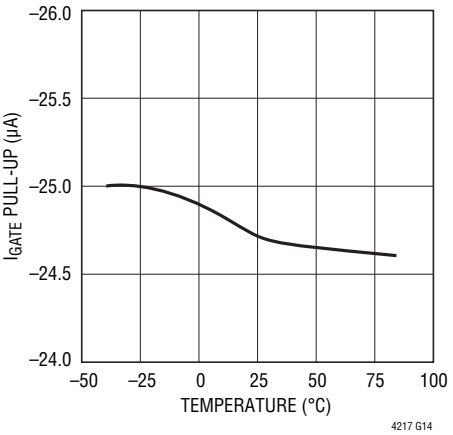
PG, $\overline{FLT}$ V_{OUT} Low vs I_{LOAD}



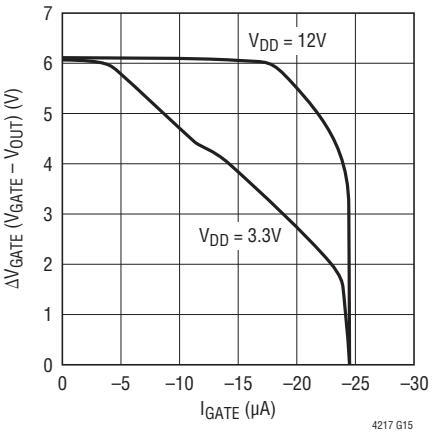
I_{MON} vs Temperature and V_{DD}



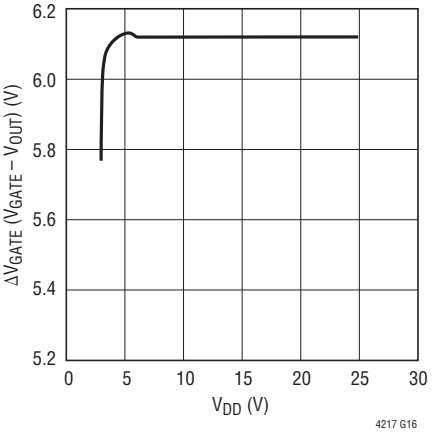
GATE Pull-Up Current vs Temperature



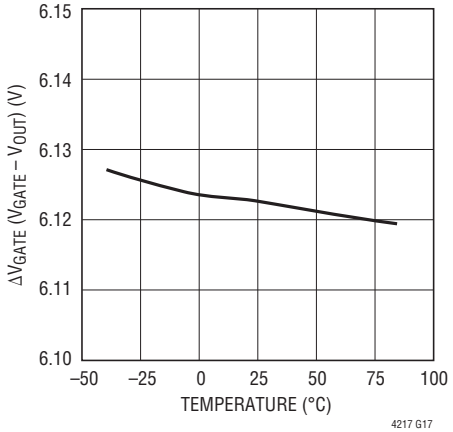
Gate Drive vs Gate Pull-Up Current



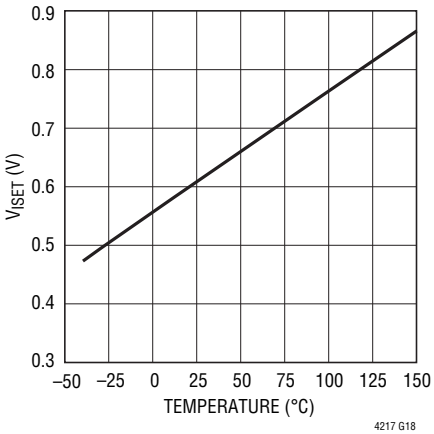
Gate Drive vs V_{DD}



Gate Drive vs Temperature



V_{ISET} vs Temperature



PIN FUNCTIONS

FB: Foldback and Power Good Input. Connect this pin to an external resistive divider from OUT for the LTC4217 (adjustable) version. The LTC4217-12 version uses a fixed internal divider with optional external adjustment. Open the pin if the LTC4217-12 thresholds for 12V operation are desired. If the voltage falls below 0.6V, the current limit is reduced using a foldback profile (see the Typical Performance Characteristics section). If the voltage falls below 1.21V, the PG pin will pull low to indicate the power is bad.

$\overline{FLT}$: Overcurrent Fault Indicator. Open-drain output pulls low when an overcurrent fault has occurred and the circuit breaker trips. For overcurrent auto-retry tie to UV pin (see the Applications Information section for details).

GATE: Gate Drive for Internal N-channel MOSFET. An internal 24µA current source charges the gate of the N-channel MOSFET. At start-up the GATE pin ramps up at a 0.3V/ms rate determined by internal circuitry. During an undervoltage or overvoltage condition a 250µA pull-down current turns the MOSFET off. During a short-circuit or undervoltage lockout condition, a 140mA pull-down current source between GATE and OUT is activated.

GND: Device Ground.

I_{MON}: Current Monitor Output. The current in the internal MOSFET switch is divided by 20,000 and sourced from this pin. Placing a 20k resistor from this pin to GND creates a 0V to 2V voltage swing when current ranges from 0A to 2A.

$INTV_{CC}$: Internal 3.1V Supply Decoupling Output. This pin must have a 1µF or larger bypass capacitor. Overloading this pin can disrupt internal operation.

I_{SET}: Current Limit Adjustment Pin. For a 2A current limit value open this pin. This pin is driven by a 20k resistor in series with a voltage source. The pin voltage is used to generate the current limit threshold. The internal 20k resistor (R_{ISET})) and an external resistor (R_{SET}) between I_{SET} and ground create an attenuator that lowers the current limit value. Due to circuit tolerance R_{SET} should not be less than 2k. In order to match the temperature variation of the sense resistor, the voltage on this pin increases at the same rate as the sense resistance increases. Therefore the voltage at I_{SET} pin is made proportional to temperature of the MOSFET switch.

OUT: Output of Internal MOSFET Switch. Connect this pin directly to the load. In the LTC4217-12 version, the PG comparator monitors an internal resistive divider between the OUT pin and GND.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD} for the LTC4217 (adjustable) version. The LTC4217-12 version uses a fixed internal divider with optional external adjustment for 12V operation. Open the pin if the LTC4217-12 thresholds are desired. If the voltage at this pin rises above 1.235V, an overvoltage is detected and the switch turns off. Tie to GND if unused.

PG: Power Good Indicator. Open-drain output pulls low when the FB pin drops below 1.21V indicating the power is bad. If the FB pin rises above 1.23V and the GATE to OUT voltage exceeds 4.2V, the open-drain pull-down releases the PG pin to go high.

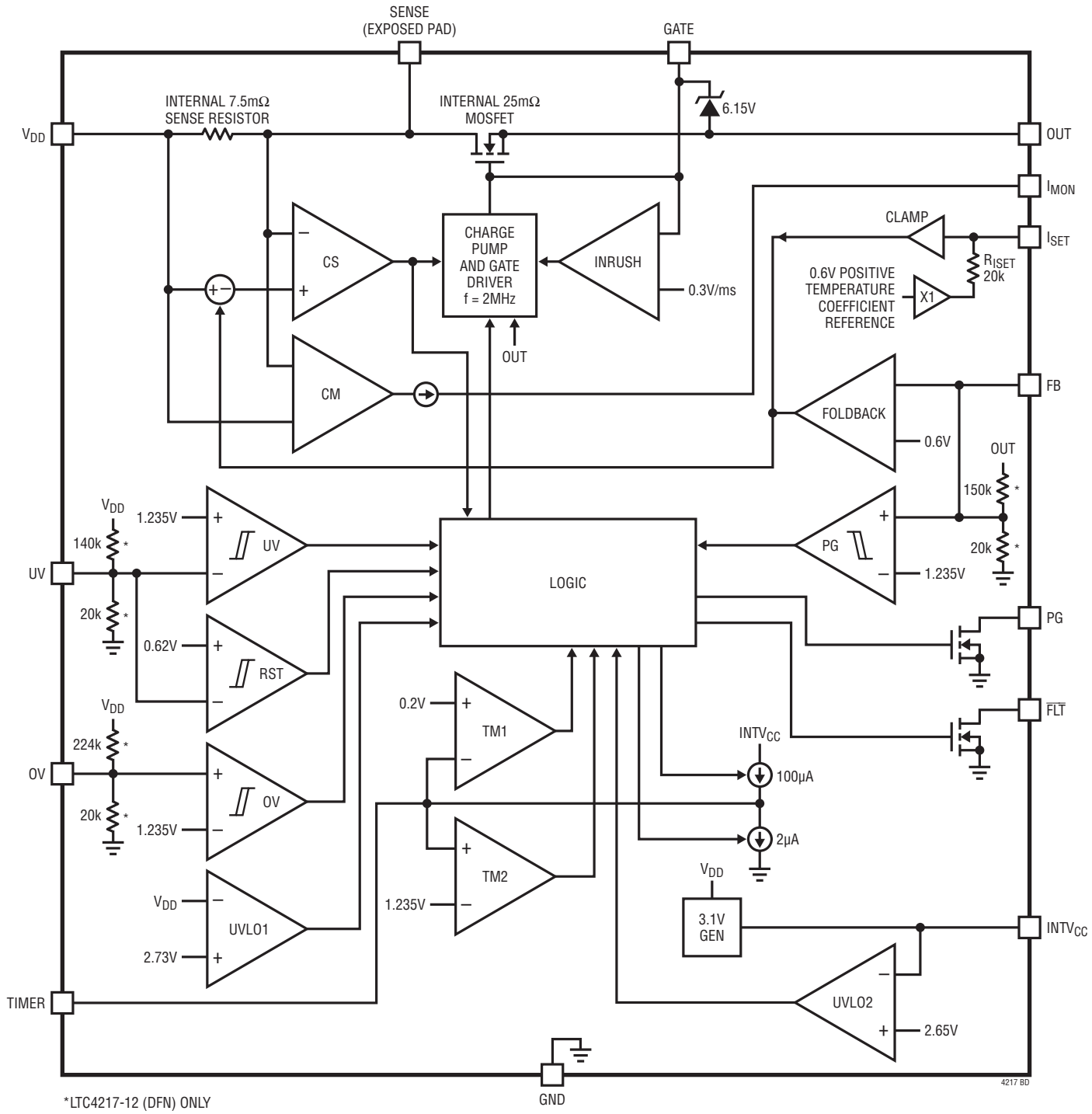
SENSE: Current Sense Node and MOSFET Drain. The current limit circuit controls the GATE pin to limit the sense voltage between the V_{DD} and SENSE pins to 15mV (2A) or less depending on the voltage at the FB pin. The exposed pad on DHC and FE packages are connected to SENSE and must be soldered to an electrically isolated printed circuit board trace to properly transfer the heat out of the package.

TIMER: Timer Input. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the switch is turned off. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following a cooldown time of 518ms/µF duration. Tie this pin to $INTV_{CC}$ for a fixed 2ms overcurrent delay and 100ms auto-retry time.

UV: Undervoltage Comparator Input. Tie high if unused. Connect this pin to an external resistive divider from V_{DD} for the LTC4217 (adjustable) version. The LTC4217-12 version drives the UV pin with an internal resistive divider from V_{DD}. Open the pin if the preset LTC4217-12 thresholds for 12V operation are desired. If the UV pin voltage falls below 1.15V, an undervoltage is detected and the switch turns off. Pulling this pin below 0.62V resets the overcurrent fault and allows the switch to turn back on (see the Applications Information section for details). If overcurrent auto-retry is desired then tie this pin to the $\overline{FLT}$ pin.

V_{DD}: Supply Voltage and Current Sense Input. This pin has an undervoltage lockout threshold of 2.73V.

FUNCTIONAL DIAGRAM



OPERATION

The Functional Diagram displays the main circuits of the device. The LTC4217 is designed to turn a board's supply voltage on and off in a controlled manner allowing the board to be safely inserted and removed from a live backplane. The LTC4217 includes a 25mΩ MOSFET and a 7.5mΩ current sense resistor. During normal operation, the charge pump and gate driver turn on the pass MOSFET's gate to provide power to the load. The inrush current control is accomplished by the INRUSH circuit. This circuit limits the GATE ramp rate to 0.3V/ms and hence controls the voltage ramp rate of the output capacitor.

The current sense (CS) amplifier monitors the load current using the voltage sensed across the current sense resistor. The CS amplifier limits the current in the load by reducing the GATE-to-OUT voltage in an active control loop. It is simple to adjust the current limit threshold using the current limit adjustment (I_{SET}) pin. This allows a different threshold during other times such as start-up.

A short circuit on the output to ground causes significant power dissipation during active current limiting. To limit this power, the foldback amplifier reduces the current limit value from 2A to 0.5A in a linear manner as the FB pin drops below 0.6V (see the Typical Performance Characteristics section).

If an overcurrent condition persists, the TIMER pin ramps up with a 100µA current source until the pin voltage exceeds 1.235V (comparator TM2). This indicates to the logic that it is time to turn off the pass MOSFET to prevent overheating. At this point the TIMER pin ramps down using the 2µA current source until the voltage drops below 0.21V (Comparator TM1) which tells the logic to start an internal 100ms timer. At this point, the pass transistor has cooled and it is safe to turn it on again. It is suitable for many applications to use an internal 2ms overcurrent timer with a 100ms cooldown period. Tying the TIMER pin to $INTV_{CC}$ sets this default timing. Latchoff is the normal operating condition following overcurrent turnoff. Retry is initiated by pulling the UV pin low for a minimum of 1µs then high. Auto retry is implemented by tying the $\overline{FLT}$ to the UV pin.

The fixed 12V version, LTC4217-12, uses two separate internal dividers from V_{DD} to drive the UV and OV pins. This version also features a divider from OUT to drive the FB pin. The LTC4217-12 is available in a DFN package while the LTC4217 (adjustable version) is in a DFN and TSSOP packages.

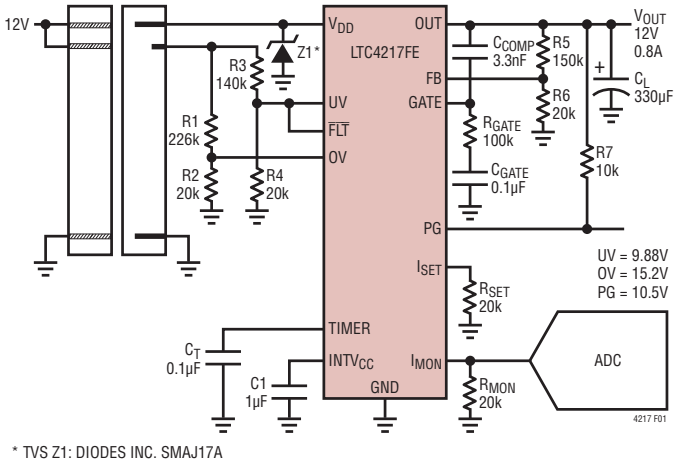
The output voltage is monitored using the FB pin and the PG comparator to determine if the power is available for the load. The power good condition is signaled by the PG pin using an open-drain pull-down transistor.

The Functional Diagram also shows the monitoring blocks of the LTC4217. The two comparators on the left side include the UV and OV comparators. These comparators determine if the external conditions are valid prior to turning on the MOSFET. But first the undervoltage lockout circuits UVLO1 and UVLO2 must validate the input supply and the internally generated 3.1V supply ($INTV_{CC}$) and generate the power up initialization to the logic circuits. If the external conditions remain valid for 100ms the MOSFET is allowed to turn on.

Other features include MOSFET current and temperature monitoring. The current monitor (CM) outputs a current proportional to the sense resistor current. This current can drive an external resistor or other circuits for monitoring purposes. A voltage proportional to the MOSFET temperature is output to the I_{SET} pin. The MOSFET is protected by a thermal shutdown circuit.

APPLICATIONS INFORMATION

The typical LTC4217 application is in a high availability system that uses a positive voltage supply to distribute power to individual cards. A complete application circuit is shown in Figure 1. External component selection is discussed in detail in the following sections.



* TVS Z1: DIODES INC. SMAJ17A

Figure 1. 0.8A, 12V Card Resident Application

Turn-On Sequence

Several conditions must be present before the internal pass MOSFET can be turned on. First the supply V_{DD} must exceed its undervoltage lockout level. Next the internally generated supply $INTV_{CC}$ must cross its 2.65V undervoltage threshold. This generates a 25µs power-on-reset pulse which clears the fault register and initializes internal latches.

After the power-on-reset pulse, the LTC4217 will go through the following sequence. First, the UV and OV pins must indicate that the input voltage is within the acceptable range. All of these conditions must be satisfied for the duration of 100ms to ensure that any contact bounce during the insertion has ended.

The MOSFET is turned on by charging up the GATE with a charge pump generated 24µA current source whose value is adjusted by shunting a portion of the pull-up current to ground. The charging current is controlled by the INRUSH circuit that maintains a constant slope of GATE voltage versus time (Figure 2). The voltage at the GATE pin rises with a slope of 0.3[V/ms] and the supply inrush current is set at:

$$I_{INRUSH} = C_L \bullet 0.3[V/ms]$$

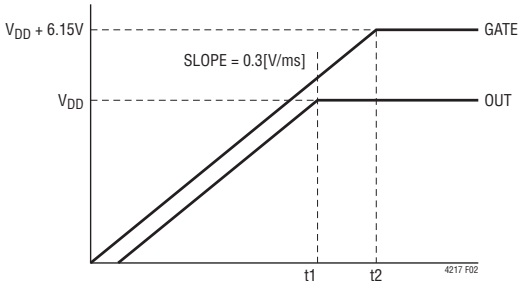


Figure 2. Supply Turn-On

This gate slope is designed to charge up a 1000µF capacitor to 12V in 40ms, with an inrush current of 300mA. This allows the inrush current to stay under the current limit threshold (500mA) for capacitors less than 1000µF. Included in the Typical Performance Characteristics section is a graph of the Safe Operating Area for the MOSFET. It is evident from this graph that the power dissipation at 12V, 300mA for 40ms is in the safe region.

Adding the R_{GATE}, C_{GATE}, and C_{COMP} network on the GATE pin will lower the inrush current below the default value set by the INRUSH circuit. The GATE is charged with an 24µA current source (when INRUSH circuit is not driving the GATE). The voltage at the GATE pin rises with a slope equal to $24\mu A/C_{GATE}$ and the supply inrush current is set at:

$$I_{INRUSH} = \frac{C_L}{C_{GATE}} \bullet 24\mu A$$

When the GATE voltage reaches the MOSFET threshold voltage, the switch begins to turn on and the OUT voltage follows the GATE voltage as it increases. Once OUT reaches V_{DD}, the GATE will ramp up until clamped by the 6.15V Zener between GATE and OUT.

APPLICATIONS INFORMATION

As the OUT voltage rises, so will the FB pin which is monitoring it. Once the FB pin crosses its 1.235V threshold and the GATE to OUT voltage exceeds 4.2V, the PG pin will cease to pull low and indicate that the power is good.

Parasitic MOSFET Oscillation

When the N-channel MOSFET ramps up the output during power-up it operates as a source follower. The source follower configuration may self-oscillate in the range of 25kHz to 300kHz when the load capacitance is less than 10µF, especially if the wiring inductance from the supply to the V_{DD} pin is greater than 3µH. The possibility of oscillation will increase as the load current (during power-up) increases. There are two ways to prevent this type of oscillation. The simplest way is to avoid load capacitances below 10µF. For wiring inductance larger than 20µH, the minimum load capacitance may extend to 100µF. A second choice is to connect an external gate capacitor C_P >1.5nF as shown in Figure 3.

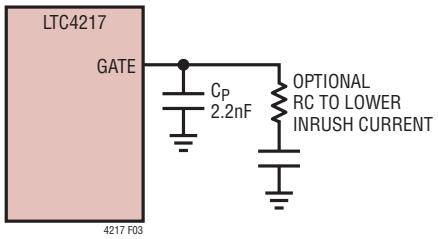


Figure 3. Compensation for Small C_{LOAD}

Turn-Off Sequence

The switch can be turned off by a variety of conditions. A normal turn-off is initiated by the UV pin going below its 1.235V threshold. Additionally, several fault conditions will turn off the switch. These include an input overvoltage (OV pin), overcurrent circuit breaker (SENSE pin) or over temperature. Normally the switch is turned off with a 250µA current pulling down the GATE pin to ground. With the switch turned off, the OUT voltage drops which pulls the FB pin below its threshold. PG then pulls low to indicate output power is no longer good.

If V_{DD} drops below 2.65V for greater than 5µs or $INTV_{CC}$ drops below 2.5V for greater than 1µs, a fast shutdown of the switch is initiated. The GATE is pulled down with a 170mA current to the OUT pin.

Overcurrent Fault

The LTC4217 features an adjustable current limit with foldback that protects against short-circuits and excessive load current. To prevent excessive power dissipation in the switch during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin. A graph in the Typical Performance Characteristics curves shows the Current Limit Threshold Foldback.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the timeout delay set by the TIMER. Current limiting begins when the MOSFET current reaches 0.5A to 2A (depending on the foldback). The GATE pin is then brought down with a 140mA GATE-to-OUT current. The voltage on the GATE is regulated in order to limit the current to less than 2A. At this point, a circuit breaker time delay starts by charging the external timing capacitor with a 100µA pull-up current from the TIMER pin. If the TIMER pin reaches its 1.235V threshold, the internal switch turns off (with a 250µA current from GATE to ground). Included in the Typical Performance Characteristics curves is a graph of the Safe Operating Area for the MOSFET. From this graph one can determine the MOSFET's maximum time in current limit for a given output power.

Tying the TIMER pin to $INTV_{CC}$ will force the part to use the internally generated (circuit breaker) delay of 2ms. In either case the $\overline{FLT}$ pin is pulled low to indicate an overcurrent fault has turned off the pass MOSFET. For a given circuit breaker time delay, the equation for setting the timing capacitor's value is as follows:

$$C_T = t_{CB} \bullet 0.083[\mu F/ms]$$

After the switch is turned off, the TIMER pin begins discharging the timing capacitor with a 2µA pull-down current.

APPLICATIONS INFORMATION

When the TIMER pin reaches its 0.21V threshold, an internal 100ms timer is started. After the 100ms delay, the switch is allowed to turn on again if the overcurrent fault latch has been cleared. Bringing the UV pin below 0.6V for a minimum of 1µs and then high will clear the fault latch. If the TIMER pin is tied to $INTV_{CC}$ then the switch is allowed to turn on again (after an internal 100ms delay), if the overcurrent fault latch is cleared.

Tying the $\overline{FLT}$ pin to the UV pin allows the part to self-clear the fault and turn the MOSFET on as soon as TIMER pin has ramped below 0.21V. In this auto-retry mode the LTC4217 repeatedly tries to turn on after an overcurrent at a period determined by the capacitor on the TIMER pin. The auto-retry mode also functions when the TIMER pin is tied to $INTV_{CC}$.

The waveform in Figure 4 shows how the output latches off following a short-circuit. The current in the MOSFET is 0.5A as the timer ramps up.

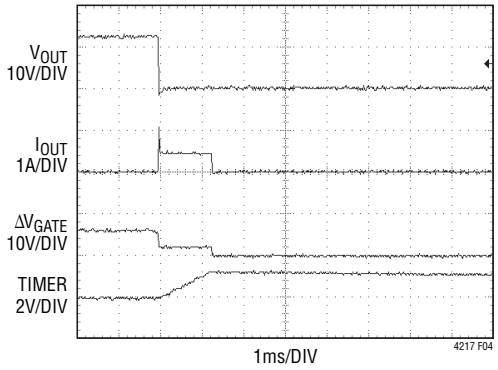


Figure 4. Short-Circuit Waveform

Current Limit Adjustment

The default value of the active current limit is 2A. The current limit threshold can be adjusted lower by placing a resistor between the I_{SET} pin and ground. As shown in the Functional Block Diagram the voltage at the I_{SET} pin (via the clamp circuit) sets the CS amplifier's built-in offset voltage. This offset voltage directly determines the active current limit value. With the I_{SET} pin open, the voltage at the I_{SET} pin is determined by a positive temperature coefficient reference. This voltage is set to 0.618V at room temperature which corresponds to a 2A current limit at room temperature.

An external R_{SET} resistor placed between the I_{SET} pin and ground forms a resistive divider with the internal 20k R_{ISET} sourcing resistor. The divider acts to lower the voltage at the I_{SET} pin and therefore lower the current limit threshold. The overall current limit threshold precision is reduced to ±16% when using a 20k resistor to halve the threshold.

Using a switch (connected to ground) in series with R_{SET} allows the active current limit to change only when the switch is closed. This feature can be used to program a reduced running current while the maximum current limit is used at start-up.

Monitor MOSFET Temperature

The voltage at the I_{SET} pin increases linearly with increasing temperature. The temperature profile of the I_{SET} pin is shown in the Typical Performance Characteristics section. Using a comparator or ADC to measure the I_{SET} voltage provides an indicator of the MOSFET temperature.

The I_{SET} voltage follows the formula:

$$V_{ISET} = \frac{R_{SET}}{R_{SET} + R_{ISET}} \bullet (T + 273°C) \bullet 2.093[mV/°C]$$

The MOSFET temperature is calculated using R_{ISET} of 20k.

$$T = \frac{(R_{SET} + 20k) \bullet V_{ISET}}{R_{SET} \bullet 2.093[mV/°C]} - 273°C$$

when R_{SET} is not present, T becomes:

$$T = \frac{V_{ISET}}{2.093[mV/°C]} - 273°C$$

There is an overtemperature circuit in the LTC4217 that monitors an internal voltage similar to the I_{SET} pin voltage. When the die temperature exceeds 145°C the circuit turns off the MOSFET until the temperature drops to 125°C.

Monitor MOSFET Current

The current in the MOSFET passes through an internal 7.5mΩ sense resistor. The voltage on the sense resistor is converted to a current that is sourced out of the I_{MON} pin. The gain of I_{SENSE} amplifier is 50µA/A from I_{MON} for 1A of MOSFET current. This output current can be converted to a voltage using an external resistor to drive a comparator

APPLICATIONS INFORMATION

or ADC. The voltage compliance for the I_{MON} pin is from 0V to $INTV_{CC}$ – 0.7V.

A microcontroller with a built-in comparator can build a simple integrating single-slope ADC by resetting a capacitor that is charged with this current. When the capacitor voltage trips the comparator and the capacitor is reset, a timer is started. The time between resets will indicate the MOSFET current.

Monitor OV and UV Faults

Protecting the load from an overvoltage condition is the main function of the OV pin. In the LTC4217-12, an internal resistive divider (driving the OV pin) connects to a comparator to turn off the MOSFET when the V_{DD} voltage exceeds 15.05V. If the V_{DD} pin subsequently falls back below 14.8V, the switch will be allowed to turn on immediately. In the LTC4217 the OV pin threshold is 1.235V when rising, and 1.215V when falling out of overvoltage.

The UV pin functions as an undervoltage protection pin or as an "ON" pin. In the LTC4217-12 the MOSFET turns off when V_{DD} falls below 9.23V. If the V_{DD} pin subsequently rises above 9.88V for 100ms, the switch will be allowed to turn on again. The LTC4217 UV turn-on/off thresholds are 1.235V (rising) and 1.115V (falling).

In the cases of an undervoltage or overvoltage the MOSFET turns off and there is indication on the PG status pin. When the overvoltage is removed the MOSFET's gate ramps up immediately at the rate determined by the INRUSH block.

Power Good Indication

In addition to setting the foldback current limit threshold, the FB pin is used to determine a power good condition. The LTC4217-12 uses an internal resistive divider on the OUT pin to drive the FB pin. The PG comparator indicates logic high when OUT pin rises above 10.5V. If the OUT pin subsequently falls below 10.3V the comparator toggles low. On the LTC4217 the PG comparator drives high when the FB pin rises above 1.235V and low when falls below 1.215V.

Once the PG comparator is high the GATE pin voltage is monitored with respect to the OUT pin. Once the GATE minus OUT voltage exceeds 4.2V the PG pin goes high. This indicates to the system that it is safe to load the OUT pin while the MOSFET is completely turned "on". The PG pin goes low when the GATE is commanded off (using the UV, OV or SENSE pins) or when the PG comparator drives low.

12V Fixed Version

In the LTC4217-12 the UV, OV and FB pins are driven by internal dividers which may need to be filtered to prevent false faults. By placing a bypass capacitor on these pins the faults are delayed by the RC time constant. Use the R_{IN} value from the electrical characteristics table for this calculation.

In cases where the fixed thresholds need a slight adjustment, placing a resistor from the UV or OV pins to V_{DD} or GND will adjust the threshold up or down. Likewise placing a resistor between FB pin to OUT or GND adjusts the threshold. Again use the R_{IN} value from the electrical characteristics table for this calculation.

An example in Figure 5 raises the UV turn-on voltage from 9.88V to 10.5V. Increasing the UV level requires adding a resistor between UV and ground. The resistor, R_{SHUNT1}, can be calculated using electrical table parameters as follows:

$$R_{SHUNT1} = \frac{R_{(IN)} \bullet V_{OLD}}{(V_{NEW} - V_{OLD})} = \frac{18k \bullet 9.88V}{(10.5V - 9.88V)} = 287k$$

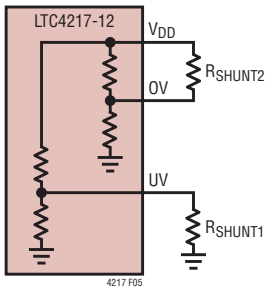


Figure 5. Adjusting LTC4217-12 Thresholds

APPLICATIONS INFORMATION

In this same figure the OV threshold is lowered from 15.05V to 13.5V. Decreasing the OV threshold requires adding a resistor between V_{DD} and OV. This resistor can be calculated as follows:

$$R_{SHUNT2} = \frac{R_{(IN)} \bullet V_{OLD}}{V_{(TH)}} \left(\frac{\left(V_{NEW} - V_{OV(TH)}\right)}{\left(V_{OLD} - V_{NEW}\right)} \right) =$$

$$\frac{18k \bullet 15.05V}{1.235V} \left(\frac{(13.5V - 1.235V)}{(15.05V - 13.5V)} \right) = 1.736M$$

Use the equation for R_{SHUNT1} for increasing the OV and FB thresholds. Likewise use the equation for R_{SHUNT2} for decreasing the UV and FB thresholds.

Design Example

Consider the following design example (Figure 6): V_{IN} = 12V, I_{MAX} = 2A. I_{INRUSH} = 100mA, C_L = 330µF, V_{UVON} = 9.88V, V_{OVOFF} = 15.05V, $V_{PGTHRESHOLD}$ = 10.5V. A current limit fault triggers an automatic restart of the power-up sequence.

The inrush current is defined by the current required to charge the output capacitor using the fixed 0.3V/ms GATE charge-up rate. The inrush current is defined as:

$$I_{INRUSH} = C_L \bullet 0.3[V/ms] = 330\mu F \bullet 0.3[V/ms] = 100mA$$

As mentioned previously the charge-up time is the output voltage (12V) divided by the output rate of 0.3V/ms resulting in 40ms. The peak power dissipation of 12V at 100mA (or 1.2W) is within the SOA of the pass MOSFET for 40ms (see MOSFET SOA curve in the Typical Performance Characteristics section).

Next the power dissipated in the MOSFET during overcurrent must be limited. The active current limit uses a timer to prevent excessive energy dissipation in the MOSFET. The worst-case power dissipation occurs when the voltage versus current profile of the foldback current limit is at the maximum. This occurs when the current is 2A and the voltage is one half of the V_{IN} or 6V. See the Current Limit Threshold Foldback in the Typical Performance Characteristics section to view this profile. In order to survive 12W, the MOSFET SOA dictates a maximum time of 10ms (see SOA graph). Use the internal 2ms timer invoked by tying the TIMER pin to $INTV_{CC}$. After the 2ms timeout the $\overline{FLT}$ pin needs to pull-down on the UV pin to restart the power-up sequence.

Since the default values for overvoltage, undervoltage and power good thresholds for the 12V fixed version match the requirements, no external components are required for the UV, OV and FB pins.

The final schematic in Figure 6 results in very few external components. The pull-up resistor, R7, connects to the PG pin while the 20k (R_{MON}) converts the I_{MON} current to a voltage at a ratio:

$$V_{IMON} = 50[\mu A/A] \bullet 20k \bullet I_{OUT} = 1[V/A] \bullet I_{OUT}$$

In addition there is a 1µF bypass (C1) on the $INTV_{CC}$ pin.

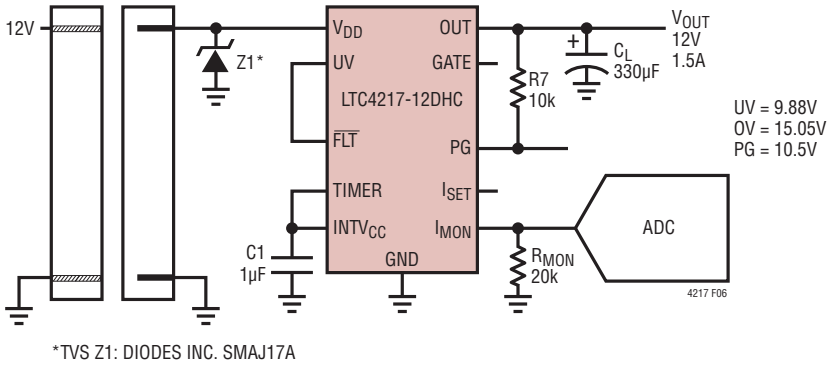


Figure 6. 1.5A, 12V Card Resident Application

APPLICATIONS INFORMATION

Layout Considerations

In Hot Swap applications where load currents can be 2A, narrow PCB tracks exhibit more resistance than wider tracks and operate at elevated temperatures. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure

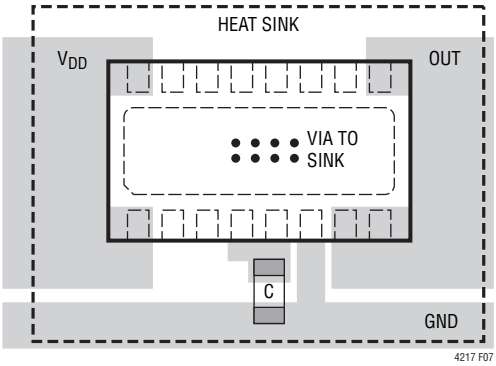


Figure 7. Recommended Layout

the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 0.5mΩ/square. Small resistances add up quickly in high current applications.

There are two V_{DD} pins on opposite sides of the package that connect to the sense resistor and MOSFET. The PCB layout should be balanced and symmetrical to each V_{DD} pin to balance current in the MOSFET bond wires. Figure 7 shows a recommended layout for the LTC4217.

Although the MOSFET is self protected from overtemperature, it is recommended to solder the backside of the package to a copper trace to provide a good heat sink. Note that the backside is connected to the SENSE pin and cannot be soldered to the ground plane. During normal loads the power dissipated in the MOSFET is as high as 0.23W. A 10mm × 10mm area of 1oz copper should be sufficient. This area of copper can be divided in many layers.

It is also important to put C1, the bypass capacitor for the $INTV_{CC}$ pin as close as possible between the $INTV_{CC}$ and GND.

Additional Applications

The LTC4217 has a wide operating range from 2.9V to 26.5V. The UV, OV and PG thresholds are set with few resistors. All other functions are independent of supply voltage.

Figure 8 shows a 3.3V application with a UV threshold of 2.87V, an OV threshold of 3.77V and a PG threshold of 3.05V. The last page includes a 24V application with a UV threshold of 19.9V, an OV threshold of 26.3V and a PG threshold of 20.75V.

In addition to Hot Swap applications, the LTC4217 also functions as a backplane resident switch for removable cards (see Figure 9).

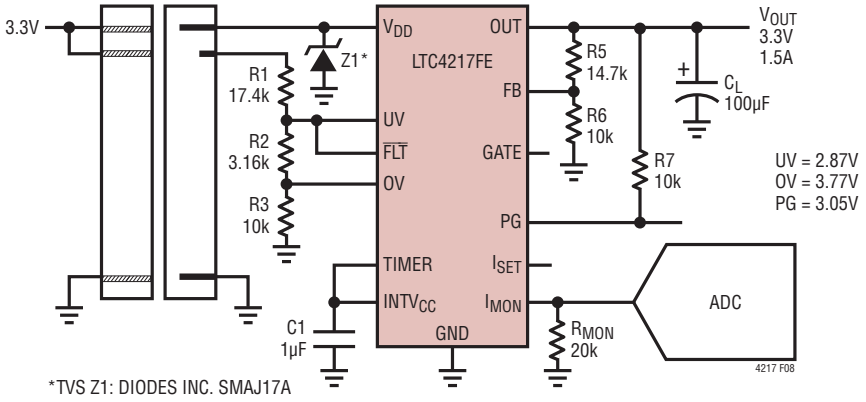
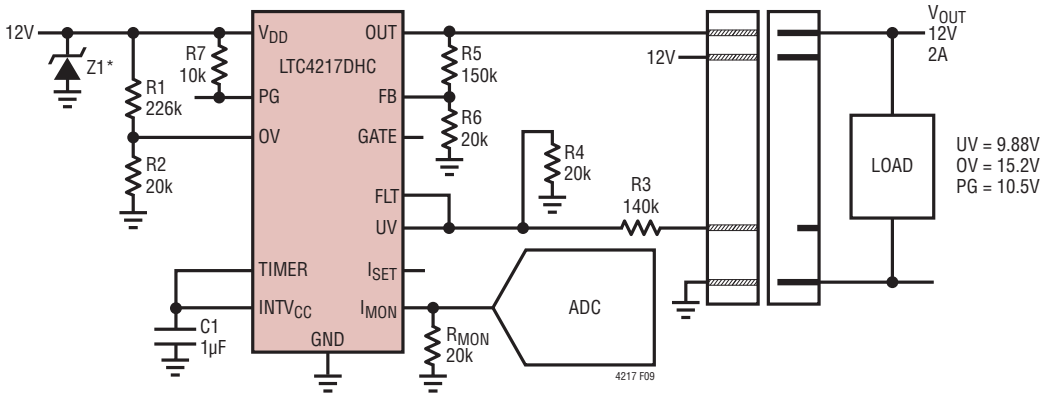


Figure 8. 3.3V, 1.5A Card Resident Application

APPLICATIONS INFORMATION



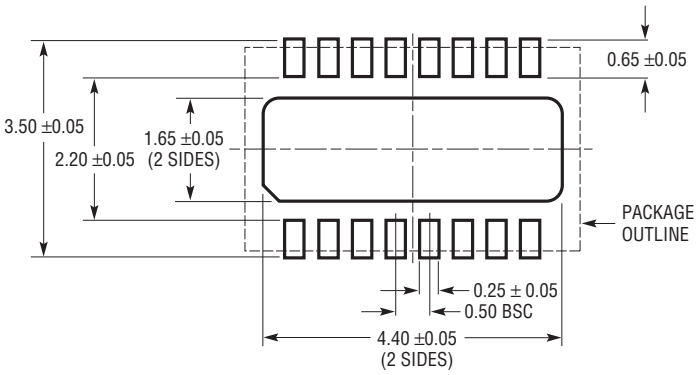
*TVS Z1: DIODES INC. SMAJ17A

Figure 9. 12V, 2A Backplane Resident Application with Insertion Activated Turn-On

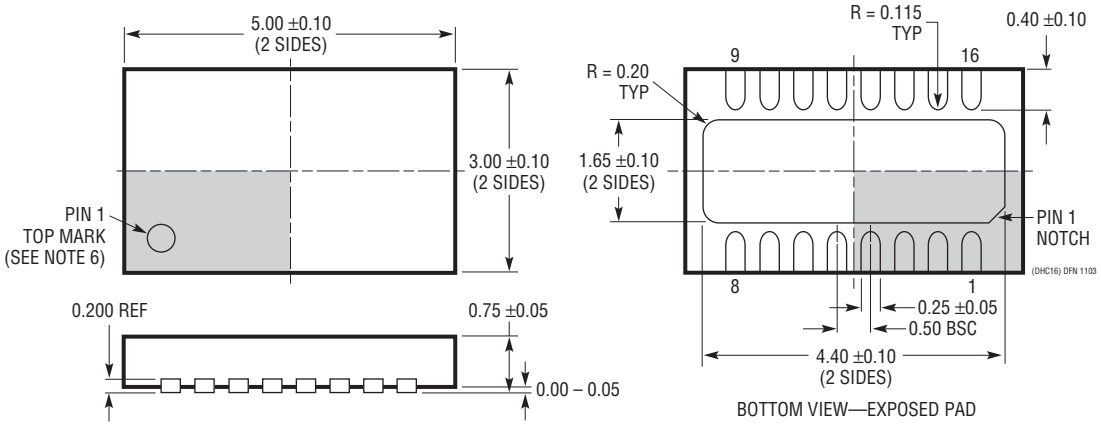
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4217#packaging for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



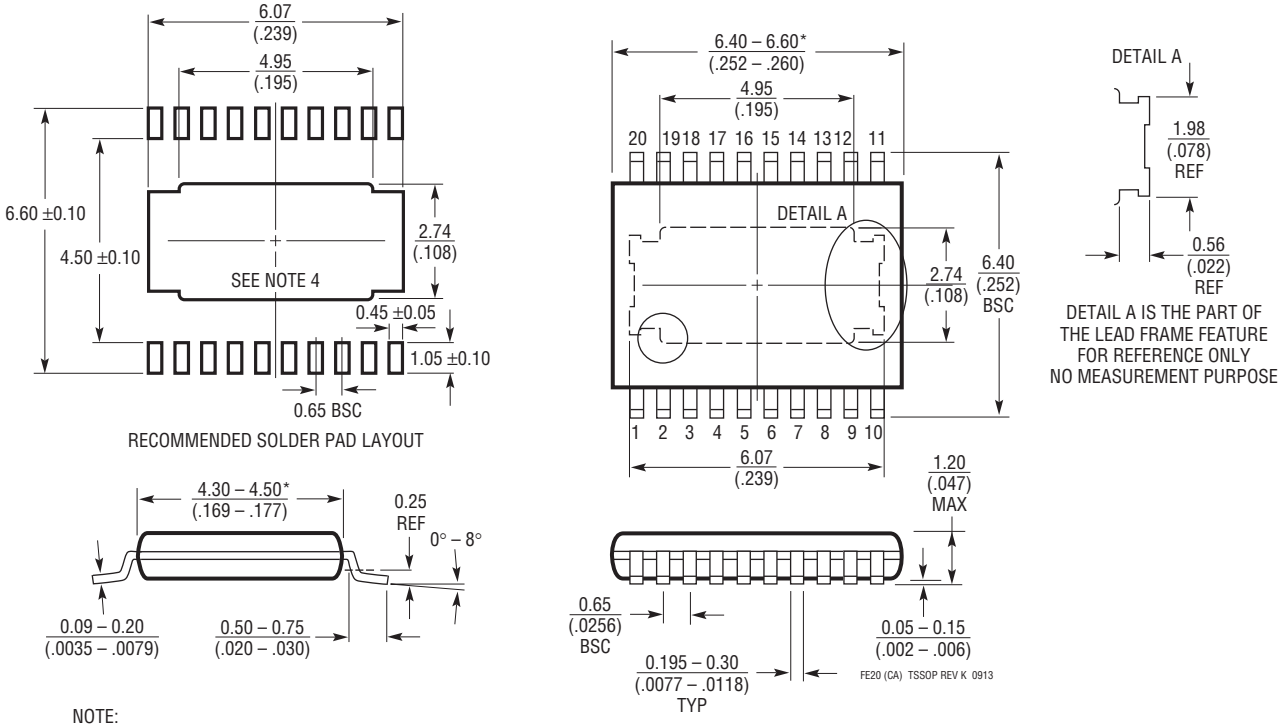
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4217#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation CA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	12/09	Revise Features, Description and Typical Application	1
		Revise Absolute Maximum Ratings Storage Temperature Range and Pin Configuration	2
		Revise Electrical Characteristics	3, 4
		Revise Graph G11	6
		Update Pin Functions	7
		Update Functional Diagram	8
		Update Operation Section	9
		Revise Figure 1 and Update Values and Equation in Applications Information Section	10-12, 14
D	1/11	Added H-grade to Absolute Maximum Ratings, Order Information, and Electrical Characteristics sections.	2-4
E	6/11	Revised R_{ISET} in the Electrical Characteristics section.	4
F	02/16	Typical Application: Added SMAJ22A; increased $INTV_{CC}$ capacitor to 1µF	1
		Raised $I_{GATE(DN)}$ maxima from 340µA to 400µA (C-, I-grade) and from 355µA to 500µA (H-grade)	4
		Updated TPCs G08, G11	5, 6
		Increased bypass capacitance on $INTV_{CC}$ to 1µF from 0.1µF	Multiple
		ISET Pin Function: Recommended minimum resistor value to be 2k	7
		Figure 1: Added Z1, C_{COMP}; updated C1, R1, R_{GATE}	10
		Figures 6, 8: Added Z1; updated C1 to 1µF	14, 15
		Added Figure 9	16
G	04/16	Changed TVS to SMAJ17A in application circuits	1, 10, 14, 15, 16
		Clarified that operating temperature range refers to ambient	2
		Added BW_{IMON} and $t_{D(FAULT)}$ specifications	4
		Updated $INTV_{CC}$ and I_{SET} pin functions	7
		Added equations to calculate MOSFET temperature	12