Dual Hot Swap Controller/ Power Sequencer with Dual Speed, Dual Level Fault Protection

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Configurable Power Supply Sequencing**
- **Soft-Start with Current Foldback Limits Inrush Current**
- **No External Gate Capacitor Required**
- **Adjustable Dual Level Circuit Breaker Protection**
- Controls Supply Voltages from 1V to 13.5V
- Independent N-Channel MOSFET High Side Drivers
- FB Pin Monitors V_{OUT} for Overvoltage Protection
- Latch Off or Automatic Retry on Current Fault
- $\overline{FAULT}$ and PWRGD Outputs
- Narrow 16-Pin SSOP Package

APPLICATIONS

- Electronic Circuit Breaker
- Power Supply Sequencing
- Live Board Insertion and Removal
- Industrial High Side Switch/Circuit Breaker

DESCRIPTION

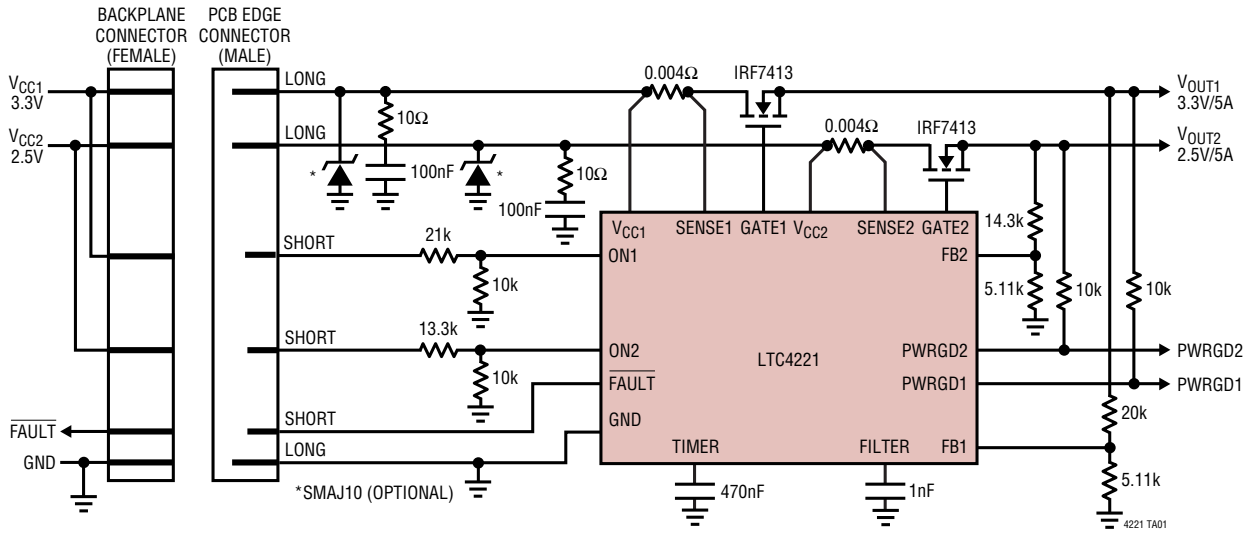
The LTC®4221 is a 2-channel Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. Using two independent high side gate drivers to control two external N-channel pass transistors, the output voltages can be ramped up with current foldback to limit the inrush current during the start-up period. No external compensation capacitors are required at the GATE pins. The two channels can be configured to ramp up and down separately or simultaneously for supply voltages ranging from 2.7V to 13.5V and 1V to 13.5V for channels 1 and 2 respectively.

Each channel has two current limit comparators that provide dual level and dual speed overcurrent circuit breaker protection after the start-up period. If any current sense voltage exceeds 100mV for 1µs or 25mV for the timeout delay (set by the C_{FILTER} at the FILTER pin), then the $\overline{FAULT}$ latch is set and both GATE pins are pulled low.

The FB pins monitor the respective channel output voltages and provide the inputs for the PWRGD comparators as well as overvoltage protection.

TYPICAL APPLICATION

2-Channel Hot Swap Controller

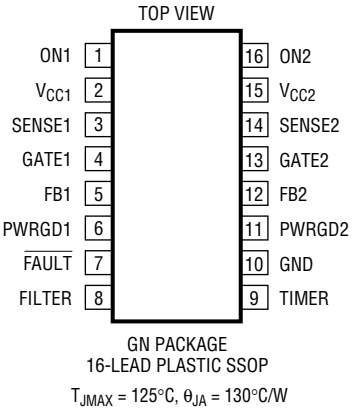


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CCn}) 17V
SENSE*n* Pins ..... –0.3V to (V_{CCn} + 0.3V)
FB, ON Pins ..... –0.3V to (V_{CC1} + 0.3V)
TIMER Pin ..... –0.3V to 2V
GATE Pins (Note 3) ..... –0.3V to 21V
PWRGD, $\overline{FAULT}$, FILTER Pins ..... –0.3V to 17V
Operating Temperature Range
LTC4221C ..... 0°C to 70°C
LTC4221I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4221CGN#PBF	LTC4221CGN#TRPBF	4221	16-Lead Plastic SSOP	0°C to 70°C
LTC4221IGN#PBF	LTC4221IGN#TRPBF	4221I	16-Lead Plastic SSOP	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4221CGN	LTC4221CGN#TR	4221	16-Lead Plastic SSOP	0°C to 70°C
LTC4221IGN	LTC4221IGN#TR	4221I	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = 5V, V_{CC2} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC1}	Supply Voltage Channel 1		●	2.7		13.5	V
V_{CC2}	Supply Voltage Channel 2	$V_{CC2} \le V_{CC1}$	●	1		13.5	V
I_{CC1}	V_{CC1} Supply Current	ON1, ON2 = 2V	●		2.2	3	mA
I_{CC2}	V_{CC2} Supply Current	ON1, ON2 = 2V	●		0.05	0.15	mA
$V_{CC1(UVL)}$	Undervoltage Lockout for Channel 1	V_{CC1} Rising	●	2.1	2.5	2.675	V
$\Delta V_{CC1(HYST)}$	Undervoltage Lockout Hysteresis				110		mV
$V_{CC2(UVL)}$	Undervoltage Lockout for Channel 2	V_{CC2} Rising	●	0.65	0.8	0.975	V
$\Delta V_{CC2(HYST)}$	Undervoltage Lockout Hysteresis				25		mV
$I_{SENSE1(IN)}$	SENSE1 Pin Input Current	$0V \le V_{SENSE1} \le V_{CC1}$	●		±0.03	±5	µA
$I_{SENSE2(IN)}$	SENSE2 Pin Input Current	$V_{SENSE2} = V_{CC2}$ V_{SENSE2} = 0V	● 		±0.2 1000	±5 	µA µA
$V_{SENSE(FC)}$	SENSE*n* Threshold Voltage	Channel*n* Fast Comparator Threshold	●	85	100	115	mV
$V_{SENSE(SC)}$	SENSE*n* Threshold Voltage	Channel*n* Slow Comparator Threshold	 ●	22.5 20.5	25 25	27.5 29.5	mV mV
$V_{SENSE(ACL)}$	SENSE*n* Voltage at Active Current Limit	V_{FBn} = 0 V_{FBn} = 0.65V		4 17.5	9 25	16 32.5	mV mV

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = 5V, V_{CC2} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{GATE(UP)}$	GATE*n* Output Current	$V_{ON1} = V_{ON2}$ = 2V, V_{GATEn} = 0V	●	–7	–9.5	–12	µA
$I_{GATE(DN)}$	GATE*n* Output Current	$V_{ON1} = V_{ON2}$ = 0.6V, V_{GATEn} = 3.3V	●	75	100	125	µA
$I_{GATE(FSTDN)}$	GATE*n* Output Current	UVLO with V_{GATEn} = 3.3V or $\overline{FAULT}$ Latched with V_{GATEn} = 3.3V			16		mA
ΔV_{GATE}	External N-Channel Gate Drive	$V_{GATEn} – V_{CC1}$ for V_{CC1} = 2.7V, V_{CC2} = 1V $V_{GATEn} – V_{CC1}$ for V_{CC1} = 3.3V, V_{CC2} = 2.5V $V_{GATEn} – V_{CC1}$ for V_{CC1} = 5V, V_{CC2} = 3.3V $V_{GATEn} – V_{CC1}$ for V_{CC1} = 12V, V_{CC2} = 12V	● ● ● ●	4.5 5 8 7		13 16 16 18	V V V V
$V_{GATE(OV)}$	GATE*n* Overvoltage Lockout Threshold		●		0.4	0.5	V
$I_{ON(IN)}$	ON*n* Pin Input Current	0V ≤ V_{ONn} ≤ V_{CC1}	●		±0.01	±1	µA
$V_{ON(RESET)}$	ON1 Reset Threshold	V_{ON1} Falling	●	0.375	0.4	0.425	V
$\Delta V_{ON(RESETHYST)}$	ON1 Reset Threshold Hysteresis				25		mV
$V_{ON(OFF)}$	ON*n* Off Threshold	High to Low, GATE*n* Turns Off by 100µA Pull-Down	●	0.796	0.821	0.846	V
$\Delta V_{ON(OFFHYST)}$	ON*n* Off Threshold Hysteresis				30		mV
$I_{FB(IN)}$	FB*n* Input Current	0V ≤ V_{FBn} ≤ V_{CCn}	●		±0.01	±1	µA
$V_{FB(UV)}$	FB*n* Undervoltage Threshold	FB*n* Falling	●	0.605	0.617	0.629	V
$\Delta V_{FB(UVHYST)}$	FB*n* Undervoltage Threshold Hysteresis				3		mV
$\Delta V_{FB(LREG)}$	FB*n* Threshold Line Regulation	2.7V ≤ V_{CC1} ≤ 13.5V			2		mV
$V_{FB(OV)}$	FB*n* Overvoltage Threshold	FB*n* Rising	●	0.805	0.822	0.838	V
$I_{FILTER(UP)}$	FILTER Pull-Up Current	During Current Fault Condition	●	–80	–105	–132	µA
$I_{FILTER(DN)}$	FILTER Pull-Down Current	During Normal Cycle	●	1.15	1.8	2.45	µA
$V_{FILTER(TH)}$	FILTER Threshold	Latched Off Threshold, FILTER Rising	●	1.18	1.24	1.30	V
$\Delta V_{FILTER(HYST)}$	FILTER Threshold Hysteresis				105		mV
$I_{TMR(UP1)}$	TIMER Pull-Up Current 1	Initial Timing Cycle	●	–1.2	–1.9	–2.6	µA
$I_{TMR(UP2)}$	TIMER Pull-Up Current 2	Start-Up Cycle	●	–15	–20	–25	µA
$I_{TMR(FSTDN)}$	TIMER Pull-Down Current	V_{TIMER} = 1.5V, End of Initial Timing Cycle			9		mA
$V_{TMR(H)}$	TIMER High Threshold	TIMER Rising	●	1.172	1.234	1.27	V
$V_{TMR(L)}$	TIMER Low Threshold	TIMER Falling	●	0.1	0.4	0.5	V
$I_{\overline{FAULT}(UP)}$	$\overline{FAULT}$ Pull-Up Current		●	–2.5	–3.8	–5	µA
$V_{\overline{FAULT}(TH)}$	$\overline{FAULT}$ Threshold	$\overline{FAULT}$ Falling	●	0.791	0.816	0.841	V
$\Delta V_{\overline{FAULT}(HYST)}$	$\overline{FAULT}$ Hysteresis				35		mV
$V_{\overline{FAULT}(OL)}$	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 1.6mA, V_{CC1} = 5V	●		0.14	0.4	V
$I_{PWRGD(LK)}$	PWRGD*n* Leakage Current	V_{PWRGDn} = V_{CC1}, V_{FBn} = 0.7V, Normal Cycle	●		±0.01	±10	µA
$V_{PWRGD(OL)}$	PWRGD*n* Output Low Voltage	I_{PWRGDn} = 1.6mA, V_{CC1} = 5V, V_{FBn} = 0V, Normal Cycle	●		0.14	0.4	V
$t_{P(FC-GATE)}$	Fast Comparator Trip to GATE*n* Discharging	V_{SENSEn} = V_{CCn} to (V_{CCn} – 200mV) Step	●		1	1.5	µs
$t_{P(SC-FAULT)}$	Slow Comparator Trip to FILTER High and $\overline{FAULT}$ Latched	V_{SENSEn} = V_{CCn} to (V_{CCn} – 50mV) Step. FILTER Open	●		15	35	µs

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = 5V, V_{CC2} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{P(\overline{FAULT}\text{-GATE})}$	$\overline{FAULT}$ Low to GATE*n* Discharging	$V_{\overline{FAULT}}$ = 3.3V to 0V	●		15	35	µs
$t_{P(OV\text{-}GATE)}$	FB*n* OV Comparator Trip to GATE*n* Discharging	V_{FBn} = 0V to 1V	●		18	35	µs
$t_{P(FILTER\text{-}GATE)}$	Filter Comparator Trip to GATE*n* Discharging	V_{FILTER} = 0V to 1.5V	●		15	35	µs
t_{RESET}	Circuit Breaker Reset Delay Time	V_{ON1} < 0.4V to $\overline{FAULT}$ High	●		15	30	µs
$t_{P(ON\text{-}GATE)}$	Turn Off Propagation Delay	$V_{ONn} \leq$ 0.821V to GATE*n* Discharging	●		15	35	µs

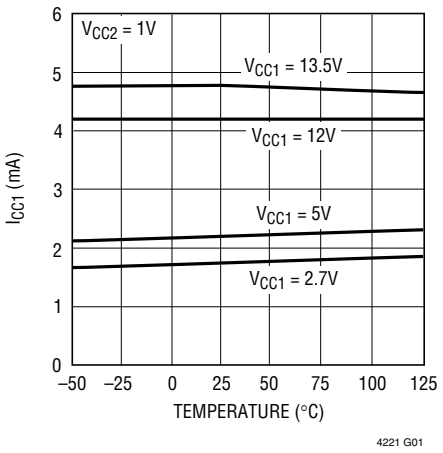
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All current into device pins are positive. All voltages are referenced to ground unless otherwise specified.

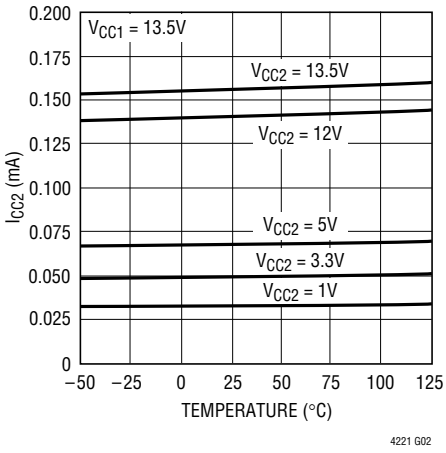
Note 3: An internal zener on each GATE pin clamps the charge pump voltage to a typical maximum operating voltage of 26V. External overdrive of either GATE pin beyond its internal zener voltage may damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

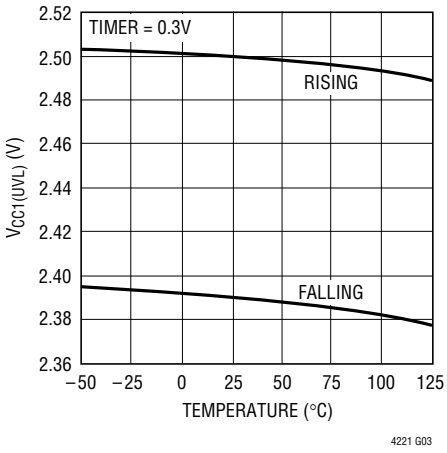
I_{CC1} vs Temperature



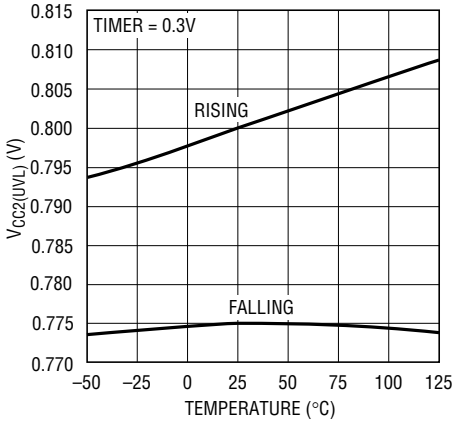
I_{CC2} vs Temperature



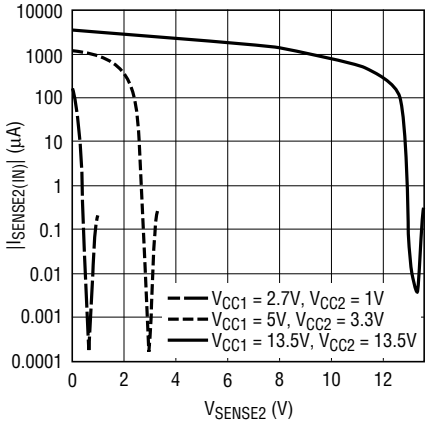
$V_{CC1(UVL)}$ vs Temperature



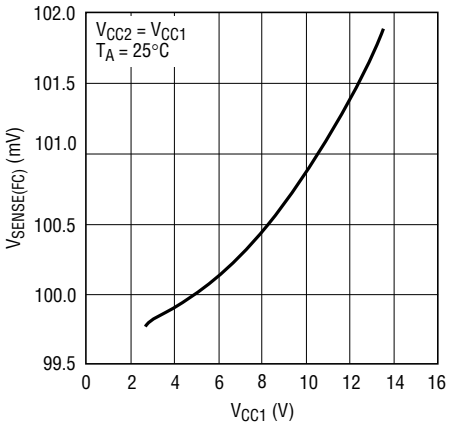
$V_{CC2(UVL)}$ vs Temperature



$|I_{SENSE2(IN)}|$ vs V_{SENSE2}

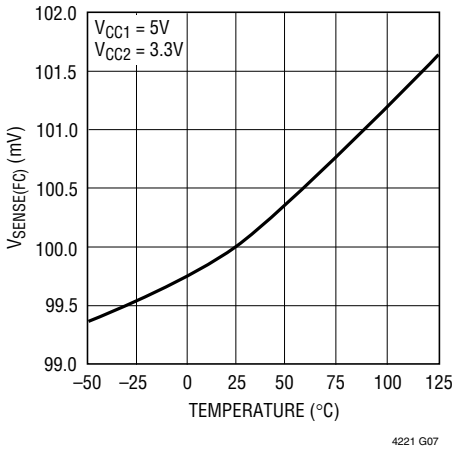


$V_{SENSE(FC)}$ vs V_{CC1}

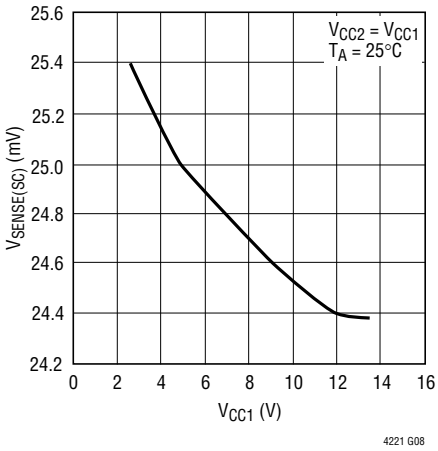


TYPICAL PERFORMANCE CHARACTERISTICS

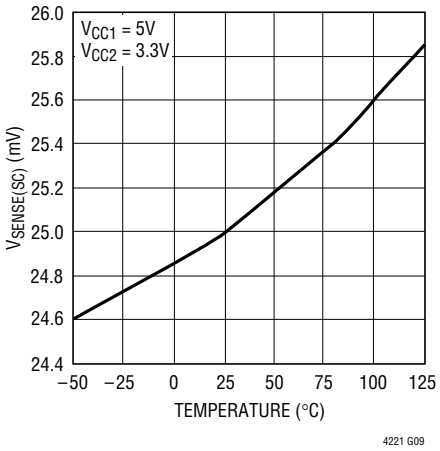
$V_{SENSE(FC)}$ vs Temperature



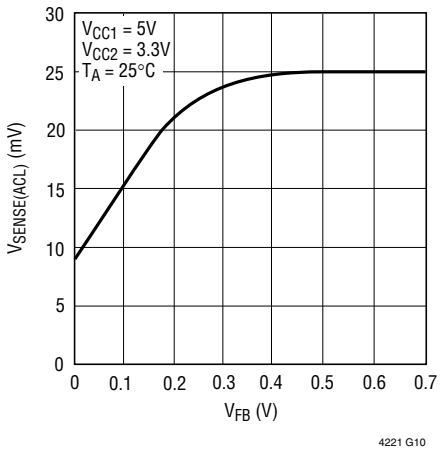
$V_{SENSE(SC)}$ vs V_{CC1}



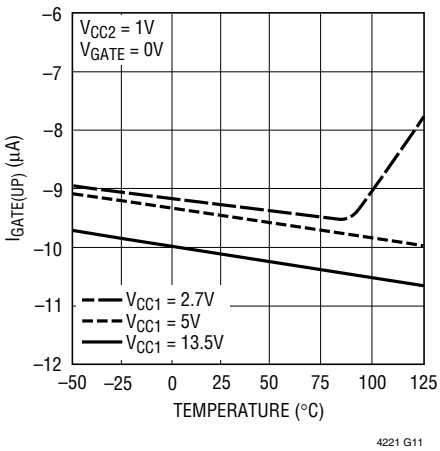
$V_{SENSE(SC)}$ vs Temperature



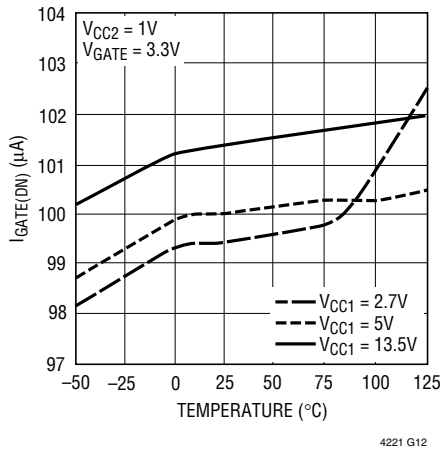
$V_{SENSE(ACL)}$ vs V_{FB}



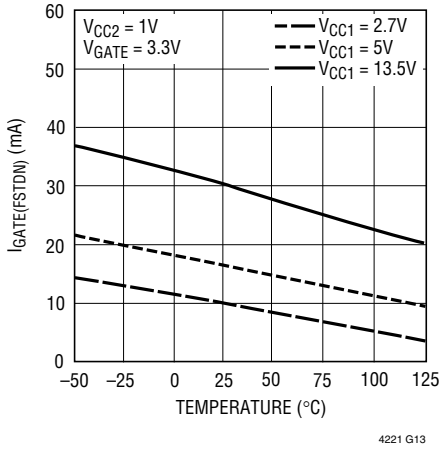
$I_{GATE(UP)}$ vs Temperature



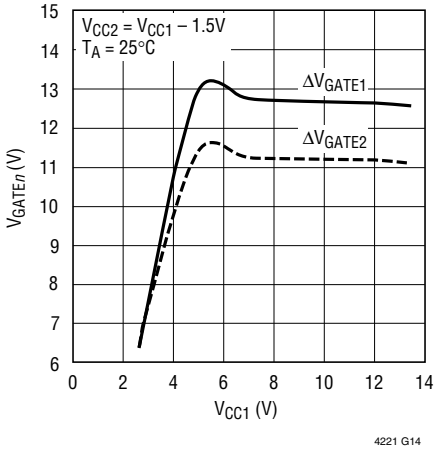
$I_{GATE(DN)}$ vs Temperature



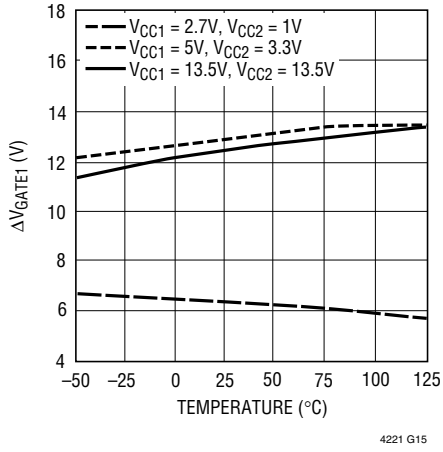
$I_{GATE(FSTDN)}$ vs Temperature



ΔV_{GATEn} ($V_{GATEn} - V_{CC1}$) vs V_{CC1}

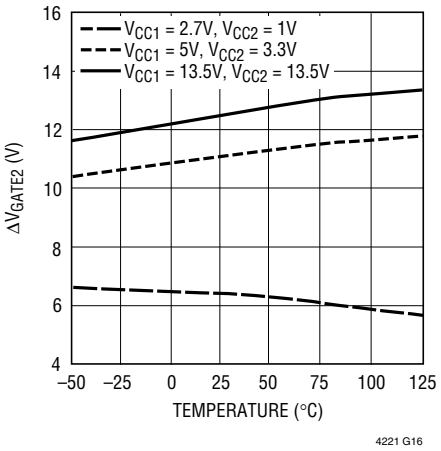


ΔV_{GATE1} ($V_{GATE1} - V_{CC1}$) vs Temperature

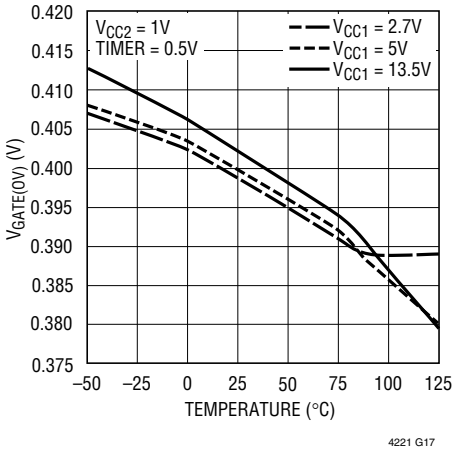


TYPICAL PERFORMANCE CHARACTERISTICS

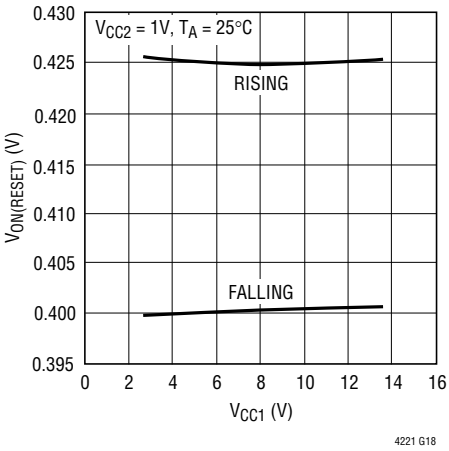
ΔV_{GATE2} ($V_{GATE2} - V_{CC1}$) vs Temperature



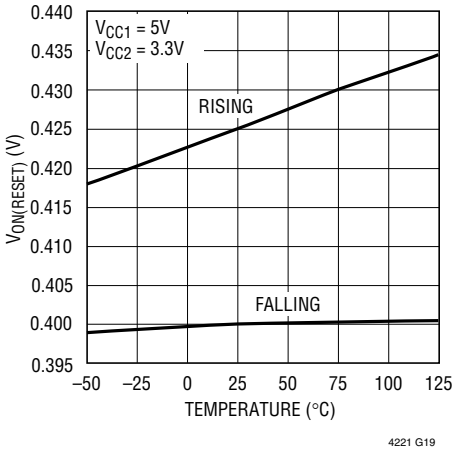
$V_{GATE(OV)}$ vs Temperature



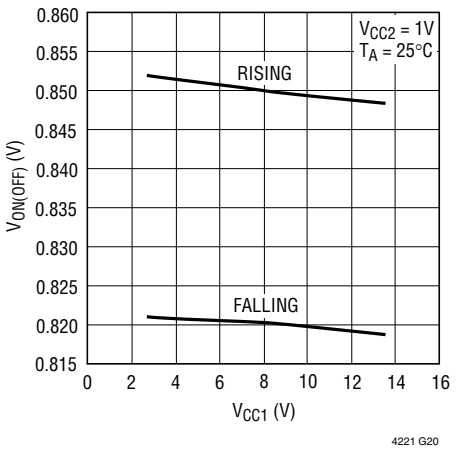
$V_{ON(RESET)}$ vs V_{CC1}



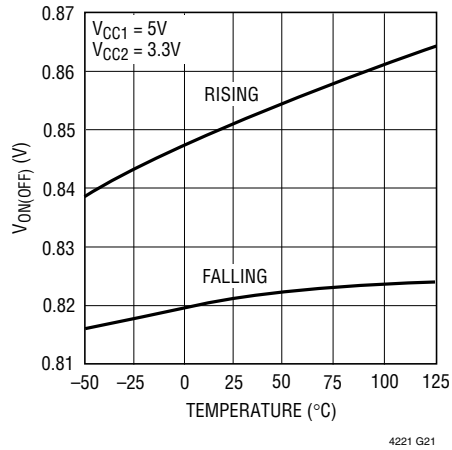
$V_{ON(RESET)}$ vs Temperature



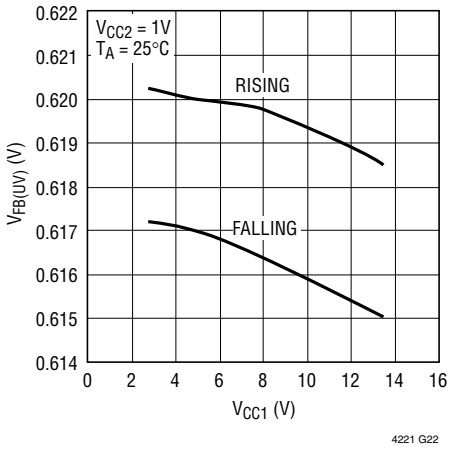
$V_{ON(OFF)}$ vs V_{CC1}



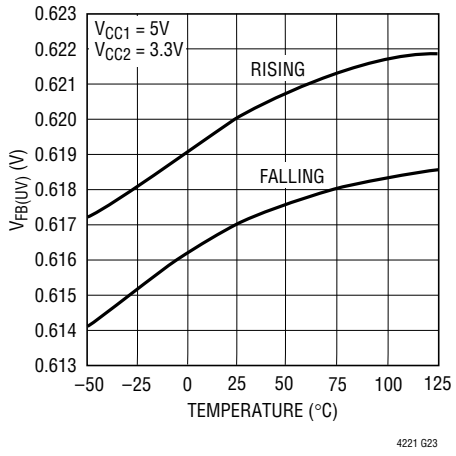
$V_{ON(OFF)}$ vs Temperature



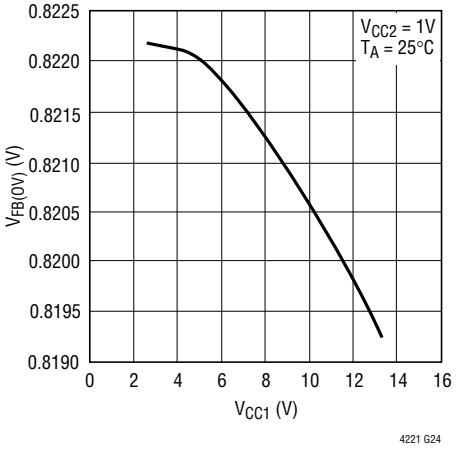
$V_{FB(UV)}$ vs V_{CC1}



$V_{FB(UV)}$ vs Temperature

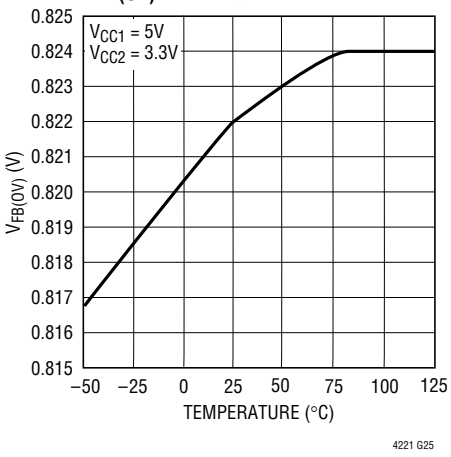


$V_{FB(OV)}$ vs V_{CC1}

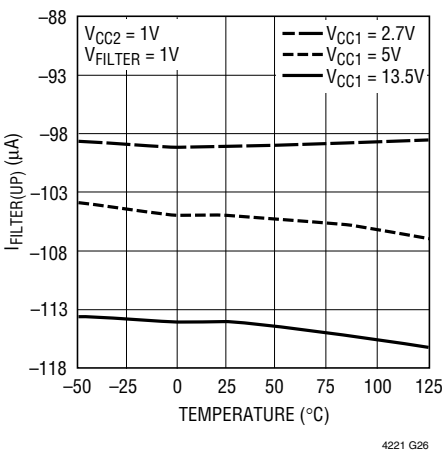


TYPICAL PERFORMANCE CHARACTERISTICS

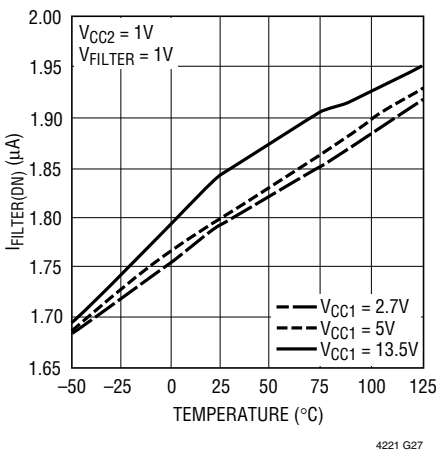
$V_{FB(OV)}$ vs Temperature



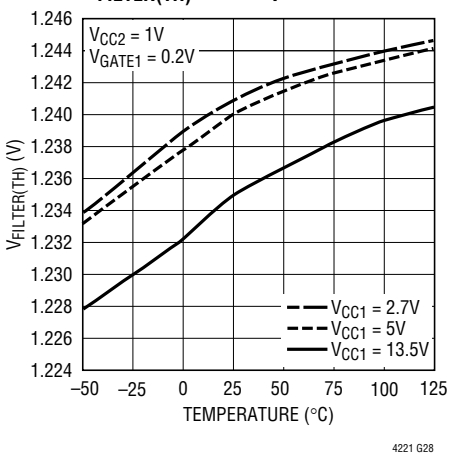
$I_{FILTER(UP)}$ vs Temperature



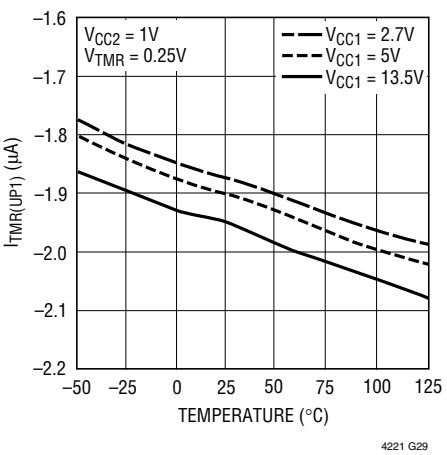
$I_{FILTER(DN)}$ vs Temperature



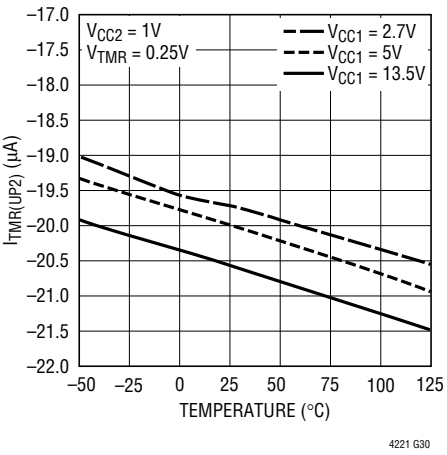
$V_{FILTER(TH)}$ vs Temperature



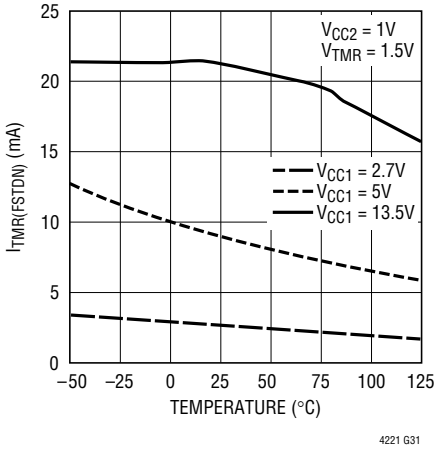
$I_{TMR(UP1)}$ vs Temperature



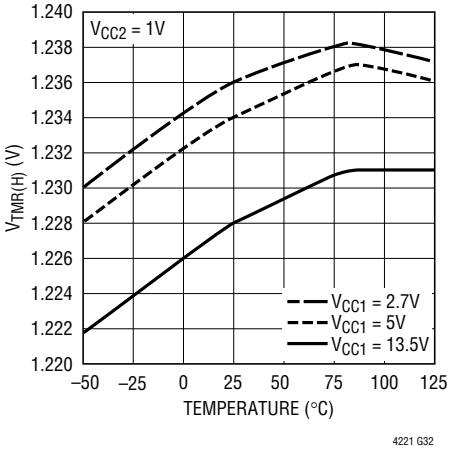
$I_{TMR(UP2)}$ vs Temperature



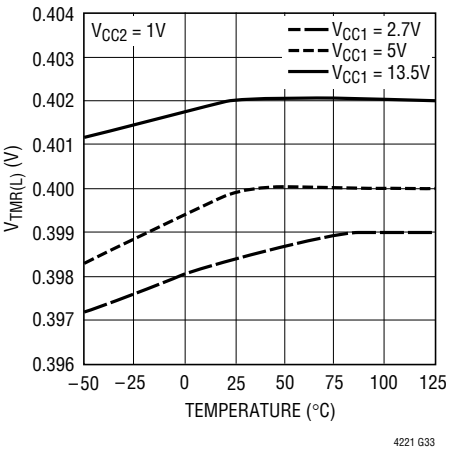
$I_{TMR(FSTDN)}$ vs Temperature



$V_{TMR(H)}$ vs Temperature

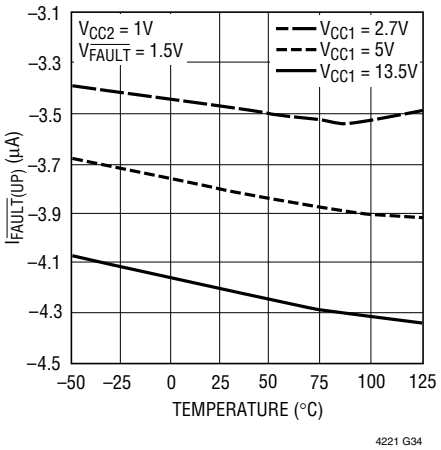


$V_{TMR(L)}$ vs Temperature

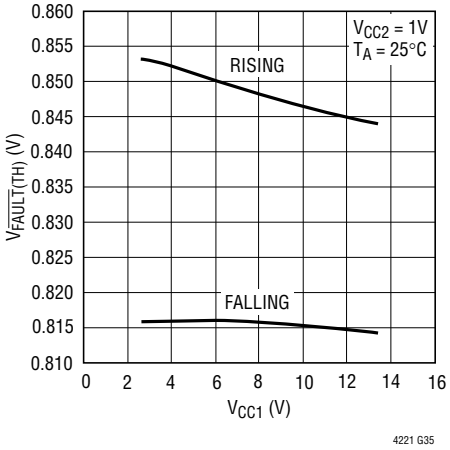


TYPICAL PERFORMANCE CHARACTERISTICS

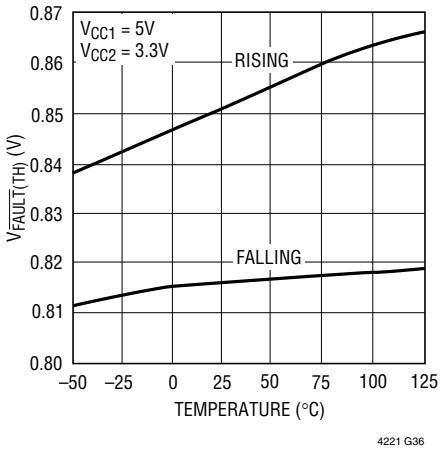
$I_{\overline{FAULT}(UP)}$ vs Temperature



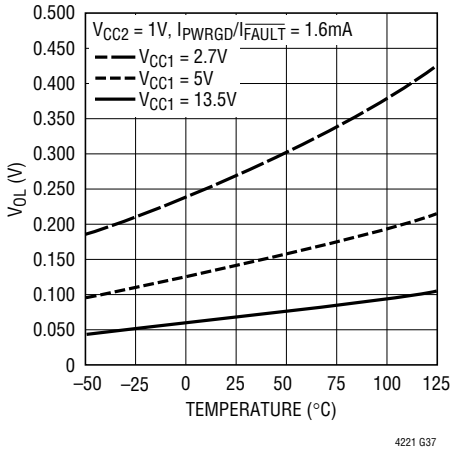
$V_{\overline{FAULT}(TH)}$ vs V_{CC1}



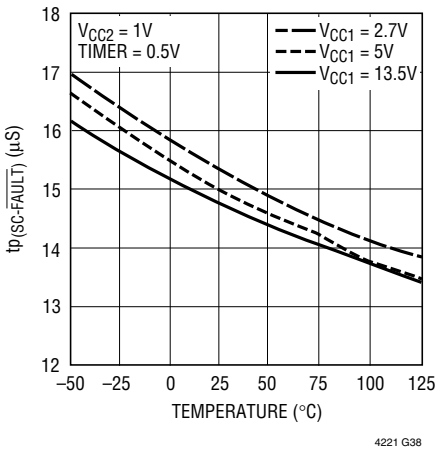
$V_{\overline{FAULT}(TH)}$ vs Temperature



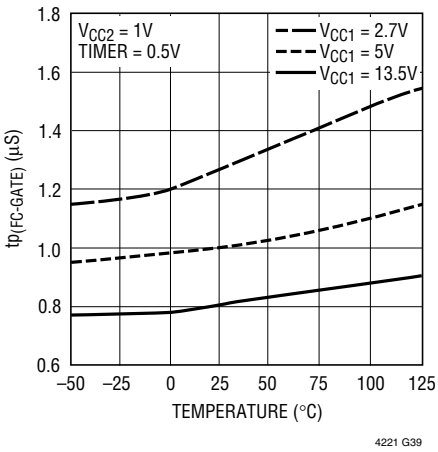
$V_{PWRGD(OL)}/V_{\overline{FAULT}(OL)}$ vs Temperature



$tp_{(SC\text{-}\overline{FAULT})}$ vs Temperature



$tp_{(FC\text{-}GATE)}$ vs Temperature



PIN FUNCTIONS

ON1 (Pin 1): System/Channel 1 On Input. Both GATE pins are pulled low by internal 100µA pull-downs and the $\overline{FAULT}$ latch is reset when $V_{ON1} < 0.4V$. When $0.425V < V_{ON1} < 0.821V$, the $\overline{FAULT}$ latch is released from reset. When $V_{ON1} > 0.851V$, GATE1 ramps up after an initial timing cycle.

V_{CC1} (Pin 2): Channel 1 Positive Supply Input. It powers all the internal circuitry. V_{CC1} can range from 2.7V to 13.5V for normal operation but it must be $\geq V_{CC2}$. An undervoltage lockout circuit disables both channels whenever the voltage at V_{CC1} is less than 2.5V.

SENSE1 (Pin 3): Channel 1 Current Sense Input. A sense resistor R_{SENSE1} is placed in the supply path between V_{CC1} and SENSE1 to sense channel 1 load current. If $V_{RSENSE1}$ exceeds 100mV for more than 1µs or 25mV for an adjustable time (set by the C_{FILTER}), the $\overline{FAULT}$ latch is set and fast pull-down circuits are triggered to discharge both GATEs low. During the start-up cycle, GATE1 ramp-up is controlled to servo $V_{RSENSE1} \leq V_{SENSE(ACL)}$. $V_{SENSE(ACL)}$ increases from 9mV to 25mV as V_{FB1} ramps from 0V to 0.5V. To disable the current limit and circuit breaker function for channel 1, tie SENSE1 to V_{CC1}.

PIN FUNCTIONS

GATE1 (Pin 4): Channel 1 Gate Drive. This pin is the high side gate drive of an external N-channel MOSFET. When V_{ON1} < 0.821V, GATE1 is held low by a 100µA current source. When V_{ON1} > 0.851V, an initial timing cycle is followed by a start-up cycle when an internal charge pump provides a 9.5µA pull-up to ramp up GATE1 with inrush current limiting. UVLO, overvoltage, overcurrent and externally generated faults override the ON1 pin and pull GATE1 low.

FB1 (Pin 5): V_{OUT1} Feedback Input. FB1 monitors the channel 1 output voltage with an external resistive divider. When V_{FB1} < 0.617V, the PWRGD1 pin is pulled low. When V_{FB1} > 0.822V, overvoltage is detected, the $\overline{FAULT}$ latch is set and both GATEs are pulled low. The FB1 pin is also used to control the channel 1 current limit during its start-up cycle.

PWRGD1 (Pin 6): Channel 1 Power Good Output. PWRGD1 is pulled low when V_{FB1} < 0.617V, during the initial timing cycle or when the chip is in UVLO. An external pull-up is required to generate a logic high at the open-drain PWRGD1 pin.

$\overline{FAULT}$ (Pin 7): Fault Status Input/Output. $\overline{FAULT}$ is a bidirectional pin. As an input, pulsing $V_{\overline{FAULT}}$ < 0.816V will set the $\overline{FAULT}$ latch and bring the LTC4221 into the fault state. As an output, $\overline{FAULT}$ is pulled high by an internal 3.8µA pull-up under normal operating conditions. When an overcurrent fault is detected by a SENSE pin or a overvoltage fault detected by an FB pin, the $\overline{FAULT}$ latch is set and the LTC4221 goes into the fault state. The $\overline{FAULT}$ latch is reset by a UVLO or the ON1 pin being driven below 0.4V.

FILTER (Pin 8): Overcurrent Fault Timing Filter. The FILTER pin requires an external capacitor to ground to adjust the response time of the two slow comparators. The FILTER pin can be left unconnected for a default slow comparator response time of 15µs.

TIMER (Pin 9): Analog System Timer. The TIMER pin requires an external capacitor to ground to generate timing delay cycles during start-up. The LTC4221's initial and start-up timing cycles are controlled by C_{TIMER} and the internal current sources connected to the TIMER pin.

GND (Pin 10): Ground. Connect to a ground plane for optimum performance.

PWRGD2 (Pin 11): Channel 2 Power Good Output. Similar functionality as PWRGD1. Controlled by FB2.

FB2 (Pin 12): V_{OUT2} Feedback Input. Similar functionality as FB1. Monitors channel 2 output voltage, controls PWRGD2 output and channel 2 start-up current limit.

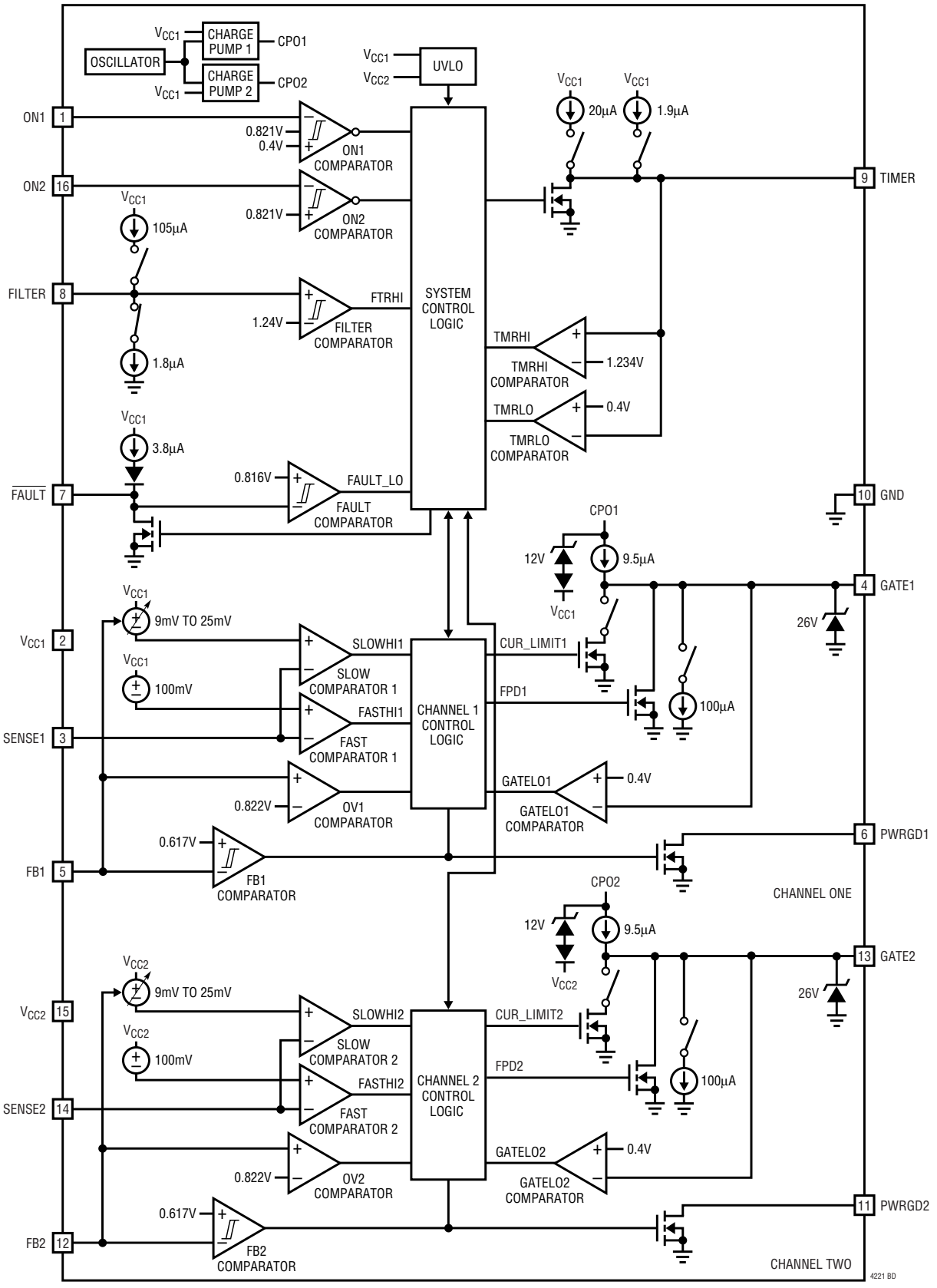
GATE2 (Pin 13): Channel 2 Gate Drive. Similar functionality as GATE1. Controls the gate drive of the channel 2 external N-channel MOSFET. ON2 controls GATE2 in the same manner as ON1 controls GATE1. V_{ON1} < 0.4V overrides conditions at ON2 and GATE2 is held low by a 100µA current source. UVLO, overvoltage, overcurrent and externally generated faults override conditions at ON1 and ON2, and pull GATE2 low.

SENSE2 (Pin 14): Channel 2 Current Sense Input. Similar functionality as SENSE1. Monitors channel 2 load current through R_{SENSE2} placed in the supply path between V_{CC2} and SENSE2. To disable the current limit and circuit breaker function for channel 2, tie SENSE2 to V_{CC2}.

V_{CC2} (Pin 15): Channel 2 Positive Supply Input. V_{CC2} can range from 1V to 13.5V for normal operation but it must be ≤V_{CC1}. An undervoltage lockout circuit disables both channels whenever the voltage at V_{CC2} is less than 0.8V.

ON2 (Pin 16): Channel 2 On Input. GATE2 is pulled to ground by a 100µA current source when V_{ON2} < 0.821V. When V_{ON2} > 0.851V, GATE2 ramps up after an initial timing cycle.

BLOCK DIAGRAM



OPERATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors can draw huge transient currents from the power bus as they charge. The flow of current may damage the connector pins and glitch the power bus, causing other boards in the system to reset.

The LTC4221 is designed to turn on and off a circuit board's supply voltages in a controlled manner, allowing insertion or removal without glitches or connector damage. The LTC4221 can reside on the backplane or on the removable circuit board for hot insertion applications. It controls the path between the backplane power bus and the daughter board load with an external MOSFET switch. Both inrush control and short-circuit protection are provided by the external MOSFET. Each LTC4221 controls two channels, each with its individual MOSFET for supplies from 1V to 13.5V.

Overview

The timing diagram in Figure 1 shows some typical waveforms of the LTC4221. The V_{CC} and GND pins receive power through the longest connector pins and are the first to connect when the board is inserted. During the undervoltage lockout (UVLO) state before time point 1, both GATE pins are held low by internal N-channel MOSFET pull-downs, turning the external MOSFETs off. Once both V_{CC} pins are valid at time point 1, the LTC4221 enters into a reset state as ON1 is below its reset threshold. At time point 2, ON1 clears its reset threshold and the device goes from the reset state to an off state. When either ON1 or ON2 clears its off threshold, both GATE pins are < 0.4V and TIMER < 0.4V (time points 3 and 4), the TIMER pin sources 1.9µA and an initial timing cycle starts. Any transition of ON1 and ON2 through their off thresholds will reset the initial timing cycle. At time point 5, TIMER reaches its high threshold and is pulled down by an internal N-channel MOSFET to its low threshold at time point 6. The LTC4221 then checks that FILTER pin voltage is low and $\overline{\text{FAULT}}$ pin voltage is high. If both conditions are met, the electronic circuit breaker is armed. The channel 1 start-up timing cycle starts at time point 6 since ON1 has cleared its off threshold and ON2 has not.

During the start-up cycle, TIMER sources 20µA and GATE1 sources 9.5µA. As GATE1 ramps up, MOSFET1 starts to turn on and current flows through to charge up the load capacitance. As V_{OUT1} and FB1 ramp up, the load current is monitored through the external SENSE1 resistor. Between time points 7 and 8, the GATE1 9.5µA pull-up is controlled to servo the voltage across R_{SENSE1} to be less than the SENSE1 active current limit voltage, which has a component controlled by the FB1 voltage (see Applications Information: Start-Up Cycle with Current Limit). In this way, inrush current is limited and MOSFET1 does not overheat during the start-up cycle. When FB1 clears its undervoltage threshold, PWRGD1 asserts high. At time point 9, TIMER reaches its high threshold and is pulled down by an internal N-channel MOSFET to its low threshold at time point 10. Channel 1's slow comparator is armed at time point 9 and enters a fault monitor mode, bringing the channel 1 start-up cycle to an end.

At time point 10, ON2 voltage is monitored and since ON2 has cleared its off threshold, the start-up timing cycle repeats for channel 2. The inrush current is low and GATE2 ramps up without need for current limiting. Channel 2's slow comparator is armed at time point 11 and enters a fault monitor mode, ending the channel 2 start-up cycle.

Overcurrent faults translate to an increase in either V_{RSENSE}. At time point 13, $V_{RSENSE1}$ > 25mV (slow comparator threshold). The 1.8µA pull-down on the FILTER changes to a 105µA pull-up. When the FILTER pin hits its threshold at time point 14, it triggers a fault state when $\overline{\text{FAULT}}$ is latched low and both GATE pins are pulled low by internal N-channel MOSFETs, turning off the external MOSFETs. As each channel output discharges, its FB pin goes below the undervoltage threshold and the PWRGD pin deasserts. Higher overcurrents when either V_{RSENSE} > 100mV (fast comparator threshold) for more than 1µs will trigger the same condition. This fault state can only be cleared by a UVLO at either V_{CC} pin or a hard reset at the ON1 pin, as at time point 15, when ON1 is pulled below its reset threshold. The LTC4221 then reverts back to its reset state as between time points 1 and 2.

OPERATION

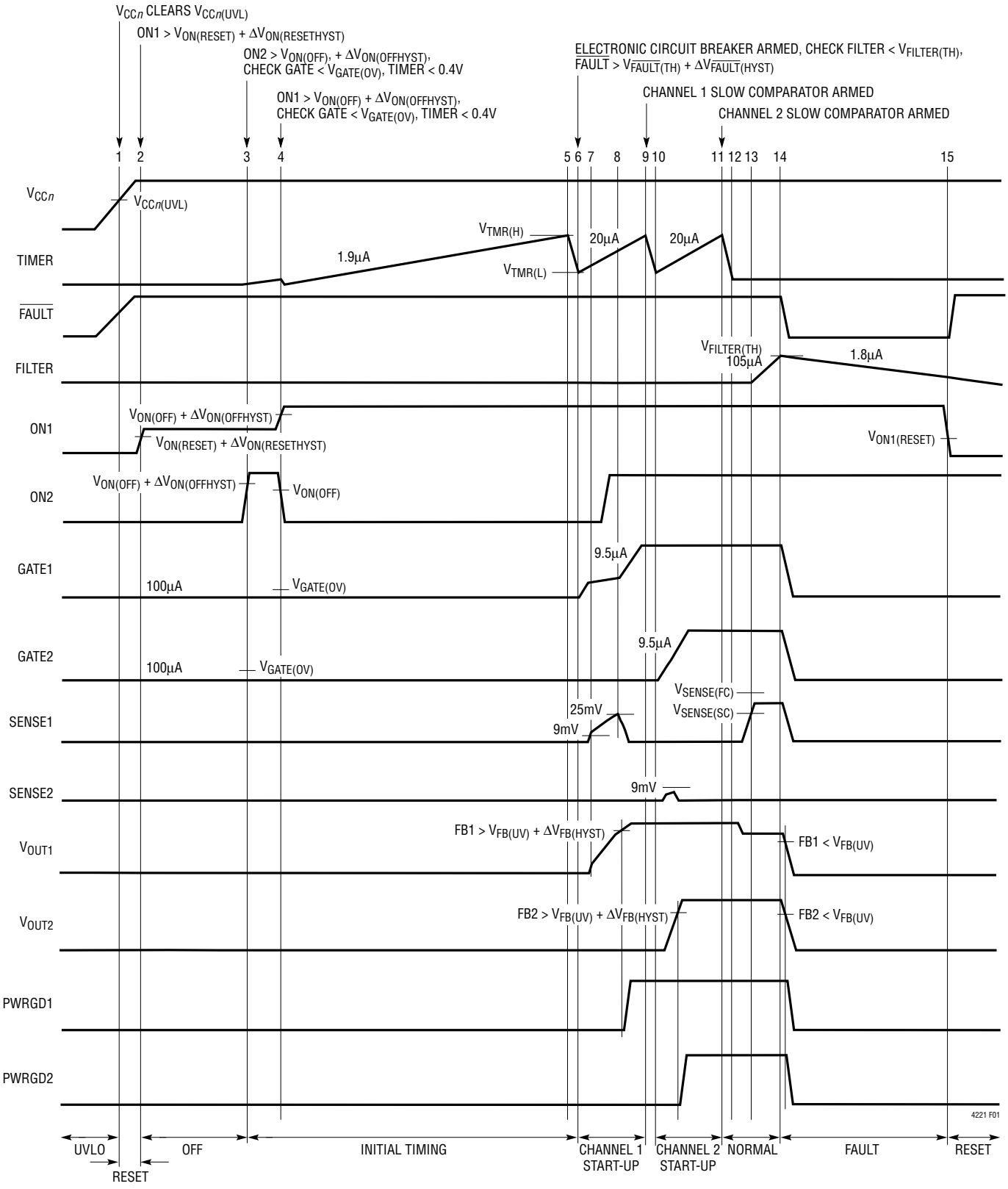


Figure 1. LTC4221 Operation

APPLICATIONS INFORMATION

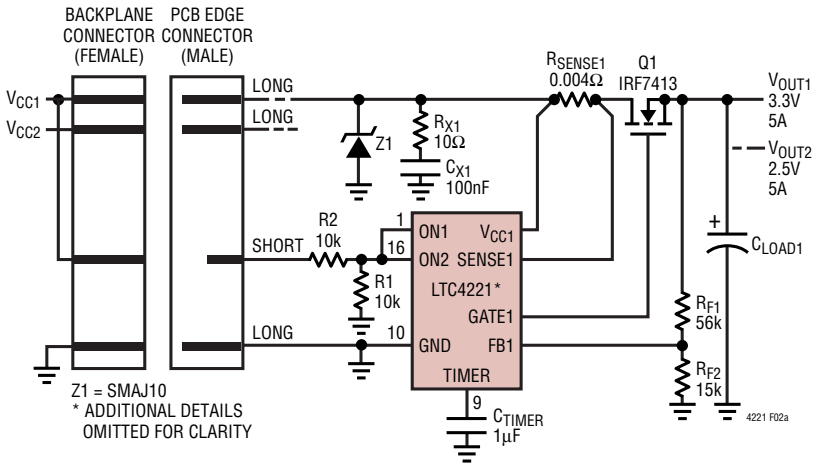
Undervoltage Lockout

An internal undervoltage lockout (UVLO) occurs if either V_{CC} supply is too low for normal operation. The LTC4221 is kept in lockout mode in which the internal charge pumps are off, the GATE pins, TIMER are held low by internal N-channel MOSFET pull-downs and the FAULT latch reset, cutting off both channels. V_{CC1} has a low-to-high UVLO threshold of 2.5V with 110mV hysteresis. V_{CC2} has a low-to-high UVLO threshold of 0.8V with 25mV hysteresis. Both UVLOs have glitch filters that filter out dips that are less than 30µs, allowing for bus supply transients. An additional requirement for normal operation is $V_{CC1} \geq V_{CC2}$.

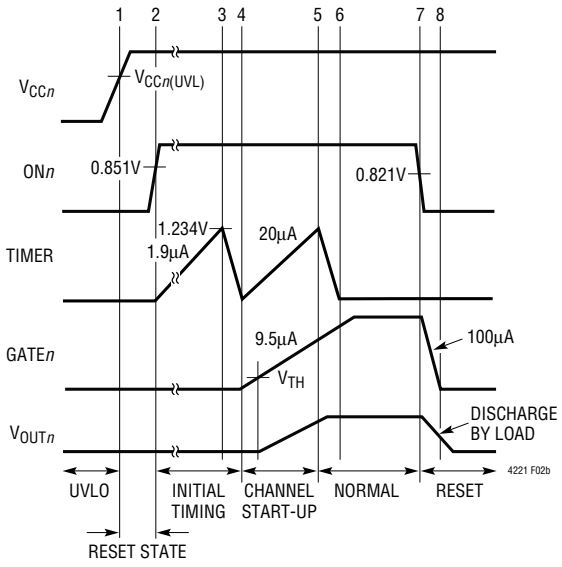
ON Pin Functions

The ON1 pin serves as a global reset for the LTC4221. It has an internal reset comparator with a high-to-low threshold of 0.4V, a 25mV hysteresis and a high-to-low glitch filter of 15µs. Pulling ON1 below this threshold will put the LTC4221 into a reset state in which the TIMER is pulled low by an internal N-channel MOSFET pull-down, the GATE pins are pulled low by separate internal 100µA pull-downs and the FAULT latch resets. A low-to-high transition on the ON1 pin past the reset threshold releases the reset on the FAULT latch and both channels go into an off state.

In addition to its global reset function, ON1 also serves as an on/off switch for channel 1. ON2 performs the same role for channel 2. Both pins have an off comparator with a high-to-low threshold of 0.821V and 30mV hysteresis. With these, ON1 and ON2 can be used to force a simultaneous or sequential power-up/power-down of the two channels. A simultaneous power-up and power-down is shown in Figure 2b. Both V_{CC} pins clear their respective UVLO at time point 1 and both channels enter reset state. When ON1 clears its reset threshold, either ON1 or ON2 clears its off threshold, both GATEs < 0.4V and TIMER < 0.4V (time point 2), an initial timing cycle starts. At time point 4, the initial timing cycle completes and the LTC4221 checks that FILTER is low and FAULT is high. If both conditions are met, it then monitors the voltage of ON1 and ON2. As long as its ON pin has cleared its off threshold, each channel powers up regardless of the state of the other channel. Similarly, if its ON pin goes below its off threshold, each channel pulls its GATE pin down with an internal 100µA pull-down and turns off its external MOSFET regardless of the state of the other channel. As the circuit in Figure 2a has its two ON pins shorted together, a simultaneous power-up is programmed at time points 4 to 5 and a simultaneous power down is programmed between time points 7 and 8. The timing waveforms in Figure 3 show a



(2a) Circuit



(2b) Timing Waveforms

Figure 2. Simultaneous Power On/Off

APPLICATIONS INFORMATION

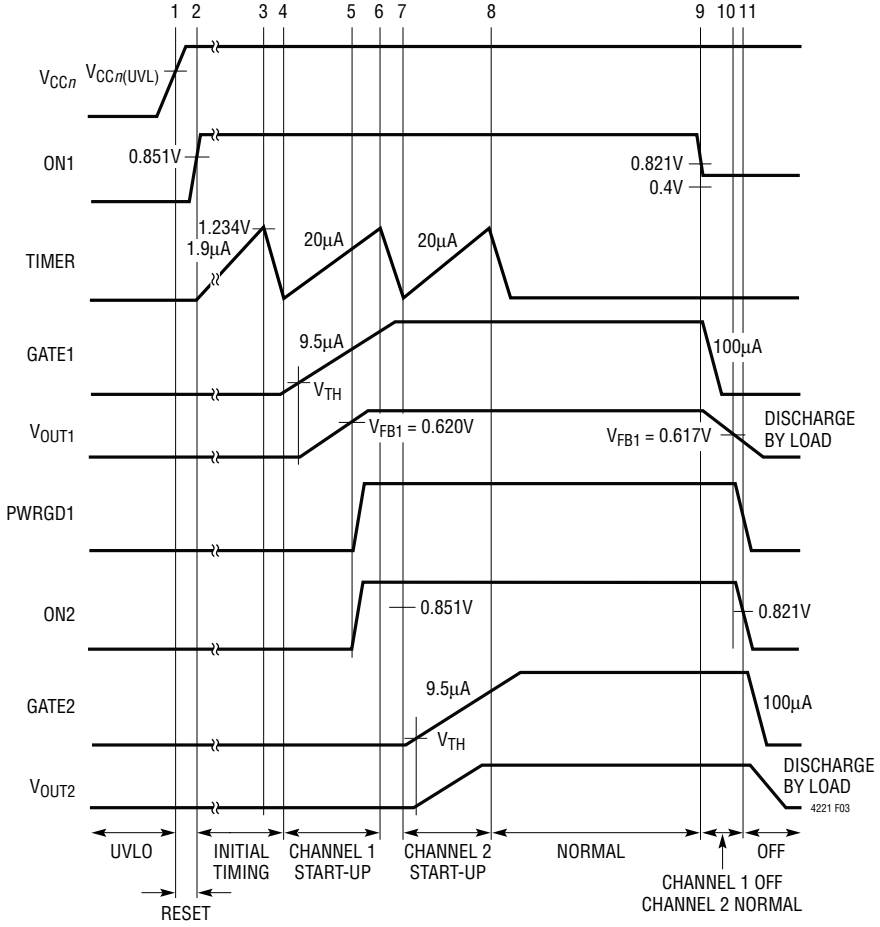


Figure 3. Sequential Power On/Off Timing Waveforms

sequential power up from time points 4 to 8 and a sequential power-down programmed from time points 9 to 11. To achieve this the circuit requires the functionality of the PWRGD1 pin and will be featured in the next section.

The circuit in Figure 2a sits on a daughter board with staggered pins on its edge connectors. Supply voltage and ground connections are wired to long-edge connector pins while both ON pins are connected to a short-edge connector pin through a resistive divider. Until the connectors are fully mated, ON1 is pulled low and holds both channels in the reset state. When the connectors have properly seated, the ON pins are pulled above 0.851V and an initial timing cycle starts. This cycle is restarted by any transitions on the ON pins across their off thresholds and adds a further delay for the plug-in transients to die off before allowing a start-up cycle. The Typical Application circuit on the first page of this data sheet shows similar considerations in the design of its PCB edge connectors, and the resistive dividers connected to ON1 and ON2 act as an external UVLO to override the internal one. An RC filter can be added at the ON1 pin to increase the delay time at card insertion to allow bus supply transients to stabilize.

FB and PWRGD Pin Functions

Each FB pin is used to detect undervoltage and overvoltage in its channel output voltage (V_{OUT}) through a resistive divider. Each FB pin has an undervoltage comparator with a high-to-low threshold of 0.617V and 3mV hysteresis. The output of this comparator controls the channel's open-drain PWRGD output. During UVLO, both PWRGD pins are pulled low by internal N-channel MOSFET pull-downs. As both channels come out of UVLO, control of PWRGD1 is passed to FB1and control of PWRGD2 to FB2. Each PWRGD pin can be connected to a pull-up resistor to

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generate a logic high output to indicate that V_{OUT} is valid. An internal high-to-low glitch filter helps to prevent negative voltage transients on each FB pin from deasserting its PWRGD. The relationship between glitch filter time and an FB pin transient voltage is shown in Figure 4. Using the functionality of the PWRGD1 pin, the LTC4221 can be configured to do sequential power-up and power-down as shown by the circuit in Figure 5. Referring back to Figure 3, ON2 is held low until V_{OUT1} ramps high enough for FB1 to exceed its undervoltage threshold at time point 5 when PWRGD1 ramps up, pulling ON2 high. At time point 7, the control logic sees ON2 exceeding its off threshold and so commences a start-up cycle for channel 2. Similarly, when ON1 is forced low by Q2 at time point 9, GATE1 is pulled low by its 100µA pull-down while ON2 is held high by the R4 pull-up on PWRGD1. Its is only when channel 1 is powered off and V_{OUT1} discharges below its undervoltage threshold at time point 10 that PWRGD1's internal N-channel MOSFET pull-down is triggered and ON2 goes low. At time point 11, ON2 trips its off threshold and GATE2 pulls low with a 100µA pull-down, powering off channel 2.

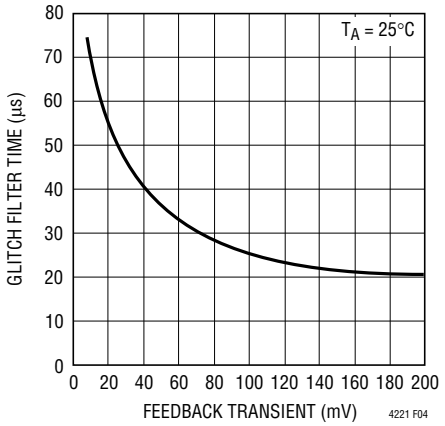

Figure 4. FB Comparator Glitch Filter Time vs Feedback Transient Voltage

For V_{OUT} overvoltage detection, each FB pin has an overvoltage comparator with a low-to-high threshold of 0.822V and a low-to-high glitch filter of 18µs. This threshold is designed to be 33% higher than the undervoltage threshold. If either FB pin trips this threshold, the fault latch is set, all GATE pins are pulled low with internal NFET pull-downs and the LTC4221 goes into a fault state.

In the third function, each FB pin is used to control its channel's current limit during its start-up cycle. This will be featured in the Start-Up Cycle with Current Limit section.

GATE Pin Functions

Each GATE pin controls the gate of its channel's external N-channel MOSFET. Individual internal charge pumps powered by V_{CC1} guarantee a gate drive of minimum 4.5V and maximum 18V (internally clamped) for GATE1 and GATE2. During UVLO, the internal charge pumps are off and both GATE pins are pulled low by internal N-channel MOSFET pull-downs. Outside UVLO, when ON1 is below its off threshold, the charge pumps are on and GATE1 is held low by an internal 100µA current pull-down. Once

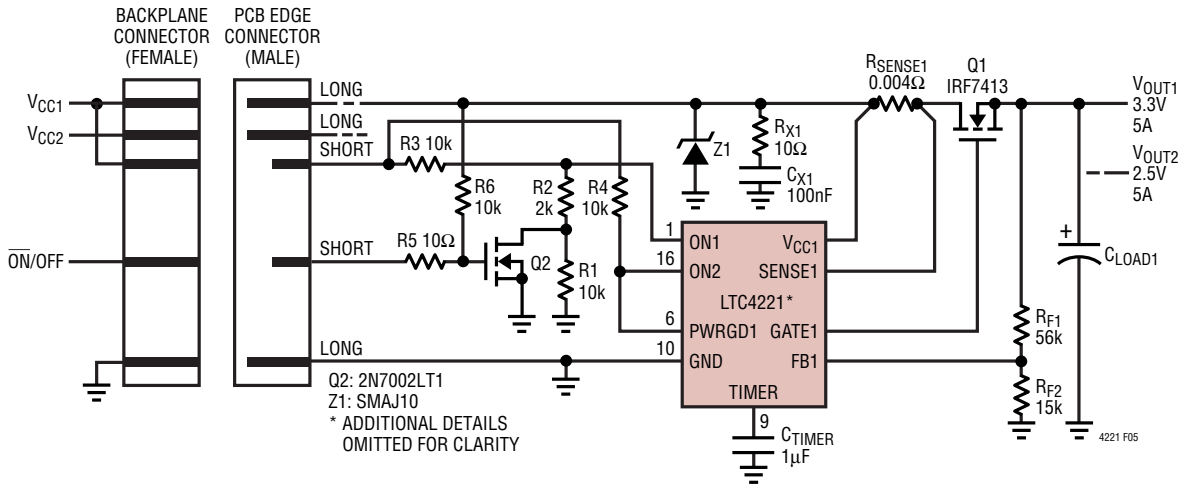

Figure 5. Using PWRGD1 to Configure Sequential Power-Up/Power-Down

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ON1 clears its off threshold and the initial timing cycle is complete, the GATE1 pin is pulled up by a 9.5µA current source connected to the charge pump output during the channel start-up cycle. GATE1 can be servoed by adjusting the ramp up current to <9.5µA to control the inrush current to the load during start-up. ON2 controls GATE2 in a similar manner but is overwritten by ON1's global reset function. During an overcurrent fault condition that sets the fault latch, both GATE pins are pulled down by their respective internal N-channel MOSFET pull-downs.

During hot insertion of the PCB, an abrupt application of supply voltage charges the external MOSFET drain/gate capacitance. This can cause an unwanted gate voltage spike. An internal proprietary circuit holds both GATE pins low before the internal circuitry wakes up. This reduces the MOSFET current surges substantially at insertion.

Electronic Circuit Breaker

The LTC4221 features an electronic circuit breaker function that protects against supply overvoltage, externally generated fault conditions and shorts or excessive load current conditions on any of the supplies. If the circuit breaker trips, both GATE pins are immediately pulled to ground, the external N-channel MOSFETs are quickly turned OFF and $\overline{\text{FAULT}}$ is latched low.

During the normal cycle, a supply overvoltage on channel *n* propagates via the V_{OUTn} resistive dividers to the FB*n* pin. A supply overvoltage high enough to pull either FB pin above 0.822V for more than 18µs will trip the circuit breaker.

The circuit breaker can also be made to trip by externally forcing the bidirectional $\overline{\text{FAULT}}$ pin below 0.816V. The $\overline{\text{FAULT}}$ pin has 35mV of hysteresis. An internal glitch filter of 15µs filters out noise on the $\overline{\text{FAULT}}$ pin.

The slow comparator of channel *n* trips the circuit breaker if $V_{RSENSEn} = (V_{CCn} – V_{SENSEn})$ is greater than its 25mV threshold for more than 15µs. There may be applications where this inherent response time is not long enough, for example, because of excessive supply voltage noise. To adjust the response time of the slow comparator, a capacitor can be connected from the FILTER pin to GND. If this pin is left unused, each slow comparator's delay defaults to 15µs. During normal operation, the FILTER output pin is held low by an internal 1.8µA pull-down current source. During an overcurrent condition on either channel as shown in Figure 6, the 1.8µA pull-down on the FILTER pin becomes an internal 105µA pull-up and C_{FILTER} charges up. Once the FILTER pin voltage ramps past its low-to-high threshold of 1.24V at time point 2, the electronic circuit breaker trips and the LTC4221 shuts down. The FILTER pin's internal 1.8µA pull-down discharges C_{FILTER} and holds FILTER low. Each slow comparator's response time from an overcurrent fault condition is:

$$t_{FILTER} = \frac{1.24V \bullet C_{FILTER}}{105\mu A} + 15\mu s \quad (1)$$

Intermittent overloads may exceed the current limit as in Figure 7, but if the duration is sufficiently short, the FILTER pin may not reach the $V_{FILTER(TH)}$ threshold and the LTC4221 will not shut down. To handle this situation, the FILTER discharges with 1.8µA whenever both V_{RSENSE} are below 25mV. Any intermittent overload with an aggregate

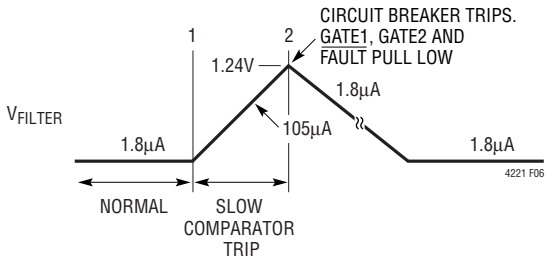

Figure 6. A Continuous Fault Timing

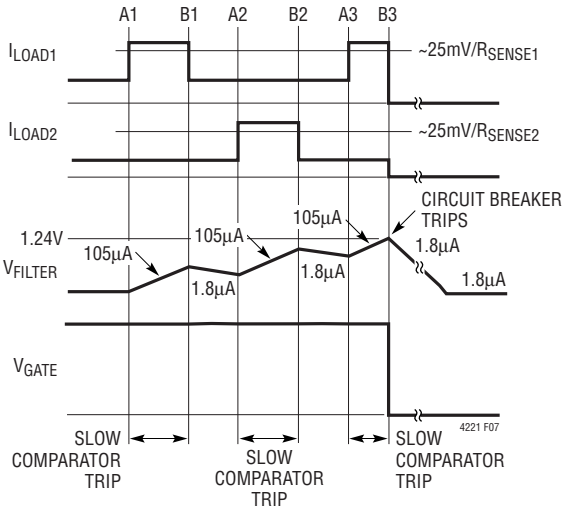

Figure 7. Multiple Intermittent Overcurrent Condition

APPLICATIONS INFORMATION

duty cycle of more than 1.8% will eventually trip the circuit breaker. Figure 8 shows the circuit breaker response time in seconds normalized to 1µF. The asymmetric charging and discharging of FILTER is a fair gauge of MOSFET heating.

$$\frac{t}{C_{FILTER}(\mu F)} = \frac{1.24V}{(105\mu A \bullet D) - 1.8\mu A} \quad (2)$$

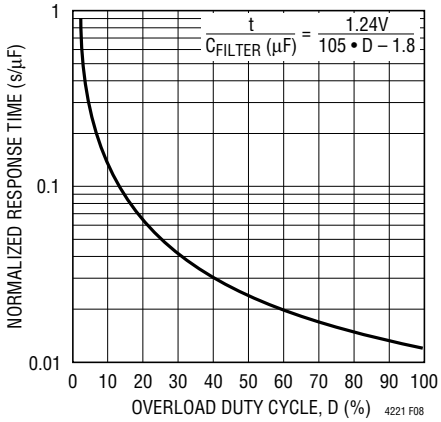

Figure 8. Circuit Breaker Filter Response for Intermittent Overload

The fast comparators trip the circuit breaker to protect against fast load overcurrents if V_{RSENSE} is greater than $V_{SENSE(FC)}$ (100mV) for 1µs. The response time of each fast comparator is fixed at 1µs nominal. The timing diagram in Figure 9 illustrates the operation of the LTC4221 when the load current conditions cause V_{RSENSE} of channel 1 to exceed 100mV for more than 1µs between time points 7 and 8. Figure 9 also illustrates when the LTC4221's electronic circuit breaker is armed. After the initial timing cycle, it is armed at time point 3. Arming the circuit breaker at time point 3 ensures that the system is protected against an overcurrent condition during the channel start-up cycle. At time point 4, the slow comparators are armed when the internal control loop is disengaged.

Autoretry After a Fault

Once the LTC4221 circuit breaker is tripped, $\overline{FAULT}$ is latched low and both GATE pins are pulled to ground. To clear the internal $\overline{FAULT}$ latch and to restart the LTC4221, its ON1 pin must be pulsed below its reset threshold ($V_{ON(RESET)}$ = 0.4V) for at least 15µs.

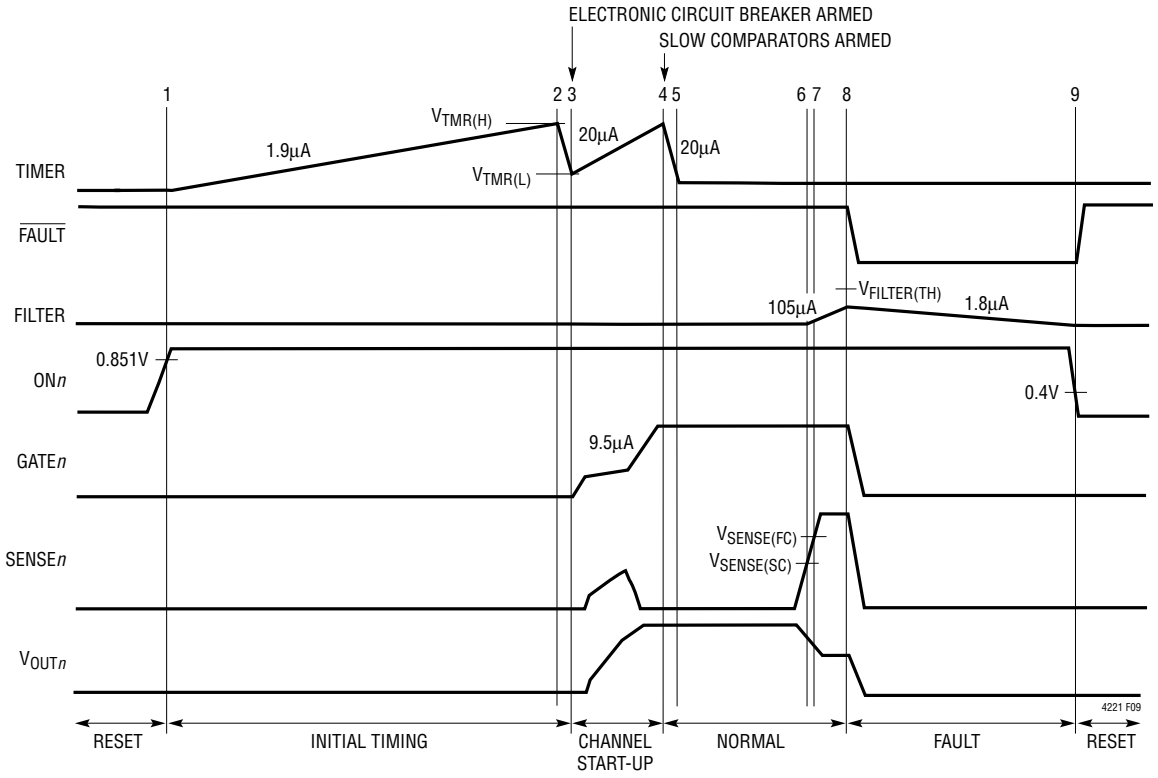

Figure 9. Fast Comparator Trip Timing Waveforms

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The LTC4221 can also be configured to automatically retry after a fault condition. As shown in Figure 10, the $\overline{\text{FAULT}}$ (which has an internal 3.8µA pull-up current source) and both ON pins are connected together. The timing diagram in Figure 11 illustrates a simultaneous start-up sequence where the LTC4221 is powered up into a load overcurrent condition on channel 1. After the slow comparators are armed at the end of the start-up cycle at time point 4, slow comparator 1 immediately trips and FILTER ramps up. FILTER ramps past its high threshold at time point 6 and trips the circuit breaker. $\overline{\text{FAULT}}$ and both ON pins are pulled low by an internal N-channel MOSFET and overshoots below the 0.4V reset threshold of the ON1 pin. Once ON1 < 0.4V for more than 15µs, the internal fault

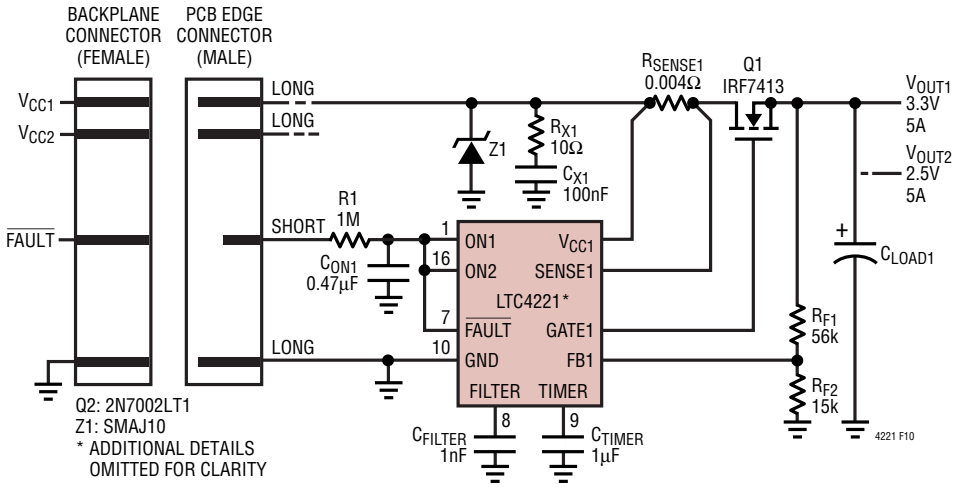

Figure 10. Using $\overline{\text{FAULT}}$ to Configure Autoretry

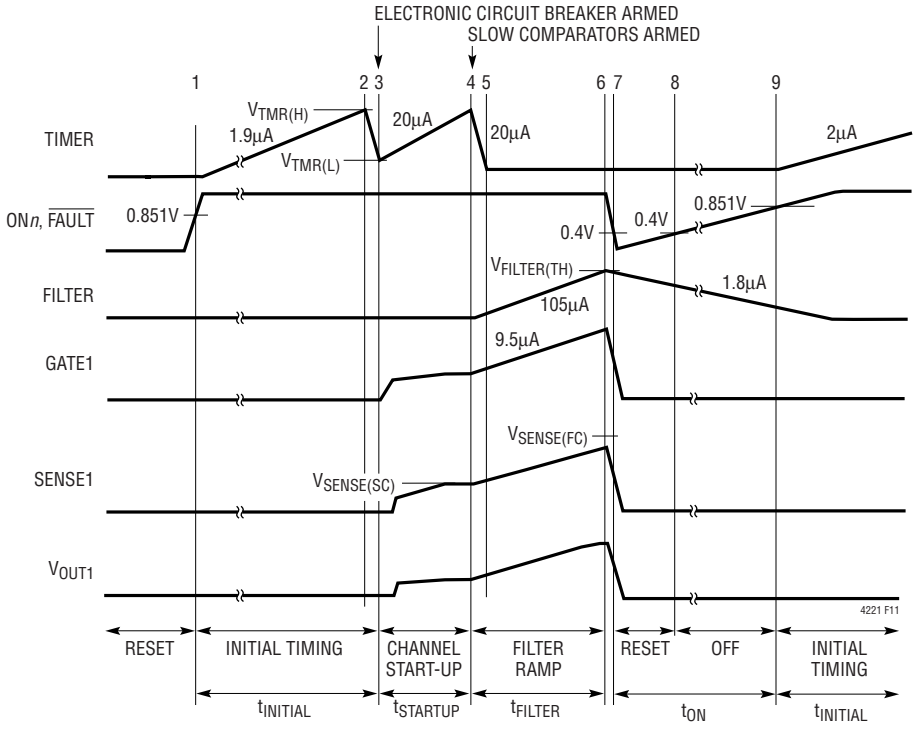

Figure 11. Autoretry Timing Waveforms

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latch is cleared and the $\overline{FAULT}$ pin sources a 3.8µA pull-up current to charge up C_{ON1}. The typical delay t_{ON} is :

$$t_{ON} = (0.851V - 0.4V) \bullet \frac{C_{ON1}}{3.8\mu A} \quad (3)$$

As shown in the timing diagram of Figure 11, the autoretry circuitry will attempt to restart the LTC4221 with a duty cycle:

$$\text{Duty Cycle} = \frac{(t_{STARTUP} + t_{FILTER}) \bullet 100\%}{t_{ON} + t_{INITIAL} + t_{STARTUP} + t_{FILTER}} \quad (4)$$

t_{FILTER} is defined in Equation 1 and t_{ON} is defined in Equation 3. $t_{INITIAL}$, the initial timing cycle delay, is given in Equation 9 located in the Initial Timing Cycle section. $t_{STARTUP}$, the start-up cycle delay, is given in Equation 10 and found in the Start-Up Cycle Without Current Limit section. Using the capacitor values as shown in Figure 10, the Autoretry Duty cycle works out to be approximately 6%.

Sense Resistor Consideration

The fault current level at which the LTC4221's internal electronic circuit breaker trips is determined by sense resistors connected between each channel's V_{CC} and SENSE pins. For both channels, the slow comparator trip current and the fast comparator trip current are given by equations (5) and (6) respectively.

$$I_{TRIP(SC)} = \frac{V_{SENSE(SC)}}{R_{SENSE}} = \frac{25mV}{R_{SENSE}} \quad (5)$$

$$I_{TRIP(FC)} = \frac{V_{SENSE(FC)}}{R_{SENSE}} = \frac{100mV}{R_{SENSE}} \quad (6)$$

The power rating of the sense resistor should be rated at the fault current level. Table 1 in the Appendix lists some common sense resistors.

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and each channel's V_{CC} and SENSE pins are strongly recommended. The drawing in Figure 12 illustrates the connections between the LTC4221 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

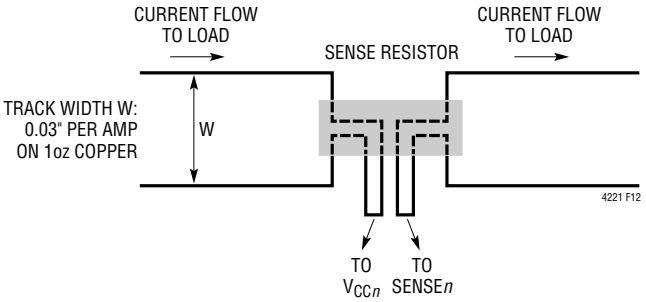

Figure 12. PCB Connections to the Sense Resistor

Calculating Current Limit

For a selected R_{SENSE}, the load current must not exceed $I_{TRIP(SC)}$. The minimum $I_{TRIP(SC)}$ is given by Equation 7:

$$I_{TRIP(SCMIN)} = \frac{V_{SENSE(SCMIN)}}{R_{SENSE(MAX)}} = \frac{20.5mV}{R_{SENSE(MAX)}} \quad (7)$$

where

$$R_{SENSE(MAX)} = R_{SENSE} \bullet \left(1 + \frac{R_{TOL}}{100}\right)$$

The maximum $I_{TRIP(SC)}$ is given by Equation 8:

$$I_{TRIP(SCMAX)} = \frac{V_{SENSE(SCMAX)}}{R_{SENSE(MIN)}} = \frac{29.5mV}{R_{SENSE(MIN)}} \quad (8)$$

where

$$R_{SENSE(MIN)} = R_{SENSE} \bullet \left(1 - \frac{R_{TOL}}{100}\right)$$

If a 7mΩ sense resistor with ±1% tolerance is used for current limiting, the nominal slow comparator trip current is 3.57A. From Equations 7 and 8, $I_{TRIP(SCMIN)}$ = 2.9A and $I_{TRIP(SCMAX)}$ = 4.26A. For proper operation, the minimum $I_{TRIP(SC)}$ must exceed the circuit maximum operating load current. For reliability purposes, the operation at the maximum trip current must be evaluated carefully. If necessary, two resistors with the same R_{TOL} can be connected in parallel to yield a nominal R_{SENSE} value that fits the circuit requirements.

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Timer Function

The TIMER pin controls the initial cycle and the channel start-up cycles with an external capacitor, C_{TIMER}. There are two comparator thresholds: $V_{TMR(H)}$ (1.234V) and $V_{TMR(L)}$ (0.4V). In addition, the pin has a 1.9µA pull-up current, a 20µA pull-up current and a N-channel MOSFET pull-down.

Initial Timing Cycle

When the card is being inserted into the bus connector, the long pins mate first which brings up the supplies at time point 1 of Figure 13. The LTC4221 is in reset mode as the ON1 pin is low. Both GATE pins and the TIMER pin are pulled low. At time point 2, the short pin makes contact and both ON pins are pulled high. At this instant, a start-up check requires that both supply voltages be above UVLO, at least one ON pin be above 0.851V, both GATE pins < 0.4V and TIMER < 0.4V. When these four conditions are fulfilled, the initial cycle begins and the TIMER pin is pulled high with 1.9µA. At time point 3, the TIMER reaches $V_{TMR(H)}$ and is pulled down below $V_{TMR(L)}$ by the N-channel MOSFET pull-down, ending the initial cycle at time point 4. The initial cycle delay is:

$$t_{INITIAL} = 1.234V \bullet \frac{C_{TIMER}}{1.9\mu A} \quad (9)$$

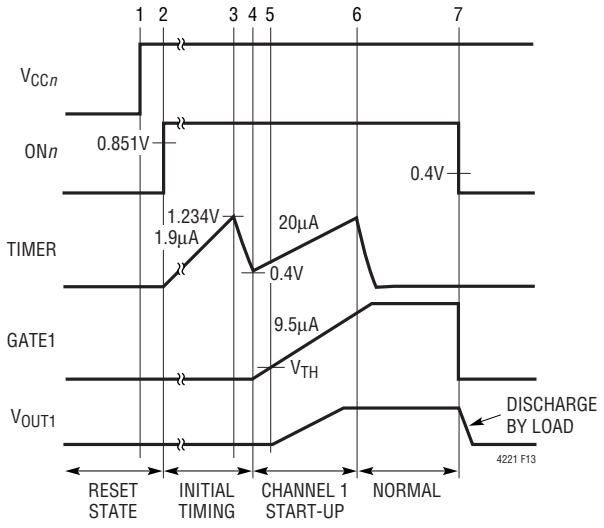

Figure 13. Channel 1 Start-Up Without Current Limit

At time point 4, the LTC4221 checks whether the FILTER pin is <1.24V and $\overline{FAULT}$ is > 0.851V. If both conditions are met, a channel start-up cycle commences.

Start-Up Cycle Without Current Limit

During a channel start-up cycle, the TIMER pin ramps up with a 20µA internal pull-up so the start-up cycle delay is:

$$t_{STARTUP} = (1.234V - 0.4V) \bullet \frac{C_{TIMER}}{20\mu A} \quad (10)$$

At the beginning of the start-up timing cycle (time point 4), the LTC4221's electronic circuit breaker is armed and each channel has an internal 9.5µA current source working with an internal charge pump to provide the gate drive to its external pass transistor. At time point 5, GATE1 reaches the external pass transistor threshold and V_{OUT1} starts to follow the GATE1 ramp-up. If the inrush current is below current limit, GATE1 ramps at a constant rate of:

$$\frac{\Delta V_{GATE}}{\Delta T} = \frac{I_{GATE}}{C_{GATE}} \quad (11)$$

where C_{GATE} is the total capacitance at the GATE1 pin. The inrush current through R_{SENSE1} can be divided into two components; I_{CLOAD} due to the total load capacitance C_{LOAD} and I_{LOAD} due to the noncapacitive load elements. The load bypass capacitance typically dominates C_{LOAD}. For a successful channel start-up without current limit, I_{INRUSH} < active current limit. Due to the voltage follower configuration, the V_{OUT1} ramp rate approximately tracks V_{GATE1}. The inrush current during a start-up cycle without current limit is :

$$I_{INRUSH} = \left(C_{LOAD} \bullet \frac{\Delta V_{OUT}}{\Delta T}\right) + I_{LOAD}$$

$$I_{INRUSH} = \left(C_{LOAD} \bullet \frac{\Delta V_{GATE}}{\Delta T}\right) + I_{LOAD} \quad (12)$$

$$I_{INRUSH} = \left(C_{LOAD} \bullet \frac{I_{GATE}}{C_{GATE}}\right) + I_{LOAD}$$

At time point 6, V_{OUT1} is approximately V_{CC1} but GATE1 ramp-up continues until it reaches a maximum voltage. This maximum voltage is determined either by the charge pump or the internal clamp.

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Start-Up Cycle With Current Limit

During a channel start-up cycle, if the inrush current as according to Equation (12) is large enough to cause a voltage drop greater than the active current limit threshold ($V_{SENSE(ACL)}$) across the sense resistor, an internal servo loop controls the operation of the 9.5µA current source at the GATE pin to regulate the load current to:

$$I_{INRUSH} = \frac{V_{SENSE(ACL)}}{R_{SENSE}} \quad (13)$$

The active current limit threshold for channel *n* has a component controlled by the voltage at the FB*n* pin. When FB*n* = 0V, $V_{SENSE(ACL)}$ = 9mV. As V_{OUTn} and FB*n* ramp up, $V_{SENSE(ACL)}$ increases linearly until FB*n* reaches 0.5V, where $V_{SENSE(ACL)}$ saturates at 25mV. In this fashion, the inrush current is controlled by this "foldback" limiting that tends to keep the power dissipation in the external MOSFET constant during the start-up cycle.

The timing diagram in Figure 14 illustrates the operation of the LTC4221 in a channel start-up cycle with limited inrush current as described by Equation 13. Between time points 5 and 6, the GATE2 pin ramps up with I_{GATE} = 9.5µA. At time point 6, the inrush current increases enough to trip $V_{SENSE(ACL)}(t)$ and an internal servo loop engages, limiting the inrush current to the level as in Equation 13 by decreasing I_{GATE} (<9.5µA). As a result, the ramp rate of both V_{GATE2} and V_{OUT2} decreases and V_{SENSE2} increases linearly until it saturates at 25mV at time point 7. At time point 8, the external MOSFET enters triode operation. I_{INRUSH} drops as the ramp rate of V_{OUT2} falls below that of V_{GATE2} so I_{GATE} reverts back to 9.5µA. At time point 9, the internal servo loop to control I_{INRUSH} is disengaged and channel 2 slow comparator is armed, ending the channel 2 start-up cycle. So if C_{LOAD2} is not fully charged up at this point, I_{INRUSH} will be subject to the slow comparator threshold and actions as outlined in the Electronic Circuit Breaker section. For a successful channel start-up, the current limited part of the V_{OUT} ramp-up (time points 6 and 8 of Figure 14) must not exceed the sum of start-up cycle delay as given by Equation 10 and the slow comparator response time as given by Equation 1. An example of an unsuccessful start-up is Figure 11 which shows a channel powering up into an overcurrrent at the load.

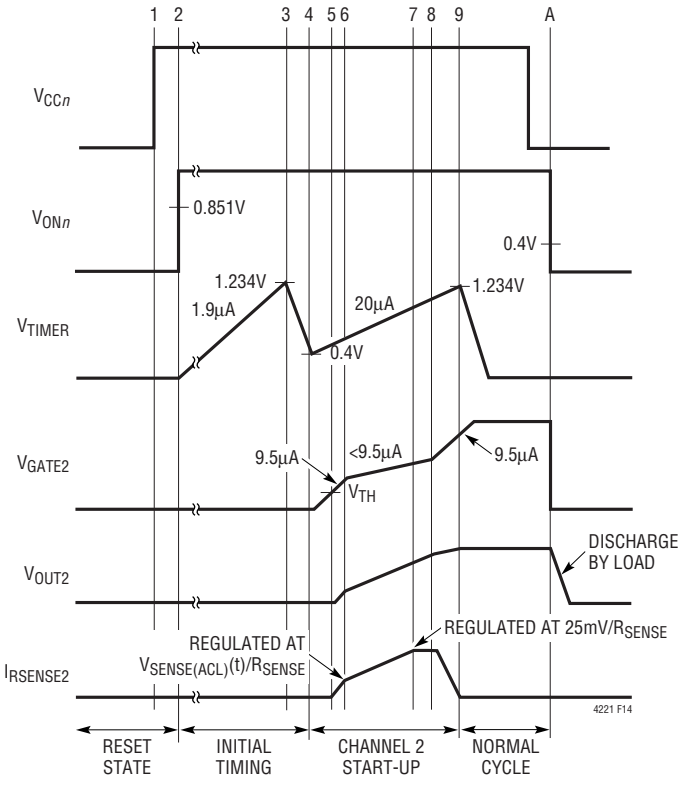

Figure 14. Channel 2 Start-Up with Current Limit

The fast comparators of both channels are armed at the end of the initial timing cycle at time point 4 of Figure 14. If a short circuit during the start-up cycle overrides the servo loop and causes V_{RSENSE} of either channel to exceed 100mV for more than 1µs, the electronic circuit breaker trips and the LTC4221 enters the fault state.

Frequency Compensation at Start-Up Cycle

If a channel's external gate input capacitance (C_{ISS}) is greater than 600pF, no external gate capacitor is required at GATE to stabilize the internal current-limiting loop during start-up with current limit. The servo loop that controls the external MOSFET during current limiting has a unity-gain frequency of about 105kHz and phase margin of 80° for external MOSFET gate input capacitances to 2.5nF.

Power MOSFET

Power MOSFETs can be classified by $R_{DS(ON)}$ at V_{GS} gate drive ratings of 10V, 4.5V, 2.5V and 1.8V. Those rated for $R_{DS(ON)}$ at 10V V_{GS} usually have a higher V_{GS} absolute maximum rating than those at 4.5V and 2.5V. At low

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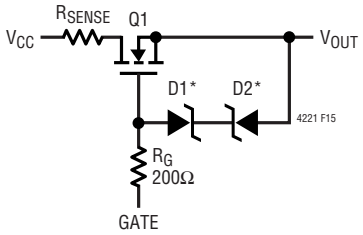
supply voltages, the LTC4221 can drive any MOSFET rated with 4.5V or 2.5V gate drive. For higher supply voltages up to 13.5V, the LTC4221 can drive any MOSFET rated with a 10V or 4.5V gate drive. The selected MOSFET should fulfill two V_{GS} criteria:

1. Positive V_{GS} absolute maximum rating > LTC4221's maximum ΔV_{GATE}.
2. Negative V_{GS} absolute maximum rating > supply voltage. The gate of the MOSFET can discharge faster than V_{OUT} when shutting down the MOSFET with a large C_{LOAD}.

If one of the conditions cannot be met, an external zener clamp shown on Figure 15 can be used. The clamp network is connected from each channel's GATE to the V_{OUT} pins. V_{GS} is clamped in both directions and R_G limits the current flow into the GATE*n* pin's internal zener clamp during transient events.

A MOSFET with a V_{GS} absolute maximum rating of ±20V meets the two criteria for all the LTC4221 application ranges from 1V to 13.5V. Typically most 10V gate rated MOSFETs have V_{GS} absolute maximum ratings of ±20V or greater, so no external V_{GS} zener clamp is needed. There are 4.5V gate rated MOSFETs with V_{GS} absolute maximum ratings of ±20V. In addition to the MOSFET gate drive rating and V_{GS} absolute maximum rating, other criteria such as V_{BDSS}, $I_{D(MAX)}$, $R_{DS(ON)}$, P_D, θ_{JA}, $T_{J(MAX)}$ and maximum safe operating area (SOA) should also be carefully reviewed. V_{BDSS} should exceed the maximum supply voltage inclusive of spikes and ringing. $I_{D(MAX)}$ must exceed the maximum short-circuit current in the channel during a fault



*USER SELECTED VOLTAGE CLAMP
(A LOW BIAS CURRENT ZENER DIODE IS RECOMMENDED)
1N4688 (5V)
1N4692 (7V): LOGIC-LEVEL MOSFET
1N4695 (9V)
1N4702 (15V): STANDARD-LEVEL MOSFET

Figure 15. Gate Protection Zener Clamp

condition. $R_{DS(ON)}$ determines the MOSFET V_{DS} which together with V_{RSENSE} yields an error in the V_{OUT} voltage. For example, at 1V V_{CC2}, V_{DS} + $V_{RSENSE2}$ = 50mV gives a 5% V_{OUT2} error. At higher V_{CC} voltages the V_{DS} requirement can be relaxed in which case the MOSFET's thermal requirements (P_D, $T_{J(MAX)}$, SOA) may limit the value of $R_{DS(ON)}$.

The power dissipated in the MOSFET is $(I_{LOAD})^2 \bullet R_{DS(ON)}$ and this should be less than the maximum power dissipation, P_D, allowed in that package. Given power dissipation, the MOSFET junction temperature, T_J can be computed from the operating temperature (T_A) and the MOSFET package thermal resistance (θ_{JA}). The operating T_J should be less than the $T_{J(MAX)}$ specification. The $V_{DS} \bullet I_{LOAD}$ figure must also be well within the manufacturer's recommended safe operating area (SOA) with sufficient margin. These three thermal parameters must not be exceeded for all conditions in a channel including normal mode operation, start-up with or without current limit, fault and autoretry after a fault. To ensure a reliable design, fault tests should be evaluated in the laboratory.

V_{CC} Transient Protection

Good engineering practice calls for bypassing the supply rail of any analog circuit. Bypass capacitors are often placed at the supply connection of every active device, in addition to one or more large value bulk bypass capacitors per supply rail. If power is connected abruptly, the large bypass capacitors slow the rate of rise of the supply voltage and heavily damp any parasitic resonance of lead or PC track inductance working against the supply bypass capacitors.

The opposite is true for LTC4221 Hot Swap circuits mounted on plug-in cards since controlling the surge current to bypass capacitors at plug-in is the primary motivation for the Hot Swap controller. In most cases, there is no supply bypass capacitor present on the powered supply voltage side of the MOSFET switch. Although wire harness, backplane and PCB trace inductances are usually small, these can create large spikes when large currents are suddenly drawn, cut off or limited. Abrupt intervention can prevent subsequent damage caused by a catastrophic fault but it does cause a large supply transient. These ringing transients appear as a fast edge on

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the input supply line, exhibiting a peak overshoot to 2.5 times the steady-state value. This peak is followed by a damped sinusoidal response whose duration and period are dependent on the resonant circuit parameters. This can cause detrimental damage to board components unless measures are taken.

The energy stored in the lead/trace inductance is easily controlled with snubbers and/or transient voltage suppressors. Even when ferrite beads are used for electromagnetic interference (EMI) control, the low saturating current of ferrite will not pose a major problem if the transient voltage suppressors with adequate ratings are used. The transient associated with a GATE turn off can be controlled with a snubber and/or transient voltage suppressor. Snubbers such as RC networks are effective especially at low voltage supplies. The choice of RC is usually determined experimentally. The value of the snubber capacitor is usually chosen between 10 to 100 times the MOSFET C_{OSS}. The value of the snubber resistor is typically between 3Ω to 100Ω. When the supply exceeds 7V or EMI beads exist in the wire harness, a transient voltage suppressor and snubber are recommended to clip off large spikes and reduce the ringing. For supply voltages of 6V or below, a snubber network should be sufficient to protect against transient voltages. These protection networks should be mounted very close to each of LTC4221's two supply voltages using short lead lengths to minimize lead inductance. This is shown schematically in the Typical Application on the front page of this data sheet. In many cases, a simple short-circuit test can be performed to determine the need of the transient voltage suppressor. Additional overvoltage protection is provided by the FB*n* pins.

PCB Layout Considerations

A recommended layout for the SENSE resistors, the power MOSFETs, V_{CC} transient protection devices and GATE drive components around the LTC4221 is shown in Figure 16. For proper operation of the LTC4221's electronic circuit breaker, a 4-wire Kelvin connection to each SENSE resistor is used. Also, PCB layout for the external N-channel MOSFETs emphasizes optimal thermal management of MOSFET power dissipation to keep θ_{JA} as low as possible. The V_{CC} transient protection devices are positioned close to the supply pins to reduce lead inductance and thus overshoot voltage.

In Hot Swap applications where load currents can reach 10A or more, PCB track width must be appropriately sized to keep track resistance and temperature rise to a minimum. Consult Appendix A of LTC Application Note 69 for details on sizing and calculating trace resistances as a function of copper thickness.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PC board. For 1oz copper foil plating, a good starting point is 1A of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

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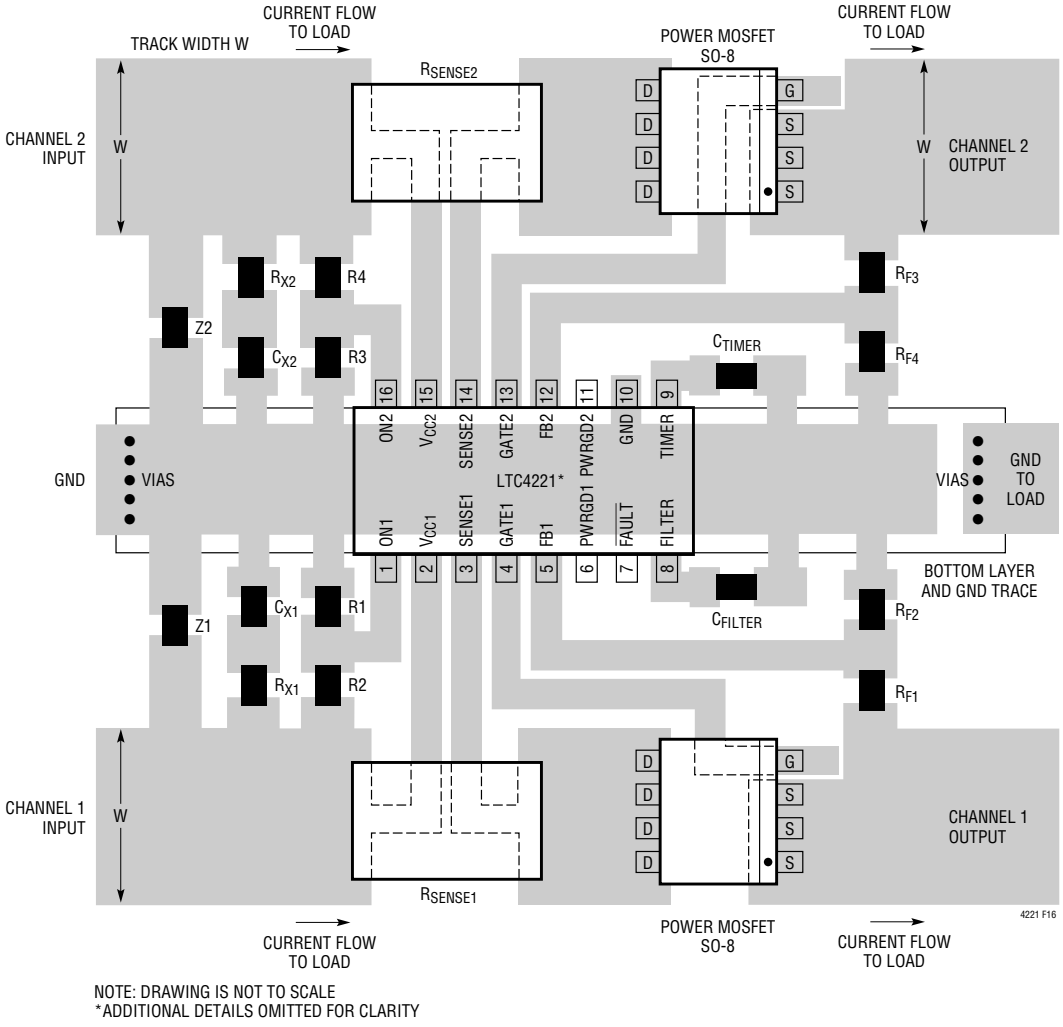


NOTE: DRAWING IS NOT TO SCALE
*ADDITIONAL DETAILS OMITTED FOR CLARITY

Figure 16. Recommended Layout for LTC4221 R_{SENSE}, Power MOSFETs and Feedback Networks

APPENDIX

Table 1 lists some current sense resistors that can be used with the circuit breaker. Table 2 lists some power MOSFETs that are available. Table 3 lists the web sites of several manufacturers. Since this information is subject to change, please verify the part numbers with the manufacturer.

Table 1. Sense Resistor Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LRF120601R020F	0.02Ω 0.5W 1% Resistor	IRC-TT
2A	LRF120601R010F	0.01Ω 0.5W 1% Resistor	IRC-TT
2.5A	WSL25127L000F	0.007Ω 1W 1% Resistor	Vishay-Dale
3.3A	WSL25126L000F	0.006Ω 1W 1% Resistor	Vishay-Dale
5A	WSL25124L000F	0.004Ω 1W 1% Resistor	Vishay-Dale
10A	WSL25122L000F	0.002Ω 1W 1% Resistor	Vishay-Dale

APPENDIX

Table 2. N-Channel Selection Guide

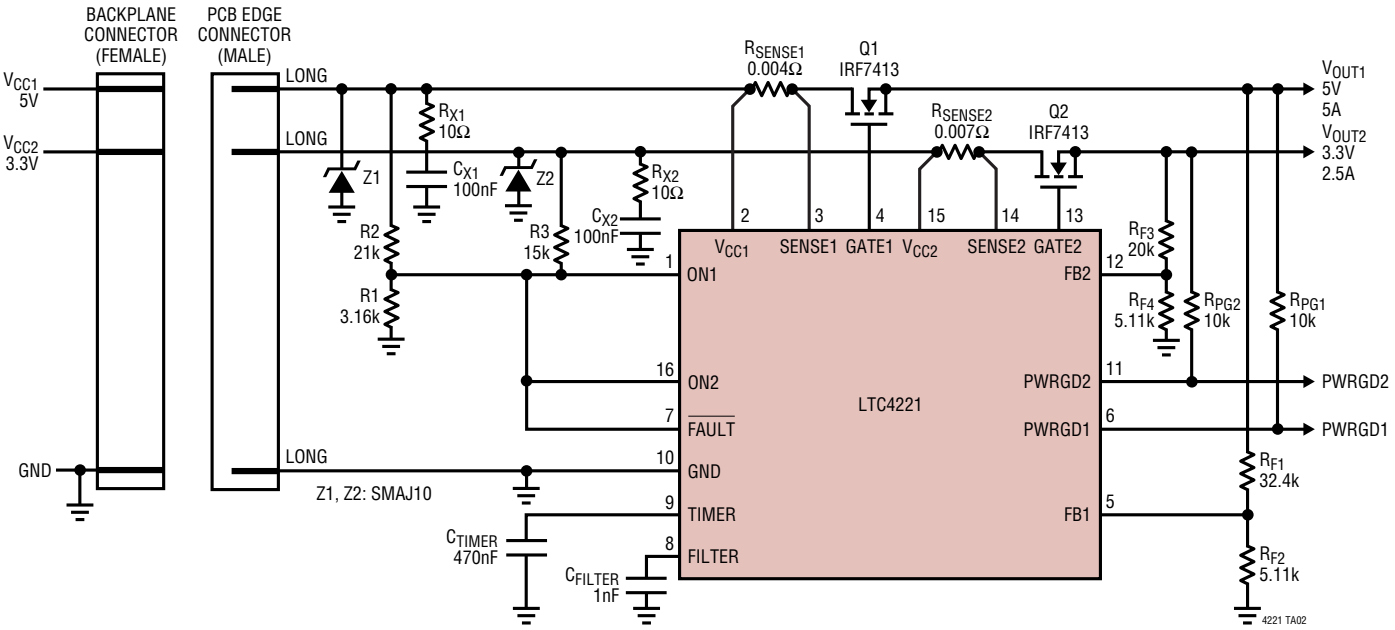
CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	MMDF3N02HD	Dual N-Channel SO-8 $R_{DS(ON)}$ = 0.1Ω, C_{ISS} = 455pF	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.025Ω, C_{ISS} = 1130pF	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.028Ω, C_{ISS} = 1570pF	ON Semiconductor
10 to 20	MTB75N05HD	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.0095Ω, C_{ISS} = 2600pF	ON Semiconductor

Table 3. Manufacturers' Web Sites

MANUFACTURER	WEB SITE
TEMIC Semiconductor	www.temic.com
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
Harris Semiconductor	www.semi.harris.com
IRC-TT	www.irctt.com
Vishay-Dale	www.vishay.com
Vishay-Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

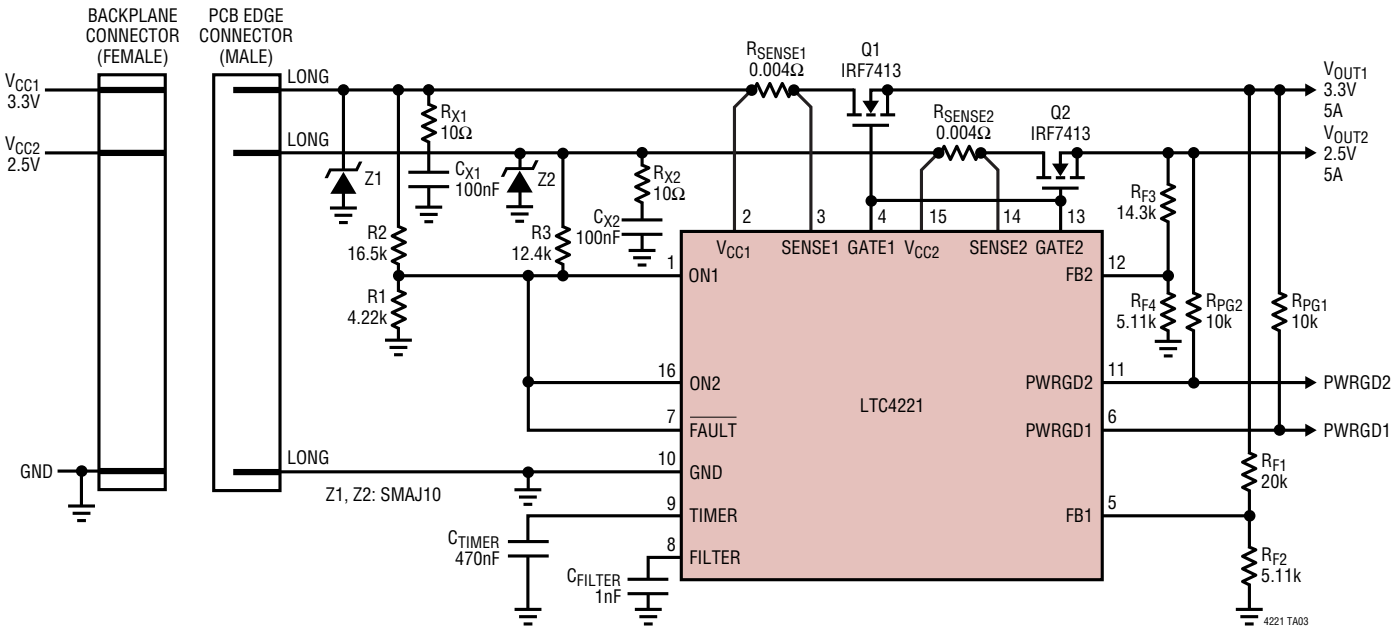
TYPICAL APPLICATIONS

Simultaneous Turn-On with Autoretry Function—Individual Current Limits

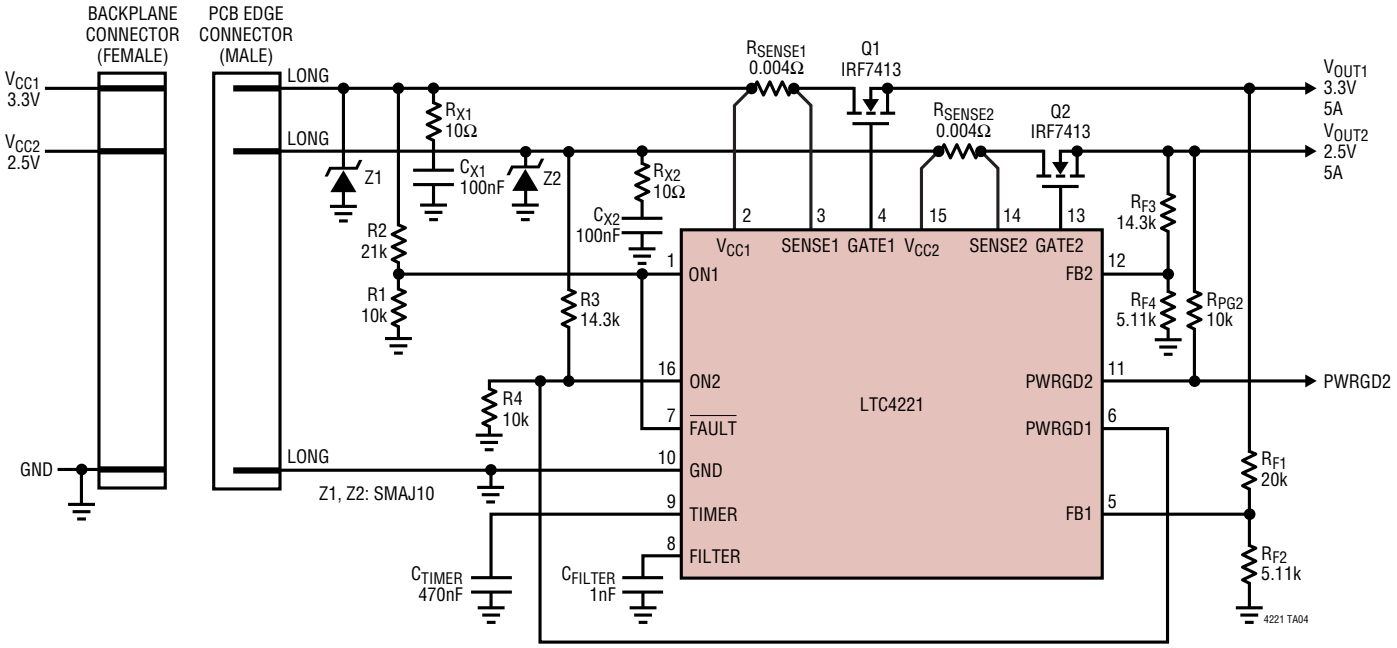


TYPICAL APPLICATIONS

Simultaneous Turn-On with Autoretry Function—Linked Current Limits

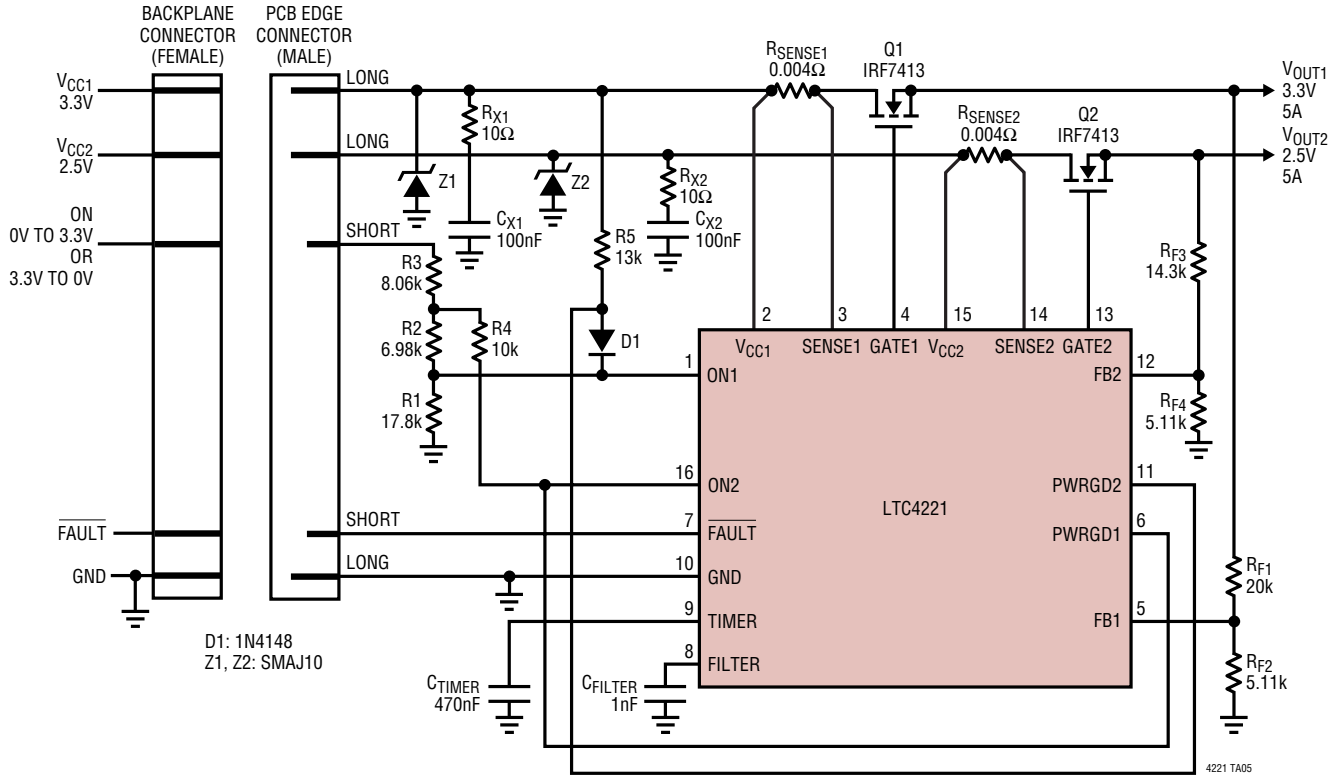


Sequenced Turn-On



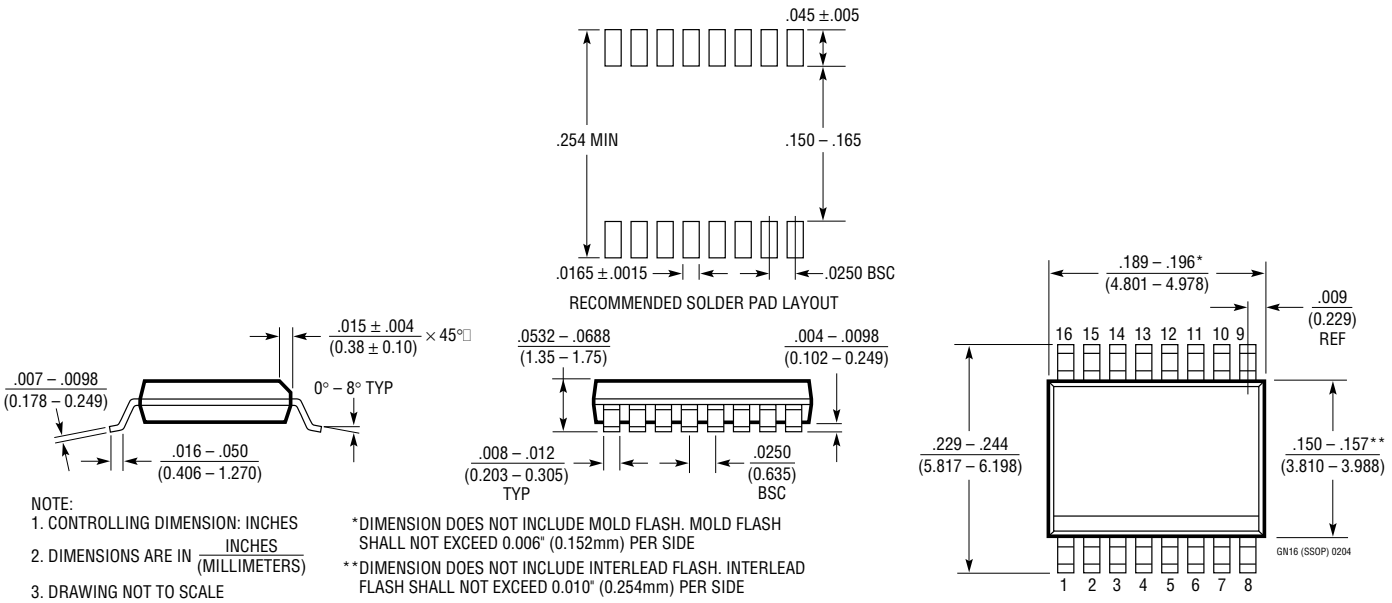
TYPICAL APPLICATIONS

Sequenced Up/Down, Channel 1 Up First, Down Last



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE