Dual Hot Swap Controller with I²C Compatible Monitoring

FEATURES

- **Allows Safe Insertion Into a Live Backplane**
- **10-Bit ADC Monitors Currents and Voltages**
- **I²C/SMBus Interface**
- **Wide Operating Voltage Range: 2.9V to 29V**
- **dI/dt Controlled Soft-Start**
- High Side Drive for External N-Channel MOSFETs
- No External Gate Capacitors Required
- Input Overvoltage/Undervoltage Protection
- Optional Latchoff or Auto-Retry After Faults
- Alert Host After Faults
- Inrush Current Limit with Foldback
- Available in 32-Pin (5mm × 5mm) QFN and 36-Pin SSOP Packages

APPLICATIONS

- Live Board Insertion
- Electronic Circuit Breakers
- Computers, Servers
- Platform Management

DESCRIPTION

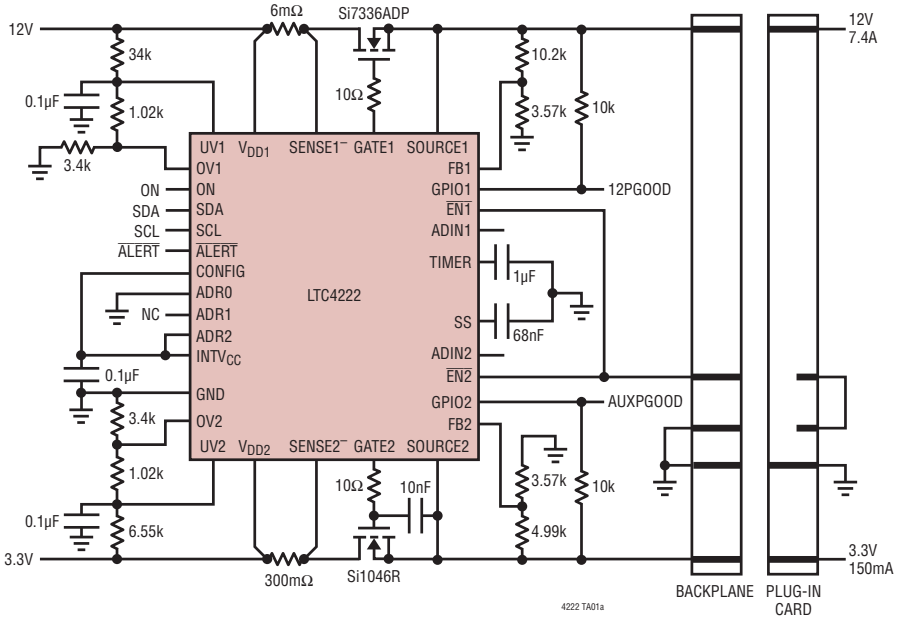
The LTC®4222 Hot Swap™ controller allows two power paths to be safely inserted and removed from a live backplane. Using external N-channel pass transistors, board supply voltages and inrush currents are ramped up at an adjustable rate. An I²C interface and onboard ADC allows for monitoring of current, voltage and fault status for each channel.

The device features adjustable, analog, foldback current limit circuits and a soft-start circuit that sets the dI/dt of the inrush currents. An I²C interface may configure the part to latch off or automatically restart after the LTC4222 detects a fault on either channel.

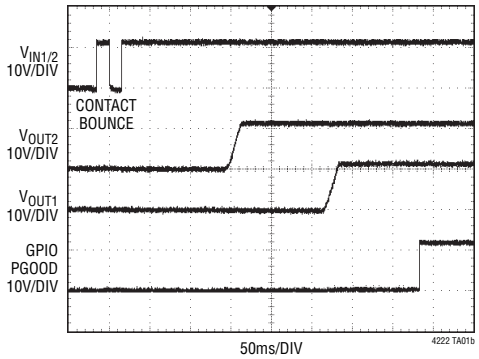
The controller has additional features to interrupt the host when a fault has occurred, notify when output power is good, detect insertion of a load card and power-up either automatically upon insertion or wait for an I²C command to turn on.

TYPICAL APPLICATION

Advanced Mezzanine Card Application



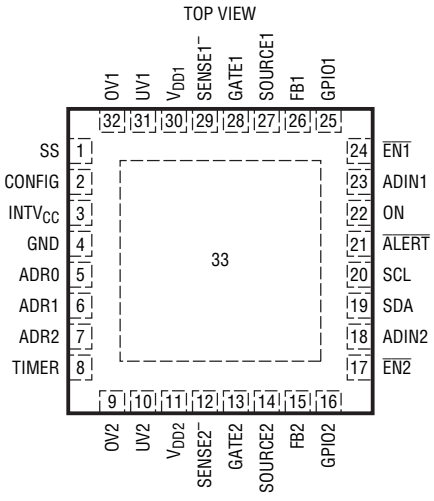
Start-Up Waveform with Sequencing



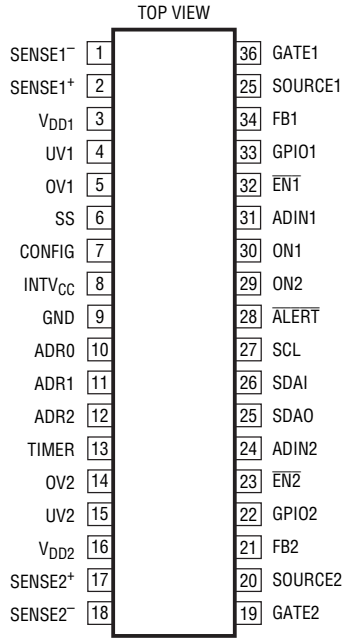
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages (V_{DDn}) ..... –0.3V to 35V
Supply Voltage ($INTV_{CC}$) ..... –0.3V to 6.5V
Input Voltages
GATEn – SOURCEn (Note 3) ..... –0.3V to 5V
$SENSE^+n$ ..... V_{DDn} – 6.5V to V_{DDn} + 0.3V
$SENSE^-n$ ..... –0.3V to $SENSE^+n$ + 0.3V
SOURCEn ..... –5V to 35V
UVn ..... –0.3V to $SENSE^+n$ + 0.3V
$\overline{EN}n$, FBn, ON, OVn ..... –0.3V to 12V
ADR0-2, TIMER, SS ..... –0.3V to $INTV_{CC}$ + 0.3V
ADINn, CONFIG ..... –0.3V to 12V
$\overline{ALERT}$, SCL, SDA, SDAI, SDAO ..... –0.3V to 6.5V
Output Voltages
GATEn, GPIOn ..... –0.3V to 35V
Operating Temperature Range
LTC4222C ..... 0°C to 70°C
LTC4222I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
SSOP ..... 300°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33), PCB GND CONNECTION OPTIONAL



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4222CG#PBF	LTC4222CG#TRPBF	LTC4222CG	36-Lead Plastic SSOP	0°C to 70°C
LTC4222IG#PBF	LTC4222IG#TRPBF	LTC4222IG	36-Lead Plastic SSOP	–40°C to 85°C
LTC4222CUH#PBF	LTC4222CUH#TRPBF	LTC4222	32-Lead (5mm × 5mm) Plastic QFN	0°C to 70°C
LTC4222IUH#PBF	LTC4222IUH#TRPBF	LTC4222	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{DDn}	Input Supply Range		●	2.9		29	V
I_{DD1}	V_{DD1} Input Supply Current	V_{DD1} = 12V	●		0.85	1.25	mA
I_{DD2}	V_{DD2} Input Supply Current	V_{DD2} = 12V, I_{INTVCC} = 0mA	●		3	4.5	mA
$V_{DDn(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.34	2.43	2.53	V
$V_{DDn(HYST)}$	Input Supply Undervoltage Lockout Hysteresis		●	60	80	100	mV
$INTV_{CC}$	Internal Regulator Voltage	I_{INTVCC} = 0mA	●	3.15	3.3	3.45	V
$INTV_{CC(UVL)}$	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising	●	2.55	2.64	2.73	V
$INTV_{CC(HYST)}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis		●	35	50	65	mV
Current Limit and Circuit Breaker (Both Channels)							
$\Delta V_{SENSE(TH)}$	Circuit Breaker Threshold (V_{DD} – V_{SENSE})		●	47.5 48.75	50 50	52.5 51.25	mV mV
ΔV_{SENSE}	Current Limit Voltage (V_{DD} – V_{SENSE})	V_{FB} = 1.3V V_{FB} = 0V Start-Up Timer Expired	● ● ●	46 14 130	50 16.6 150	54 19 165	mV mV mV
$t_{D(OC)}$	OC Fault Filter	ΔV_{SENSE} = 100mV	●	10	20	30	µs
$I_{SENSE(IN)}$	$SENSE^+$/$SENSE^-$ Pin Input Current	V_{SENSE} = 12V	●	0	20	45	µA
Gate Drive							
ΔV_{GATE}	External N-Channel Gate Drive (V_{GATE} – V_{SOURCE}) (Note 3)	V_{DD} = 2.9V to 29V	●	4.7	5.9	6.5	V
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate On, V_{GATE} = 0V	●	–8	–12	–18	µA
$I_{GATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Off, V_{GATE} = 15V	●	0.8	1	2.0	mA
$I_{GATE(LIM)}$	Pull-Down Current from GATE to SOURCE During OC/UVLO	V_{GATE} = 15V, (V_{DD} – V_{SENSE})n = 200mV			450		mA
$t_{PHL(SENSE)}$	(V_{DD} – SENSE) High to GATE Low	V_{DD} – SENSE = 200mV, C_{GATE} = 10nF	●		0.5	1	µs
$V_{GS(POWERBAD)}$	(GATE-SOURCE) Voltage for Power Bad Fault	V_{SOURCE} = 2.9V to 29V	●	3.8	4.3	4.7	V
Comparator Inputs							
$V_{INPUT(TH)}$	CONFIG, $\overline{EN}$, FB, ON, OV and UV Input Threshold	V_{IN} Rising	●	1.215	1.235	1.255	V
$\Delta V_{CONFIG,\overline{EN},ON(HYST)}$	CONFIG, $\overline{EN}$, ON Hysteresis		●	80	128	180	mV
$\Delta V_{FB(HYST)}$	FB Power Good Hysteresis		●	2	7	20	mV
$\Delta V_{OV(HYST)}$	OV Hysteresis		●	16	24	32	mV
$\Delta V_{UV(HYST)}$	UV Hysteresis		●	60	90	110	mV
$I_{(IN)}$	CONFIG, FB, ON, OV and UV Input Current	V_{IN} = 3V	●		0	±1	µA
$I_{\overline{EN}(UP)}$	$\overline{EN}$ Pull-Up Current	$V_{\overline{EN}}$ = 0V	●	5	10	20	µA
$V_{UV(RTH)}$	UV Reset Threshold Voltage	V_{UV} Falling	●	0.36	0.4	0.46	V
$\Delta V_{UV(RHYST)}$	UV Reset Threshold Hysteresis		●	60	125	180	mV
$V_{GPIO(TH)}$	GPIO Input Threshold	V_{GPIO} Rising	●	0.8	1	1.2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Other Pin Functions							
$V_{GPIO(OL)}$	GPIO Output Low Voltage	I_{GPIO} = 5mA	●		0.25	0.4	V
$I_{GPIO(OH)}$	GPIO Input Leakage Current	V_{GPIO} = 15V	●		0	±1	µA
I_{SOURCE}	SOURCE Input Current	SOURCE = 15V	●	70	115	170	µA
$t_{P(GATE)}$	Input (ON, OV, UV, $\overline{EN}$) to GATE Off Propagation Delay		●		3	5	µs
$t_{D(GATE)}$	GATE Turn-On Delay	ON UV, OV, $\overline{EN}$ Overcurrent Auto-Retry	● ● ●	 75 4.2	4 100 5	8 125 6.7	µs ms s
$V_{TIMERL(TH)}$	TIMER Low Threshold		●	0.18	0.2	0.22	V
$V_{TIMERH(TH)}$	TIMER High Threshold		●	1.215	1.235	1.260	V
$I_{TIMER(UP)}$	TIMER Pull-Up Current		●	90	100	110	µA
$I_{TIMER(DOWN)}$	TIMER Pull-Down Current for OC Auto-Retry		●	1.6	2.15	2.6	µA
$I_{TIMER(UP/DOWN)}$	TIMER Pin OC Auto-Retry Duty Cycle		●	38	50	58	N/A
I_{SS}	Soft-Start Ramp Pull-Up Current	Ramping Waiting for GATE to Slew	● ●	7.5 0.5	10 0.75	12.5 0.95	µA µA
ADC							
RES	Resolution (No Missing Codes)		●	10			Bits
V_{FS}	Full-Scale Voltage (1023 • V_{LSB})	(V_{DD} – SENSE) SOURCE ADIN			64 32 1.28		mV V V
LSB	LSB Step Size	(V_{DD} – SENSE) SOURCE ADIN			62.5 31.25 1.25		µV mV mV
V_{OS}	Offset Error	(V_{DD} – SENSE) SOURCE ADIN	● ● ●			±3 ±2 ±2	LSB LSB LSB
INL	Integral Nonlinearity	(Note 5)	●			±0.5	LSB
TUE	Total Unadjusted Error/Full-Scale Error	(V_{DD} – SENSE) SOURCE ADIN	● ● ●			±1.5 ±1 ±1	% % %
R_{ADIN}	ADIN Sampling Resistance	V_{ADIN} = 1.28V	●	1	2		MΩ
I_{ADIN}	ADIN Input Current	V_{ADIN} = 1.28V	●		0	±0.1	µA
	Conversion Rate				15		Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Interface							
$V_{ADR(H)}$	ADR0, ADR1, ADR2 Input High Voltage		●	$INTV_{CC}$ – 0.8	$INTV_{CC}$ – 0.4	$INTV_{CC}$ – 0.2	V
$I_{ADR(IN,Z)}$	ADR0, ADR1, ADR2 Hi-Z Input Current	ADR0, ADR1, ADR2 = 0.8V, $INTV_{CC}$ – 0.8V	●	5	0	–5	µA
$V_{ADR(L)}$	ADR0, ADR1, ADR2 Input Low Voltage		●	0.2	0.4	0.8	V
$I_{ADR(IN)}$	ADR0, ADR1, ADR2 Input Current	ADR0, ADR1, ADR2 = 0V, $INTV_{CC}$	●	–80		80	µA
$V_{\overline{ALERT}(OL)}$	$\overline{ALERT}$ Output Low Voltage	$I_{\overline{ALERT}}$ = 3mA	●		0.2	0.4	V
$I_{\overline{ALERT}(OH)}$	$\overline{ALERT}$ Input Current	$\overline{ALERT}$ = $INTV_{CC}$	●			±1	µA
$V_{SDA,SCL(TH)}$	SDA, SCL Input Threshold		●	1.5	1.7	1.9	V
$I_{SDA,SCL(OH)}$	SDA, SCL Input Current	SCL, SDA = $INTV_{CC}$	●			±1	µA
$V_{SDA(OL)}$	SDA Output Low Voltage	I_{SDA} = 3mA	●		0.2	0.4	V
I²C Interface Timing							
$f_{SCL(MAX)}$	SCL Clock Frequency	Operates with $f_{SCL} \le f_{SCL(MAX)}$		400	1000		kHz
$t_{BUF(MIN)}$	Bus Free Time Between Stop/Start Condition				0.12	1.3	µs
$t_{HD,STA(MIN)}$	Hold Time After (Repeated) Start Condition				100	600	ns
$t_{SU,STA(MIN)}$	Repeated Start Condition Set-Up Time				30	600	ns
$t_{SU,STO(MIN)}$	Stop Condition Set-Up Time				140	600	ns
$t_{HD,DAT(MIN)}$	Data Hold Time (Input)				30	100	ns
$t_{HD,DATO}$	Data Hold Time (Output)			300	600	900	ns
$t_{SU,DAT(MIN)}$	Data Set-Up Time				30	600	ns
t_{SP}	Suppressed Spike Pulse Width			50	110	250	ns
t_{RST}	Stuck-Bus Reset Time	SCL or SDA Held Low		25	32	40	ms
C_X	SCL, SDA Input Capacitance	SDAI Tied to SDAO (Note 5)				10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a minimum of 5V above SOURCE. Driving this pin to voltages beyond the clamp may damage the device.

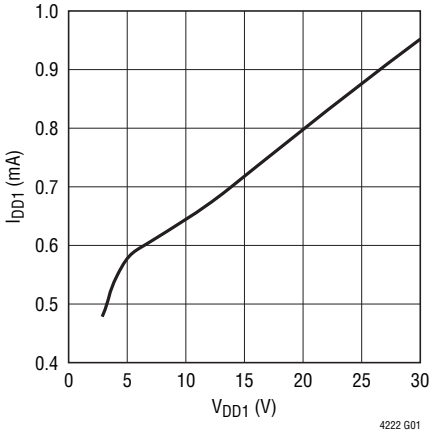
Note 4: Integral Nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size and the single shot measurement. Typical specifications are measured from 1/4, 1/2, 3/4 areas of the quantization band.

Note 5: Guaranteed by design and not subject to test.

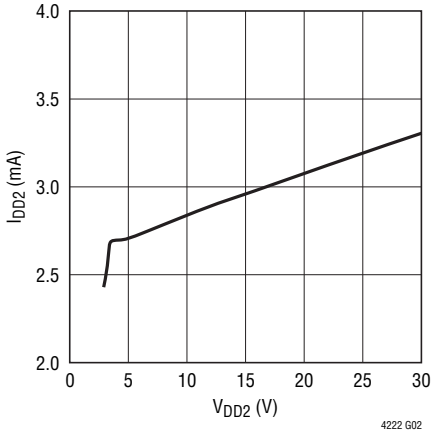
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{DDn} = 12V unless otherwise noted.

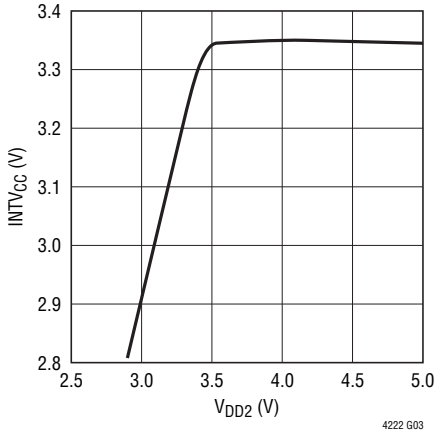
I_{DD1} vs V_{DD1}



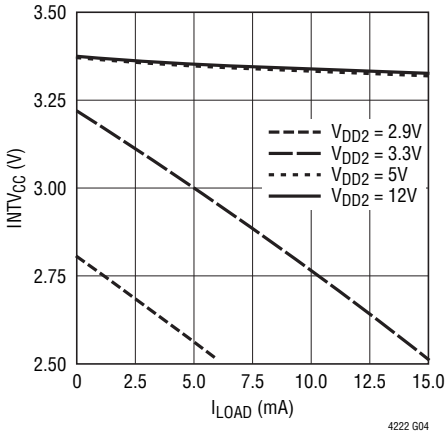
I_{DD2} vs V_{DD2}



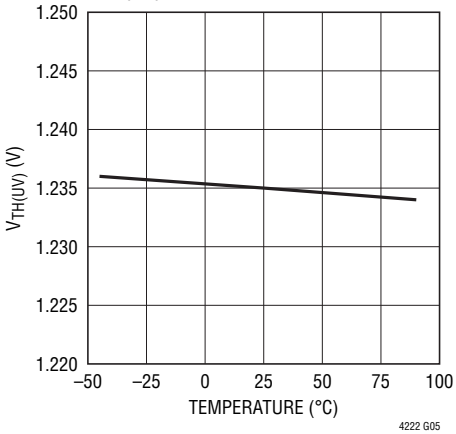
$INTV_{CC}$ vs V_{DD2}



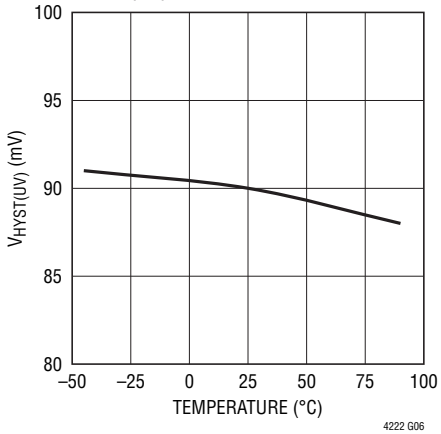
$INTV_{CC}$ vs I_{LOAD}



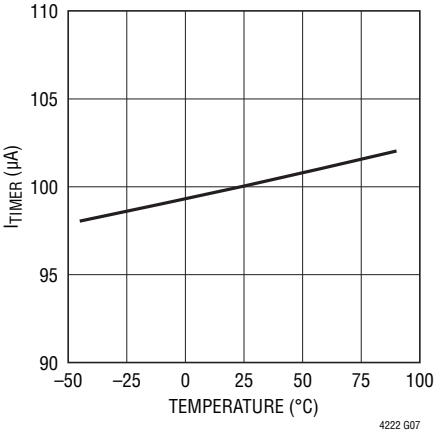
$V_{TH(UV)}$ vs Temperature



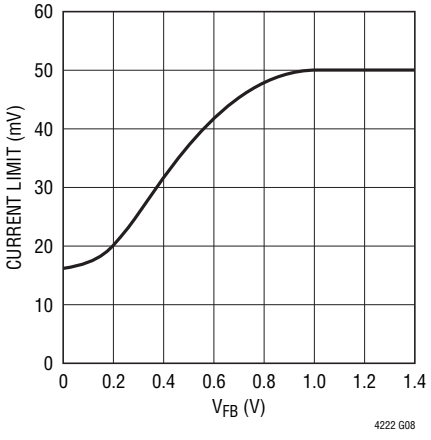
$V_{HYST(UV)}$ vs Temperature



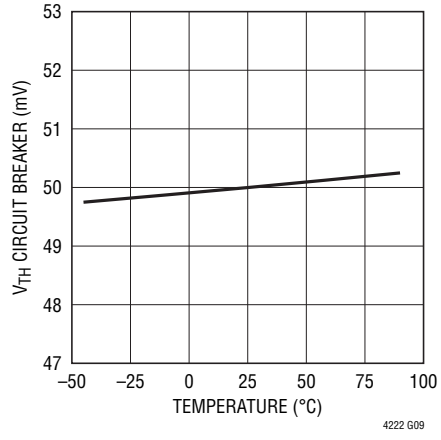
I_{TIMER} vs Temperature



Current Limit vs V_{FB}



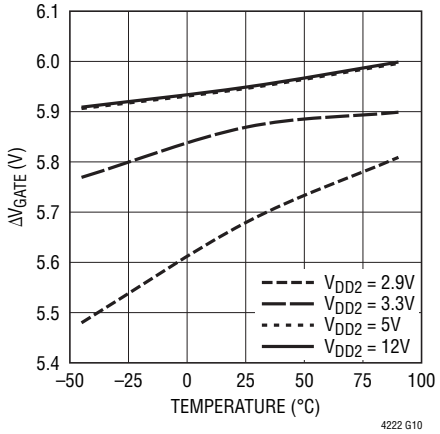
V_{TH} Circuit Breaker vs Temperature



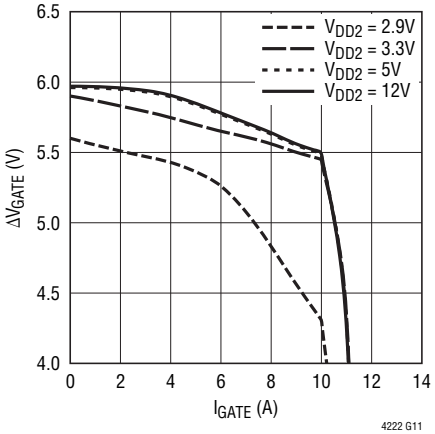
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{DDn} = 12V unless otherwise noted.

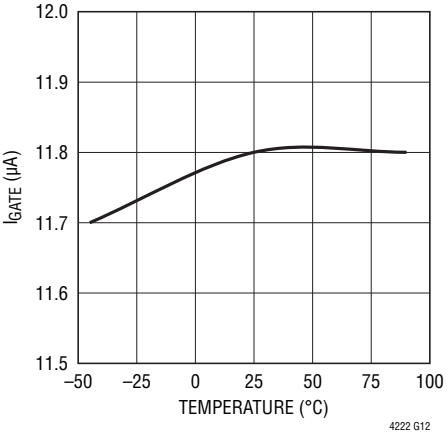
ΔV_{GATE} vs Temperature



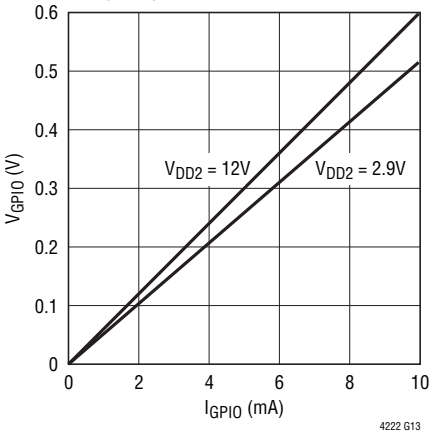
ΔV_{GATE} vs I_{GATE}



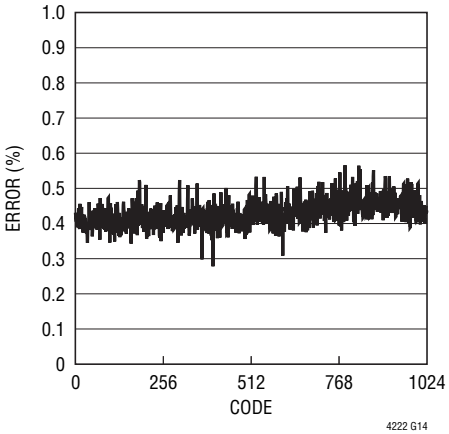
I_{GATE} vs Temperature



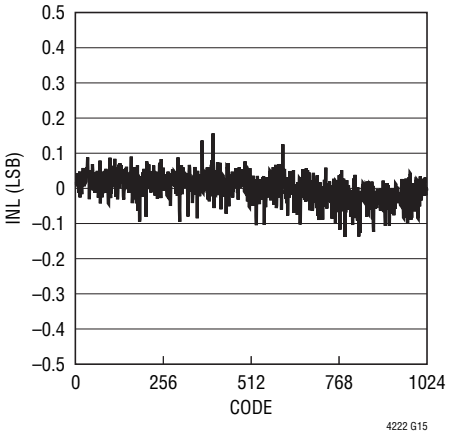
$V_{OL(GPIO)}$ vs I_{GPIO}



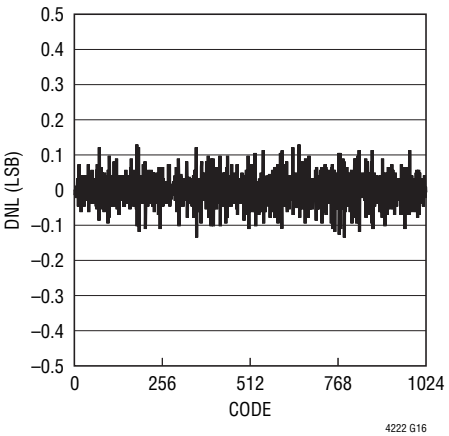
ADC Total Unadjusted Error vs CODE (ADIN1)



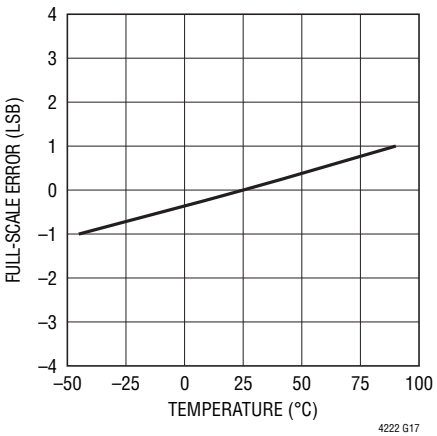
ADC INL vs CODE (ADIN1)



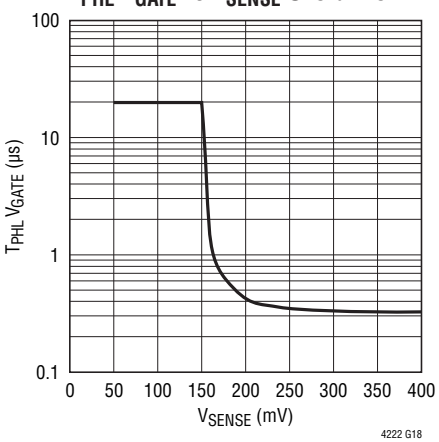
ADC DNL vs CODE (ADIN1)



ADC Full-Scale Error vs Temperature



T_{PHL} V_{GATE} vs V_{SENSE} Overdrive



PIN FUNCTIONS

ADIN: ADC Input. A voltage between 0 and 1.28V applied to this pin is measured by the on-board ADC. Tie to ground if unused.

ADR0, ADR1, ADR2: Serial Bus Address Inputs. Tying these pins to ground, open, or $INTV_{CC}$ configures one of 27 possible addresses. See Table 1 in Applications Information.

$\overline{ALERT}$: Fault Alert Output. Open-drain logic output that is pulled to ground when a fault occurs to alert the host controller. A fault alert is enabled by setting the corresponding bit in the $\overline{ALERT}$ register as shown in Table 4. See Applications Information. Tie to ground if unused.

CONFIG: Configuration Input. Configures the part to control the two channels together or independently. When CONFIG is tied to GND both channels start up at the same time. A fault, $\overline{EN}$ or ON turn-off command on either channel will shut down both channels. When CONFIG is tied to $INTV_{CC}$, either channel can start up independently. A fault, $\overline{EN}$ or ON turn-off command will result in the associated channel turning off, while the other channel remains on. If one channel is commanded to turn on while another channel is in the turn-on sequence, the LTC4222 waits until the first channel has finished its turn-on sequence before turning on the second channel.

$\overline{EN1}$, $\overline{EN2}$: Enable Input. Ground this pin to indicate a board is present and enable the N-channel MOSFET to turn-on. When this pin is high, the MOSFET is not allowed to turn on. An internal 10µA current source pulls up this pin. Transitions on this pin are recorded in the FAULT register. A high-to-low transition activates the logic to read the state of the ON pin and clear faults. See Applications Information.

EXPOSED PAD: (Pin 33, QFN Package) Exposed Pad. May be left open or connected to device ground.

FB1, FB2: Foldback Current Limit and Power-Good Input. A resistive divider from the output is tied to this pin. When the voltage at this pin drops below 1.235V, power is not considered good. The power bad condition may result in the GPIO pin pulling low or going high impedance depending on the configuration of CONTROL register bits 6 and 7. Also a power bad fault is logged when the FB pin is low, the LTC4222 has finished the startup cycle and the GATE pin is high. See Applications Information. The start-up current limit folds back from 50mV sense voltage to 16.6mV as the FB voltage drops from 0.8V to 0.2V. Foldback is not active once the part leaves startup and the current limit is increased to 150mV.

GATE1, GATE2: Gate Drive for External N-Channel MOSFET. An internal 12µA current source charges the gate of the MOSFET. No compensation capacitor is required on the GATE pin, but a resistor and capacitor network from this pin to ground may be used to set the turn-on output voltage slew rate. During turn-off there is a 1mA pull-down current. During a short circuit or undervoltage lockout (V_{DD} or $INTV_{CC}$), a 450mA pull-down current source between GATE and SOURCE is activated.

GND: Device Ground.

GPIO1, GPIO2: General Purpose Input/Output. Open-drain logic output or logic input. Defaults to an output set to pull low to indicate power is not good. Configure according to Table 3.

$INTV_{CC}$: Low Voltage Supply Decoupling Output. Connect a 0.1µF capacitor from this pin to ground.

ON: (QFN Package) On Control Input. Formed by internally tying the ON1 and ON2 lines together.

ON1, ON2: (SSOP Package) On Control Inputs. A rising edge turns on the external N-channel FET and a falling edge turns it off. This pin also configures the state of the FET ON register bit (and hence the external FET) at power up. For example, if the ON pin is tied high, then the FET ON bit (Control bit 3 in Table 3) goes high 100ms after power-up. Likewise if the ON pin is tied low then the channel remains off after power-up until the FET ON bit is set high using the I^2C bus. A high-to-low transition on this pin clears the fault register for the related channel. The two ON pins are tied together internally on the QFN package.

OV1, OV2: Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin rises above 1.235V, an overvoltage fault is detected and the GATE turns off. Tie to GND if unused.

PIN FUNCTIONS

SCL: Serial Bus Clock Input. Data at the SDA pin is shifted in or out on rising edges of SCL. This is a high impedance pin that is generally driven by an open-collector output from a master controller. An external pull-up resistor or current source is required.

SDAO: (SSOP Package) Serial Bus Data Output. Open-drain output for sending data back to the master controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required. Internally tied to SDAI in QFN package.

SDAI: (SSOP Package) Serial Bus Data Input. A high impedance input for shifting in address, command or data bits. Normally tied to SDAO to form the SDA line. Internally tied to SDAO in QFN package.

SDA: (QFN Package) Serial Bus Data Input/Output Line. Formed by internally tying the SDAO and SDAI lines together. An external pull-up resistor or current source is required.

SENSE1$^-$, SENSE2$^-$: Negative Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls the corresponding GATE pin voltage to limit the sense voltage between the SENSE$^+$ and SENSE$^-$ pins to the level set by the soft-start and foldback characteristic, with a maximum of 50mV during start-up and to 150mV independent of soft-start and foldback after the start-up timer has expired. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 50mV for 20µs.

SENSE1$^+$, SENSE2$^+$: (SSOP Package) Positive Current Sense Input. Connect this pin to the input of the current sense resistor. It must be connected to the same trace as V_{DDn}. Internally tied to V_{DDn} in the QFN package.

SOURCE1, SOURCE2: N-Channel MOSFET Source and ADC Input. Connect this pin to the source of the external N-channel MOSFET switch for gate drive return. This pin also serves as the ADC input to monitor output voltage. The pin provides a return for the gate pull-down circuit.

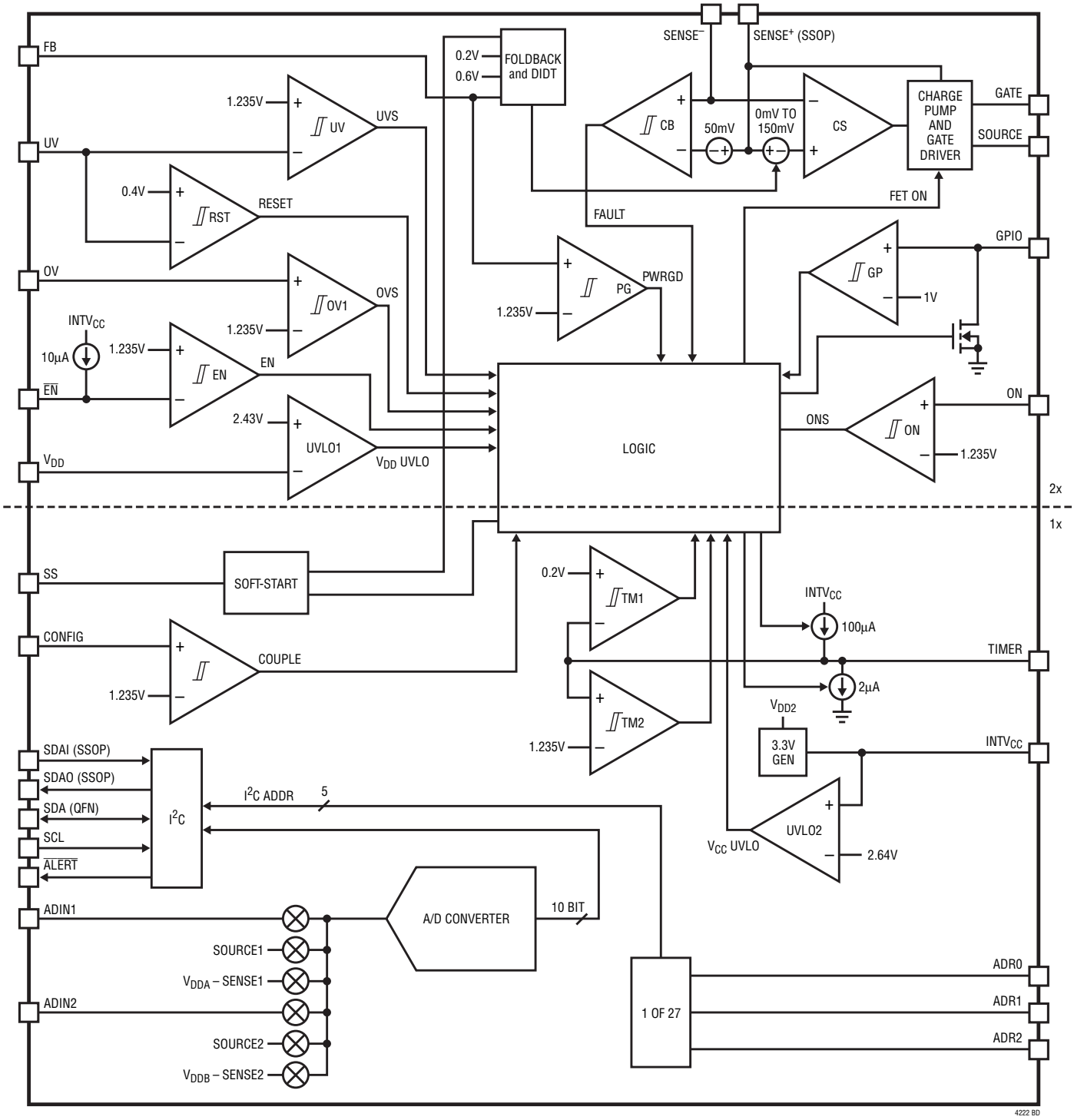
SS: Soft-Start Input. Sets the inrush current slew rate at start-up. Connect a 68nF capacitor to provide 5mV/ms as the slew rate for the sense voltage in start-up. This corresponds to 1A/ms with a 5mΩ sense resistor. Note that a large soft-start capacitor and a small TIMER capacitor may result in a condition where the timer expires before the inrush current has started. Allow an additional 2nF of timer capacitance per 1nF of soft-start capacitor to ensure proper start-up.

TIMER: Start-Up Timer Input. Connect a capacitor between this pin and ground to set a 12.3ms/µF duration for start-up, after which an overcurrent fault is logged if the inrush is still current limited. The duration of the off time is 600ms/µF when overcurrent auto-retry is enabled, resulting in a 1:50 duty cycle. An internal timer provides a 100ms start-up time and 5 second auto-retry time if this pin is tied to $INTV_{CC}$. Allow an additional 2nF of timer capacitance per 1nF of soft-start (SS) capacitor to ensure proper start-up.

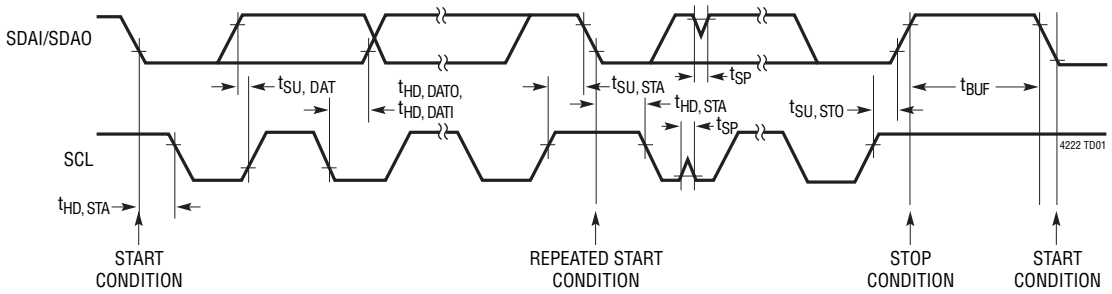
UV1, UV2: Undervoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin falls below 1.145V, an undervoltage fault is detected and the GATE turns off. Pulling this pin below 0.4V resets the fault register for that channel except for the UV fault bit. Tie to $INTV_{CC}$ if unused.

V_{DD1}, V_{DD2}: Supply Voltage Input and Positive Current Sense Input. This pin has an undervoltage lockout threshold of 2.43V. In the QFN package this pin is also the positive current sense input.

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



OPERATION

The LTC4222 is designed to turn two supply voltages on and off in a controlled manner, allowing boards to be safely inserted or removed from a live backplane. During normal operation, the charge pump and gate drivers turn on external N-channel MOSFET gates to pass power to the loads. The gate driver circuits use a charge pump that derives its power from the V_{DD1} or V_{DD2} pin, whichever is higher. Also included in the gate driver circuits are internal 6.5V GATE-to-SOURCE clamps to protect the oxide of logic-level MOSFETs. During start-up the inrush currents are tightly controlled by using current limit foldback, soft-start dI/dt limiting and output dI/dt limiting. The LTC4222 is capable of controlling both channels independently, or coupling control signals so that both channels start up and turn off together.

The current sense (CS) amplifiers monitor the load currents using the difference between the $SENSE^+$ (V_{DD} for QFN) and $SENSE^-$ pin voltages. A CS amplifier limits the current in the load by pulling back on the GATE-to-SOURCE voltage in an active control loop when the sense voltage exceeds the commanded value. The CS amplifiers require 20µA input bias current from both the $SENSE^+$ and the $SENSE^-$ pins.

A short circuit on an output to ground results in excessive power dissipation during active current limiting. To limit this power, the corresponding CS amplifier regulates the voltage between the $SENSE^+$ and $SENSE^-$ pins at 150mV.

If an overcurrent condition persists, the internal circuit breaker (CB) registers a fault when the sense voltage exceeds 50mV for more than 20µs. This indicates to the logic that it is time to turn off the GATE to prevent overheating. At this point the TIMER capacitor starts to discharge with the 2µA current source until the voltage drops below 0.2V (comparator TM1) which tells the logic that the pass transistor has cooled and it is safe to turn on again if overcurrent auto-retry is enabled. If the TIMER pin is tied to $INTV_{CC}$, the cool-down time defaults to 5 seconds using an internal system timer.

The output voltages are monitored using the FB resistive divider and the power good (PG) comparators to determine when output voltages are acceptable for the loads. The power good conditions are signaled by the GPIO1 and GPIO2 pins using open-drain pull-down transistors. The GPIO pins may also be independently configured to signal power bad, or as general purpose inputs (GP comparators), or general purpose open-drain outputs.

The Functional Diagram shows the monitoring blocks of the LTC4222. The group of comparators on the left side includes the undervoltage (UV), overvoltage (OV), reset (RST), enable ($\overline{EN}$) and on (ON) comparators for channel 1 or 2. These comparators determine if the external conditions are valid prior to turning on their corresponding GATE. The two undervoltage lockout circuits, UVLO1 and UVLO2, validate the input supplies and the internally generated 3.3V supply, $INTV_{CC}$. UVLO2 also generates the power-up initialization to the logic circuits as $INTV_{CC}$ crosses this rising threshold.

The CONFIG pin is used to select the desired start-up behavior of the LTC4222. When the CONFIG pin is low, both channels will start up and turn off simultaneously and a fault on either channel will result in both channels turning off, or prevent both channels from starting up.

OPERATION

When the CONFIG pin is high the two channels work completely independently and ignore the behavior of the other channel. This allows for the channels to start up in sequence by connecting the GPIO (power good) output of one channel to the UV pin of the other channel.

The two channels share the TIMER and SS (soft-start) pins that control start-up behavior. If the CONFIG pin is high and one channel is enabled while the other channel is starting up, the LTC4222 will wait for the start-up cycle to end before starting up the second channel to ensure that it gets a full timer cycle. The exception to this is the ON pins, which turn on the corresponding channel immediately. When both channels start up simultaneously, the inrush current for both channels is limited by whichever FB pin is lowest.

Included in the LTC4222 is a 10-bit A/D signal. The 6-input multiplexer ahead of the A/D converter allows to select between the two ADIN pins, the two SOURCE pins and the two current sense devices.

An I^2C interface is provided to read the A/D registers. It also allows the host to poll the device and determine if faults have occurred. If the $\overline{ALERT}$ line is configured as an interrupt, the host is enabled to respond to faults in real time. The SDA line is divided into an SDAI (input) and SDAO (output). This simplifies applications using an optoisolator driven directly from the SDAO output. The I^2C device address is forwarded to the address decoder from the ADR0, ADR1 and ADR2 pins. These inputs have three states each that decode into a total of 27 device addresses.

APPLICATIONS INFORMATION

A typical LTC4222 application is in a high availability system in which two positive voltage supplies are distributed to one or more cards. The device measures card voltages and currents and records past and present fault conditions for both channels. The system queries each LTC4222 over the I^2C periodically and reads status and measurement information.

A basic LTC4222 application circuit is shown in Figure 1. The following sections cover turn-on, turn-off and acts upon various faults that the LTC4222 detects. External component selection is discussed in detail in the Design Example section.

Turn-On Sequence

The power supplies on a board are controlled by using external N-channel pass transistors (Q1 and Q2) placed in the power path. Note that resistor R_{Sn} provides current detection. Resistors R1n, R2n and R3n define undervoltage and overvoltage levels for the two channels. R5n prevents high frequency oscillations in Qn and R6n. C1n forms an optional network that may be used to provide an output dV/dt limited start-up.

Several conditions must be present before the external MOSFET for a given channel turns on. First the external supplies, V_{DDn}, must exceed their 2.44V undervoltage lockout levels. Next the internally generated supply, $INTV_{CC}$, must cross its 2.64V undervoltage threshold. This generates a 60µs to 120µs power-on-reset pulse. During reset the fault registers are cleared and the control registers are set or cleared as described in the register section.

After a power-on-reset pulse, the LTC4222 goes through the following turn-on sequence for one or both channels. First the UV and OV comparators indicate that input power is within the acceptable range, which is indicated by STATUS bits 0 to 1 in Table 5. Second, the $\overline{EN}$ pin is externally pulled low. Finally, all of these conditions must be satisfied for the duration of 100ms to ensure that any contact bounce during insertion has ended. Additionally, if the CONFIG pin is low all initial conditions for both channels must be met before the pair are allowed to turn on together.

When these initial conditions are satisfied, the ON pin is checked and its state written to bit 3 in the CONTROL register (Table 3). If it is high, the external MOSFET is turned on. If the ON pin is low, the external MOSFET is turned on when the ON pin is brought high or if a serial bus turn-on command is sent by setting CONTROL bit 3. If the CONFIG pin is low, either both ON pins must be high or both CONTROL registers third bits must be set in order for the external MOSFETs to be turned on simultaneously.

APPLICATIONS INFORMATION

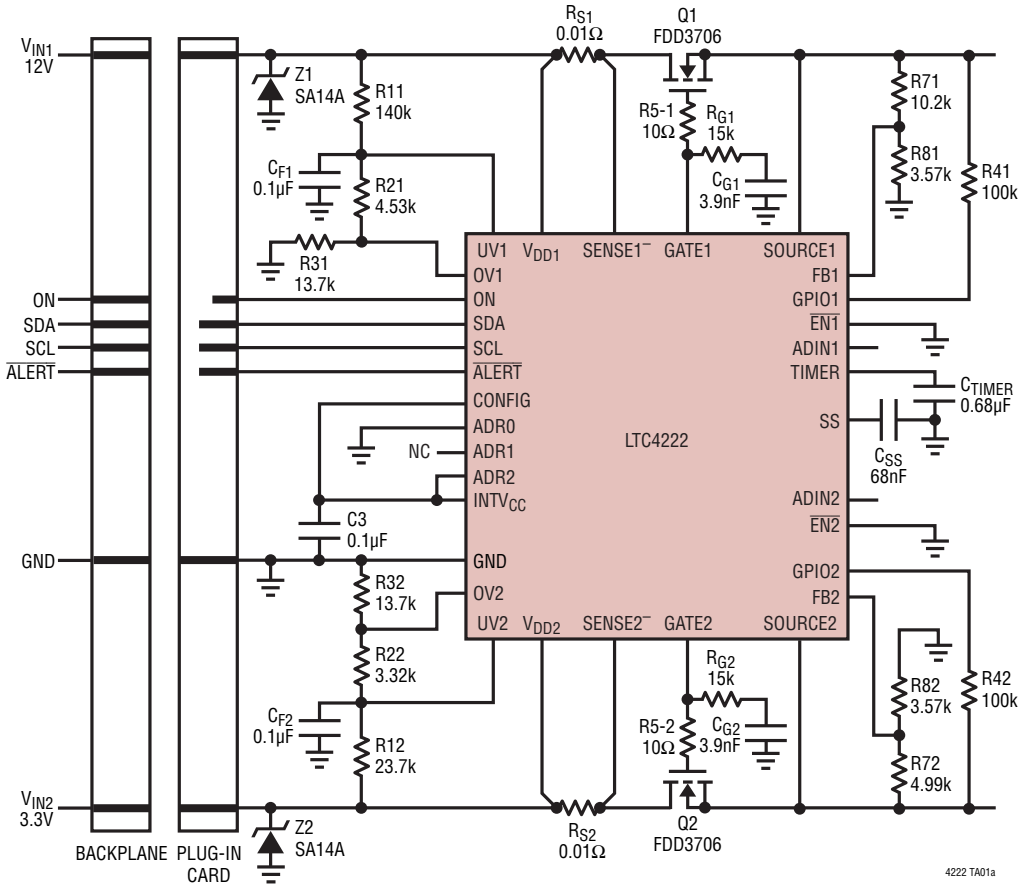


Figure 1. Typical Application

A MOSFET is turned on by charging up the GATE with a 12µA current source. When the GATE voltage reaches the MOSFET threshold voltage, the MOSFET begins to turn on and the SOURCE voltage then follows the GATE voltage as it increases.

While the MOSFET is turning on, the inrush current increases linearly at a dI/dt rate selected by capacitor C_{SS}. This is accomplished using the current limit amplifier controlling the GATE pin voltage. Once the inrush current reaches the limit set by the FB pin, the dI/dt ramp stops and the inrush current follows the foldback profile as shown in Figure 2. When both channels turn on simultaneously, the foldback current limit is set by the lower of the two FB pins.

A start-up timer is used to prevent damaging the MOSFET when starting up into a short-circuit. The TIMER capacitor integrates at 100µA during start-up and once the TIMER pin reaches threshold of 1.235V, the part checks to see if it is in current limit. If this is the case, the overcurrent fault bit, FAULT bit 2 in Table 6, is set and the part turns off. If the part is not in current limit, the 50mV circuit breaker is armed and the current limit is switched to 150mV. Alternately an internal 100ms start-up timer may be selected by tying the TIMER pin to $INTV_{CC}$.

As the SOURCE voltage rises, the FB pin voltage follows as set by R7 and R8. Once FB crosses its 1.235V threshold, and the start-up timer has expired, the corresponding GPIO pin, in the default power good configuration, ceases to pull low and indicates that power is now good. Alternately STATUS bit 3 can be read to check power-good status, where a zero indicates that power is good.

If a series resistor and capacitor from GATE to GROUND (R6 and C1) are employed to provide a constant inrush current during start-up, which provides a constant dV/dt at

APPLICATIONS INFORMATION

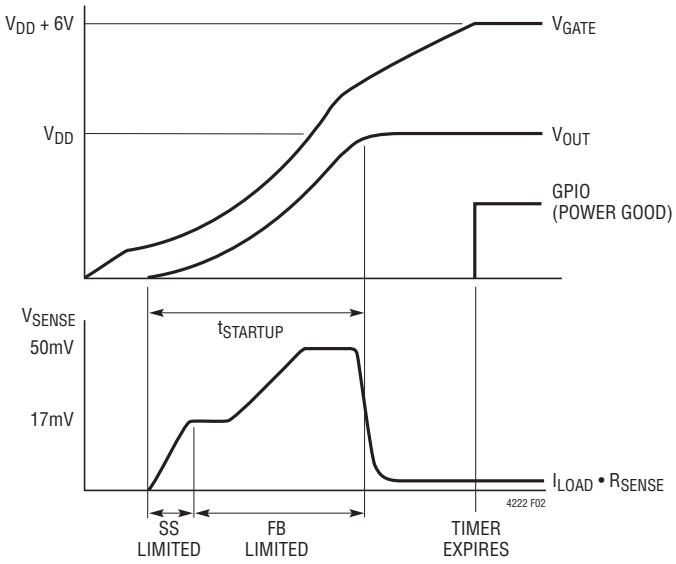


Figure 2. Power-Up Waveform

the output, a 12µA pull-up current (I_{GATE}) from the GATE pin slews the gate upwards and resulting current is less than the current limit. Because the inrush current is less than the current limit, the start-up timer can expire without producing an overcurrent fault and a small timer capacitor may be used. After the timer has expired power good will not be signaled until the FB pin crosses its threshold and the GATE-to-SOURCE voltage crosses the 4.3V threshold that indicates the MOSFET is fully enhanced. When both those conditions are met the output voltage is suitable for the load to be turned on and the impedance back to the supply through the MOSFET is low. Power good is then asserted with the GPIO pin or read via the interface, signaling that it is safe to turn on downstream loads. A power-bad fault is not generated when starting up in this manner because the FB pin will cross its threshold before the GATE-to-SOURCE threshold is crossed. R_G should be chosen such that $I_{GATE} \bullet R_G$ is less than the threshold of the MOSFET to avoid a current spike at the beginning of startup. Reducing R_G degrades the stability of the current limit circuit, see applications information on current limit stability.

GATE Pin Voltage

A curve of GATE-to-SOURCE voltage vs V_{DD} is shown in the Typical Performance Characteristics. At minimum input supply voltage of 2.9V, the minimum GATE-to-SOURCE drive voltage is 4.7V. The GATE-to-SOURCE voltage is clamped below 6.5V to protect the gates of logic-level N-channel MOSFETs.

Turn-Off Sequence

One or both GATE pins are turned off by a variety of conditions. A normal turn-off is initiated by an ON pin going low or a serial bus turn-off command. Additionally, several fault conditions cause a GATE to turn off. These include an input overvoltage (OV pin), input undervoltage (UV pin), overcurrent circuit breaker (SENSE$^-$ pin), or $\overline{EN}$ transitioning high. Writing a logic one into the UV, OV or OC fault bits (FAULT register bits 0 to 2 in Table 6) also latches off the associated GATE if their auto-retry bits are set to false.

A MOSFET is turned off with a 1mA current pulling down the GATE pin to ground. With the MOSFET turned off, the SOURCE and FB voltages drop as C_L discharges. When the FB voltage crosses below its threshold, GPIO may be configured to pull low to indicate that the output power is no longer good.

If the $INTV_{CC}$ pin drops below 2.60V for greater than 1µs, or the associated V_{DD} pin falls below 2.35V for greater than 2µs, a fast shut down of the MOSFET is initiated. In this case the GATE pin is pulled down with a 450mA current to the SOURCE pin.

Overcurrent Fault

The LTC4222 has different current limiting behavior during start-up, when the output supply ramps up under TIMER, SS and FB control, and normal operation. As such it can generate an overcurrent fault during both phases of operation. Both set the faulting supply's overcurrent fault bit (FAULT register bit 2) and shut off the faulting GATE, or both GATEs if the CONFIG pin is low.

During start-up when both TIMER and SS are ramping, the current limit is a function of SS pin voltage and the voltage on the FB pins. A supply could power up entirely in current limit depending on the bypass capacitor at the outputs of the ramping supplies. The TIMER pin sets the time duration for current limit during start-up, either 12.3ms/µF when using a timer capacitor, or 100ms when the TIMER pin is tied to $INTV_{CC}$. If the supply is still in current limit at the end of the timing cycle, an overcurrent

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fault is declared for that supply and the MOSFET is turned off. If the CONFIG pin is low, then both channels will turn off together. After the switch has turned off due to an OC fault the part will wait for a cool-down period before allowing the switch to turn on again. If the TIMER pin is tied to V_{CC} the cool-down period will be 5 seconds on the internal timer. Otherwise if using a TIMER capacitor, the capacitor will discharge at 2µA and the internal 100ms timer is started, when the 100ms timer expires and the TIMER pin reaches its 0.2V lower threshold the part is allowed to restart if the overcurrent fault bit (FAULT register bit 2) has been cleared or the overcurrent auto-retry bit (CONTROL register bit 2) has been set.

After start-up, a supply has dual-level glitch-tolerant protection against overcurrent faults. The sense resistor voltage drop is monitored by a 50mV electronic circuit breaker and a 150mV active current limit. In the event that a supply's current exceeds the circuit breaker threshold, an internal 20µs timer is started. If the supply is still overcurrent after 20µs the circuit breaker trips and the switch is turned off. An analog current limit loop prevents the supply current from exceeding the 150mV current limit in the event of a short circuit. The 20µs filter delay and the higher current limit threshold prevent unnecessary resets of the board due to minor current surges. The LTC4222 will stay in the latched off state unless the overcurrent auto-retry bit (CONTROL register bit 2) is set, in which case the switch turns on again after 100ms when using the external TIMER capacitor to set the start-up time, or 5 seconds when using the internal timer. Note that current limit foldback is not active after start-up.

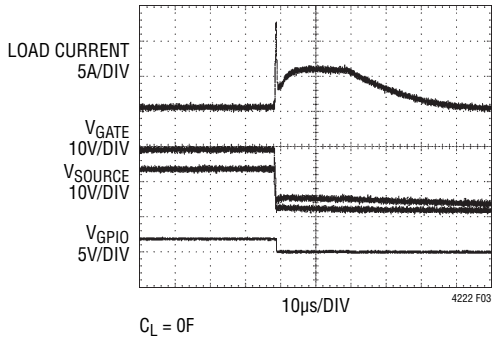

Figure 3. Short-Circuit Waveform

Overvoltage Fault

An overvoltage fault occurs when an OV pin rises above its 1.235V threshold for more than 2µs. This shuts off the corresponding GATE with a 1mA current to ground and sets the overvoltage present STATUS bit 0 and the overvoltage FAULT bit 0. If the pin subsequently falls back below the threshold for 100ms, the GATE is allowed to turn on again unless overvoltage auto-retry has been disabled by clearing CONTROL bit 0. If the CONFIG pin is tied low, an OV fault on either channel will shut off both channels simultaneously.

Undervoltage Fault

An undervoltage fault occurs when a UV pin falls below its 1.235V threshold for more than 2µs. This turns off the corresponding GATE with a 1mA current to ground and sets undervoltage present STATUS bit 1 and undervoltage FAULT bit 1. If the UV pin subsequently rises above the threshold for 100ms, the GATE is turned on again unless undervoltage auto-retry has been disabled by clearing CONTROL bit 1. When power is applied to the device, if UV is below its 1.235V threshold after $INTV_{CC}$ crosses its 2.64V undervoltage lockout threshold, an undervoltage fault is logged in the FAULT register. If the CONFIG pin is tied low, an UV fault on either channel will shut off both channels simultaneously.

ON Signals and the CONFIG Pin

Turn-on commands are issued from the ON pins or the I^2C interface. Internally, rising and falling edges of the ON pins set and reset the FET_ON register bits. Unlike the other control signals such as UV, OV and $\overline{EN}$, the rising edge of the ON signal is not filtered by the 100ms internal timer and instead turns on the corresponding channel immediately. Cycling an ON signal cancels the corresponding channel's overcurrent auto-retry cool-down period, allowing the channel to restart after a 100ms delay.

To start up and shut down both channels at the same time set the CONFIG pin low. Both channels then start up when all the UV, OV, $\overline{EN}$ and ON signals are in the correct state to turn on both channels, and when any of these signals turns one channel off, both channels turn off.

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Setting the CONFIG pin high allows the two channels to start up and turn off independently. When both ON signals are brought high sequentially, the channel turned on first immediately begins to start up and the second channel has a 200ns window to assert it's ON signal in order to start up in the same timer period. If the second ON signal is asserted after the 200ns window but before the end of the first channel's start-up time, the second channel start-up is delayed. The second channel will then start 100ms after the first channel's start-up timer has expired and the TIMER pin, if used, reaches its 200mV low threshold.

When an external TIMER capacitor is used, the TIMER capacitor voltage ramps up with a 100µA current. Once the TIMER pin reaches its 1.235V threshold the TIMER begins to discharge. While the TIMER capacitor is discharging, the ON signal for the second channel should not be asserted for 2ms/µF of TIMER capacitance. This allows the TIMER capacitor to return to its low state and ensures that the next channel to start receives a full timer cycle. This wait time is unnecessary when using the internal 100ms timer.

Board Present Change of State

The $\overline{EN}$ pins may be used to detect the presence of one or two downstream cards. Whenever an $\overline{EN}$ pin toggles, FAULT bit 4 is set to indicate a change of state. When the $\overline{EN}$ pin goes high, indicating board removal, the corresponding GATE turns off immediately (with a 1mA current to ground) and the board present STATUS bit 4, is cleared. If the $\overline{EN}$ pin is pulled low, indicating a board insertion, all fault bits for that channel except FAULT bit 4 are cleared and enable STATUS bit 4, is set. If the $\overline{EN}$ pin remains low for 100ms the state of the ON pin is captured in 'FET On' CONTROL bit 3. This turns the switch on if the ON pin is tied high. There is an internal 10µA pull-up current source on the $\overline{EN}$ pin. If the CONFIG pin is tied low, both $\overline{EN}$ pins must be low for 100ms for the two channels to be enabled and if either $\overline{EN}$ pin goes high both channels will turn off.

If a channel shuts down due to a fault, it may be desirable to restart that channel simply by removing and reinserting the related load card. In cases where the LTC4222 and the switch reside on a backplane or midplane and the load resides on a plug-in card, the $\overline{EN}$ pin detects when the plug-in card is removed. Figure 4 shows an example where the $\overline{EN}$ pin is used to detect insertion. Once the plug-in card is reinserted the fault register is cleared except for FAULT bit 4. After 100ms the state of the ON pin is latched into bit 3 of the CONTROL register. At this point the channel starts up again.

If a connection sense on the plug-in card is driving an $\overline{EN}$ pin, insertion or removal of the card may cause the pin voltage to bounce. This results in clearing the fault register when the card is removed. The pin may be debounced using a filter capacitor, $C_{\overline{EN}}$, on the $\overline{EN}$ pin as shown in Figure 4. The filter time is given by:

$$t_{FILTER} = C_{\overline{EN}} \bullet 123\ (ms/\mu F)$$

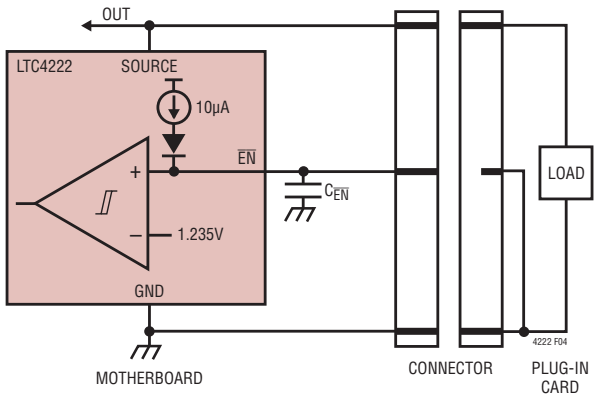

Figure 4. Plug-In Card Insertion/Removal

FET Short Fault

A FET short fault is reported if the data converter measures a current sense voltage greater than or equal to 2mV while the corresponding GATE is turned off. This condition sets FET short bit, Fault bit 5.

Power-Bad Fault

A power-bad fault is reported if a FB pin voltage drops below its 1.235V threshold for more than 2µs when the corresponding GATE is above the 4.3V gate to source threshold. This pulls the GPIO pin low immediately in the default power good configuration, and sets power-bad present bit, STATUS bit 3, and power-bad bit, FAULT bit 3. A circuit prevents power-bad faults if the GATE-to-SOURCE voltage is low, eliminating false power-bad faults during power-up or power-down. If the FB pin voltage subsequently rises back above the threshold, a power good configured GPIO pin returns to a high impedance state and STATUS bit 3 is reset.

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Fault Alerts

When any of the fault bits in a FAULT register (see Table 4) are set, an optional bus alert is generated if the appropriate bit in the ALERT register has been set. This allows only selected faults to generate alerts. At power-up the default state is to not alert on faults and the $\overline{\text{ALERT}}$ pin is high. If an alert is enabled, the corresponding fault causes the $\overline{\text{ALERT}}$ pin to pull low. After the bus master controller broadcasts the Alert Response Address, the LTC4222 responds with its address on the SDA line and releases $\overline{\text{ALERT}}$ as shown in Table 7. If there is a collision between two LTC4222s responding with their addresses simultaneously, then the device with the lower address wins arbitration and responds first. The $\overline{\text{ALERT}}$ line is also released if the device is addressed by the bus master if $\overline{\text{ALERT}}$ is pulled low due to an alert.

Once the $\overline{\text{ALERT}}$ signal has been released for one fault, it is not pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults do not generate alerts until the associated FAULT register bit has been cleared.

Resetting Faults

Faults are reset with any of the following conditions on a given channel. First, a serial bus command writing zeros to the FAULT register bits 0 to 5 clears the associated faults. Second, FAULT register bits 0 to 5 are cleared when the corresponding switch is turned off by the ON pin or STATUS bit 3 going from high to low, if the corresponding UV pin is brought below its 0.4V reset threshold for 2µs, or if $INTV_{CC}$ falls below its 2.64V undervoltage lockout threshold. Finally, when $\overline{\text{EN}}$ is brought from high to low, only corresponding FAULT bits 0-3 and 5 are cleared, and bit 4, which indicates a $\overline{\text{EN}}$ change of state, is set. Note that faults that are still present, as indicated in the STATUS registers, cannot be cleared.

The FAULT registers are not cleared when auto-retrying. When auto-retry is disabled the existence of an overvoltage, undervoltage, or overcurrent fault keeps the switch off. As soon as the fault is cleared, the switch turns on. If auto-retry is enabled, then a high value in STATUS register bits 0 or 1 holds the switch off and the fault register is ignored. Subsequently, when STATUS register bits 0 and 1 are cleared by removal of the fault condition, the switch is allowed to turn on again. The LTC4222 will set FAULT bit 2 and turn off in the event of an overcurrent fault, preventing it from remaining in an overcurrent condition. If configured to auto-retry, the LTC4222 will continually attempt to restart after cool-down cycles until it succeeds in starting up without generating an overcurrent fault. Note that if a switch is on after an auto-retry and the FAULT bit has not been reset, clearing the corresponding auto-retry bit will turn the channel off.

Data Converter

The LTC4222 incorporates a 10-bit A/D converter that continuously scans six different voltages. The SOURCE pins have a 1/24 resistive divider to monitor a full-scale voltage of 32V with 31.25mV resolution. The ADIN pins are monitored with a 1.28V full scale and 1.25mV resolution, and the voltage between the V_{DD} and SENSE pins is monitored with a 64mV full scale and 62.5µV resolution.

Results from each conversion are stored, left justified, in registers as seen in Tables 7 and 8, and are updated 15 times per second. Setting ADC_CONTROL register bit 0 invokes a test mode that halts the data converter so that the data converter result registers may be written to and read from for software testing.

The data converter also has a direct address mode that allows the user to take a specific measurement at a specific time and hold that value for later readback. Direct address mode is entered by setting the Halt bit, bit 0, in the ADC_CONTROL register (see Table 9). Then when the channel address bits, ADC_CONTROL bits 1 to 3, are written to, the ADC will make a single measurement on the channel indicated by those bits, then stop. Setting the ADC Alert bit, ADC_CONTROL bit 4, will enable an interrupt when the data converter finishes the conversion, resulting in the $\overline{\text{ALERT}}$ pin pulling low when the data is ready. Alternately, the ADC Busy bit, ADC_CONTROL bit 5, can be polled to check for the end of the conversion, after a direct address conversion the ADC Busy bit will go low. In normal mode ADC Busy is always high. Resetting the Halt bit returns the data converter to the scan mode.

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Configuring the GPIO Pins

Table 3 describes the possible states of the GPIO pins using the CONTROL registers bits 6 and 7. At power-up, the default state is for a GPIO pin to go high impedance when power is good (FB pin greater than 1.235V). Other applications for a GPIO pin are to pull down when power is good, a general purpose output and a general purpose input.

A simple application of the GPIO pin in the power good configuration is to connect it to the UV pin of the other channel with the CONFIG pin high. This will result in the second channel being turned on after the first channel has started up and signaled power good.

Current Limit Stability

For many applications the LTC4222 current limit will be stable without additional components. However there are certain conditions where additional components may be needed to improve stability. The dominant pole of the current limit circuit is set by the capacitance and resistance at the gate of the external MOSFET, and larger gate capacitance makes the current limit loop more stable. Usually a total of 8nF gate to source capacitance is sufficient for stability and is typically provided by inherent MOSFET C_{GS}, however the stability of the loop is degraded by increasing R_{SENSE} or by reducing the size of the resistor on a gate RC network if one is used, which may require additional gate to source capacitance. Board level short-circuit testing is highly recommended as board layout can also affect transient performance, for stability testing the worst-case condition for current limit stability occurs when the output is shorted to ground after a normal start-up.

There are two possible parasitic oscillations when the MOSFET operates as a source follower when ramping at power-up or during current limiting. The first type of oscillation occurs at high frequencies, typically above 1MHz. This high frequency oscillation is easily damped with R5 as shown in Figure 1. In some applications, one may find that R5 helps in short-circuit transient recovery as well. However, too large of an R5 value will slow down the turn-off time. The recommended R5 range is between 5Ω and 500Ω.

The second type of source follower oscillation occurs at frequencies between 200kHz and 800kHz due to the load capacitance being between 0.2µF and 9µF, the presence of R5 resistance, the absence of a drain bypass capacitor, a combination of bus wiring inductance and bus supply output impedance. To prevent this second type of oscillation avoid load capacitance below 10µF, alternately connect an external capacitor from the MOSFET gate to ground with a value greater than 1.5nF.

Supply Transients

The LTC4222 is designed to ride through supply transients caused by load steps. If there is a shorted load and the parasitic inductance back to the supply is greater than 0.5µH, there is a chance that the supply collapses before the active current limit circuit brings down the GATE pin. If this occurs, the undervoltage monitors pull the corresponding GATE pin low. The undervoltage lockout circuit has a 2µs filter time after V_{DD} drops below 2.35V. The UV pin reacts in 2µs to shut the GATE off, but it is recommended to add a filter capacitor, C_F, to prevent unwanted shutdown caused by a transient. Eventually either the UV pin or undervoltage lockout responds to bring the current under control before the supply completely collapses.

Supply Transient Protection

The LTC4222 is safe from damage with supply voltages up to 35V. However, spikes above 35V may damage the part. During a short-circuit condition, large changes in current flowing through power supply traces may cause inductive voltage spikes which exceed 35V. To minimize such spikes, the power trace inductance should be minimized by using wider traces or heavier trace plating. Also, a snubber circuit dampens inductive voltage spikes. Build a snubber by using a 100Ω resistor in series with a 0.1µF capacitor between V_{DD} and GND. A surge suppressor, Z1 in Figure 1, at the input can also prevent damage from voltage surges.

Design Example

As a design example, take the following specifications for channel 1: V_{IN} = 12V, I_{MAX} = 5A, I_{INRUSH} = 1A, dI/dt_{INRUSH} = 10A/ms, C_L = 330µF, $V_{UV(RISING)}$ = 10.75V, $V_{OV(FALLING)}$ = 14.0V, $V_{PWRGD(UP)}$ = 11.6V, and I^2C ADDRESS = 1000111. This completed design is shown in Figure 1.

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Selection of the sense resistor, R_S, is set by the overcurrent threshold of 50mV:

$$R_S = \frac{50mV}{I_{MAX}} = 0.01\Omega$$

The MOSFET is sized to handle the power dissipation during inrush when output capacitor C_{OUT} is being charged. A method to determine power dissipation during inrush is based on the principle that:

Energy in C_L = Energy in Q1

This uses:

$$\text{Energy in } C_L = \frac{1}{2}\ CV^2 = \frac{1}{2}\ (0.33mF)(12)^2$$

or 0.024 joules. Calculate the time it takes to charge up C_{OUT}:

$$t_{STARTUP} = \frac{C_L \bullet V_{DD}\ I_{INRUSH}}{I_{INRUSH}} = \frac{0.33mF \bullet 12V}{1A} = 4ms$$

The power dissipated in the MOSFET:

$$P_{DISS} = \frac{\text{Energy in } C_L}{t_{STARTUP}} = 6W$$

The SOA (safe operating area) curves of candidate MOSFETs must be evaluated to ensure that the heat capacity of the package tolerates 6W for 4ms. The SOA curves of the Fairchild FDC653N provide for 2A at 12V (24W) for 10ms, satisfying this requirement. Since the FDC653N has less than 8nF of gate capacitance and we are using a GATE RC network, the short-circuit stability of the current limit should be checked and improved by adding a capacitor from GATE to SOURCE if needed.

The inrush current is set to 1A using C1:

$$C1 = \frac{C_L \bullet I_{GATE}}{I_{INRUSH}}$$

$$C1 = \frac{0.33mF \bullet 12\mu A}{1A} \text{ or } C1 = 3.9nF$$

The inrush dI/dt is set to 10A/ms using C_{SS}:

$$C_{SS} = \frac{I_{SS}}{dI/dt\left(\frac{A}{s}\right)} \bullet 0.0429 \bullet \frac{1}{R_{SENSE}}$$

$$= \frac{10\mu A \bullet 0.0429 \bullet 1}{10000 \bullet 0.01\Omega} = 4.3nF \text{ choose } 4.7nF$$

For a start-up time of 4ms with a 2x safety margin we choose:

$$C_{TIMER} = \frac{2 \bullet t_{STARTUP}}{12.3ms/\mu F} + C_{SS} \bullet 2$$

$$C_{TIMER} = \frac{8ms}{12.3ms/\mu F} + 4.7nF \bullet 2 = 0.68\mu F$$

Note the minimum value of C_{TIMER} is 10nF.

The UV and OV resistor string values can be solved in the following method. First pick R3 based on I_{STRING} being 1.235V/R3 at the edge of the OV rising threshold. Then solve the following equations:

$$R2 = \frac{V_{OV(OFF)}}{V_{UV(ON)}} \bullet R3 \bullet \frac{UV_{TH(RISING)}}{OV_{TH(FALLING)}} - R3$$

$$R1 = \frac{V_{UV(ON)} \bullet (R3 + R2)}{UV_{TH(RISING)}} - R3 - R2$$

In our case we choose R3 to be 3.4k to give a resistor string current below 100µA.

Then solving the equations results in R2 = 1.16k and R1 = 34.6k.

The FB divider is solved by picking R8 and solving for R7, choosing 3.57k for R8 we get:

$$R7 = \frac{V_{PWRGD(UP)} \bullet R8}{FB_{TH(RISING)}} - R8$$

Resulting in R7 = 30k

A 0.1µF capacitor, C_F, is placed on the UV pins to prevent supply glitches from turning off the GATE via UV or OV.

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The address is set with the help of Table 1, which indicates binary address 1000111 corresponds to address 4. Address 4 is set by setting ADR2 low, ADR1 open and ADR0 high.

Next the value of R5 and R6 are chosen to be the default values 10Ω and 15kΩ as discussed previously.

In addition a 0.1µF ceramic bypass capacitor is placed on the $INTV_{CC}$ pin.

Layout Considerations

To achieve accurate current sensing, a Kelvin connection is required. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ. Small resistances add up quickly in high current applications. To improve noise immunity, put the resistive dividers to the UV, OV and FB pins close to the device and keep traces to V_{DD} and GND short. It is also important to put the bypass capacitor for the $INTV_{CC}$ pin, C3, as close as possible between $INTV_{CC}$ and GND. 0.1µF capacitors from the UV pins (and OV pins through resistor R2) to GND also helps reject supply noise. Figure 5 shows a layout that addresses these issues. Note that surge suppressor, Z1 is placed between supply and ground using wide traces.

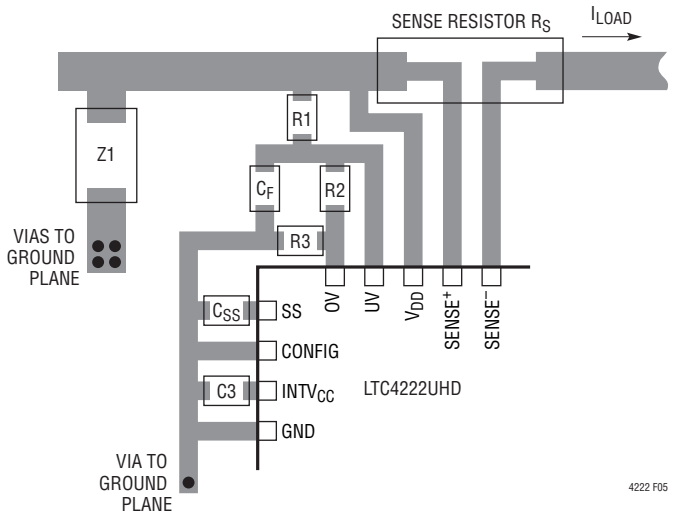

Figure 5. Recommended Layout

Digital Interface

The LTC4222 communicates with a bus master using a 2-wire interface compatible with I^2C Bus and SMBus, an I^2C extension for low power devices. The LTC4222 is a read-write slave device and supports SMBus bus Read Byte, Write Byte, Read Word and Write Word commands. A complete list of the resistors of the LTC4222 is shown in Table 2. The second word in a Read Word command is the contents of the subsequent 8-bit register. The second word in a Write Word command is ignored. Data formats for these commands are shown in Figures 6 to 11.

The LTC4222 interface also features a 25ms timeout feature to prevent the bus being stuck low if a communication error occurs. If either the SCL or SDA lines remain low for more than 25ms the LTC4222 will reset it's interface and release the SDAO pin, freeing the bus to resume communication.

The LTC4222 also features PMBus compatibility, the interface will not acknowledge unsupported commands and the internal addresses are in the manufacturer specified address space under the PMBus specification.

START and STOP Conditions

When the bus is idle, both SCL and SDA are high. A bus master signals the beginning of a transmission with a start condition by transitioning SDA from high to low while SCL is high, as shown in Figure 6. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

I^2C Device Addressing

Twenty seven distinct bus addresses are available using three 3-state address pins, ADR0, ADR1 and ADR2. Table 1 shows the correspondence between pin states and addresses. In addition, the LTC4222 responds to two special addresses. Address (1100 0110) is a mass write address that writes to all LTC4222s, regardless of their individual address settings. Mass write can be disabled by setting register bit 4 in the CONTROL register of channel 2 to zero. Address (0001 100) is the SMBus Alert Response Address. If the LTC4222 is pulling low on the $\overline{ALERT}$ pin due to an

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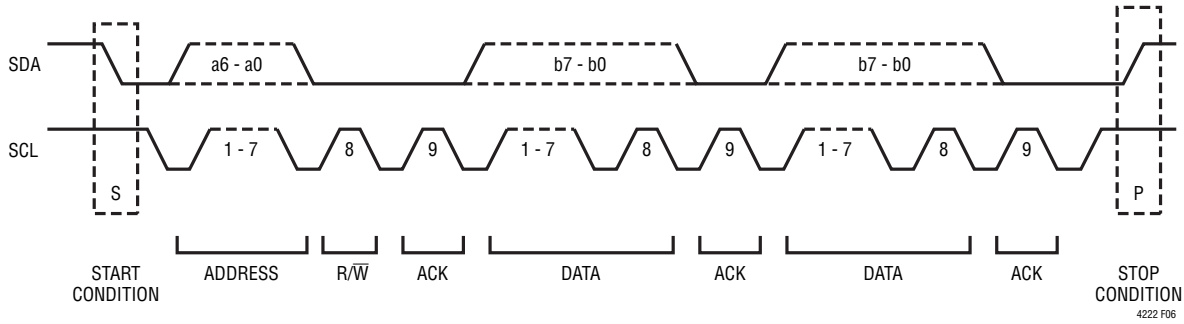

Figure 6. Data Transfer Over I²C or SMBus

alert, it acknowledges this address by broadcasting its address and releasing the $\overline{\text{ALERT}}$ pin.

Acknowledge

The acknowledge signal is used in handshaking between transmitter and receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. When the slave is the receiver, it pulls down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master may abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master pulls down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master leaves the SDA line HIGH (not acknowledge) and issues a stop condition to terminate the transmission.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the R/W bit set to zero, as shown in Figure 7. The addressed LTC4222 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTC4222 acknowledges this and then latches the lower three bits of the command byte into its internal Register Address pointer. The master then delivers the data byte and the LTC4222 acknowledges once more and latches the data into its control register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a Write Word command, the second data byte is acknowledged by the LTC4222 but ignored, as shown in Figure 8.

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the R/W bit set to zero, as shown in Figure 9. The addressed LTC4222 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to read. The LTC4222 acknowledges this and then latches the lower three bits of the command byte into its internal Register Address pointer. The master then sends a repeated START condition followed by the

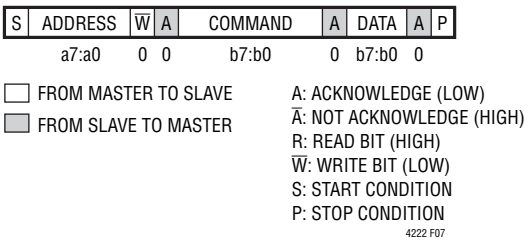

Figure 7. LTC4222 Serial Bus SDA Write Byte Protocol

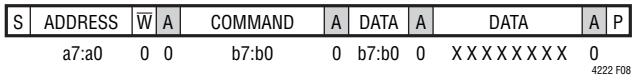

Figure 8. LTC4222 Serial Bus SDA Write Word Protocol

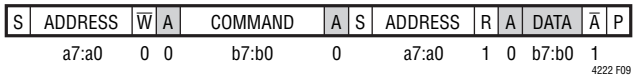

Figure 9. LTC4222 Serial Bus SDA Read Byte Protocol

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same seven bit address with the R/W bit now set to one. The LTC4222 acknowledges and send the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a Read Word command, Figure 10, the LTC4222 repeats the requested register as the second data byte.

Alert Response Protocol

When any of the fault bits in the FAULT register are set, an optional bus alert is generated if the appropriate bit in the ALERT register is also set. If an alert is enabled, the corresponding fault causes the $\overline{\text{ALERT}}$ pin to pull low. After the bus master controller broadcasts the Alert Response Address, the LTC4222 responds with its address on the SDA line and then release $\overline{\text{ALERT}}$ as shown in Figure 11. The $\overline{\text{ALERT}}$ line is also released if the device is addressed by the bus master. The $\overline{\text{ALERT}}$ signal is not pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults do not generate alerts until the associated FAULT register bit has been cleared.

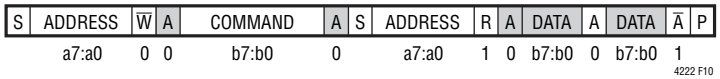

Figure 10. LTC4222 Serial Bus SDA Read Word Protocol

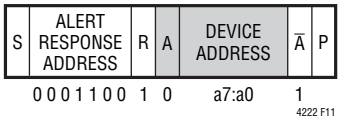

Figure 11. LTC4222 Serial Bus SDA Alert Response Protocol

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Table 1. LTC4222 I²C Device Addressing

DESCRIPTION	DEVICE ADDRESS	DEVICE ADDRESS								LTC4222 ADDRESS PINS		
	h	7	6	5	4	3	2	1	0	ADR2	ADR1	ADR0
Mass Write	C6	1	1	0	0	0	1	1	0	X	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X	X
0	88	1	0	0	0	1	0	0	X	L	NC	L
1	8A	1	0	0	0	1	0	1	X	L	H	NC
2	8C	1	0	0	0	1	1	0	X	L	NC	NC
3	8E	1	0	0	0	1	1	1	X	L	NC	H
4	98	1	0	0	1	1	0	0	X	L	L	L
5	9A	1	0	0	1	1	0	1	X	L	H	H
6	9C	1	0	0	1	1	1	0	X	L	L	NC
7	9E	1	0	0	1	1	1	1	X	L	L	H
8	A8	1	0	1	0	1	0	0	X	NC	NC	L
9	AA	1	0	1	0	1	0	1	X	NC	H	NC
10	AC	1	0	1	0	1	1	0	X	NC	NC	NC
11	AE	1	0	1	0	1	1	1	X	NC	NC	H
12	B8	1	0	1	1	1	0	0	X	NC	L	L
13	BA	1	0	1	1	1	0	1	X	NC	H	H
14	BC	1	0	1	1	1	1	0	X	NC	L	NC
15	BE	1	0	1	1	1	1	1	X	NC	L	H
16	C8	1	1	0	0	1	0	0	X	H	NC	L
17	CA	1	1	0	0	1	0	1	X	H	H	NC
18	CC	1	1	0	0	1	1	0	X	H	NC	NC
19	CE	1	1	0	0	1	1	1	X	H	NC	H
20	D8	1	1	0	1	1	0	0	X	H	L	L
21	DA	1	1	0	1	1	0	1	X	H	H	H
22	DC	1	1	0	1	1	1	0	X	H	L	NC
23	DE	1	1	0	1	1	1	1	X	H	L	H
24	E8	1	1	1	0	1	0	0	X	L	H	L
25	EA	1	1	1	0	1	0	1	X	NC	H	L
26	EC	1	1	1	0	1	1	0	X	H	H	L

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Table 2. LTC4222 Register Addresses and Contents

REGISTER ADDRESS		REGISTER NAME	DESCRIPTION
Decimal	Hex		
208	D0h	Control1 (A1)	Sets Behavior for Channel 1
209	D1h	Alert1 (B1)	Selects Which Channel 1 Faults Generate Alerts
210	D2h	Status1 (C1)	Displays the Status of Channel 1
211	D3h	Fault1 (D1)	Fault Log for Channel 1
212	D4h	Control2 (A2)	Sets Behavior for Channel 2
213	D5h	Alert2 (B2)	Selects which Channel 2 Faults Generate Alerts
214	D6h	Status2 (C2)	Displays the Status of Channel 2
215	D7h	Fault2 (D2)	Fault Log for Channel 2
216	D8h	SOURCE1 MSB	ADC SOURCE1 MSB data
217	D9h	SOURCE1 LSB	ADC SOURCE1 LSB data
218	DAh	SOURCE2 MSB	ADC SOURCE2 MSB data
219	DBh	SOURCE2 LSB	ADC SOURCE2 LSB data
220	DCh	ADIN1 MSB	ADC ADIN1 MSB
221	DDh	ADIN1 LSB	ADC ADIN1 LSB
222	DEh	ADIN2 MSB	ADC ADIN2 MSB
223	DFh	ADIN2 LSB	ADC ADIN2 LSB
224	E0h	SENSE1 MSB	ADC SENSE1 MSB
225	E1h	SENSE1 LSB	ADC SENSE1 LSB
226	E2h	SENSE2 MSB	ADC SENSE2 MSB
227	E3h	SENSE2 LSB	ADC SENSE2 LSB
228	E4h	ADC CONTROL	Configures Behavior of the ADC

+ Set bit ADC_CONTROL(0) before writing

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Table 3. CONTROL Registers A – Read/Write

BIT	CONTROL 1 (D0h)	CONTROL 2 (D4h)	OPERATION
7:6	GPIO1 Configure	GPIO2 Configure	<table><tr><th>FUNCTION</th><th>A6</th><th>A7</th><th>GPIO PIN</th></tr><tr><td>Power Good (Default)</td><td>0</td><td>0</td><td>GPIO = $\overline{C3}$</td></tr><tr><td>$\overline{\text{Power Good}}$</td><td>0</td><td>1</td><td>GPIO = C3</td></tr><tr><td>General Purpose Output</td><td>1</td><td>0</td><td>GPIO = A5</td></tr><tr><td>General Purpose Input</td><td>1</td><td>1</td><td>C6 = GPIO</td></tr></table>
5	GPIO1 Output	GPIO2 Output	Output Data for GPIO Pins When Configured as General Purpose Output 1 = High Impedance, 0 = Pulled Low
4	Reserved	Mass Write Enable	Allows Mass Write Addressing 1 = Mass Write Enabled (Default), 0 = Mass Write Disabled
3	Channel 1 FET On Control	Channel 2 FET On Control	On Control Bit, Latches the State of the On Pin at the End of the Debounce Delay 1 = FET On, 0 = FET Off
2	Channel 1 Overcurrent Auto-Retry	Channel 2 Overcurrent Auto-Retry	Overcurrent Auto-Retry Bit 1 = Auto-Retry After Overcurrent, 0 = Latch Off After Overcurrent (Default)
1	Channel 1 Undervoltage Auto-Retry	Channel 2 Undervoltage Auto-Retry	Undervoltage Auto-retry 1 = Auto-Retry After Undervoltage (Default), 0 = Latch Off After Undervoltage
0	Channel 1 Overvoltage Auto-Retry	Channel 2 Overvoltage Auto-Retry	Overvoltage Auto-retry 1 = Auto-Retry After Overvoltage (Default), 0 = Latch Off After Overvoltage

Table 4. ALERT Registers B – Read/Write

BIT	ALERT 1 (D1h)	ALERT 2 (D5h)	OPERATION
7	Reserved	Reserved	Not Used
6	Reserved	Reserved	Not Used
5	Channel 1 FET Short Alert	Channel 2 FET Short Alert	Enables Alert for FET Short Condition 1 = Enable Alert, 0 = Disable Alert (Default)
4	$\overline{EN1}$ State Change Alert	$\overline{EN2}$ State Change Alert	Enables Alert When $\overline{EN}$ Changes State 1 = Enable Alert, 0 = Disable Alert (Default)
3	Channel 1 Power Bad Alert	Channel 2 Power Bad Alert	Enables Alert When Output Power is Bad 1 = Enable Alert, 0 = Disable Alert (Default)
2	Channel 1 Overcurrent Alert	Channel 2 Overcurrent Alert	Enables Alert for Overcurrent Condition 1 = Enable Alert, 0 = Disable Alert (Default)
1	Channel 1 Undervoltage Alert	Channel 2 Undervoltage Alert	Enables Alert for Undervoltage Condition 1 = Enable Alert, 0 = Disable Alert (Default)
0	Channel 1 Overvoltage Alert	Channel 2 Overvoltage Alert	Enables Alert for Overvoltage Condition 1 = Enable Alert, 0 = Disable Alert (Default)

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Table 5. STATUS Registers C – Read

BIT	STATUS 1 (D2h)	STATUS 2 (D6h)	OPERATION
7	FET On	FET On	1 = FET On, 0 = FET Off
6	GPIO1 Input	GPIO2 Input	Reports the State of the GPIO1 Pin 1 = GPIO1 High, 0 = GPIO1 Low
5	Channel 1 FET Short Status	Channel 2 FET Short Status	Reports the State of the GPIO2 Pin 1 = GPIO2 High, 0 = GPIO2 Low
4	$\overline{EN1}$ Status	$\overline{EN2}$ Status	Indicates If the Channel is Enabled When $\overline{EN}$ is Low 1 = $\overline{EN}$ pin Low, 0 = $\overline{EN}$ pin High
3	Channel 1 Power Bad	Channel 2 Power Bad	Indicates Power is Bad When FB is Low 1 = FB Low, 0 = FB High
2	Channel 1 Overcurrent	Channel 2 Overcurrent	Indicates Overcurrent Condition; 1 = Overcurrent, 0 = Not Overcurrent
1	Channel 1 Undervoltage	Channel 2 Undervoltage	Indicates Input Undervoltage When UV is Low 1 = UV Low, 0 = UV High
0	Channel 1 Overvoltage	Channel 2 Overvoltage	Indicates Input Overvoltage When OV is High 1 = OV High, 0 = OV Low

Table 6. FAULT Registers D – Read/Write

BIT	FAULT 1 (D3h)	FAULT 2 (D7h)	OPERATION
7	Reserved	Reserved	Reserved
6	Reserved	Reserved	Reserved
5	Channel 1 FET Short Fault Occurred	Channel 2 FET Short Fault Occurred	Indicates Potential FET Short was Detected When Measured Current Sense Voltage Exceeded 1mV While FET was Off 1 = FET was Shorted, 0 = FET is Good
4	Channel 1 $\overline{EN}$ Changed State	Channel 2 $\overline{EN}$ Changed State	Indicates That the LTC4215-1 was Enabled or Disabled When $\overline{EN}$ Changed State 1 = $\overline{EN}$ Changed State, 0 = $\overline{EN}$ Unchanged
3	Channel 1 Power Bad Fault Occurred	Channel 2 Power Bad Fault Occurred	Indicates Power was Bad When FB Went Low 1 = FB was Low, 0 = FB was High
2	Channel 1 Overcurrent Fault Occurred	Channel 2 Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred 1 = Overcurrent Fault Occurred, 0 = No Overcurrent Faults
1	Channel 1 Undervoltage Fault Occurred	Channel 2 Undervoltage Fault Occurred	Indicates Input Undervoltage Fault Occurred When UV Went Low 1 = UV was Low, 0 = UV was High
0	Channel 1 Overvoltage Fault Occurred	Channel 2 Overvoltage Fault Occurred	Indicates Input Overvoltage Fault Occurred When OV Went High 1 = OV was High, 0 = OV was Low

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Table 7. ADC Register Data Format: ADINn, SOURCEn, SENSEn MSB Bytes – Read/Write*

BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
Data (9)	Data (8)	Data (7)	Data (6)	Data (5)	Data (4)	Data (3)	Data (2)

*Set bit ADC_CONTROL(0) before writing

Table 8. ADC Register Data Format: ADINn, SOURCEn, SENSEn LSB Bytes – Read/Write*

BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
Data (1)	Data (0)	Reserved**	Reserved**	Reserved**	Reserved**	Reserved**	Reserved**

*Set bit ADC_CONTROL(0) before writing

**Read as zero

Table 9. ADC CONTROL Register E – Read/Write

BIT	ADC_CONTROL (E4h)	OPERATION
7	Reserved	Reserved
6	Reserved	Reserved
5	ADC Busy	Status Bit That is High When the ADC is Converting. Always High in Free-Run Mode, Low When ADC is Halted or After a Point and Shoot Conversion. Read Only
4	ADC Alert	Enables the $\overline{\text{ALERT}}$ Pin to Pull Low When the ADC Finishes a Measurement
3 2 1	ADC Channel Address	These Bits May Be Written to Cause the ADC to Make a Single Measurement of the Desired Channel When the Halt Bit is High
0	Halt	Stops the Data Converter and Enables Point and Shoot Mode

FUNCTION	SF2-0
SOURCE1	000
SOURCE2	001
ADIN1	010
ADIN2	011
SENSE1	100
SENSE2	101

TYPICAL APPLICATIONS

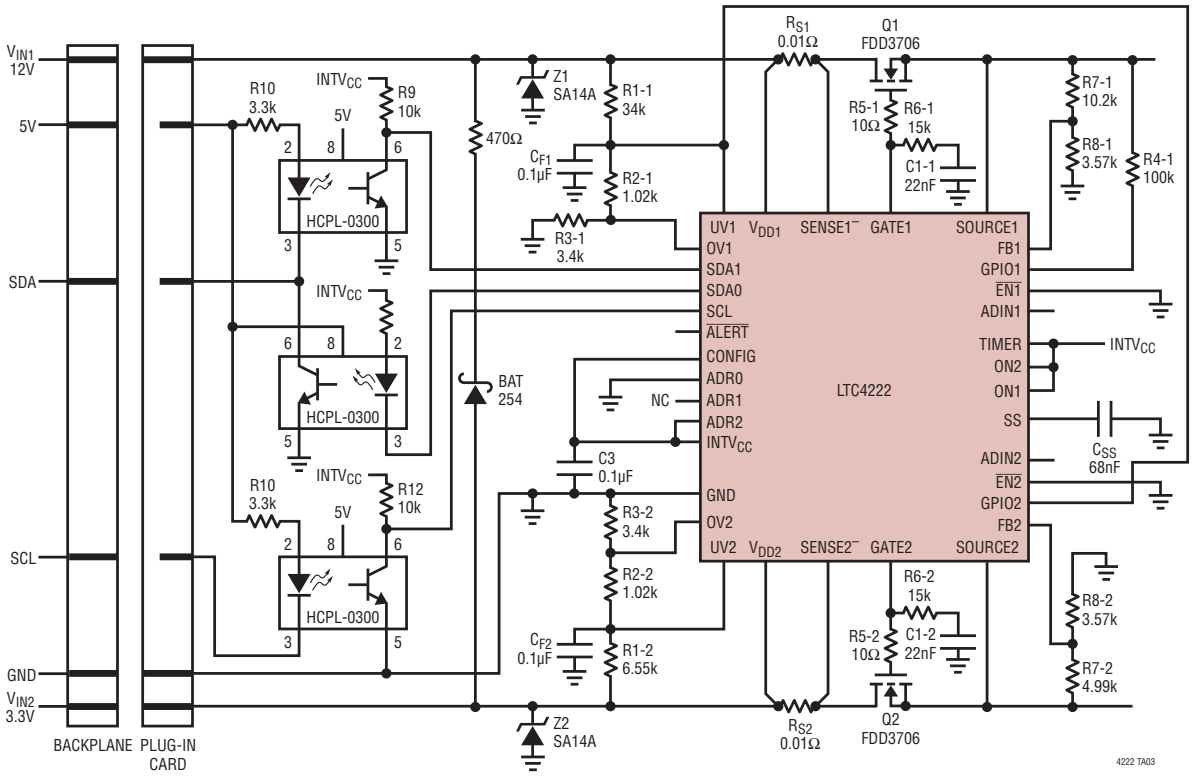
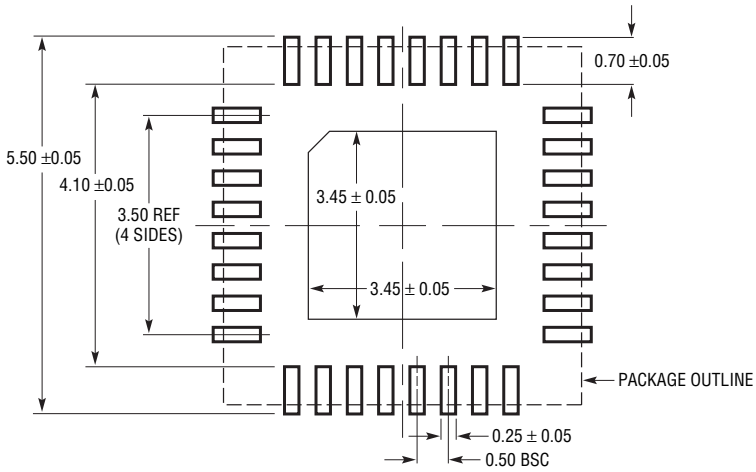


Figure 12. 3.3V and 12V Application with Sequenced Turn-On Optically Isolated I²C Communication and 5A Current Limits. Schottky Diode Allows 3.3V Switch to Turn On When 12V is Absent

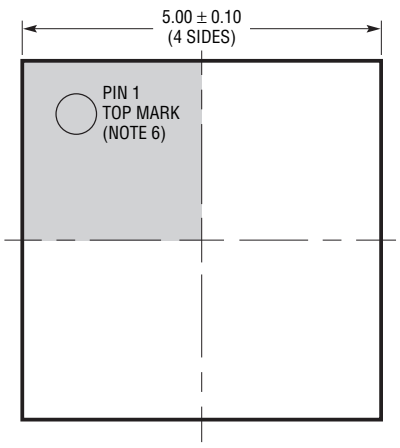
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

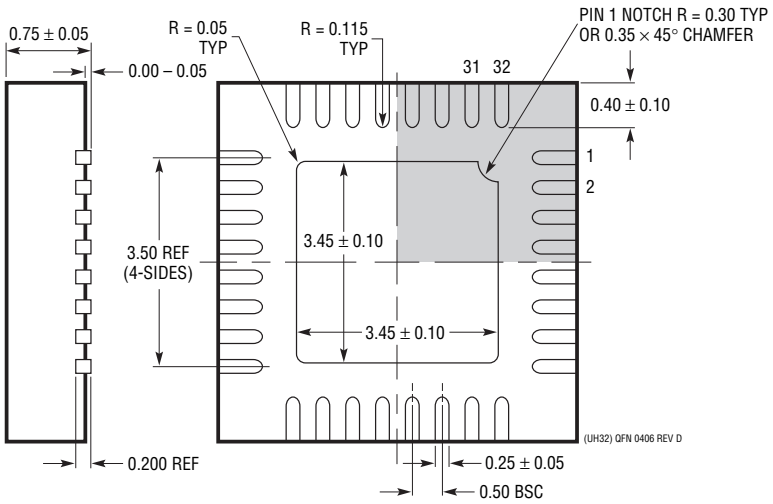
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



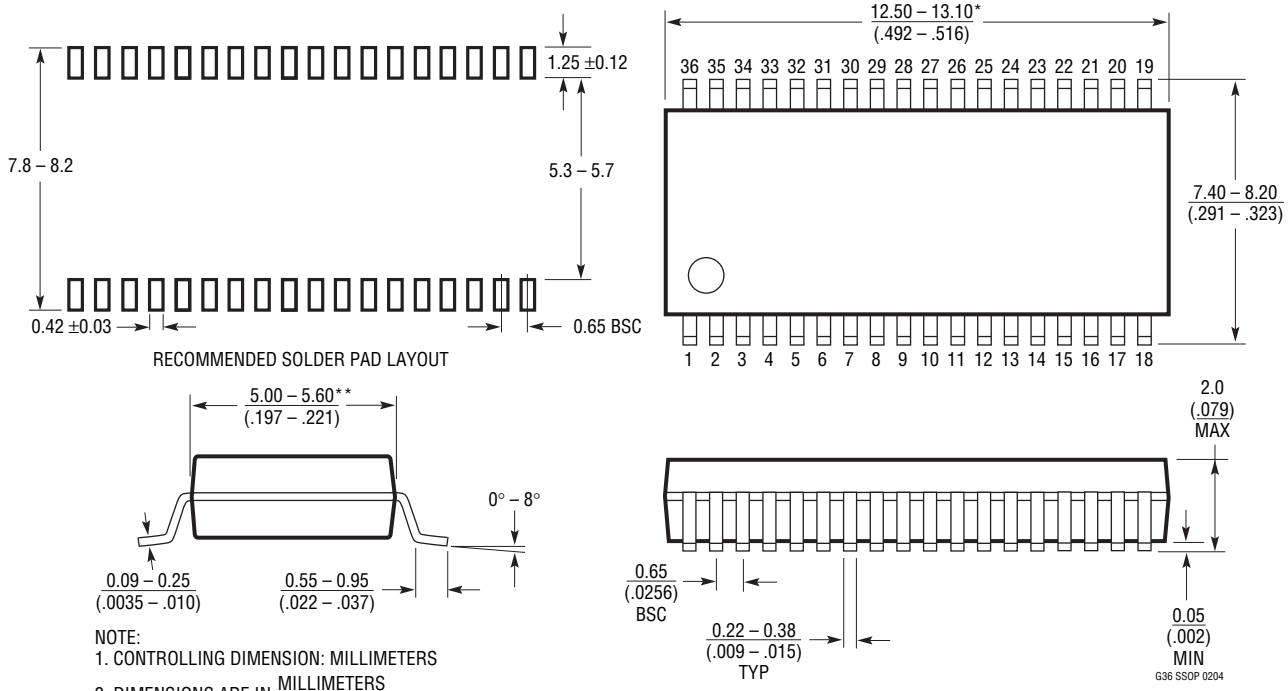
BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	3/12	Updated Typical Application	1
		Revised Electrical Characteristics limits	3, 4
		Revised Figure 2 and Figure 12	15, 29
		Corrected Comments for LTC4215 in Related Parts	32