Compact Dual Low Voltage Hot Swap Controller

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Load Voltages from 1V to 6V**
- **No Gate Components Required**
- **Adjustable Current Limit with Circuit Breaker**
- **Limits Peak Fault Current in ≤1µs**
- No External Timing Capacitor Required
- Adjustable Supply Voltage Power-Up Rate
- Gate Drive for External N-channel MOSFET
- LTC4224-1: Latchoff After Fault
- LTC4224-2: Automatic Retry After Fault
- 10-Lead MSOP and 3mm × 2mm DFN Packages

APPLICATIONS

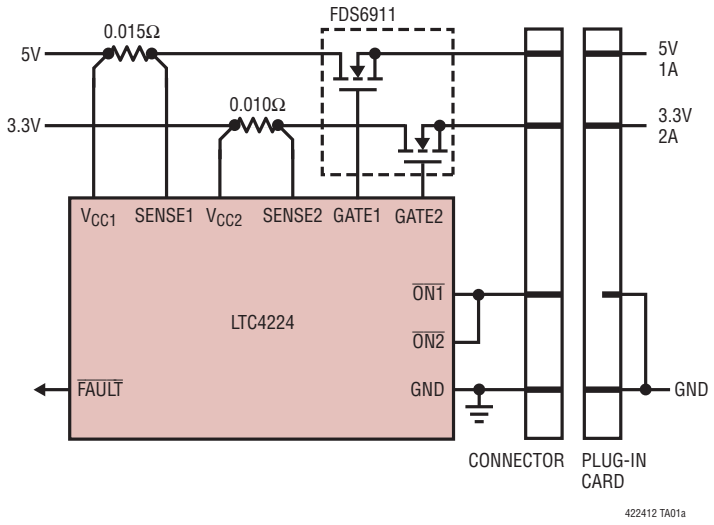
- Optical Networking
- Low Voltage Hot Swap
- Electronic Circuit Breakers

DESCRIPTION

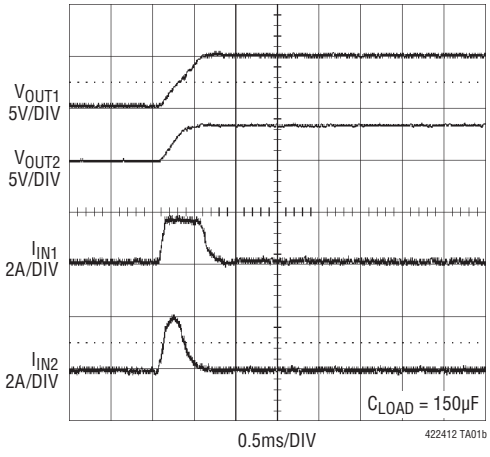
The LTC®4224 Dual Low Voltage Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane. It controls two supplies with external N-channel MOSFETs and operates with one supply as low as 1V provided the other supply is 2.7V or greater. The LTC4224 can ramp up the supplies in any order and at adjustable ramp rates. To minimize the number of external components and PCB area, the gate capacitor is optional, all timing delays are generated internally, and the $\overline{ON}$ pins have integrated pull-up currents.

Protection against overcurrent faults is provided by a fast-acting current limit and timed circuit breakers. A $\overline{FAULT}$ pin signals overcurrent faults. The LTC4224-1 remains off after a fault, while the LTC4224-2 automatically tries to apply power again after a four second cool-down period.

TYPICAL APPLICATION



Normal Power-Up Waveform

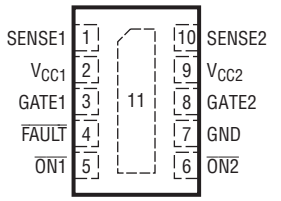


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

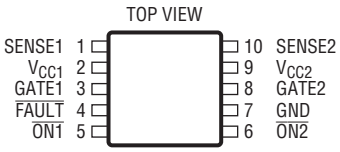
Supply Voltage (V_{CCn}) ..... –0.3V to 9V
Input Voltages
  SENSEn, $\overline{ONn}$ ..... –0.3V to 9V
Output Voltages
  GATEn – V_{CC} (Note 4) ..... –0.3V to 5V
  $\overline{FAULT}$ ..... –0.3V to 9V

Operating Temperature Range
  LTC4224C ..... 0°C to 70°C
  LTC4224I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature Range (Soldering, 10 sec)
  MSOP Package ..... 300°C

PIN CONFIGURATION



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) PCB GND CONNECTION OPTIONAL



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4224CDDB-1#PBF	LTC4224CDDB-1#TRPBF	LDTT	10-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC4224CDDB-2#PBF	LTC4224CDDB-2#TRPBF	LDNV	10-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC4224IDDB-1#PBF	LTC4224IDDB-1#TRPBF	LDTT	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC4224IDDB-2#PBF	LTC4224IDDB-2#TRPBF	LDNV	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC4224CMS-1#PBF	LTC4224CMS-1#TRPBF	LTDTV	10-Lead Plastic MSOP	0°C to 70°C
LTC4224CMS-2#PBF	LTC4224CMS-2#TRPBF	LTDNW	10-Lead Plastic MSOP	0°C to 70°C
LTC4224IMS-1#PBF	LTC4224IMS-1#TRPBF	LTDTV	10-Lead Plastic MSOP	–40°C to 85°C
LTC4224IMS-2#PBF	LTC4224IMS-2#TRPBF	LTDNW	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. T_A = 25°C, V_{CC1} = 5V, V_{CC2} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	V_{CC} Supply Range	V_{CC} = Max (V_{CC1}, V_{CC2})	●	2.7		6	V
I_{CC}	V_{CC} Supply Current		●		1.4	3	mA
$V_{CC(UVL)}$	V_{CC} Undervoltage Lockout	V_{CC} Rising	●	2.2	2.4	2.65	V
V_{CCLO}	V_{CCLO} Supply Range	V_{CCLO} = Min (V_{CC1}, V_{CC2}), $V_{CC} \geq$ 2.7V	●	1		6	V
I_{CCLO}	V_{CCLO} Supply Current		●		40	100	µA
$V_{CCLO(UVL)}$	V_{CCLO} Undervoltage Lockout	V_{CCLO} Falling	●	0.76	0.8	0.84	V
External Gate Drive							
ΔV_{GATE}	Gate Drive ($V_{GATEn} - V_{CC}$)	I_{GATEn} = 0µA, –1µA	●	4.5	5.5	7	V
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, V_{GATEn} = 1V	●	–7	–10	–13	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	$V_{\overline{ONn}}$ = 1V, V_{GATEn} = 10V	●	0.5	1.5	3	mA
$I_{GATE(FPD)}$	Gate Fast Pull-Down Current	Fast Turn-Off, V_{GATEn} = 10V	●	50	125	200	mA
Current Limit							
$\Delta V_{SENSE(CB)}$	Circuit Breaker Trip Sense Voltage (V_{CCn} – SENSEn)		●	22.5	25	27.5	mV
I_{SENSE}	SENSE Input Current	V_{SENSE1} = 5V, V_{SENSE2} = 3.3V	●		40	100	µA
Inputs and Outputs							
$V_{\overline{ON}(TH)}$	$\overline{ONn}$ Threshold Voltage	$V_{\overline{ONn}}$ Rising	●	0.76	0.8	0.84	V
$\Delta V_{\overline{ON}(HYST)}$	$\overline{ONn}$ Hysteresis		●	15	30	50	mV
$I_{\overline{ON}(IN)}$	$\overline{ONn}$ Pull-Up Current	$V_{\overline{ONn}}$ = 1V	●	–5	–10	–15	µA
V_{OL}	Output Low Voltage ($\overline{FAULT}$)	$I_{\overline{FAULT}}$ = 3mA	●		0.2	0.4	V
Delay							
t_{CB}	Circuit Breaker Delay		●	2.5	5	7.5	ms
$t_{PHL(SENSE)}$	Sense Voltage, (V_{CCn} – SENSEn) High to GATE Low	ΔV_{SENSE} = 200mV, C_{GATE} = 10nF	●		0.4	1	µs
$t_{PLH(GATE)}$	$\overline{ONn}$ Low or Input Supply High to GATEn High Prop Delay		●	5	10	15	ms
$t_{PLH(UVL)}$	V_{CCn} Low to GATEn Low Prop Delay		●		8	16	µs
$t_{D(UV)}$	UV Turn-On Delay	V_{CC} Out of UV	●	80	160	240	ms
$t_{D(COOL)}$	Auto-Retry Cooling Delay	Note 3	●	2	4	6	s
t_{BLANK}	Start-Up Circuit Breaker Blanking Delay		●	2.5	5	7.5	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

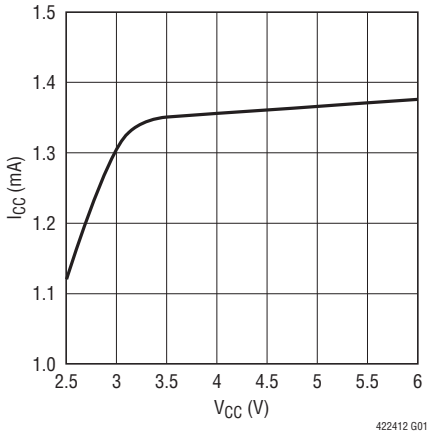
Note 3: LTC4224-2 only.

Note 4: The greater of V_{CC1} and V_{CC2} is the internal supply voltage (V_{CC}). An internal clamp limits the GATE pin to a minimum 5V above V_{CC}. Driving this pin beyond the clamp may damage the device.

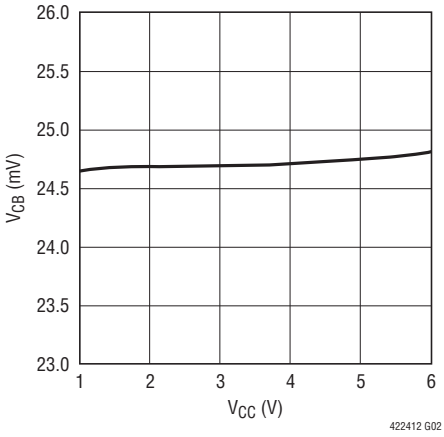
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are T_A = 25°C, V_{CC1} = 5V, V_{CC2} = 3.3V, unless otherwise specified.

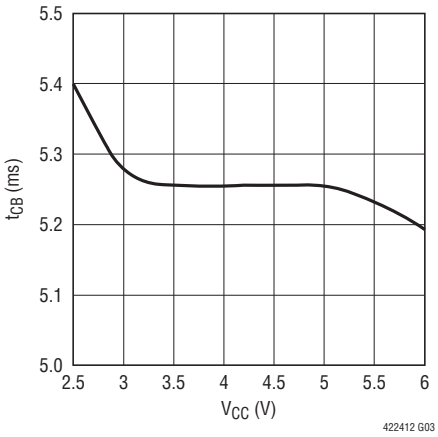
I_{CC} vs V_{CC}



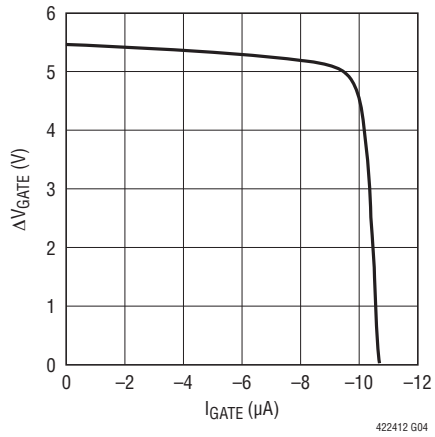
Circuit Breaker Trip Voltage vs V_{CC}



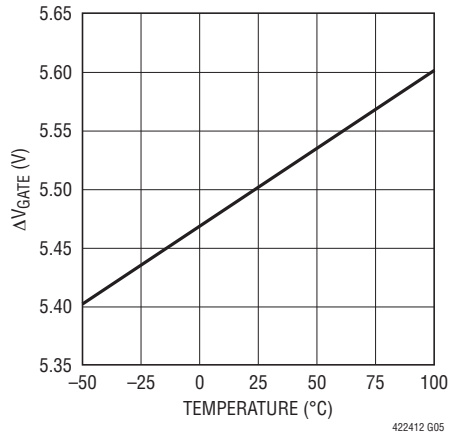
Circuit Breaker Delay vs V_{CC}



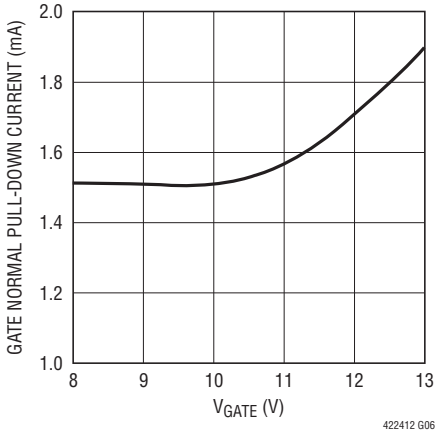
Gate Drive vs I_{GATE}



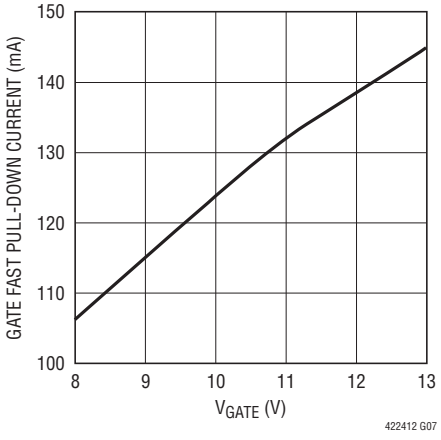
Gate Drive vs Temperature



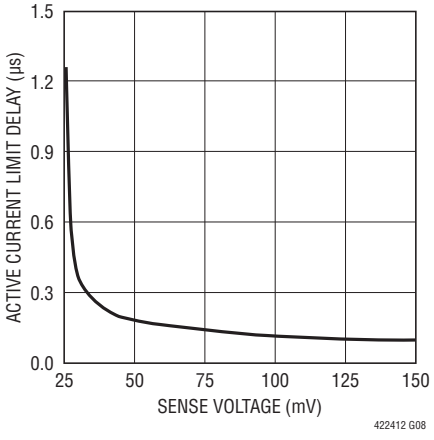
Gate Pull-Down Current vs Gate Voltage



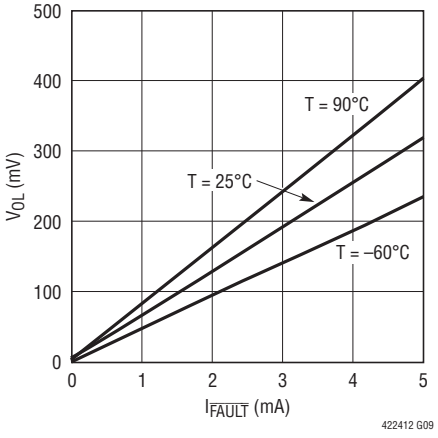
Gate Fast Pull-Down Current vs Gate Voltage



Active Current Limit Delay vs Sense Voltage



$\overline{FAULT}$ Voltage vs $\overline{FAULT}$ Sink Current



PIN FUNCTIONS

SENSE1, SENSE2 (Pins 1,10): Current Sense Input. Connect this pin to an external sense resistor. The current limit circuit controls GATEn to limit the voltage between V_{CCn} and SENSEn to 25mV. An Electronic Circuit Breaker (ECB) is active during current limiting and trips after 5ms. To disable current limit, connect this pin to V_{CCn}.

V_{CC1}, V_{CC2} (Pins 2, 9): Supply Voltage and Current Sense Input. An undervoltage lockout circuit disables the part until V_{CC}, the higher of V_{CC1} and V_{CC2}, exceeds 2.4V. The lower supply is disabled until it exceeds 0.8V.

GATE1, GATE2 (Pins 3, 8): Gate Drive for External N-channel MOSFET. A charge pump sources 10µA from GATE to turn on the external MOSFET. An internal clamp limits the gate voltage to 5.5V above the higher of V_{CC1} and V_{CC2}. During turn-off, a 1.5mA pulldown current discharges GATE to ground. During short-circuits, a 125mA pulldown current is activated to discharge GATE to ground.

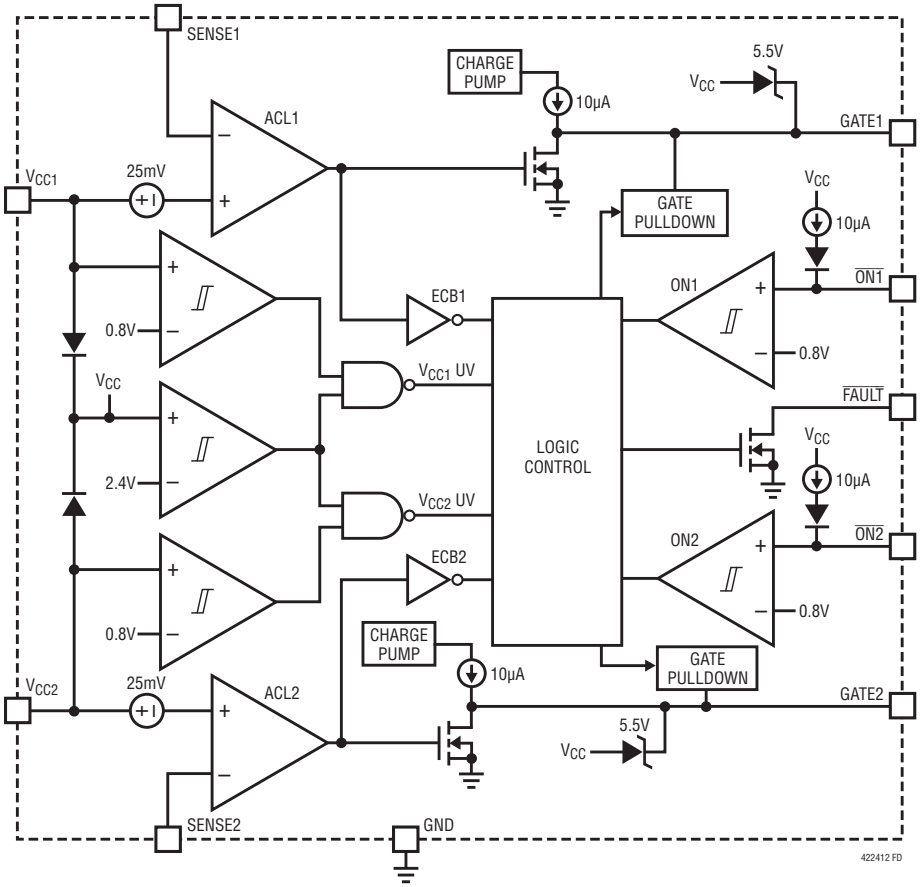
$\overline{\text{FAULT}}$ (Pin 4): Fault Status Output. Open-drain output that is normally pulled high to V_{CC1} or V_{CC2} by an external resistor. It is pulled low when the ECB trips due to an overcurrent condition at either supply. This pin may be left open if unused.

$\overline{\text{ON1}}$, $\overline{\text{ON2}}$ (Pins 5, 6): On Control Input. A falling edge turns on the external N-channel MOSFET and a rising edge turns it off. A low to high transition on this pin resets an ECB fault for the corresponding channel. Internally pulled up to V_{CC} by a 10µA current source.

GND (Pin 7): Device Ground.

Exposed Pad (DFN Package Only): Exposed Pad may be left open or connected to device ground.

FUNCTIONAL DIAGRAM



OPERATION

The LTC4224 is designed to control power on a live backplane, allowing boards to be safely inserted and removed. It controls two supplies (V_{CC1}, V_{CC2}) with operating voltages between 1V and 6V via two external N-channel MOSFETs. For applications where the total load current is 5A or less, dual MOSFETs such as the FDS6911 can be used to save board area. The two supplies can be turned on and off independently using the active low $\overline{ON1}$ and $\overline{ON2}$ pins. Internal 10µA current sources pull these pins to V_{CC}.

Pulling the $\overline{ON}$ pin low turns on a charge pump which sources 10µA at the GATE pin thereby ramping up the gate of the external MOSFET. When the MOSFET turns on, the inrush current is limited at a level set by an external sense resistor. Inrush current can be further reduced, if desired, by adding a capacitor from GATE to GND. To protect the external MOSFET, the GATE pins are clamped to about 5.5V above the higher of the two supplies.

Each supply is continuously monitored for undervoltage and overcurrent conditions. The undervoltage monitor shuts off the external MOSFET when the corresponding supply is too low.

Current is monitored by an active current limit amplifier (ACL) and a timed electronic circuit breaker (ECB). Like all timing delays in the LTC4224, the ECB delay of 5ms is generated internally without requiring any external timing capacitors. The ECB threshold is slightly below the ACL threshold and shuts off the external MOSFET after 5ms. $\overline{FAULT}$ is latched low to indicate an overcurrent fault.

The LTC4224-1 remains latched off until reset by either turning off and then on the affected supply or its $\overline{ON}$ pin. The LTC4224-2 automatically restarts after four seconds to allow time for the MOSFET to cool down.

APPLICATIONS INFORMATION

The typical LTC4224 application is in a high availability system where two positive supply voltages are distributed to power individual cards. The LTC4224 detects board presence during insertion and removal, allowing power to be delivered in a controlled manner without damaging the connector. It reports overcurrent faults to the system controller through its $\overline{FAULT}$ pin, which can light an LED or can be monitored by a system controller.

The basic LTC4224 application circuit is shown in Figure 1. The following sections cover V_{CC} selection, the normal turn-on and turn-off sequence, various fault conditions and recovery from fault situations. External component selection is discussed in detail in the Design Example section.

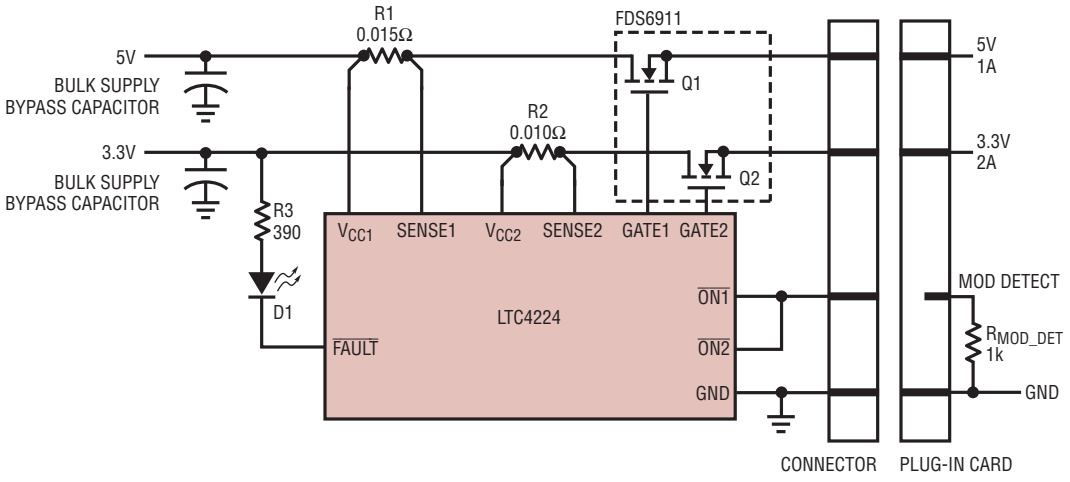


Figure 1. Typical Application

APPLICATIONS INFORMATION

V_{CC} Selection

The LTC4224 is powered from the higher of its two supply pins, V_{CC1} and V_{CC2}.This allows the part to control a supply voltage as low as 1V, while the other supply is 2.7V or greater. If both supplies are tied together, the part derives its power from both equally. The Functional Diagram shows the V_{CC} selection circuit in an ideal diode OR-ing arrangement. It is designed to ensure swift and smooth internal power switchover from one supply to the other.

Turn-On Sequence

Separate $\overline{ON1}$ and $\overline{ON2}$ pins allow the V_{CC1} and V_{CC2} supplies to be turned on in any order. The power supplies delivered to a plug-in card are controlled by external N-channel MOSFETs, Q1 and Q2. For X2/XENPAK defined optical transceiver modules, it has been specified that the MOD DETECT pin pulls low inside the module through a 1k resistor (R_{MOD_DET}), as shown in Figure 1. Several conditions must be satisfied to turn on the MOSFETs. First, V_{CC1} or V_{CC2} must exceed the 2.4V V_{CC} undervoltage lockout level for longer than an internal UV turn-on delay of 160ms. Next, if V_{CCn} is greater than 0.8V and $\overline{ONn}$ is low (<0.8V), a debounce delay of 10ms is started. If V_{CCn} drops below 0.8V or $\overline{ONn}$ goes high before the end of the 10ms debounce delay, the debounce delay is restarted the next time these pins are properly conditioned.

When the 10ms debounce delay expires, the external MOSFET is turned on by charging up the GATE with a 10µA charge pump generated current source. When the GATE voltage reaches the MOSFET threshold voltage, the inrush current can build up quickly as the GATE continues to rise. The ACL amplifier actively controls the gate voltage to maintain 25mV across the sense resistor. In this condition, the inrush current is given by:

$$I_{INRUSH} = \frac{25mV}{R_{SENSE}}$$

As the inrush current charges up the load capacitor, the output rises with a corresponding increase in gate voltage. When the supply is no longer in current limit, an internal charge pump pulls the gate to 5.5V above the higher of V_{CC1} or V_{CC2} to achieve a low resistance power path. Figure 2 shows a typical start-up sequence with $C_{LOAD1} = C_{LOAD2} = 150\mu F$, $R_{LOAD1} = 4.7\Omega$ and $R_{LOAD2} = 2\Omega$.

The inrush current can be reduced to below the current limit level by adding an external gate capacitor as shown in Figure 3.

GATE capacitor C_{GATE} provides gate slew rate control to limit the inrush current. However, C_{GATE} could cause parasitic high frequency self oscillation in Q1. A 10Ω resistor, R_G, as shown in Figure 3 can be used to prevent the oscillation. To be effective, R_G needs to be laid out close to Q1.

The voltage at the GATE pin rises with a slope equal to I_{GATE}/C_{GATE}. For a given supply inrush current I_{INRUSH} and load capacitor C_{LOAD}, C_{GATE} can be calculated according to:

$$C_{GATE} = \frac{I_{GATE}}{I_{INRUSH}} \bullet C_{LOAD}$$

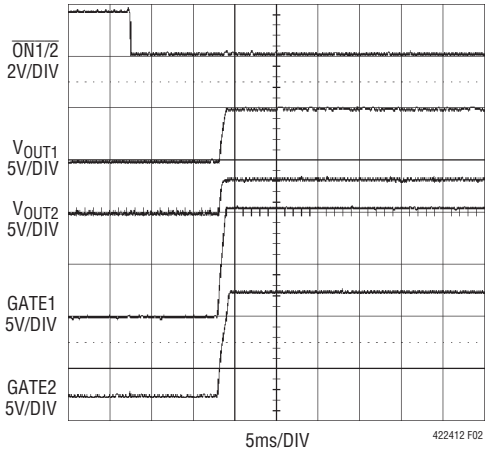


Figure 2. Normal Power-Up Sequence

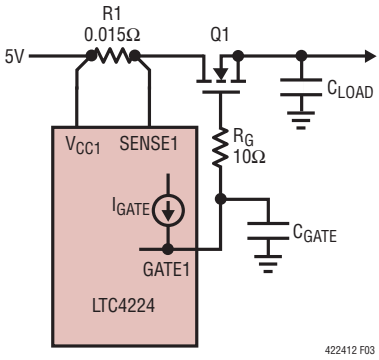


Figure 3. Inrush Current Control by Gate Capacitor

APPLICATIONS INFORMATION

If the voltage across the sense resistor R1 becomes too high, the inrush current is limited by the internal current limit circuitry.

Turn-Off Sequence

The MOSFETs can be turned off by the conditions summarized in Table 1.

Table 1. Turn-Off Conditions

CONDITION	RESULT CHANNEL 1	RESULT CHANNEL 2	CLEARED BY
$\overline{ON1}$ Goes High	Turns Off	No Effect	$\overline{ON1}$ Low
$\overline{ON2}$ Goes High	No Effect	Turns Off	$\overline{ON2}$ Low
UVLO on V_{CC}	Turns Off	Turns Off	V_{CC} > UVLO
UVLO on V_{CC1}	Turns Off	No Effect	V_{CC1} > UVLO
UVLO on V_{CC2}	No Effect	Turns Off	V_{CC2} > UVLO
CH1 Overcurrent Fault	Turns Off	No Effect	$\overline{ON1}$ High, UVLO on V_{CC1}
CH2 Overcurrent Fault	No Effect	Turns Off	$\overline{ON2}$ High, UVLO on V_{CC2}

When $\overline{ON1}$ or $\overline{ON2}$ is pulled high, the corresponding GATE pin is pulled to ground by 1.5mA. With the MOSFET off, the load current discharges the load capacitor. Figure 4 shows V_{CC1} supply turning off by pulling $\overline{ON1}$ high with R_{LOAD1} = 4.7Ω discharging C_{LOAD1} = 150µF.

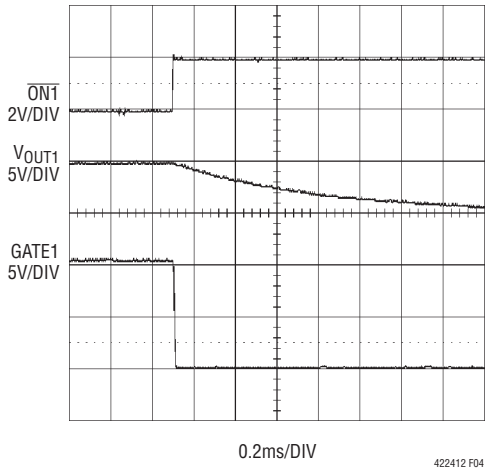


Figure 4. Normal Power-Down Sequence

Overcurrent Fault

The LTC4224 features an adjustable current limit with circuit breaker function that protects external MOSFETs against short circuits or excessive load current. The voltage across the external sense resistor is monitored by the active current limit (ACL) amplifier and the electronic circuit breaker (ECB) comparator. An overcurrent condition results in the current being limited by the ACL amplifier. During current limiting, the ECB is activated and initiates a chain of logic and timing events to handle the fault.

Figure 5 illustrates the LTC4224's response to an overcurrent condition on one supply output. Start-up and overcurrent control for the two supplies are independent. Before time point t_1, the $\overline{ON}$ pin is high and the part is in reset. When the $\overline{ON}$ pin goes low, a 10ms debounce delay is started. After 10ms (time point t_2), the external MOSFET is turned on by charging GATE with 10µA. The load capacitor starts to charge up and the output voltage increases. At the same

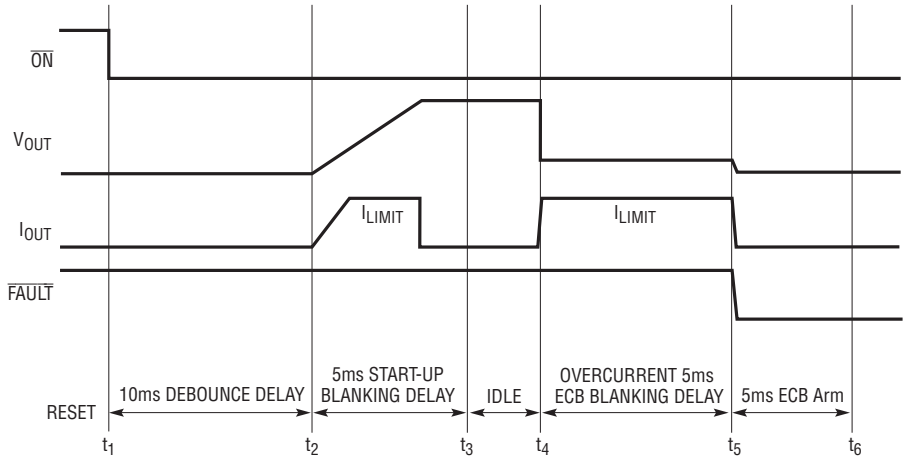


Figure 5. Fault Handling Sequence

APPLICATIONS INFORMATION

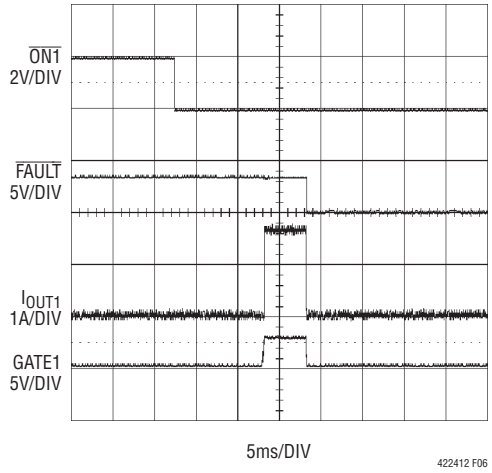


Figure 6. Start-Up with Short at Output

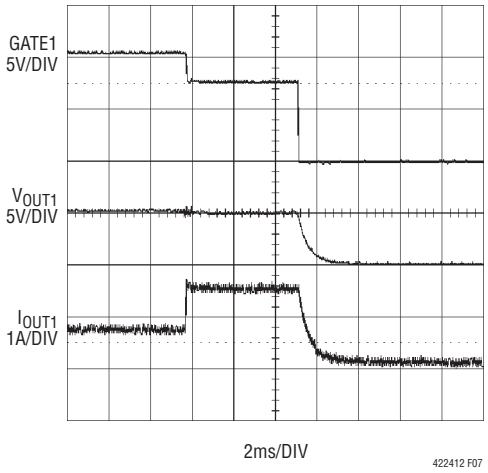


Figure 7. Overcurrent Fault on Output

time, a 5ms start-up blanking delay begins during which the circuit breaker is not allowed to latchoff the MOSFET. If the ECB is tripped at the end of 5ms (time point t_3), the MOSFET is latched off by pulling GATE down with 1.5mA and $\overline{FAULT}$ is latched low. The waveform in Figure 6 shows an unsuccessful start-up due to a short circuit at the output. To ensure start-up, the load capacitor must be charged up sufficiently to exit current limit before the end of the 5ms blanking delay. For large load capacitors, it may be necessary to connect an external capacitor from GATE to GND as described in the Turn-On Sequence section.

After start-up, any transient overcurrent faults lasting less than 100µs are ignored. Any overcurrent condition lasting more than 100µs will initiate the 5ms ECB blanking delay (time point t_4). After the ECB blanking delay, the ECB is armed for the following 5ms (time point t_5 to t_6). Any 100µs overcurrent pulse during this time latches off the MOSFET. In summary, for 5ms to 10ms after a 100µs or greater overcurrent fault is detected, a second 100µs fault condition causes the MOSFET to latchoff. If no overcurrent condition is detected during this time, the part re-enters the IDLE state and another blanking delay following an overcurrent condition is again required before the MOSFET latches off. Figure 7 shows how the output latches off following an overcurrent fault.

During a severe short-circuit (see Figure 8), the output load current can briefly surge to tens of amperes. The LTC4224 rapidly brings the current under control by discharging

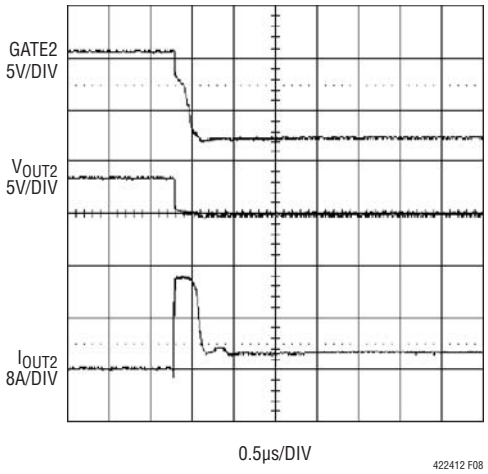


Figure 8. Severe Short-Circuit on Output

the MOSFET's gate with 125mA towards ground. After a short delay, the ACL amplifier regulates the gate voltage until the ECB trips at the end of 5ms.

Undervoltage Fault

An undervoltage fault occurs if either V_{CC1} or V_{CC2} falls below 0.8V for longer than 8µs. This turns off the affected supply's switch by discharging GATE with 1.5mA and clears its fault latch. An undervoltage fault on one supply does not affect the operation of the other supply. If V_{CC}, the higher of V_{CC1} and V_{CC2}, falls below 2.4V for more than 12µs, all supply switches are turned off and all fault latches are cleared.

APPLICATIONS INFORMATION

If there is significant supply lead inductance, a severe output short may collapse the input to ground before the LTC4224 can bring the current under control. In this case, the undervoltage lockout activates after an 8µs filter delay, and the GATE is pulled down by 1.5mA.

Resetting Faults

Following an overcurrent fault, the LTC4224-1 latches off while the LTC4224-2 automatically restarts after a four second cool down period. An overcurrent fault on either supply causes the ECB for that supply to turn off the MOSFET and pull the $\overline{FAULT}$ pin low. Faults are reset by pulling the $\overline{ON}$ pin high for at least 20µs, after which the $\overline{FAULT}$ pin releases and the turn-on sequence begins. Taking the lower supply below $V_{CCLO(UVL)}$ clears only that supply's fault and the turn-on sequence commences immediately. Pulling the higher supply below $V_{CC(UVL)}$ clears both supplies' faults and the turn-on sequence begins after a 160ms UV turn-on delay. When both supplies are above 2.5V, either supply going low only resets its own fault.

For the auto-retry version (LTC4224-2), if the fault is not cleared within four seconds, the latched fault will be cleared automatically. $\overline{FAULT}$ will go high and the turn-on sequence will begin. A persistent fault results in an auto-retry duty cycle of about 0.1%. Figure 9 shows an auto-retry sequence as a result of an overcurrent fault.

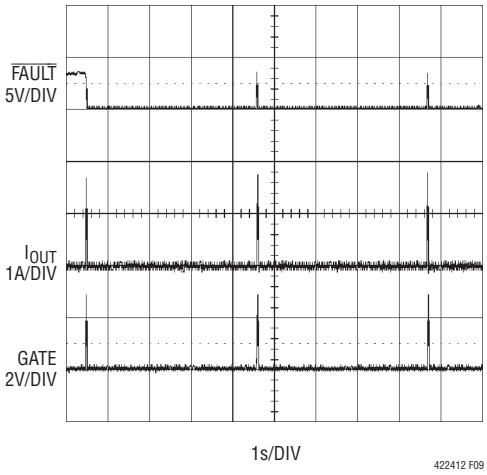


Figure 9. Auto-Retry After Overcurrent Fault

Gate Pin Voltage

The gate drive is compatible with logic level MOSFETs, but caution is required if one supply is low. The guaranteed range of gate drive is 4.5V to 7V, with a typical value of 5.5V. Each GATE pin is clamped with respect to V_{CC}, the higher of the two input supplies. When V_{CC} is at 5V, both GATE pins can be as high as 12V above ground. If the lower supply is at 0V, the gate-to-source voltage of its MOSFET can be 12V. In such applications, MOSFETs with gate-to-source breakdown ratings of 12V or greater are recommended.

Active Current Loop Compensation

The active current loop is compensated by the parasitic capacitance of the external MOSFET. No further compensation components are normally required. In the case where a MOSFET with less than 600pF of gate capacitance is chosen, a 600pF compensation capacitor connected between the GATE pin and ground may be required.

Supply Transient Protection

In applications where the supply inputs are fed directly from the regulated output of the backplane supply, bulk bypassing assures a spike-free operating environment. In other applications where bulk bypassing is located far from the LTC4224, spikes generated during output short-circuit events could exceed the absolute maximum ratings for V_{CC}. To minimize such spikes, use wider traces or heavier trace plating to reduce the power trace inductance.

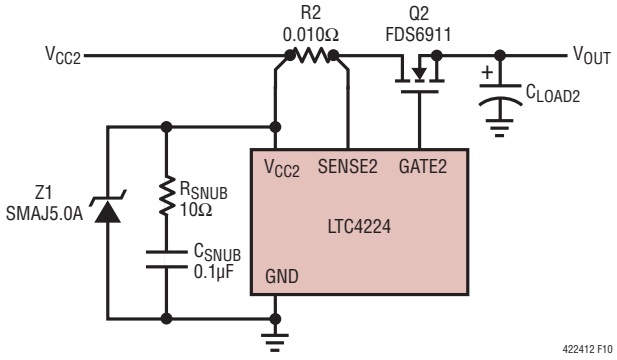


Figure 10. Input Supply Transient Protection Network for Applications without Input Capacitance

APPLICATIONS INFORMATION

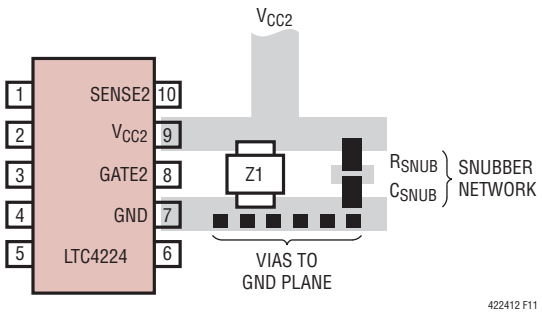


Figure 11. Recommended Layout for Input Supply Transient Protection Network

Also, bypass locally with a 10µF electrolytic and 100nF ceramic, or alternatively clamp the input with a transient voltage suppressor (Z1) as shown in Figure 10. A 10Ω, 100nF snubber damps the response and eliminates ringing. A recommended layout of the transient protection devices Z1, R_{SNUB} and C_{SNUB} around the LTC4224 is shown in Figure 11.

PCB Layout Considerations

For proper operation of the LTC4224's electronic circuit breaker, Kelvin connections to the sense resistors are strongly recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout for the sense resistors and the power MOSFET around the LTC4224 is illustrated in Figure 12. Note that it is important to keep the trace from the LTC4224's GATE pin to the FDS6911's gate short.

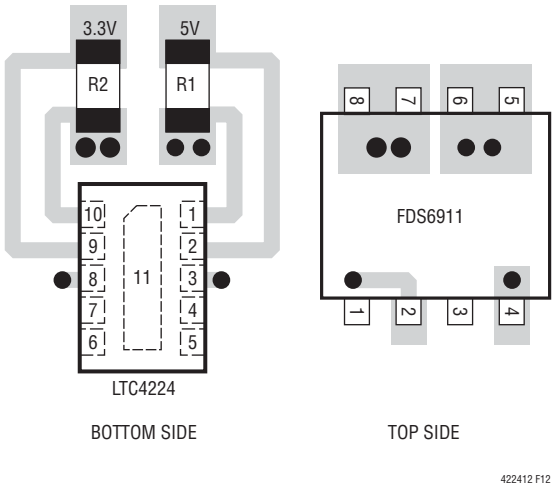


Figure 12. Recommended Layout for Power MOSFET and Sense Resistors

In Hot Swap applications where load currents can be 10A, wide PCB traces are recommended to minimize resistance and temperature rise. The suggested trace width for 1oz copper foil is 0.03" for each ampere of DC current to keep PCB trace resistance, voltage drop and temperature rise to a minimum. Note that the sheet resistance of 1oz copper foil is approximately 0.5mΩ/square and voltage drops due to trace resistances add up quickly in high current applications.

In most applications, it is necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PCB. For 1oz copper foil plating, a general rule is 1A of DC current per via. Consult your PCB fabrication facility for design rules pertaining to other plating thicknesses.

Design Example

As a design example, consider the following specifications: V_{CC1} = 5V, V_{CC2} = 3.3V, $I_{LOAD1(MAX)}$ = 1A, $I_{LOAD2(MAX)}$ = 2A, C_{LOAD1} = C_{LOAD2} = 150µF (see Figure 1).

First, select the sense resistor for each supply. Calculate the R1 and R2 values based on the maximum load current and the minimum circuit breaker threshold limit, $\Delta V_{SENSE(CB)(MIN)}$.

If a 1% tolerance is assumed for the sense resistors, then the following values of resistance should suffice:

Table 2. Sense Resistor Values

SUPPLY VOLTAGE	R_{SENSE} (1%)	$I_{TRIP(MIN)}$	$I_{TRIP(MAX)}$
5V	15mΩ	1.49A	1.85A
3.3V	10mΩ	2.23A	2.78A

For proper operation, $I_{TRIP(MIN)}$ must exceed the maximum load current with margin, so R_{SENSE1} = 15mΩ and R_{SENSE2} = 10mΩ should suffice for the V_{CC1} and V_{CC2} supplies respectively.

APPLICATIONS INFORMATION

Next, assume that there is no load current at start-up, and calculate the inrush current required to charge the load capacitor. As there is no gate capacitor, the supplies start-up in current limit. Compute the time, t_{SU}, it takes to fully charge the load capacitor:

$$t_{SU} = \frac{V_{CC} \bullet C_{LOAD}}{I_{TRIP}}$$

Table 3 lists the worst-case t_{SU} values assuming 30% tolerance for load capacitances.

Table 3. Worst-Case t_{SU}

VOLTAGE SUPPLY	$t_{SU(MIN)}$	$t_{SU(MAX)}$
5V	0.53ms	0.65ms
3.3V	0.23ms	0.29ms

The start-up ECB blanking delay is guaranteed to be at least 2.5ms, which is longer than the t_{SU} tabulated in Table 3. Hence, both supplies can start up successfully.

Next, verify that the thermal ratings of the selected external MOSFETs are not exceeded during power-up or an output short-circuit. Assuming the MOSFET dissipates power only due to inrush current charging the load capacitor, the energy dissipated in the MOSFET during power-up is the same as that stored in the load capacitor after power-up. The average power dissipated in the MOSFET is given by:

$$P_{AVG} = \frac{C_{LOAD} \bullet V_{OUT}^{2}}{2 \bullet t_{SU}}$$

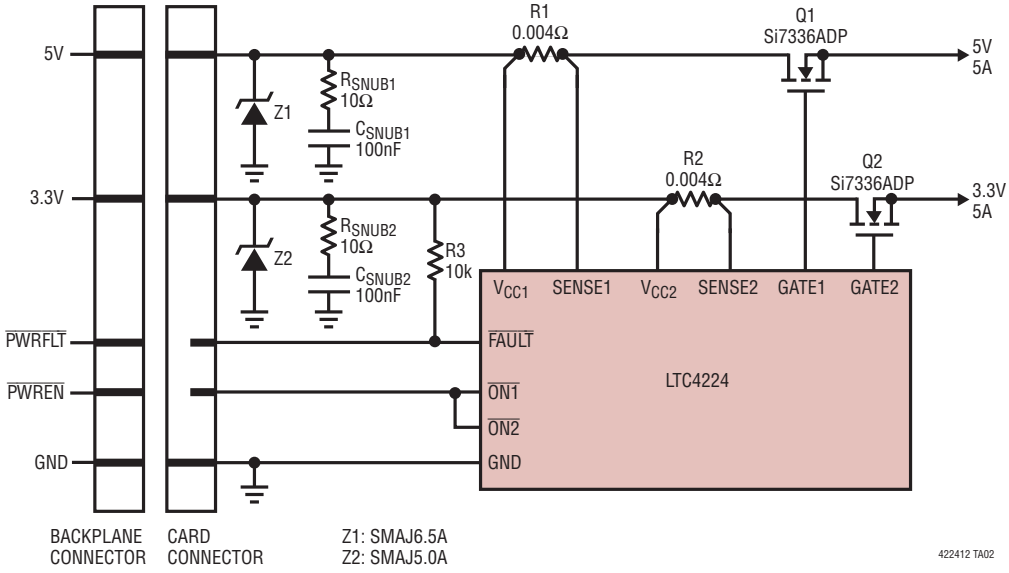
The worst-case P_{AVG} is calculated to be 4.6W for both the 5V supply and the 3.3V supply. In this example, the FDS6911 MOSFET offers a good solution. Since this MOSFET is a dual N-channel in a single SO8 package, it must be able to tolerate the combined power dissipation of both supplies during the t_{SU} start-up time. The increase in steady-state junction temperature due to power dissipated in the MOSFET is $\Delta T = P_{AVG} \bullet Z_{TH}$ where Z_{TH} is the thermal impedance.

Under this condition, the FDS6911 datasheet's Transient Thermal Impedance plot indicates that the junction temperature will increase by 6.4°C using Z_{THJC} = 0.7°C/W (single pulse). The FDS6911's on-resistance is 17mΩ at V_{GS} = 4.5V, 25°C.

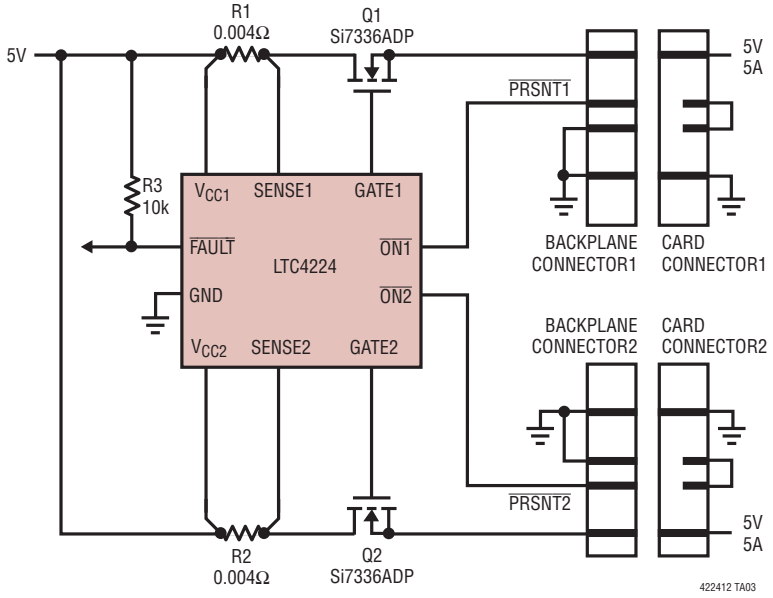
The magnitude of the power pulse that results during a severe overload is calculated to be 9.25W for the 5V supply and 9.2W for the 3.3V supply under the worst case conditions. Assuming a worst-case circuit breaker timeout period of 7.5ms, the junction temperature will increase by 25°C, with one supply short-circuited. If both supplies are short-circuited, the junction temperature will increase by 50°C in the worst-case. During auto-retry (LTC4224-2), in the event of persistent faults at both supplies, the ample four second cooling delay limits the increase in junction temperature to 50°C. The SOA curves of the FDS6911 indicate that the above conditions are safe.

TYPICAL APPLICATION

5V and 3.3V Card Resident Application

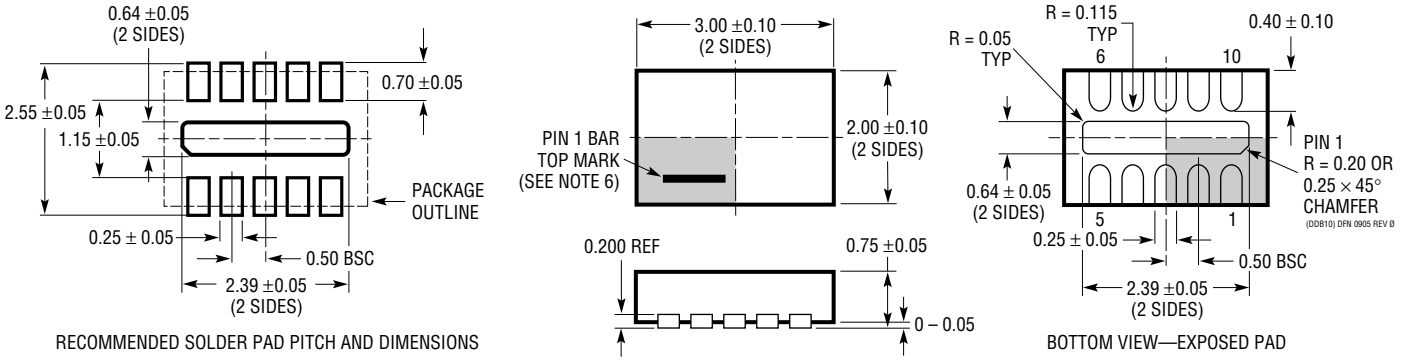


Hot Swap Application for Two Add-In Cards



PACKAGE DESCRIPTION

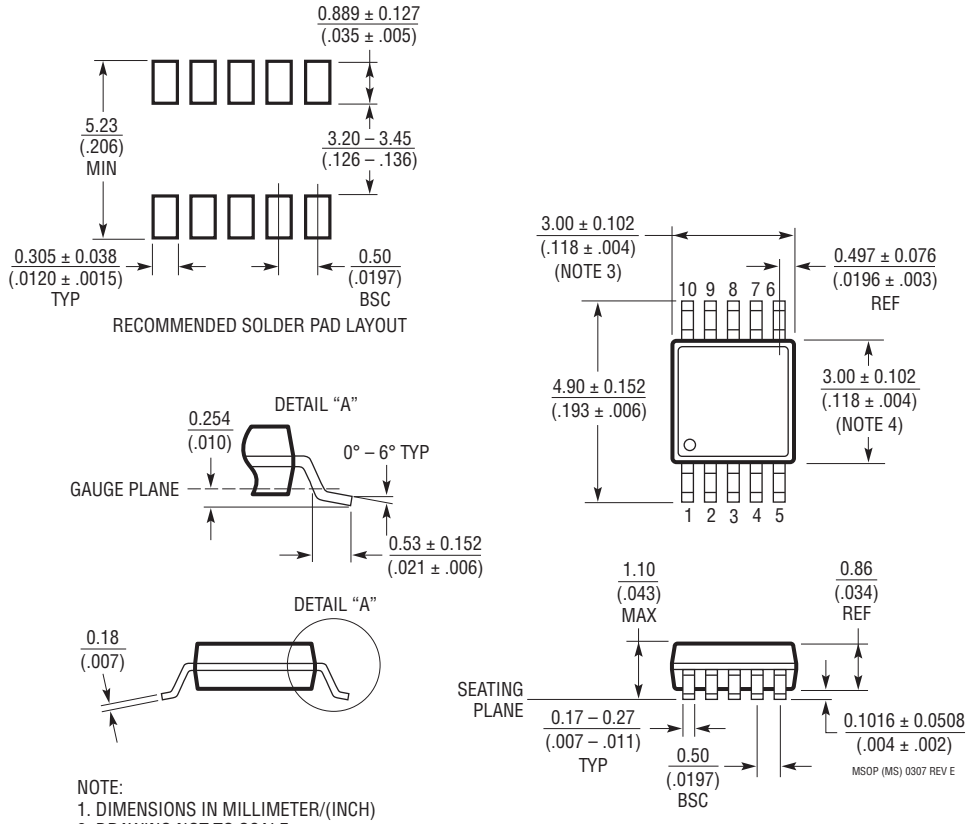
DDB Package
10-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1722)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX