Dual Ideal Diode and Hot Swap Controller

FEATURES

- **Power Path and Inrush Current Control for Redundant Supplies**
- **Low Loss Replacement for Power Schottky Diodes**
- **Allows Safe Hot Swapping from a Live Backplane**
- **2.9V to 18V Operating Range**
- **Controls N-Channel MOSFETs**
- **Limits Peak Fault Current in ≤1µs**
- **0.5µs Turn-On and Reverse Turn-Off Time**
- Adjustable Current Limit with Circuit Breaker
- Smooth Switchover without Oscillation
- Adjustable Current Limit Fault Delay
- Fault and Power Status Output
- LTC4225-1: Latch Off After Fault
- LTC4225-2: Automatic Retry After Fault
- 24-Lead 4mm × 5mm QFN and SSOP Packages

APPLICATIONS

- Redundant Power Supplies
- Supply Holdup
- MicroTCA Systems and Servers
- Telecom Networks
- Power Prioritizer

DESCRIPTION

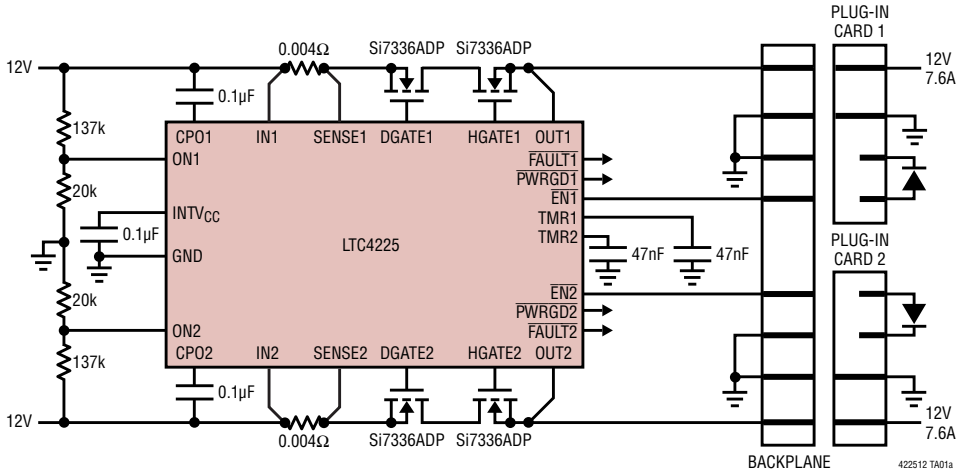
The LTC®4225 offers ideal diode and Hot Swap™ functions for two power rails by controlling external series connected N-channel MOSFETs. MOSFETs acting as ideal diodes replace two high power Schottky diodes and the associated heat sinks, saving power and board area. Hot Swap control MOSFETs allow boards to be safely inserted and removed from a live backplane by limiting inrush current. The supply output is also protected against short-circuit faults with a fast acting current limit and internal timed circuit breaker.

The LTC4225 regulates the forward voltage drop across the back-to-back MOSFETs to ensure smooth current transfer from one supply to the other without oscillation. The ideal diodes turn on quickly to reduce the load voltage droop during supply switch-over. If the input supply fails or is shorted, a fast turn-off minimizes reverse-current transients.

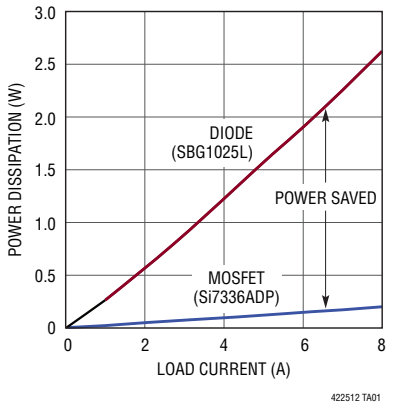
The LTC4225 allows independent on/off control, and reports fault and power good status for the supply. The LTC4225-1 features a latch-off circuit breaker, while the LTC4225-2 provides automatic retry after a fault.

TYPICAL APPLICATION

µTCA Application



Power Dissipation vs Load Current



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages
- IN1, IN2 ..... –0.3V to 24V
- $INTV_{CC}$ ..... –0.3V to 7V

Input Voltages
- ON1, ON2, $\overline{EN1}$, $\overline{EN2}$ ..... –0.3V to 24V
- TMR1, TMR2 ..... –0.3V to $INTV_{CC}$ + 0.3V
- SENSE1, SENSE2 ..... –0.3V to 24V

Output Voltages
- $\overline{FAULT1}$, $\overline{FAULT2}$, $\overline{PWRGD1}$, $\overline{PWRGD2}$ ..... –0.3V to 24V
- CPO1, CPO2 (Note 3) ..... –0.3V to 35V
- DGATE1, DGATE2 (Note 3) ..... –0.3V to 35V
- HGATE1, HGATE2 (Note 4) ..... –0.3V to 35V
- OUT1, OUT2 ..... –0.3V to 24V

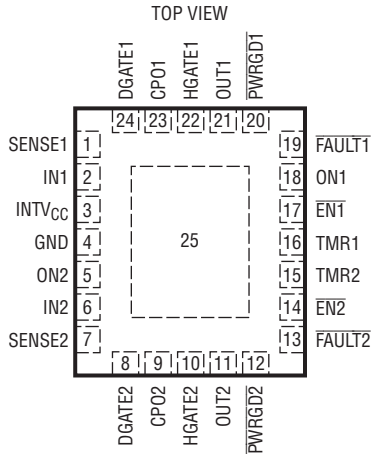
Average Currents
- $\overline{FAULT1}$, $\overline{FAULT2}$, $\overline{PWRGD1}$, $\overline{PWRGD2}$ 5mA
- $INTV_{CC}$ 1mA

Operating Temperature Range
- LTC4225C ..... 0°C to 70°C
- LTC4225I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

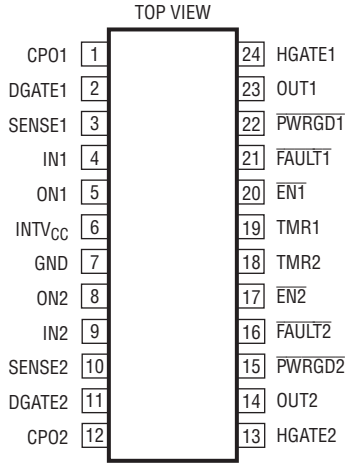
Lead Temperature (Soldering, 10 sec)
- GN Package ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 25) PCB GND CONNECTION OPTIONAL



GN PACKAGE
24-LEAD PLASTIC SSOP NARROW

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4225CUFD-1#PBF	LTC4225CUFD-1#TRPBF	42251	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4225CUFD-2#PBF	LTC4225CUFD-2#TRPBF	42252	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4225IUFD-1#PBF	LTC4225IUFD-1#TRPBF	42251	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4225IUFD-2#PBF	LTC4225IUFD-2#TRPBF	42252	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4225CGN-1#PBF	LTC4225CGN-1#TRPBF	LTC4225GN-1	24-Lead Plastic SSOP	0°C to 70°C
LTC4225CGN-2#PBF	LTC4225CGN-2#TRPBF	LTC4225GN-2	24-Lead Plastic SSOP	0°C to 70°C
LTC4225IGN-1#PBF	LTC4225IGN-1#TRPBF	LTC4225GN-1	24-Lead Plastic SSOP	–40°C to 85°C
LTC4225IGN-2#PBF	LTC4225IGN-2#TRPBF	LTC4225GN-2	24-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{IN}	Input Supply Range		●	2.9		18	V
I_{IN}	Input Supply Current		●		2.8	5	mA
$V_{IN(UVL)}$	Input Supply Undervoltage Lockout	IN Rising	●	1.75	1.9	2.05	V
$\Delta V_{IN(HYST)}$	Input Supply Undervoltage Lockout Hysteresis		●	10	50	90	mV
V_{INTVCC}	Internal Regulator Voltage		●	4.5	5	5.6	V
$V_{INTVCC(UVL)}$	Internal V_{CC} Undervoltage Lockout	$INTV_{CC}$ Rising	●	2.1	2.2	2.3	V
$\Delta V_{INTVCC(HYST)}$	Internal V_{CC} Undervoltage Lockout Hysteresis		●	30	60	90	mV
Ideal Diode Control							
$\Delta V_{FWD(REG)}$	Forward Regulation Voltage ($V_{INn} – V_{OUTn}$)		●	10	25	40	mV
ΔV_{DGATE}	External N-Channel Gate Drive ($V_{DGATEn} – V_{INn}$)	IN < 7V, ΔV_{FWD} = 0.1V, I = 0, –1µA IN = 7V to 18V, ΔV_{FWD} = 0.1V, I = 0, –1µA	● ●	5 10	7 12	14 14	V V
$I_{CPO(UP)}$	CPOn Pull-Up Current	CPO = IN = 2.9V CPO = IN = 18V	● ●	–60 –50	–95 –85	–120 –110	µA µA
$I_{DGATE(FPU)}$	DGATEn Fast Pull-Up Current	ΔV_{FWD} = 0.2V, ΔV_{DGATE} = 0V, CPO = 17V			–1.5		A
$I_{DGATE(FPD)}$	DGATEn Fast Pull-Down Current	ΔV_{FWD} = –0.2V, ΔV_{DGATE} = 5V			1.5		A
$t_{ON(DGATE)}$	DGATEn Turn-On Delay	ΔV_{FWD} = 0.2V, C_{DGATE} = 10nF	●		0.25	0.5	µs
$t_{OFF(DGATE)}$	DGATEn Turn-Off Delay	ΔV_{FWD} = –0.2V, C_{DGATE} = 10nF	●		0.2	0.5	µs
Hot Swap Control							
$\Delta V_{SENSE(CB)}$	Circuit Breaker Trip Sense Voltage ($V_{INn} – V_{SENSEn}$)		●	47.5	50	52.5	mV
$\Delta V_{SENSE(ACL)}$	Active Current Limit Sense Voltage ($V_{INn} – V_{SENSEn}$)		●	55	65	75	mV
ΔV_{HGATE}	External N-Channel Gate Drive ($V_{HGATEn} – V_{OUTn}$)	IN < 7V, I = 0, –1µA IN = 7V to 18V, I = 0, –1µA	● ●	4.8 10	7 12	14 14	V V
$\Delta V_{HGATE(PG)}$	Gate-Source Voltage for Power Good		●	3.6	4.2	4.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{HGATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, HGATE = 0V	●	–7	–10	–13	µA
$I_{HGATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, HGATE = OUT + 5V	●	150	300	500	µA
$I_{HGATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, HGATE = OUT + 5V	●	100	200	300	mA
$t_{PHL(SENSE)}$	Sense Voltage (INn – SENSEn) High to HGATEn Low	ΔV_{SENSE} = 300mV, C_{HGATE} = 10nF	●		0.5	1	µs
$t_{OFF(HGATE)}$	$\overline{EN}$n High to HGATEn Low ONn Low to HGATEn Low INn Low to HGATEn Low		● ● ●		20 10 10	40 20 20	µs µs µs
$t_{D(HGATE)}$	ONn High, $\overline{EN}$n Low to HGATEn Turn-On Delay		●	50	100	150	ms
$t_{P(HGATE)}$	ONn to HGATEn Propagation Delay	ON = Step 0.8V to 2V	●		10	20	µs
Input/Output Pin							
I_{SENSE}	SENSEn Input Current	SENSE = 12V	●	10	50	100	µA
$V_{ON(TH)}$	ONn Threshold Voltage	ON Rising	●	1.21	1.235	1.26	V
$\Delta V_{ON(HYST)}$	ONn Hysteresis		●	40	80	140	mV
$V_{ON(RESET)}$	ONn Fault Reset Threshold Voltage	ON Falling	●	0.55	0.6	0.63	V
$I_{ON(LEAK)}$	ONn Input Leakage Current	ON = 5V	●		0	±1	µA
$V_{\overline{EN}(TH)}$	$\overline{EN}$n Threshold Voltage	$\overline{EN}$ Rising	●	1.185	1.235	1.284	V
$\Delta V_{\overline{EN}(HYST)}$	$\overline{EN}$n Hysteresis		●	40	130	200	mV
$I_{\overline{EN}(UP)}$	$\overline{EN}$n Pull-Up Current	$\overline{EN}$ = 1V	●	–7	–10	–13	µA
$V_{TMR(TH)}$	TMRn Threshold Voltage	TMR Rising TMR Falling	● ●	1.198 0.15	1.235 0.2	1.272 0.25	V V
$I_{TMR(UP)}$	TMRn Pull-Up Current	TMR = 1V, In Fault Mode	●	–75	–100	–125	µA
$I_{TMR(DN)}$	TMRn Pull-Down Current	TMR = 2V, No Faults	●	1.4	2	2.6	µA
$I_{TMR(RATIO)}$	TMRn Current Ratio $I_{TMR(DN)}/I_{TMR(UP)}$		●	1.4	2	2.7	%
I_{OUT}	OUTn Current	OUT = 11V, IN = 12V, ON = 2V OUT = 13V, IN = 12V, ON = 2V	● ●		50 2.2	120 4	µA mA
V_{OL}	Output Low Voltage ($\overline{FAULT}$n, $\overline{PWRGD}$n)	I = 1mA	●		0.15	0.4	V
V_{OH}	Output High Voltage ($\overline{FAULT}$n, $\overline{PWRGD}$n)	I = –1µA	●	$INTV_{CC}$ – 1	$INTV_{CC}$ – 0.5		V
I_{OH}	Input Leakage Current ($\overline{FAULT}$n, $\overline{PWRGD}$n)	V = 18V	●		0	±1	µA
I_{PU}	Output Pull-Up Current ($\overline{FAULT}$n, $\overline{PWRGD}$n)	V = 1.5V	●	–7	–10	–13	µA
$t_{RST(ON)}$	ONn Low to $\overline{FAULT}$n High		●		20	40	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

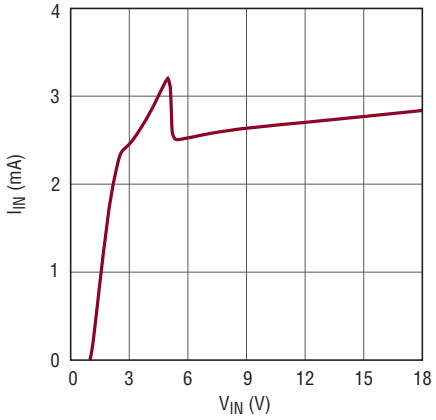
Note 2: All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the DGATE and CPO pins to a minimum of 10V above and a diode below IN. Driving these pins to voltages beyond the clamp may damage the device.

Note 4: An internal clamp limits the HGATE pin to a minimum of 10V above and a diode below OUT. Driving this pin to voltages beyond the clamp may damage the device.

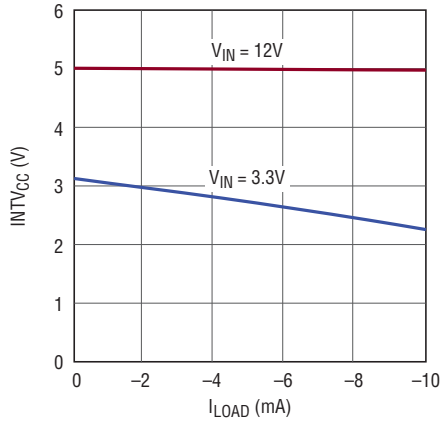
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{IN} = 12V, unless otherwise noted.

IN Supply Current vs Voltage



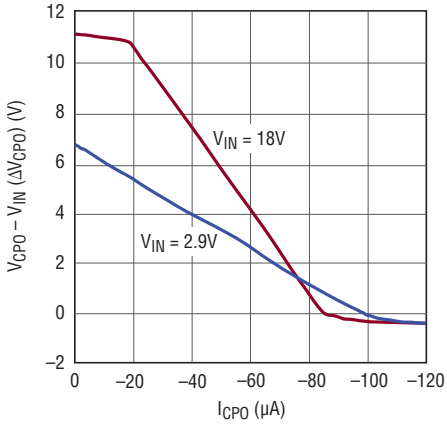
422512 G01

$INTV_{CC}$ Load Regulation



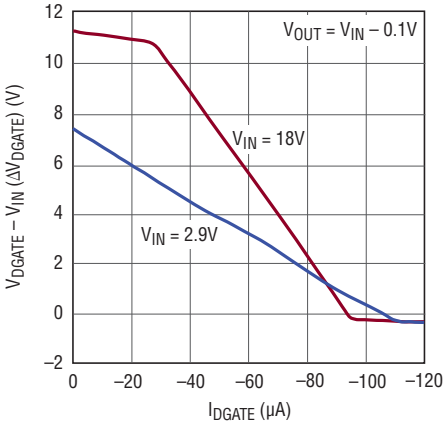
422512 G02

CPO Voltage vs Current



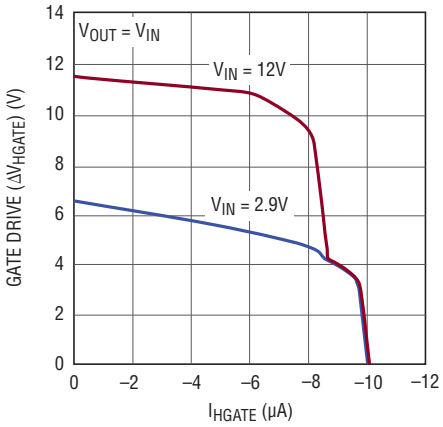
422512 G03

Diode Gate Voltage vs Current



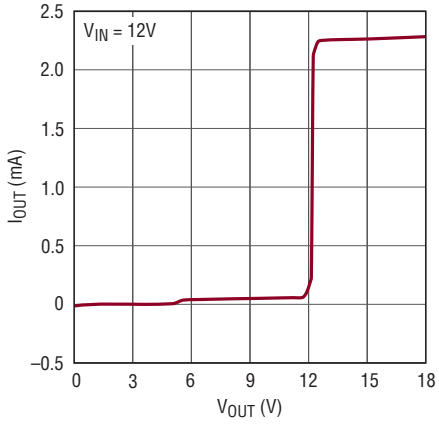
422512 G04

Hot Swap Gate Voltage vs Current



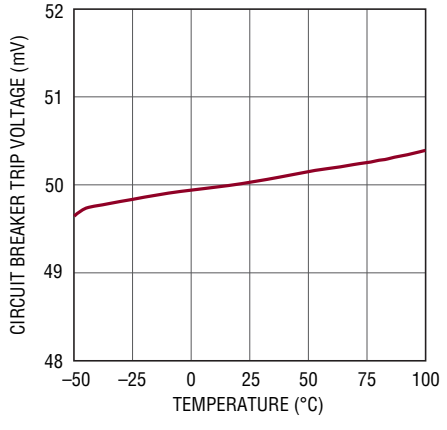
422712 G05

OUT Current vs Voltage



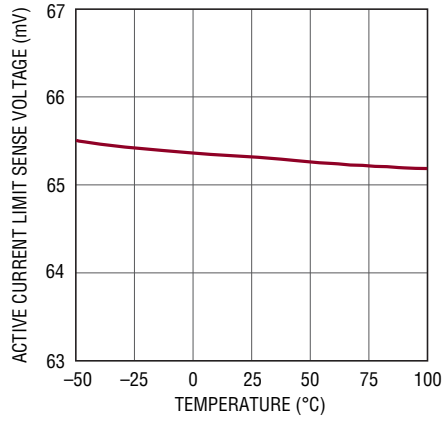
422512 G06

Circuit Breaker Trip Voltage vs Temperature



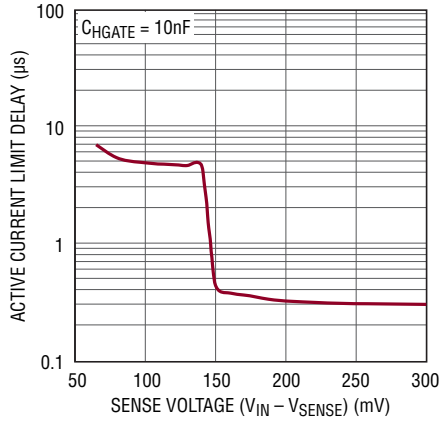
422512 G07

Active Current Limit Sense Voltage vs Temperature



422512 G08

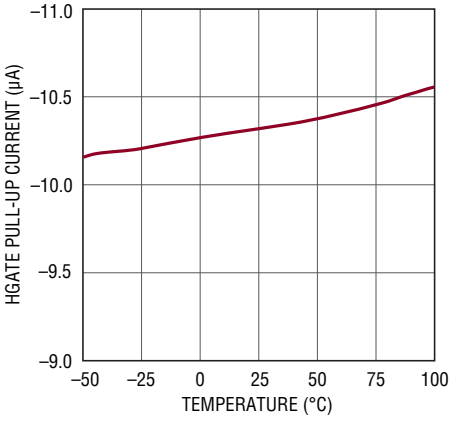
Active Current Limit Delay vs Sense Voltage



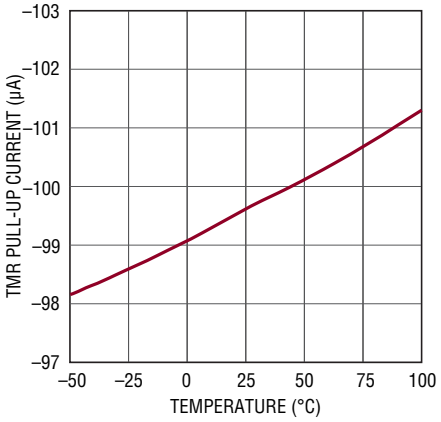
422512 G09

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{IN} = 12V, unless otherwise noted.

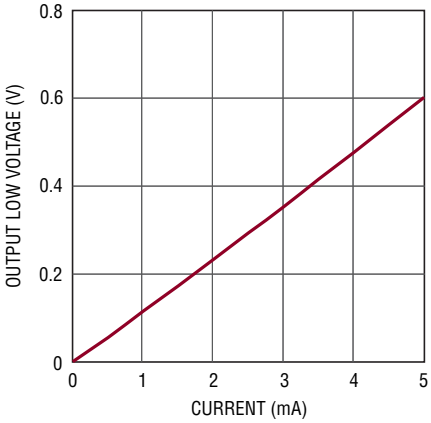
HGATE Pull-Up Current vs Temperature



TMR Pull-Up Current vs Temperature



$\overline{PWRGD}$, $\overline{FAULT}$ Output Low Voltage vs Current



PIN FUNCTIONS

CPO1, CPO2: Charge Pump Output. Connect a capacitor from CPO1 or CPO2 to the corresponding IN1 or IN2 pin. The value of this capacitor is approximately 10× the gate capacitance (C_{ISS}) of the external MOSFET for ideal diode control. The charge stored on this capacitor is used to pull up the gate during a fast turn-on. Leave this pin open if fast turn-on is not needed.

DGATE1, DGATE2: Ideal Diode MOSFET Gate Drive Output. Connect this pin to the gate of an external N-channel MOSFET for ideal diode control. An internal clamp limits the gate voltage to 12V above and a diode voltage below IN. During fast turn-on, a 1.5A pull-up charges DGATE from CPO. During fast turn-off, a 1.5A pull-down discharges DGATE to IN.

$\overline{EN1}$, $\overline{EN2}$: Enable Input. Ground this pin to enable Hot Swap control. If this pin is pulled high, the MOSFET is not allowed to turn on. A 10µA current source pulls this pin up to a diode below $INTV_{CC}$. Upon $\overline{EN}$ going low when ON is high, an internal timer provides a 100ms start-up delay for debounce, after which the fault is cleared.

Exposed Pad (UFD Package): The exposed pad may be left open or connected to device ground.

$\overline{FAULT1}$, $\overline{FAULT2}$: Fault Status Output. Open-drain output that is normally pulled high by a 10µA current source to a diode below $INTV_{CC}$. It may be pulled above $INTV_{CC}$ using an external pull-up. It pulls low when the circuit breaker is tripped after an overcurrent fault timeout. Leave open if unused.

GND: Device Ground.

HGATE1, HGATE2: Hot Swap MOSFET Gate Drive Output. Connect this pin to the gate of the external N-channel MOSFET for Hot Swap control. An internal 10µA current source charges the MOSFET gate. An internal clamp limits the gate voltage to 12V above and a diode below OUT. During turn-off, a 300µA pull-down discharges HGATE to ground. During an output short or $INTV_{CC}$ undervoltage lockout, a fast 200mA pull-down discharges HGATE to OUT.

IN1, IN2: Positive Supply Input and MOSFET Gate Drive Return. The 5V $INTV_{CC}$ supply is generated from IN1 and IN2 via an internal diode-OR. The voltage sensed at this pin is used to control DGATE for forward voltage regulation and reverse turn-off. It also senses the positive side of the current sense resistor. The gate fast pull-down current returns through this pin when DGATE is discharged.

PIN FUNCTIONS

$INTV_{CC}$: Internal 5V Supply Decoupling Output. This pin must have a 0.1µF or larger capacitor. An external load of less than 500µA can be connected at this pin.

ON1, ON2: On Control Input. A rising edge above 1.235V turns on the external Hot Swap MOSFET and a falling edge below 1.155V turns it off. Connect this pin to an external resistive divider from IN to monitor the supply undervoltage condition. Pulling the ON pin below 0.6V resets the electronic circuit breaker.

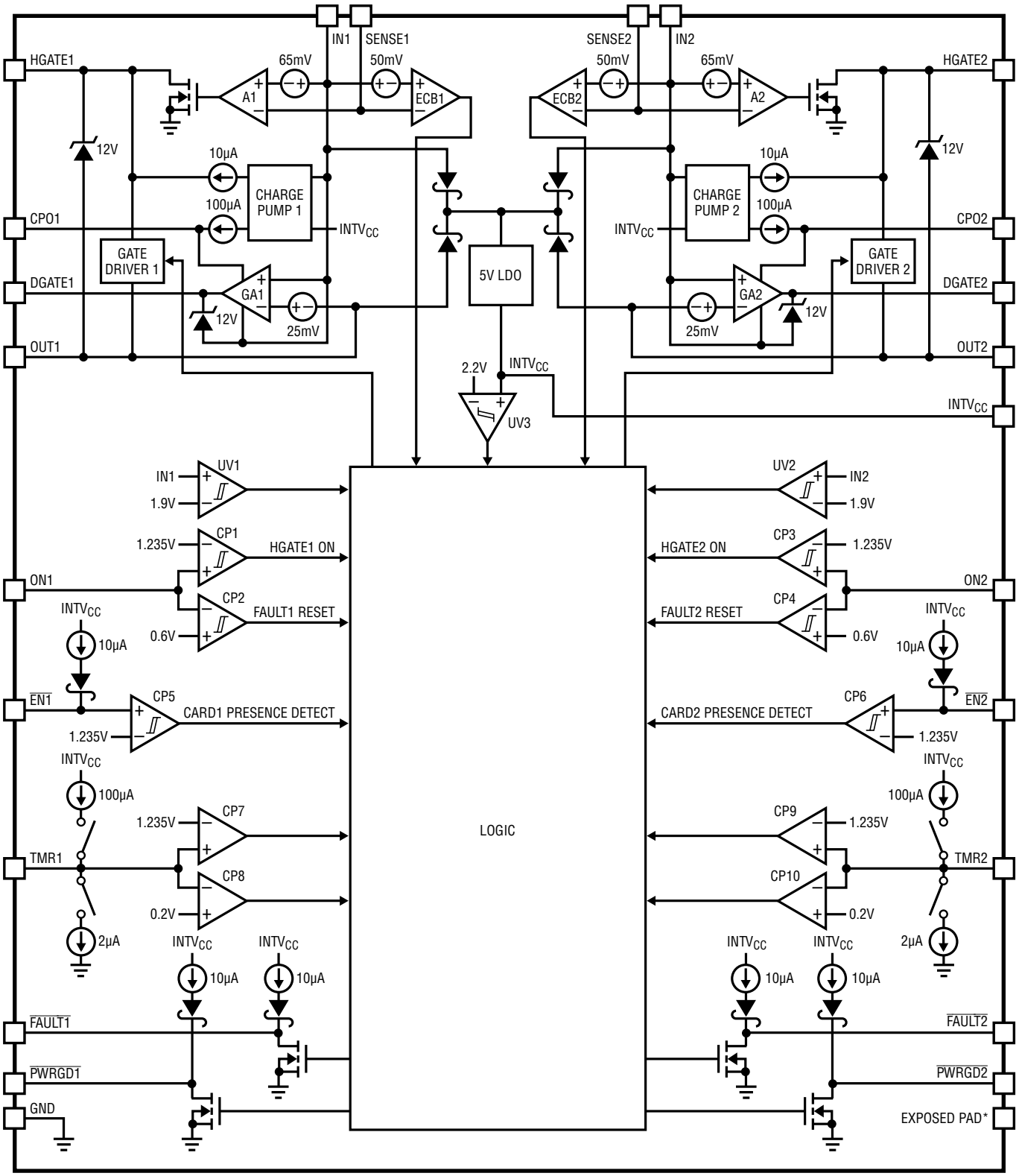
OUT1, OUT2: Output Voltage Sense and MOSFET Gate Drive Return. Connect this pin to the output side of the external MOSFET. The voltage sensed at this pin is used to control DGATE. The gate fast pull-down current returns through this pin when HGATE is discharged.

$\overline{PWRGD1}$, $\overline{PWRGD2}$: Power Status Output. Open-drain output that is normally pulled high by a 10µA current source to a diode below $INTV_{CC}$. It may be pulled above $INTV_{CC}$ using an external pull-up. It pulls low when the MOSFET gate drive between HGATE and OUT exceeds the gate-to-source voltage of 4.2V. Leave open if unused.

SENSE1, SENSE2: Negative Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls HGATE to limit the voltage between IN and SENSE to 65mV. A circuit breaker trips when the sense voltage exceeds 50mV for more than a fault filter delay configured at the TMR pin.

TMR1, TMR2: Timer Capacitor Terminal. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the external Hot Swap MOSFET is turned off. The duration of the off time is 617ms/µF, resulting in a 2% duty cycle.

BLOCK DIAGRAM



*UFD PACKAGE ONLY

OPERATION

The LTC4225 functions as an ideal diode with inrush current limiting and overcurrent protection by controlling two external back-to-back N-channel MOSFETs (M_D and M_H) on a supply path. This allows boards to be safely inserted and removed in systems with a backplane powered by redundant supplies, such as µTCA applications. The LTC4225 has two separate ideal diode and Hot Swap controllers, each providing independent control for the two input supplies.

When the LTC4225 is first powered up, the gates of the back-to-back MOSFETs are held low, keeping them off. The gate drive amplifier (GA1, GA2) monitors the voltage between the IN and OUT pins and drives the DGATE pin. The amplifier quickly pulls up the DGATE pin, turning on the MOSFET for ideal diode control, when it senses a large forward voltage drop. The stored charge in an external capacitor connected between the CPO and IN pins provides the charge needed to quickly turn on the ideal diode MOSFET. An internal charge pump charges up this capacitor at device power-up. The DGATE pin sources current from the CPO pin and sinks current into the IN and GND pins.

Pulling the ON pin high and the $\overline{EN}$ pin low initiates a 100ms debounce timing cycle. After this timing cycle, a 10µA current source from the charge pump ramps up the HGATE pin. When the Hot Swap MOSFET turns on, the inrush current is limited at a level set by an external sense resistor (R_S) connected between the IN and SENSE pins. An active current limit amplifier (A1, A2) servos the gate of the MOSFET to 65mV across the current sense resistor. Inrush current can be further reduced, if desired, by adding a capacitor from HGATE to GND. When the MOSFET's gate overdrive (HGATE to OUT voltage) exceeds 4.2V, the $\overline{PWRGD}$ pin pulls low.

When both of the MOSFETs are turned on, the gate drive amplifier controls DGATE to servo the forward voltage drop ($V_{IN}-V_{OUT}$) across the sense resistor and the back-to-back MOSFETs to 25mV. If the load current causes more than 25mV of voltage drop, the gate voltage rises to enhance the MOSFET used for ideal diode control. For large output currents, the MOSFET's gate is driven fully on and the voltage drop across the MOSFETs is equal to the sum of the $I_{LOAD} \bullet R_{DS(ON)}$ of the two MOSFETs in series.

In the case of an input supply short circuit when the MOSFETs are conducting, a large reverse current starts flowing from the load towards the input. The gate drive amplifier detects this failure condition as soon as it appears and turns off the ideal diode MOSFET by pulling down the DGATE pin.

In the case where an overcurrent fault occurs on the supply output, the current is limited to $65mV/R_S$. After a fault filter delay set by 100µA charging the TMR pin capacitor, the circuit breaker trips and pulls the HGATE pin low, turning off the Hot Swap MOSFET. Only the supply at fault is affected, with the corresponding $\overline{FAULT}$ pin latched low. At this point, the DGATE pin continues to pull high and keeps the ideal diode MOSFET on.

Internal clamps limit both the DGATE to IN and CPO to IN voltages to 12V. The same clamp also limits the CPO and DGATE pins to a diode voltage below the IN pin. Another internal clamp limits the HGATE to OUT voltage to 12V and also clamps the HGATE pin to a diode voltage below the OUT pin.

Power to the LTC4225 is supplied from either the IN or OUT pins, through an internal diode-OR circuit to a low dropout regulator (LDO). That LDO generates a 5V supply at the $INTV_{CC}$ pin and powers the LTC4225's internal low voltage circuitry.

APPLICATIONS INFORMATION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. Power ORing diodes are commonly used to connect these supplies at the point of load, but at the expense of power loss due to significant diode forward voltage drop. The LTC4225 minimizes this power loss by using external N-channel MOSFETs for the pass elements, allowing for a low voltage drop from the supply to the load when the MOSFETs are turned on. When an input source voltage drops below the output common supply voltage, the appropriate MOSFET is turned off, thereby matching the function and performance of an ideal diode. By adding a current sense resistor and configuring two MOSFETs back-to-back with separate gate control, the LTC4225 enhances the ideal diode performance with inrush current limiting and overcurrent protection (see Figure 1). This allows the boards to be safely inserted and removed from a live backplane without damaging the connector.

Internal V_{CC} Supply

The LTC4225 can operate with input supplies from 2.9V to 18V at the IN pins. The power supply to the device is internally regulated at 5V by a low dropout regulator (LDO) with an output at the $INTV_{CC}$ pin. An internal diode-OR circuit selects the highest of the supplies at the IN and OUT pins to power the device through the LDO. The diode-OR scheme permits the device's power to be temporarily kept alive by the OUT load capacitance when the IN supplies have collapsed or shut off.

An undervoltage lockout circuit prevents all of the MOSFETs from turning on until the $INTV_{CC}$ voltage exceeds 2.2V. A 0.1µF capacitor is recommended between the $INTV_{CC}$ and GND pins, close to the device for bypassing. No external supply should be connected at the $INTV_{CC}$ pin so as not to affect the LDO's operation. A small external load of less than 500µA can be connected at the $INTV_{CC}$ pin.

Turn-On Sequence

The board power supply at the OUT pin is controlled with two external back-to-back N-channel MOSFETs (M_D, M_H). The MOSFET M_D on the supply side functions as an ideal diode, while M_H on the load side acts as a Hot Swap controlling the power supplied to the output load. The sense resistor, R_S, monitors the load current for overcurrent detection. The HGATE capacitor, C_{HG}, controls the gate slew rate to limit the inrush current. Resistor R_{HG} with C_{HG} compensates the current control loop, while R_H prevents high frequency oscillations in the Hot Swap MOSFET.

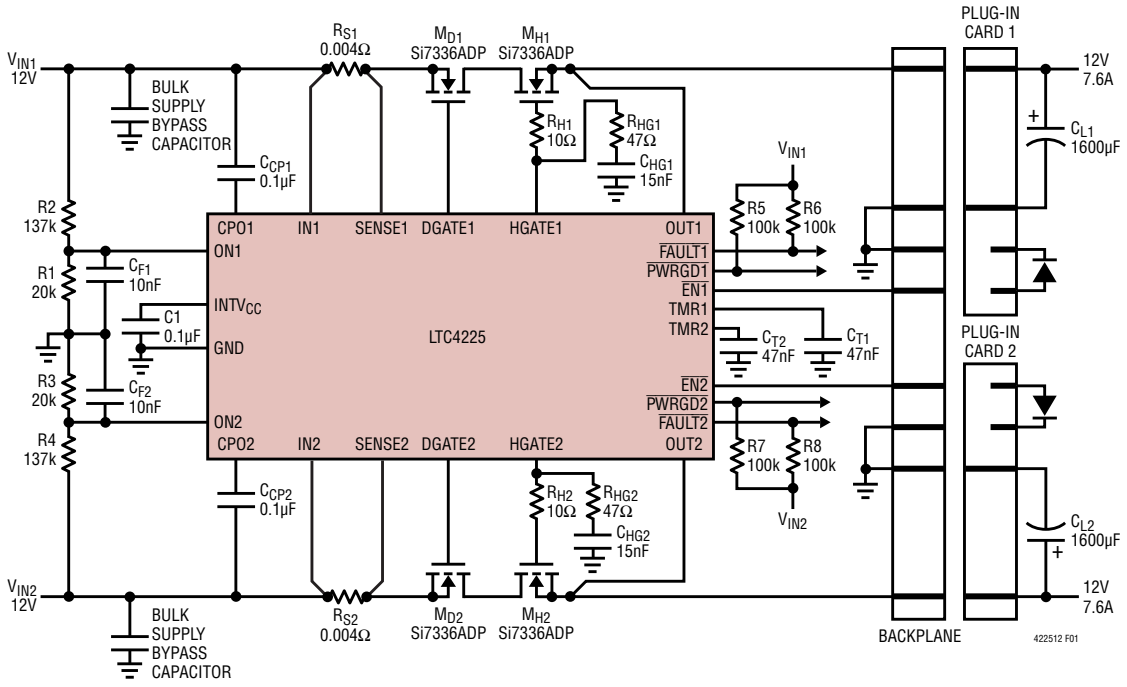


Figure 1. µTCA Application Supplying 12V Power to Two µTCA Slots

APPLICATIONS INFORMATION

During a normal power-up, the ideal diode MOSFET turns on first. As soon as the internally generated supply, $INTV_{CC}$, rises above its 2.2V undervoltage lockout threshold, the internal charge pump is allowed to charge up the CPO pins. Because the Hot Swap MOSFET is turned off at power-up, OUT remains low. As a result, the ideal diode gate drive amplifier senses a large forward drop between the IN and OUT pins, causing it to pull up DGATE to the CPO pin voltage.

Before the Hot Swap MOSFET can be turned on, $\overline{EN}$ must remain low and ON must remain high for a 100ms debounce cycle to ensure that any contact bounces during the insertion have ceased. At the end of the debounce cycle, the internal fault latches are cleared. The Hot Swap MOSFET is then allowed to turn on by charging up HGATE with a 10µA current source from the charge pump. The voltage at the HGATE pin rises with a slope equal to $10\mu A/C_{HG}$ and the supply inrush current flowing into the load capacitor, C_L, is limited to:

$$I_{INRUSH} = \frac{C_L}{C_{HG}} \bullet 10\mu A$$

The OUT voltage follows the HGATE voltage when the Hot Swap MOSFET turns on. If the voltage across the current sense resistor, R_S, becomes too high, the inrush current will be limited by the internal current limiting circuitry. Once the MOSFET gate overdrive exceeds 4.2V, the corresponding $\overline{PWRGD}$ pin pulls low to indicate that the power is good. Once OUT reaches the input supply voltage, HGATE continues to ramp up. An internal 12V clamp limits the HGATE voltage above OUT.

When both of the MOSFETs are turned on, the gate drive amplifier controls the gate of the ideal diode MOSFET, to servo its forward voltage drop across R_S, M_D and M_H to 25mV. If the load current causes more than 25mV of drop, the MOSFET gate is driven fully on and the voltage drop across the MOSFET is equal to $I_{LOAD} \bullet R_{DS(ON)}$.

Turn-Off Sequence

The external MOSFETs can be turned off by a variety of conditions. A normal turn-off for the Hot Swap MOSFET is initiated by pulling the ON pin below its 1.155V threshold (80mV ON pin hysteresis), or pulling the $\overline{EN}$ pin above its 1.235V threshold. Additionally, an overcurrent fault of sufficient duration to trip the circuit breaker also turns off the Hot Swap MOSFET. Normally, the LTC4225 turns off the MOSFET by pulling the HGATE pin to ground with a 300µA current sink.

All of the MOSFETs turn off when $INTV_{CC}$ falls below its undervoltage lockout threshold (2.2V). The DGATE pin is pulled down with a 100µA current to one diode voltage below the IN pin, while the HGATE pin is pulled down to the OUT pin by a 200mA current.

The gate drive amplifier controls the ideal diode MOSFET to prevent reverse current when the input supply falls below OUT. If the input supply collapses quickly, the gate drive amplifier turns off the ideal diode MOSFET with a fast pull-down circuit as soon as it detects that IN is 20mV below OUT. If the input supply falls at a more modest rate, the gate drive amplifier controls the MOSFET to maintain OUT at 25mV below IN.

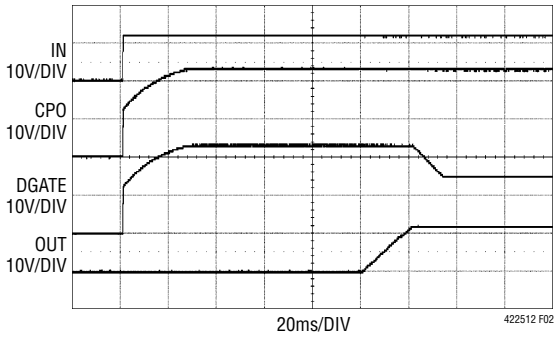


Figure 2. Ideal Diode Controller Start-Up Waveforms

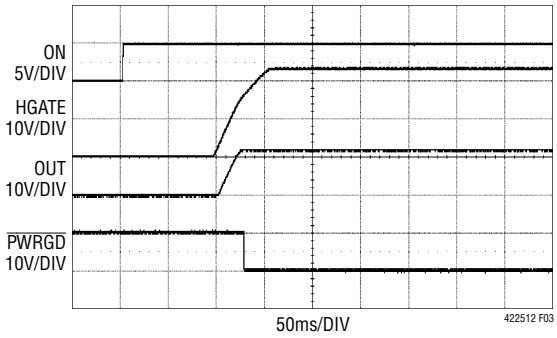


Figure 3. Hot Swap Controller Power-Up Sequence

APPLICATIONS INFORMATION

Board Presence Detect with $\overline{EN}$

If ON is high when the $\overline{EN}$ pin goes low, indicating a board presence, the LTC4225 initiates a 100ms timing cycle for contact debounce. Upon board insertion, any bounces on the $\overline{EN}$ pin restart the timing cycle. When the 100ms timing cycle is done, the internal fault latches are cleared. If the $\overline{EN}$ pin remains low at the end of the timing cycle, HGATE is charged up with a 10µA current source to turn on the Hot Swap MOSFET.

If the $\overline{EN}$ pin goes high, indicating a board removal, the HGATE pin is pulled low with a 300µA current sink after a 20µs delay, turning off the Hot Swap MOSFET without clearing any latched faults.

Overcurrent Fault

The LTC4225 features an adjustable current limit with circuit breaker function that protects the external MOSFETs against short circuits or excessive load current. The voltage across the external sense resistor (R_{S1}, R_{S2}) is monitored by an electronic circuit breaker (ECB) and active current limit (ACL) amplifier. The electronic circuit breaker will turn off the Hot Swap MOSFET with a 200mA current from HGATE to OUT if the voltage across the sense resistor exceeds $\Delta V_{SENSE(CB)}$ (50mV) for longer than the fault filter delay configured at the TMR pin.

Active current limiting begins when the sense voltage exceeds the ACL threshold $\Delta V_{SENSE(ACL)}$ (65mV), which is 1.3× the ECB threshold $\Delta V_{SENSE(CB)}$. The gate of the Hot Swap MOSFET is brought under control by the ACL amplifier and the output current is regulated to maintain the ACL threshold across the sense resistor. At this point, the fault filter starts the timeout with a 100µA current charging the TMR pin capacitor. If the TMR pin voltage exceeds its threshold (1.235V), the external MOSFET turns off with HGATE pulled to ground by 300µA, and its associated $\overline{FAULT}$ pulls low.

After the Hot Swap MOSFET turns off, the TMR pin capacitor is discharged with a 2µA pull-down current until its threshold reaches 0.2V. This is followed by a cool-off period of 14 timing cycles at the TMR pin. For the latch-off part (LTC4225-1), the HGATE pin voltage does not restart at the end of the cool-off period, unless the latched fault is cleared by pulling the ON pin low or toggling the $\overline{EN}$ pin from high to low. For the auto-retry part (LTC4225-2), the latched fault is cleared automatically at the end of the cool-off period, and the HGATE pin restarts charging up to turn on the MOSFET. Figure 4 shows an overcurrent fault on the 12V output.

In the event of a severe short-circuit fault on the 12V output as shown in Figure 5, the output current can surge to tens of amperes. The LTC4225 responds within 1µs to bring the current under control by pulling the HGATE to OUT voltage down to zero volts. Almost immediately, the gate of the Hot Swap MOSFET recovers rapidly due to the R_{HG} and C_{HG} network, and current is actively limited until the electronic circuit breaker times out. Due to parasitic supply lead inductance, an input supply without any bypass capacitor may collapse during the high current surge and then spike upwards when the current is interrupted. Figure 11 shows the input supply transient suppressors consisting of Z1, R_{SNUB1}, C_{SNUB1} and Z2, R_{SNUB2}, C_{SNUB2} for the two supplies if there is no input capacitance.

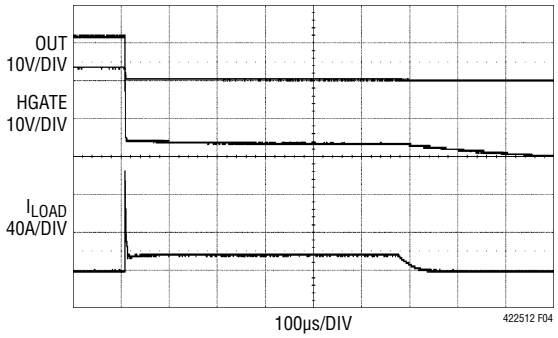


Figure 4. Overcurrent Fault on 12V Output

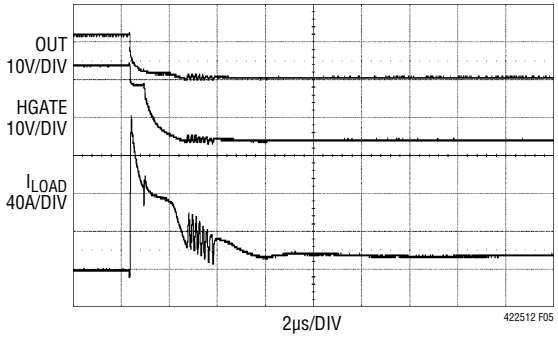


Figure 5. Severe Short-Circuit on 12V Output

APPLICATIONS INFORMATION

Active Current Loop Stability

The active current loop on the HGATE pin is compensated by the parasitic gate capacitance of the external N-channel MOSFET. No further compensation components are normally required. In the case when a MOSFET with $C_{ISS} \leq$ 2nF is chosen, an R_{HG} and C_{HG} compensation network connected at the HGATE pin may be required. The value of C_{HG} is selected based on the inrush current allowed for the output load capacitance. The resistor, R_{HG}, connected in series with C_{HG} accelerates the MOSFET gate recovery for active current limiting after a fast gate pull-down due to an output short. The value of C_{HG} should be ≤100nF and R_{HG} should be between 10Ω and 100Ω for optimum performance.

TMR Pin Functions

An external capacitor, C_T, connected from the TMR pin to GND serves as fault filtering when the supply output is in active current limit. When the voltage across the sense resistor exceeds the circuit breaker trip threshold (50mV), TMR pulls up with 100µA. Otherwise, it pulls down with 2µA. The fault filter times out when the 1.235V TMR threshold is exceeded, causing the corresponding $\overline{FAULT}$ pin to pull low. The fault filter delay or circuit breaker time delay is:

$$t_{CB} = C_T \bullet 12[ms/\mu F]$$

After the circuit breaker timeout, the TMR pin capacitor pulls down with 2µA from the 1.235V TMR threshold until it reaches 0.2V. Then, it completes 14 cooling cycles consisting of the TMR pin capacitor charging to 1.235V with a 100µA current and discharging to 0.2V with a 2µA current. At that point, the HGATE pin voltage is allowed to start up if the fault has been cleared as described in the Resetting Faults section. When the latched fault is cleared during the cool-off period, the corresponding $\overline{FAULT}$ pin pulls high. The total cool-off time for the MOSFET after an overcurrent fault is:

$$t_{COOL} = C_T \bullet 11[s/\mu F]$$

If the latched fault is not cleared after the cool-off period, the cooling cycles continue until the fault is cleared.

After the cool-off period, the HGATE pin is only allowed to pull up if the fault has been cleared for the latch-off part (LTC4225-1). For the auto-retry part (LTC4225-2), the latched fault is cleared automatically following the cool-off period and the HGATE pin voltage is allowed to restart.

Resetting Faults (LTC4225-1)

For the latch-off part (LTC4225-1), an overcurrent fault is latched after tripping the circuit breaker, and the corresponding $\overline{FAULT}$ pin is asserted low. If the LTC4225 controls the MOSFETs on two supplies, only the Hot Swap MOSFET on the supply at fault is turned off and the other is not affected.

To reset a latched fault and restart the output, pull the corresponding ON pin below 0.6V for more than 100µs and then high above 1.235V. The fault latches reset and the $\overline{FAULT}$ pin deasserts on the falling edge of the ON pin. When ON goes high again, a 100ms debounce cycle is initiated before the HGATE pin voltage restarts. Toggling the $\overline{EN}$ pin high and then low again also resets a fault, but the $\overline{FAULT}$ pin pulls high at the end of the 100ms debounce cycle before the HGATE pin voltage starts up. Bringing all the supplies below the $INTV_{CC}$ undervoltage lockout threshold (2.2V) shuts off all the MOSFETs and resets all the fault latches. A 100ms debounce cycle is initiated before a normal start-up when any of the supplies is restored above the $INTV_{CC}$ UVLO threshold.

Auto-Retry after a Fault (LTC4225-2)

For the auto-retry part (LTC4225-2), the latched fault is reset automatically after a cool-off timing cycle as described in the TMR Pin Functions section. At the end of the cool-off period, the fault latch is cleared and $\overline{FAULT}$ pulls high. The HGATE pin voltage is allowed to start up and turn on the Hot Swap MOSFET. If the output short persists, the supply powers up into a short with active current limiting until the circuit breaker times out and $\overline{FAULT}$ again pulls low. A new cool-off cycle begins with TMR ramping down with a 2µA current. The whole process repeats itself until the output short is removed. Since t_{CB} and t_{COOL} are a function of TMR capacitance, C_T, the auto-retry duty cycle is equal to 0.1%, irrespective of C_T.

Figure 6 shows an auto-retry sequence after an overcurrent fault.

APPLICATIONS INFORMATION

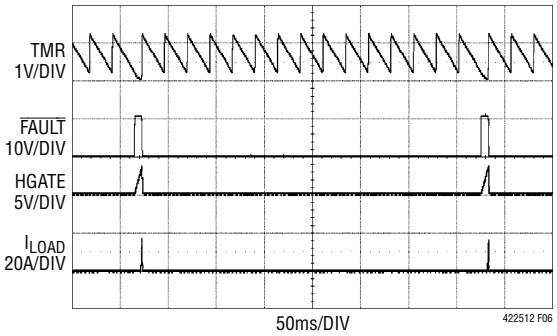


Figure 6. Auto-Retry Sequence After a Fault

Supply Undervoltage Monitor

The ON pin functions as a turn-on control and an input supply monitor. A resistive divider connected between the input supply (IN1, IN2) and GND at the respective ON pin monitors the supply undervoltage condition. The undervoltage threshold is set by proper selection of the resistors and is given by:

$$V_{IN(UVTH)} = \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right) \bullet V_{ON(TH)}$$

where $V_{ON(TH)}$ is the ON rising threshold (1.235V).

An undervoltage fault occurs if the input supply falls below its undervoltage threshold for longer than 20µs. The $\overline{FAULT}$ pin will not be pulled low. If the ON pin voltage falls below 1.155V but remains above 0.6V, the Hot Swap MOSFET is turned off by a 300µA pull-down from HGATE to ground. The Hot Swap MOSFET turns back on instantly without the 100ms debounce cycle when the input supply rises above its undervoltage threshold.

However, if the ON pin voltage drops below 0.6V, it turns off the Hot Swap MOSFET and clears the associated fault latches. The Hot Swap MOSFET turns back on only after a 100ms debounce cycle when the input supply is restored above its undervoltage threshold. An undervoltage fault on one supply does not affect the operation of the other supply. The ideal diode function controlled by the ideal diode MOSFET is unaffected by undervoltage fault conditions.

If both IN supplies fall until the internally generated supply, $INTV_{CC}$, drops below its 2.2V UVLO threshold, all the MOSFETs are turned off and the fault latches are cleared. Operation resumes from a fresh start-up cycle when the input supplies are restored and $INTV_{CC}$ exceeds its UVLO threshold.

There is a 10µs glitch filter on the ON pin to reject supply glitches. By placing a filter capacitor, C_F, with the resistive divider at the ON pin, the glitch filter delay is further extended by the RC time constant to prevent any false fault.

Power Good Monitor

Internal circuitry monitors the MOSFET gate overdrive between the HGATE and OUT pins. The power good status for each supply is reported via its respective open-drain output, $\overline{PWRGD1}$ or $\overline{PWRGD2}$. They are normally pulled high by an external pull-up resistor or the internal 10µA pull-up. The power good output asserts low when the gate overdrive exceeds 4.2V during the HGATE start-up. Once asserted low, the power good status is latched and can only be cleared by pulling the ON pin low, toggling the $\overline{EN}$ pin from low to high, or $INTV_{CC}$ entering undervoltage lockout. The power good output continues to pull low while HGATE is regulating in active current limit, but pulls high when the circuit breaker times out and pulls the HGATE pin low.

CPO and DGATE Start-Up

The CPO and DGATE pin voltages are initially pulled up to a diode below the IN pin when first powered up. CPO starts ramping up 7µs after $INTV_{CC}$ clears its undervoltage lockout level. Another 40µs later, DGATE also starts ramping up with CPO. The CPO ramp rate is determined by the CPO pull-up current into the combined CPO and DGATE pin capacitances. An internal clamp limits the CPO pin voltage to 12V above the IN pin, while the final DGATE pin voltage is determined by the gate drive amplifier. An internal 12V clamp limits the DGATE pin voltage above IN.

APPLICATIONS INFORMATION

MOSFET Selection

The LTC4225 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, BV_{DSS}, and the threshold voltage.

The gate drive for the ideal diode MOSFET and Hot Swap MOSFET is guaranteed to be greater than 5V and 4.8V respectively when the supply voltages at IN1 and IN2 are between 2.9V and 7V. When the supply voltages at IN1 and IN2 are greater than 7V, the gate drive is guaranteed to be greater than 10V. The gate drive is limited to not more than 14V. This allows the use of logic-level threshold N-channel MOSFETs and standard N-channel MOSFETs above 7V. An external Zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 14V.

The maximum allowable drain-source voltage, BV_{DSS}, must be higher than the supply voltages as the full supply voltage can appear across the MOSFET. If an input or output is connected to ground, the full supply voltage will appear across the MOSFET. The $R_{DS(ON)}$ should be small enough to conduct the maximum load current, and also stay within the MOSFET's power rating.

CPO Capacitor Selection

The recommended value of the capacitor, C_{CP}, between the CPO and IN pins is approximately 10× the input capacitance, C_{ISS}, of the ideal diode MOSFET. A larger capacitor takes a correspondingly longer time to charge up by the internal charge pump. A smaller capacitor suffers more voltage drop during a fast gate turn-on event as it shares charge with the MOSFET gate capacitance.

Supply Transient Protection

When the capacitances at the input and output are very small, rapid changes in current during input or output short-circuit events can cause transients that exceed the 24V absolute maximum ratings of the IN and OUT pins. To minimize such spikes, use wider traces or heavier trace plating to reduce the power trace inductance. Also, bypass locally with a 10µF electrolytic and 0.1µF ceramic, or alternatively clamp the input with a transient voltage suppressor (Z1, Z2). A 10Ω, 0.1µF snubber damps the response and eliminates ringing (See Figure 11).

Design Example

As a design example for selecting components, consider a 12V system with a 7.6A maximum load current for the two supplies (see Figure 1).

First, select the appropriate value of the current sense resistors (R_{S1} and R_{S2}) for the 12V supply. Calculate the sense resistor value based on the maximum load current $I_{LOAD(MAX)}$, the minimum circuit breaker trip current $I_{TRIP(MIN)}$ and the lower limit for the circuit breaker threshold $\Delta V_{SENSE(CB)(MIN)}$. A load current margin given as a ratio of $I_{TRIP(MIN)}/I_{LOAD(MAX)}$ is provided for allowing backfeeding current to flow through the sense resistor momentarily, without false tripping the circuit breaker on the higher supply before the reverse turn-off is activated on the lower supply. Assuming a load current margin of 1.5×,

$$I_{TRIP(MIN)} = 1.5 \bullet I_{LOAD(MAX)} = 1.5 \bullet 7.6A = 11.4A$$

$$R_S = \frac{\Delta V_{SENSE(CB)(MIN)}}{I_{TRIP(MIN)}} = \frac{47.5mV}{11.4A} = 4.16m\Omega$$

Choose a 4mΩ sense resistor with a 1% tolerance.

Next, calculate the $R_{DS(ON)}$ of the MOSFET to achieve the desired forward drop at maximum load. Assuming a forward drop, ΔV_{FWD} of 60mV across the two MOSFETs connected back-to-back:

$$R_{DS(ON,TOTAL)} \leq \frac{\Delta V_{FWD}}{I_{LOAD(MAX)}} = \frac{60mV}{7.6A} = 7.9m\Omega$$

The Si7336ADP offers a good choice with a maximum $R_{DS(ON)}$ of 3mΩ at V_{GS} = 10V, thereby giving a total of 6mΩ for two MOSFETs in the supply path. The input capacitance, C_{ISS}, of the Si7336ADP is about 5600pF. Slightly exceeding the 10× recommendation, a 0.1µF capacitor is selected for C_{CP1} and C_{CP2} at the CPO pins.

APPLICATIONS INFORMATION

Next, verify that the thermal ratings of the selected MOSFET, Si7336ADP, are not exceeded during power-up or an output short.

Assuming the MOSFET dissipates power due to inrush current charging the load capacitor, C_L, at power-up, the energy dissipated in the MOSFET is the same as the energy stored in the load capacitor, and is given by:

$$E_{CL} = \frac{1}{2} \bullet C_L \bullet V_{IN}^2$$

For C_L = 1600µF, the time it takes to charge up C_L is calculated as:

$$t_{CHARGE} = \frac{C_L \bullet V_{IN}}{I_{INRUSH}} = \frac{1600\mu F \bullet 12V}{1A} = 19ms$$

The inrush current is set to 1A by adding capacitance, C_{HG}, at the gate of the Hot Swap MOSFET.

$$C_{HG} = \frac{C_L \bullet I_{HGATE(UP)}}{I_{INRUSH}} = \frac{1600\mu F \bullet 10\mu A}{1A} = 16nF$$

Choose a practical value of 15nF for C_{HG}.

The average power dissipated in the MOSFET is calculated as:

$$P_{AVG} = \frac{E_{CL}}{t_{CHARGE}} = \frac{1}{2} \bullet \frac{1600\mu F \bullet (12V)^2}{19ms} = 6W$$

The MOSFET selected must be able to tolerate 6W for 19ms during power-up. The SOA curves of the Si7336ADP provide for 1.5A at 30V (45W) for 100ms. This is sufficient to satisfy the requirement. The increase in junction temperature due to the power dissipated in the MOSFET is $\Delta T = P_{AVG} \bullet Zth_{JC}$ where Zth_{JC} is the junction-to-case thermal impedance. Under this condition, the Si7336ADP data sheet indicates that the junction temperature will increase by 4.8°C using Zth_{JC} = 0.8°C/W (single pulse).

The duration and magnitude of the power pulse during an output short is a function of the TMR capacitance, C_T, and the LTC4225's active current limit. The short-circuit duration is given as $C_T \bullet 12[ms/\mu F] = 0.56ms$ for C_T = 0.047µF.

The maximum short-circuit current is calculated using the maximum active current limit threshold $\Delta V_{SENSE(ACL)(MAX)}$ and minimum R_S value.

$$I_{SHORT(MAX)} = \frac{\Delta V_{SENSE(ACL)(MAX)}}{R_{S(MIN)}} = \frac{75mV}{3.96m\Omega} = 18.9A$$

So, the maximum power dissipated in the MOSFET is 18.9A • 12V = 227W for 0.56ms. The Si7336ADP data sheet indicates that the worst-case increase in junction temperature during this short-circuit condition is 22.7°C using Zth_{JC} = 0.1°C/W (single pulse). Choosing C_T = 0.047µF will not cause the maximum junction temperature of the MOSFET to be exceeded. The SOA curves of the Si7336ADP provide for 15A at 30V (450W) for 1ms. This also satisfies the requirement.

Next, select the resistive divider at the ON1 and ON2 pins to provide an undervoltage threshold of 9.6V for the 12V supply. First, choose the bottom resistors, R1 and R3, to be 20k. Then, calculate the top resistor value for R2 and R4:

$$R_{TOP} = \left(\frac{V_{IN(UVTH)}}{V_{ON(TH)}} - 1 \right) \bullet R_{BOTTOM}$$

$$R_{TOP} = \left(\frac{9.6V}{1.235V} - 1 \right) \bullet 20k = 135k$$

Choose the nearest 1% resistor value of 137k for R2 and R4. In addition, there is a 0.1µF bypass (C1) at the $INTV_{CC}$ pin and a 10nF filter capacitor (C_F) at the ON pin to prevent the supply glitches from turning off the Hot Swap MOSFET.

PCB Layout Considerations

For proper operation of the LTC4225's circuit breaker, Kelvin connection to the sense resistor is strongly recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor and the power MOSFET should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout is illustrated in Figure 7.

APPLICATIONS INFORMATION

Connect the IN and OUT pin traces as close as possible to the MOSFETs' terminals. Keep the traces to the MOSFETs wide and short to minimize resistive losses. The PCB traces associated with the power path through the MOSFETs should have low resistance. The suggested trace width for 1oz copper foil is 0.03" for each ampere of DC current to keep PCB trace resistance, voltage drop and temperature rise to a minimum. Note that the sheet resistance of 1oz copper foil is approximately 0.5mΩ/square, and voltage drops due to trace resistance add up quickly in high current applications.

It is also important to place the bypass capacitor, C1, for the $INTV_{CC}$ pin, as close as possible between $INTV_{CC}$ and GND. Also place C_{CP1} near the CPO1 and IN1 pins, and C_{CP2} near the CPO2 and IN2 pins. The transient voltage suppressors, Z1 and Z2, when used, should be mounted close to the LTC4225 using short lead lengths.

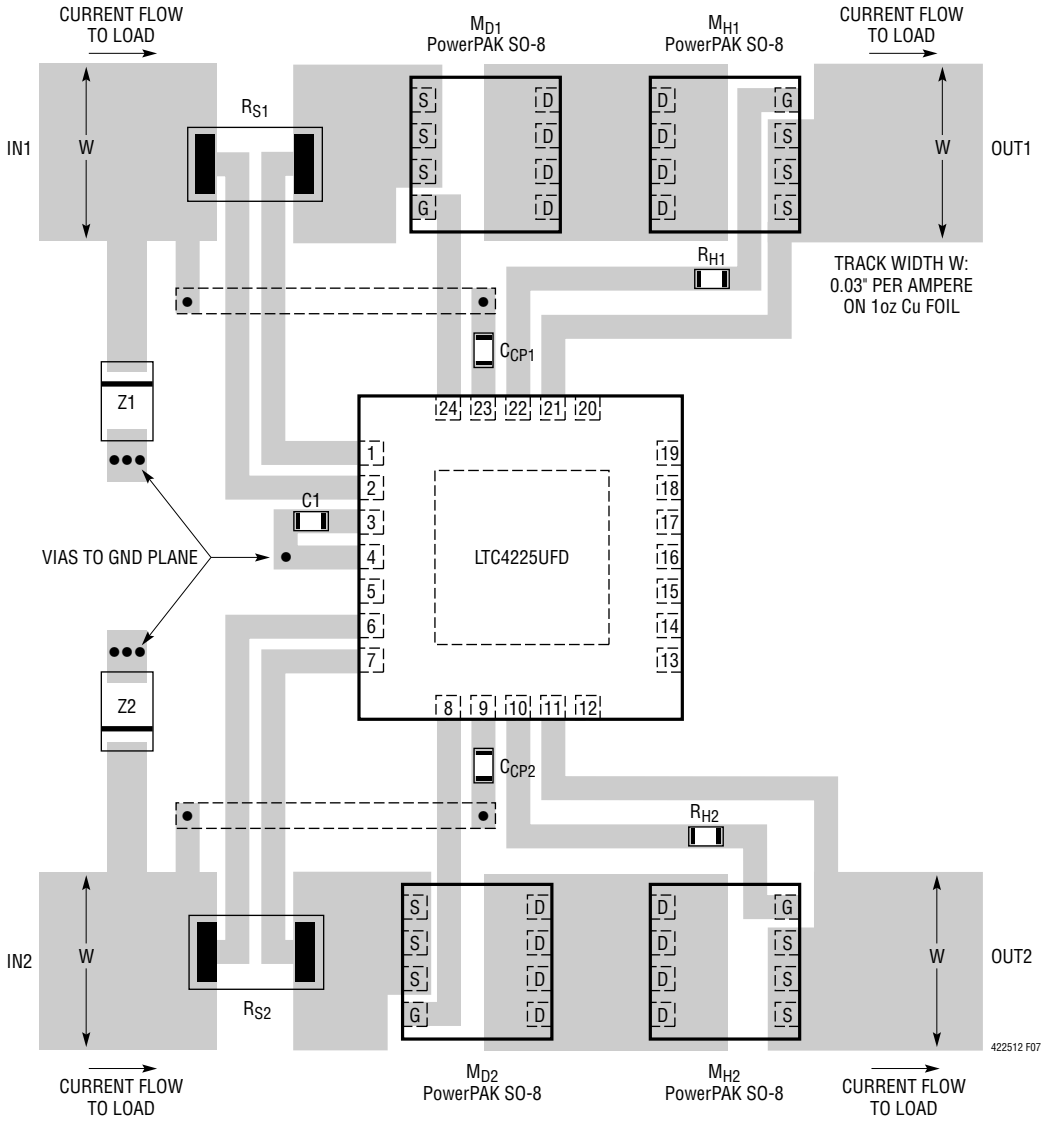


Figure 7. Recommended PCB Layout for Power MOSFETs and Sense Resistors

APPLICATIONS INFORMATION

Power Prioritizer

Figure 8 shows an application where either of two supplies is passed to the output on the basis of priority, rather than simply allowing the highest voltage to prevail. The 5V primary supply (INPUT 1) is passed to the output whenever it is available; power is drawn from the 12V backup supply (INPUT 2) only when the primary supply is unavailable. As long as INPUT 1 is above the 4.3V UV threshold set by the R1-R2 divider at the ON1 pin, M_{H1} is turned on connecting INPUT 1 to the output. When M_{H1} is on, $\overline{PWRGD1}$ goes low, which in turn pulls ON2 low and disables the IN2 path by turning M_{H2} off. If the primary supply fails and INPUT 1 drops below 4.3V, ON1 turns off M_{H1} and $\overline{PWRGD1}$ goes high, allowing ON2 to turn on M_{H2} and connect the INPUT 2 to the output. Diode D1 ensures that ON2 remains above 0.6V while in the off state so that when ON2 goes high, M_{H2} is turned on immediately without invoking the 100ms turn-on delay. When INPUT 1 returns to a viable voltage, M_{H1} turns on and M_{H2} turns off. The ideal diode MOSFETs M_{D1} and M_{D2} prevent backfeeding of one input to the other under any condition.

Additional Applications

In most applications, the back-to-back MOSFETs are configured with the MOSFET on the supply side as the ideal diode and the MOSFET on the load side as the Hot Swap control. But for some applications, the arrangement of the MOSFETs for the ideal diode and the Hot Swap control may reversed as shown in Figure 9. The Hot Swap MOSFET is placed on the supply side and the ideal diode MOSFET on the load side with the source terminals connected together. If this configuration is operated with 12V supplies, the gate-to-source breakdown voltage of the MOSFETs can be exceeded when the input or output is connected to ground as the LTC4225's internal 12V clamps only limit the DGATE-to-IN and HGATE-to-OUT pin voltages. Choose a MOSFET whose gate-to-source breakdown voltage is rated for 25V or more as 24V voltage can appear across the GATE and SOURCE pins of the MOSFET during an input or output short. As shown in Figure 9, if a MOSFET with a lower rated gate-to-source breakdown voltage is chosen, an external Zener diode clamp is required between the GATE and SOURCE pins of the MOSFET to prevent it from breaking down.

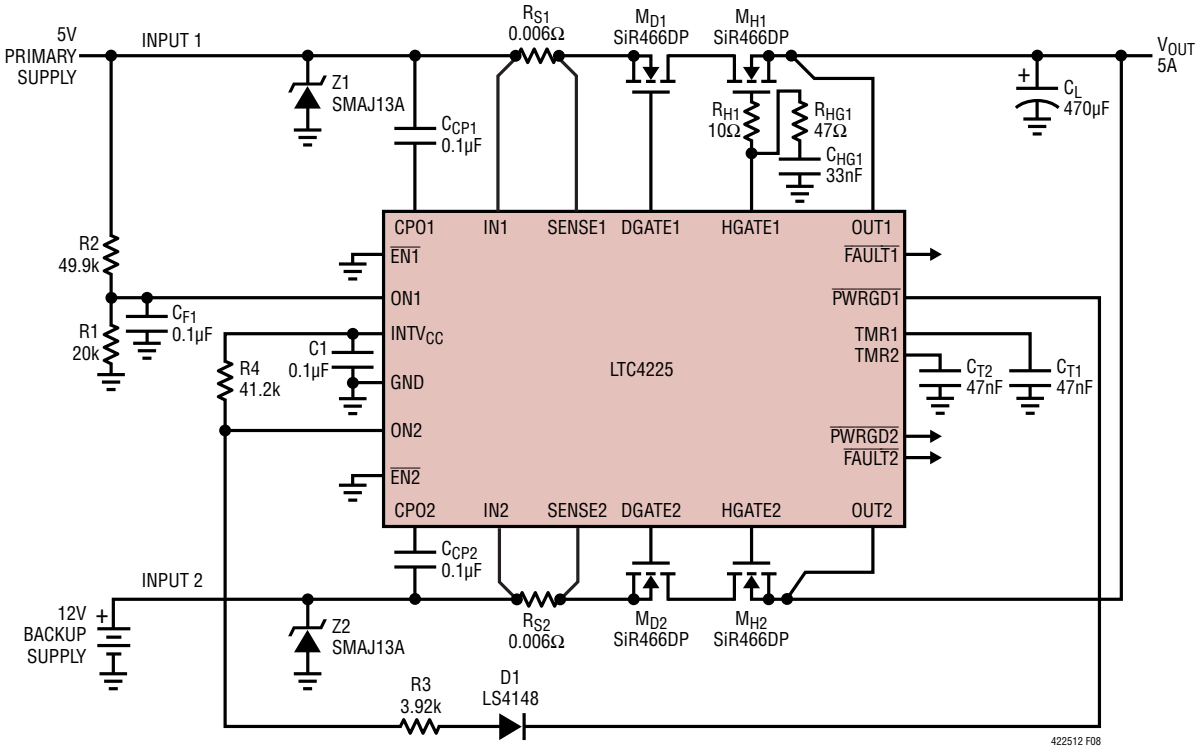


Figure 8. 2-Channel Power Prioritizer

APPLICATIONS INFORMATION

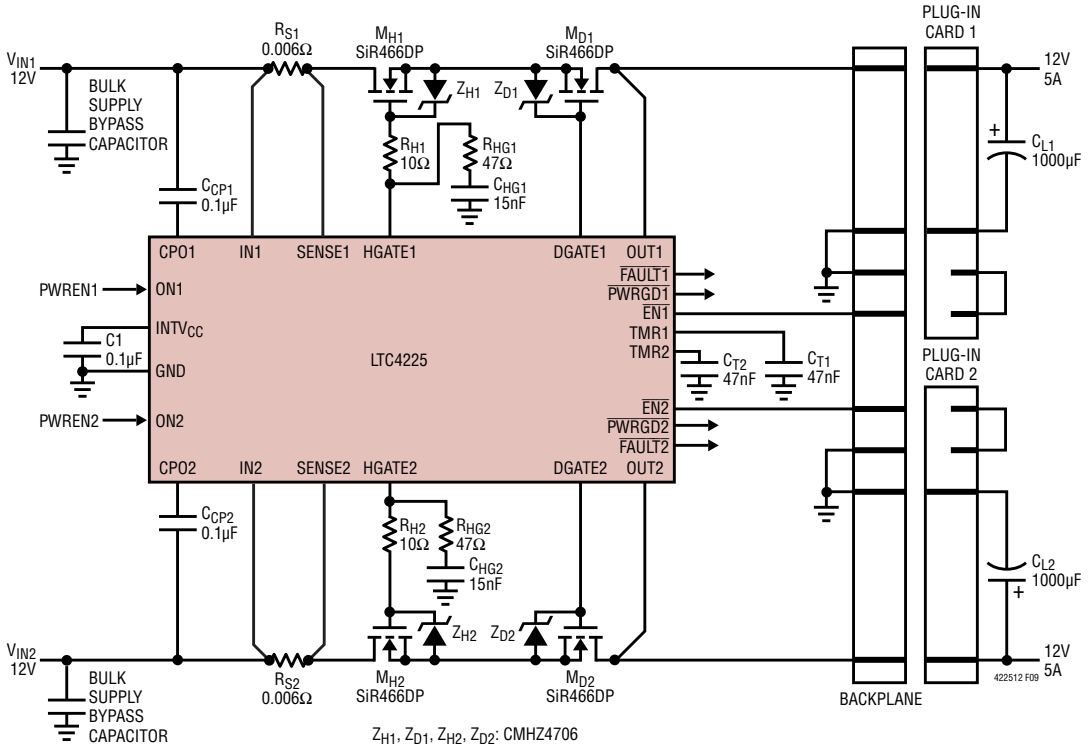


Figure 9. An Application with the Hot Swap MOSFET on the Supply Side and the Ideal Diode MOSFET on the Load Side

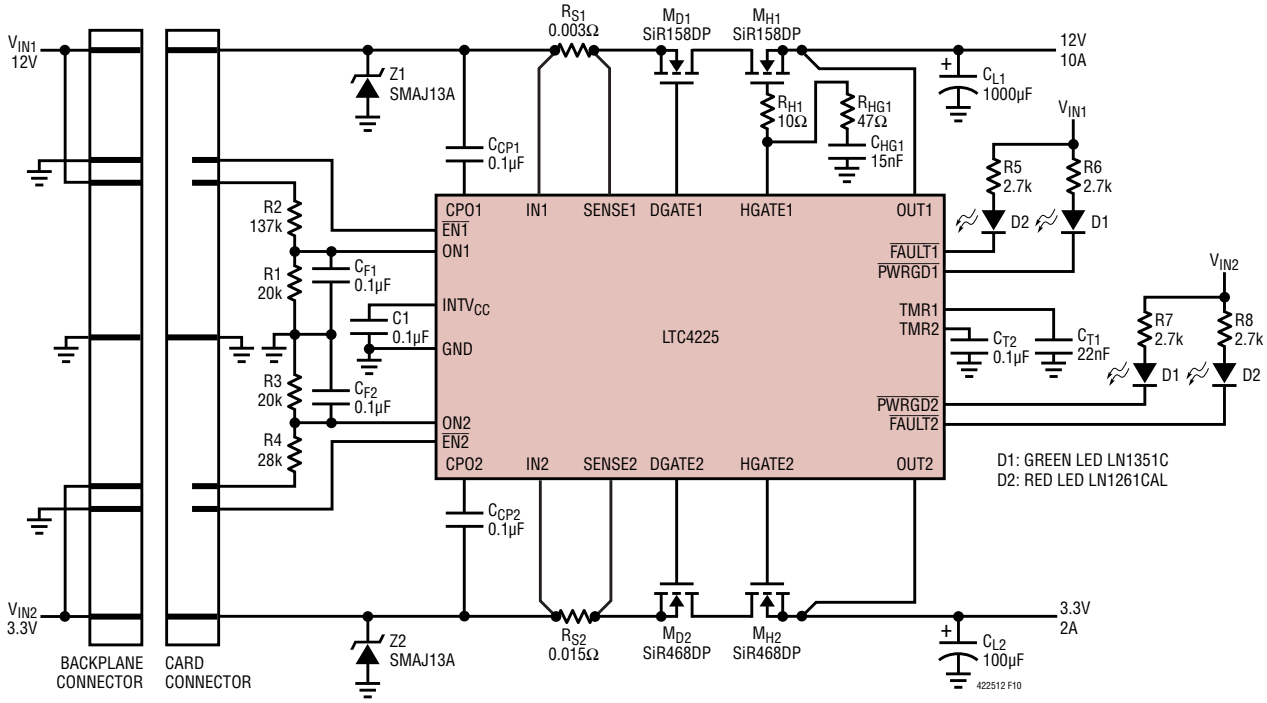


Figure 10. Plug-In Card Supply Holdup Using Ideal Diode at 12V and 3.3V Input Supplies

APPLICATIONS INFORMATION

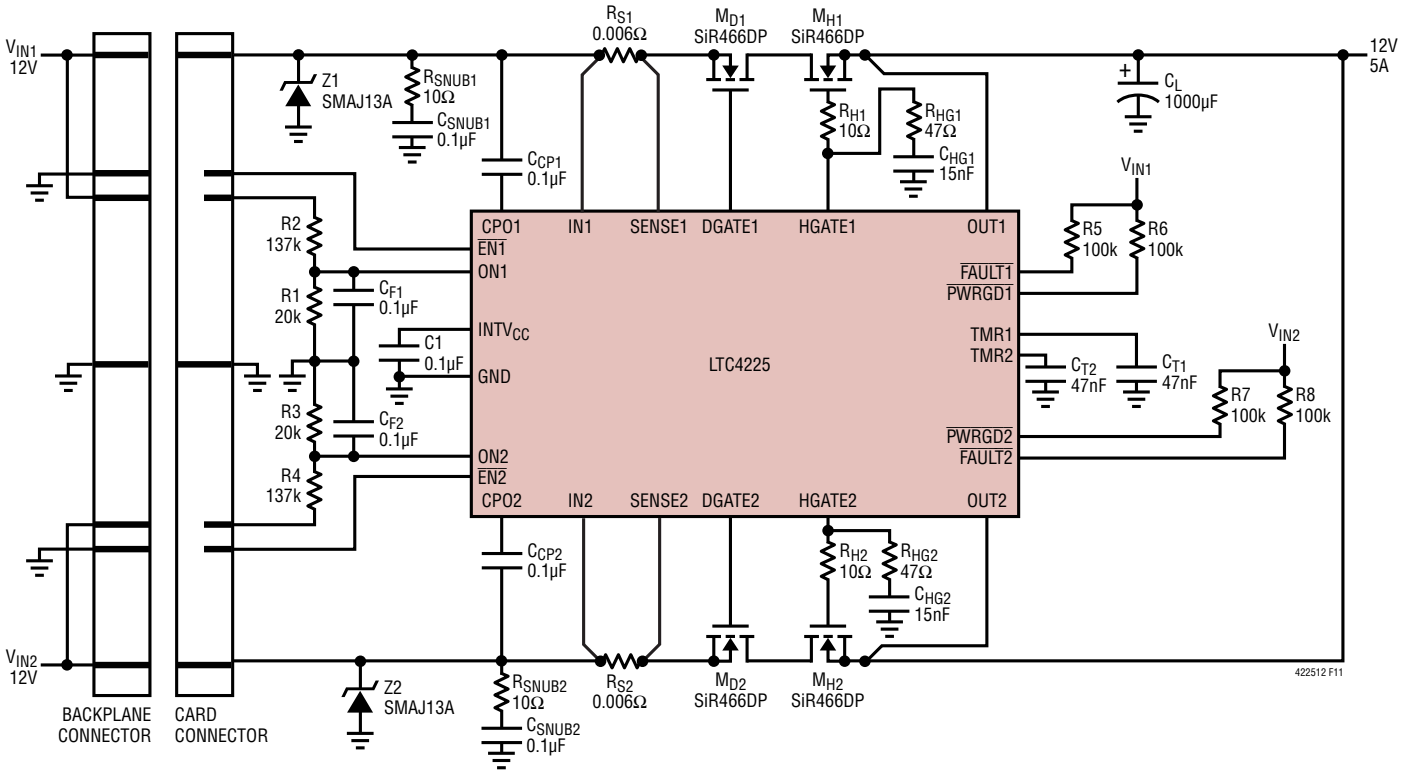


Figure 11. Card Resident Application with the Output Diode-ORed

APPLICATIONS INFORMATION

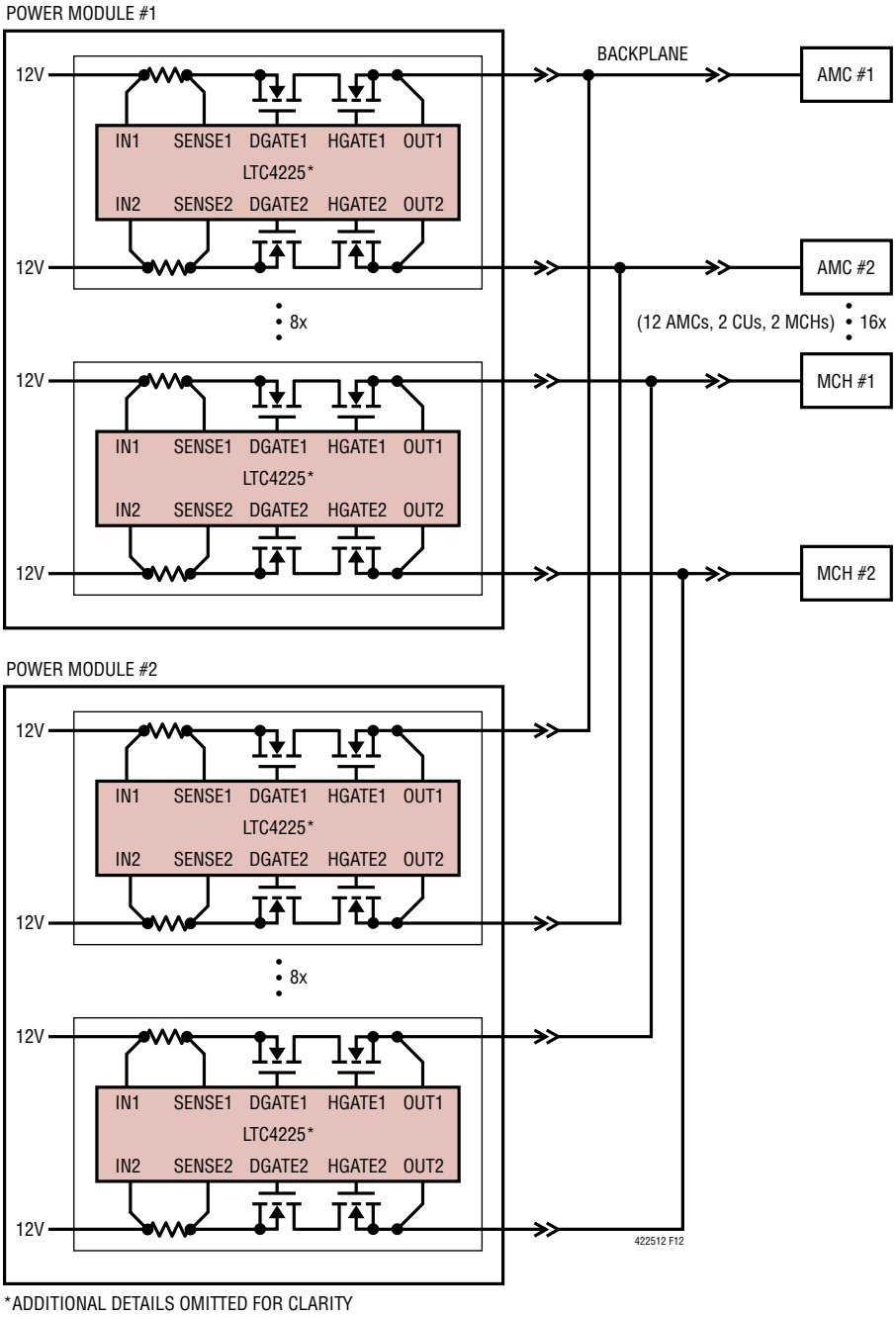
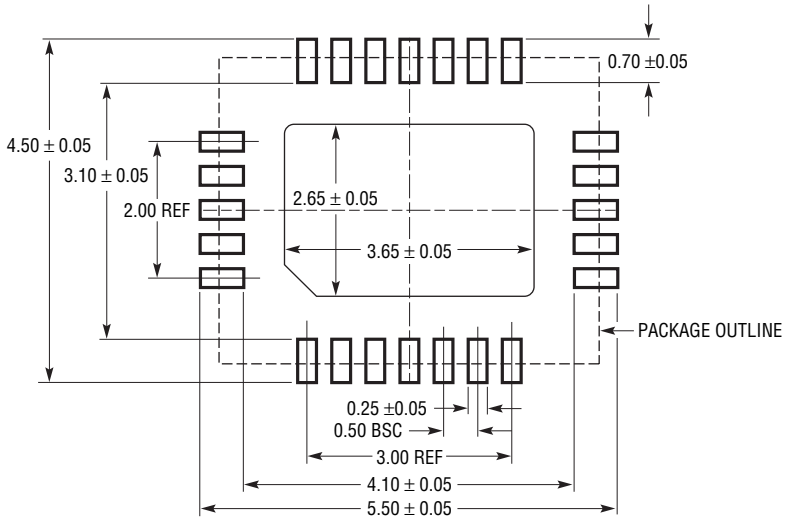


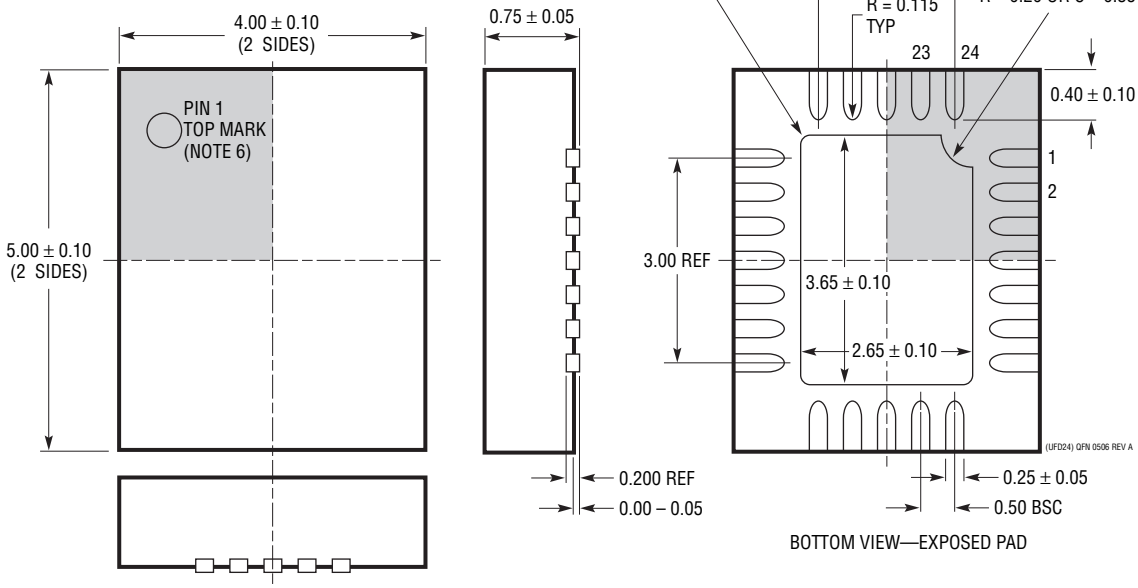
Figure 12. 12V Distribution in µTCA Redundant Power Subsystem

PACKAGE DESCRIPTION

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

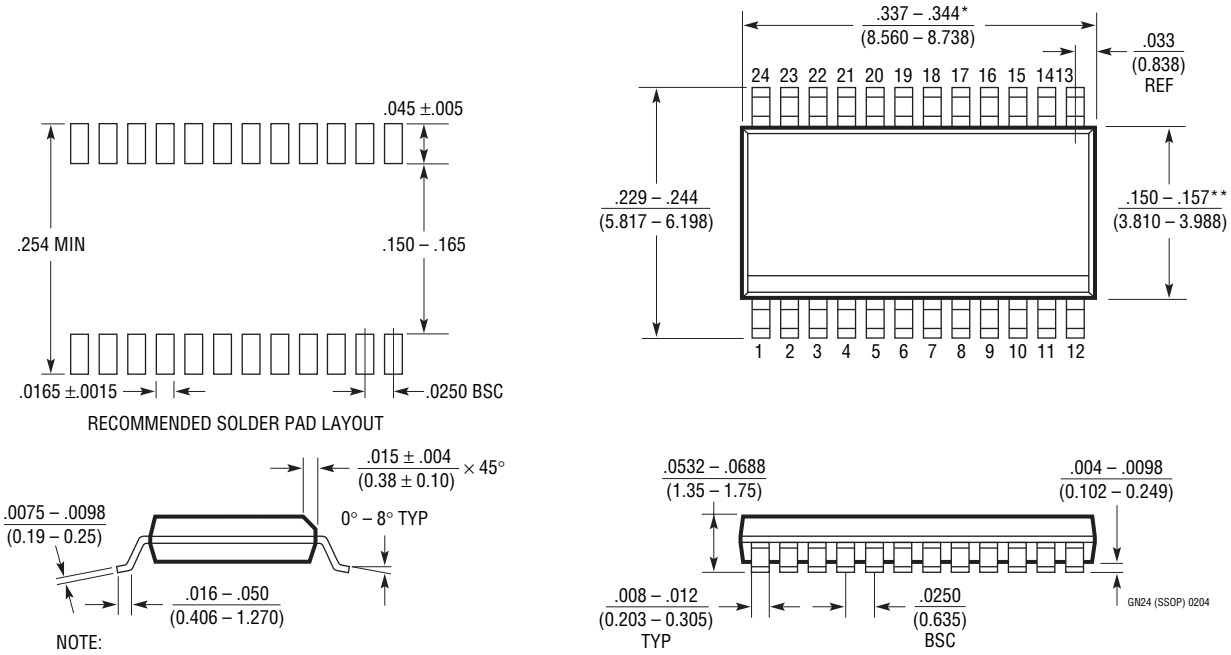


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE