Wide Operating Range Dual Hot Swap Controller

FEATURES

- **Allows Safe Board Insertion into Live Backplane**
- **Selectable Current Limit and Dual-Rate Timer Accommodate Load Surges**
- **Fast Response Limits Peak Fault Current**
- **Wide Operating Voltage Range: 4.5V to 44V**
- Optional Auto-Retry or Latchoff after Overcurrent Fault
- High Side Drive for External N-Channel MOSFET
- Allows Parallel Power Paths for High Current Applications
- Available in 16-Pin QFN (3mm × 3mm) and MSOP Packages

APPLICATIONS

- Apple FireWire/IEEE 1394
- Disk Drives
- Rugged 12V, 24V Applications
- Hot Board/Connector Insertion
- Uni/Bidirectional Current Limiter/Circuit Breaker

DESCRIPTION

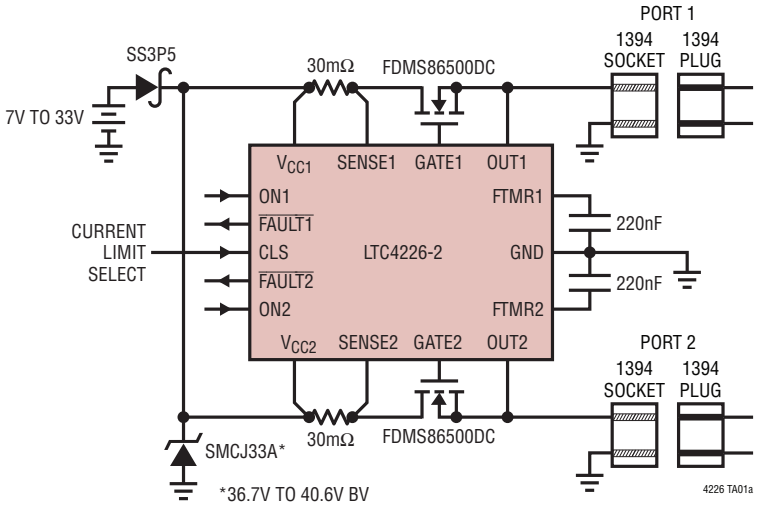
The LTC®4226 dual Hot Swap™ controller allows two power paths to be safely inserted and removed from a live backplane or powered connector. Using N-channel pass transistors, supply voltages ranging from 4.5V to 44V are ramped up at an adjustable rate.

Three selectable ratios of current limit to circuit breaker threshold accommodate noisy loads and momentary high peak currents without interruption, while a dual-rate fault timer protects the MOSFET from extended output overcurrent events. $\overline{\text{FAULT}}$ outputs indicate the circuit breaker status. The LTC4226-1 remains off after a fault while the LTC4226-2 automatically retries after a 0.5s delay.

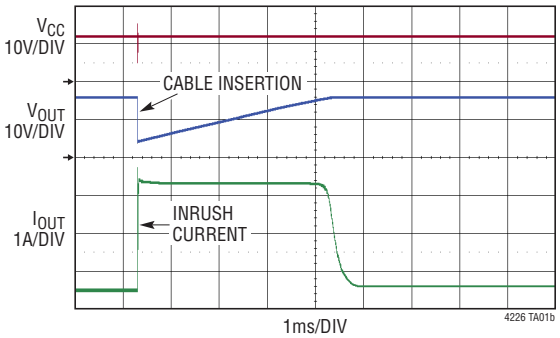
The LTC4226 can also be configured as a bidirectional current limiter/circuit breaker. For high current applications, two channels may be configured as parallel power paths.

TYPICAL APPLICATION

2 Port FireWire Application



Inrush after Load Connection



VCC = 12V
CLOAD = 1mF

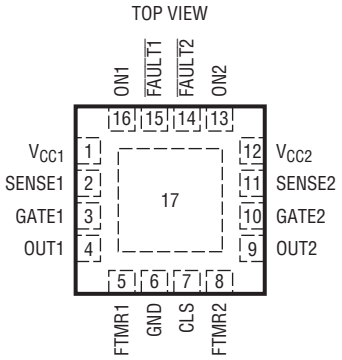
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

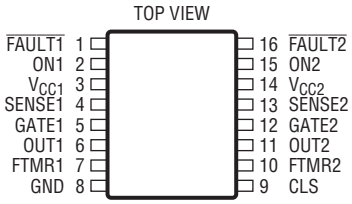
V_{CCn} ..... –0.3V to 55V
SENSEn, ONn, $\overline{FAULTn}$, CLS ..... –0.3V to 55V
GATEn (Note 3) ..... –0.3V to 68V
OUTn (Note 3) ..... –0.3V to 55V
GATEn – OUTn (Note 3) ..... –0.3V to 18V
FTMRn ..... –0.3V to 4V

Operating Ambient Temperature Range
LTC4226C ..... 0°C to 70°C
LTC4226I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
MSOP Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN 17), PCB GND CONNECTION OPTIONAL



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4226CUD-1#PBF	LTC4226CUD-1#TRPBF	LFRC	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC4226CUD-2#PBF	LTC4226CUD-2#TRPBF	LFRD	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC4226IUD-1#PBF	LTC4226IUD-1#TRPBF	LFRC	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC4226IUD-2#PBF	LTC4226IUD-2#TRPBF	LFRD	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC4226CMS-1#PBF	LTC4226CMS-1#TRPBF	42261	16-Lead Plastic MSOP	0°C to 70°C
LTC4226CMS-2#PBF	LTC4226CMS-2#TRPBF	42262	16-Lead Plastic MSOP	0°C to 70°C
LTC4226IMS-1#PBF	LTC4226IMS-1#TRPBF	42261	16-Lead Plastic MSOP	–40°C to 85°C
LTC4226IMS-2#PBF	LTC4226IMS-2#TRPBF	42262	16-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 12V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CCn}	Input Supply Range		●	4.5		44	V
I_{CCn}	Input Supply Current	V_{CC} = 12V	●		0.7	2	mA
$V_{CCn(UVL)}$	Input Supply Undervoltage Lockout	V_{CC} Rising	●	3	3.7	4.5	V
$\Delta V_{CCn(HYST)}$	Input Supply Undervoltage Lockout Hysteresis				200		mV
Circuit Breaker and Current Limit							
V_{CB}	Circuit Breaker Threshold	(V_{CC} – SENSE)	●	45	50	55	mV
	Channel-to-Channel V_{CB} Mismatch		●			±6	%
V_{LIMIT}	Current Limit Voltage	(V_{CC} – SENSE), CLS = 0V (V_{CC} – SENSE), CLS = Open (V_{CC} – SENSE), CLS = 3V	● ● ●	70 93 139	86 115 173	103 136 205	mV mV mV
	Channel-to-Channel V_{LIMIT} Mismatch		●			±6	%
I_{SENSE}	Sense Pin Input Current	(V_{CC} – SENSE = 0V)	●		40	200	µA
Gate Drive							
ΔV_{GATE}	External N-Channel Gate Drive (GATE – OUT)	I_{GATE} = 0µA, –1µA; V_{CC} > 6V I_{GATE} = 0µA, –1µA; V_{CC} < 6V	● ●	10 8	12 12	16 16	V V
$I_{GATE(UP)}$	Gate Pull-Up Current	GATE = OUT = 1V	●	–5	–9	–13	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	GATE = 12V, OUT = 0V, ON = 0V GATE = OUT = V_{CC} = 12V, ON = 0V or $\overline{FAULT}$ = 0V GATE = 5V, OUT = 0V, ON = 3V, Severe Fault	● ● ●	1 50 100	3 150 200	5 300 1000	mA µA mA
Comparator Inputs							
V_{ON}	ON Pin Threshold Voltage	V_{ON} Rising	●	1.17	1.24	1.3	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis Voltage				50		mV
I_{ON}	ON Pin Input Current	V_{ON} = 1.2V	●		0	±1	µA
Fault Timer							
$I_{FTMR(CB)}$	FTMR Pin Pull-Up Current (Circuit Breaker)	V_{FTMR} = 0V, Circuit Breaker Fault	●	–1.4	–2	–2.6	µA
$I_{FTMR(CL)}$	FTMR Pin Pull-Up Current (Current Limit)	V_{FTMR} = 0V, Current Limit Engaged, CLS = 0V V_{FTMR} = 0V, Current Limit Engaged, CLS = Open V_{FTMR} = 0V, Current Limit Engaged, CLS = 3V	● ● ●	–14 –25 –56	–20 –36 –80	–26 –46 –104	µA µA µA
$I_{FTMR(DEF)}$	FTMR Pin Pull-Down Current (Default)	V_{FTMR} = 1V, Default	●	1.4	2	2.6	µA
$I_{FTMR(RST)}$	FTMR Pin Pull-Down Current (Reset)	V_{FTMR} = 1V, Reset	●	70	100	130	µA
$V_{FTMR(H)}$	FTMR Pin Threshold Voltage (Trip)		●	1.17	1.23	1.3	V
$V_{FTMR(L)}$	FTMR Pin Threshold Voltage (Reset)		●		0.1	0.2	V
Fault I/O							
$V_{(OL)}$	$\overline{FAULT}$ Pin Low Output Voltage	Circuit Breaker Fault, $I_{\overline{FAULT}}$ = 2mA	●		0.2	0.4	V
$I_{(OL)}$	$\overline{FAULT}$ Pin Low Output Pull-Down Current	Circuit Breaker Fault, $V_{\overline{FAULT}}$ = 5V, V_{CC} = 12V	●	2	5	10	mA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Pin Input Threshold Voltage	No Internal Fault, External Input	●	0.3	0.5	0.8	V
$I_{(OH)}$	$\overline{FAULT}$ Pin Pull-Up Current	No Internal Fault, $V_{\overline{FAULT}}$ = 2V	●	–5	–10	–20	µA
$V_{(OH)}$	$\overline{FAULT}$ Pin High Output Voltage	No Internal Fault, $I_{\overline{FAULT}}$ = 0µA, V_{CC} = 12V	●	2	3.8	5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 12V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Three-State Input							
$V_{CLS(L)}$	CLS Pin Low Threshold Voltage		●			0.4	V
$V_{CLS(H)}$	CLS Pin High Threshold Voltage		●	2			V
$V_{CLS(Z)}$	CLS Pin Voltage in Open State				1.38		V
$I_{CLS(Z)}$	Allowable CLS Pin Leakage in Open State		●			±2	µA
$I_{CLS(L)}$	CLS Pin Low Input Current		●	–2	–4	–8	µA
$I_{CLS(H)}$	CLS Pin High Input Current		●	2	4	8	µA
Timing Delay							
$t_{OFF(SENSE)}$	Severe Overcurrent Fault to GATE Low	C_{GATE} = 1nF, (V_{CC} – SENSE = 4V)	●		0.1	1	µs
$t_{OFF(\overline{FAULT})}$	$\overline{FAULT}$ Input Low to GATE Low	C_{GATE} = 1nF	●	3	6	30	µs
$t_{OFF(FMTR)}$	FTMR High to GATE Low	C_{GATE} = 1nF	●	3	7	30	µs
$t_{OFF(ON)}$	ON Low to GATE Low	C_{GATE} = 1nF	●		25	60	µs
$t_{OFF(UVLO)}$	V_{CC} Enters Undervoltage to GATE Low	C_{GATE} = 1nF	●		25	60	µs
$t_{ON(ON)}$	ON High to GATE High	V_{CC} Above Undervoltage	●	5	10	20	ms
	Channel-to-Channel $t_{ON(ON)}$ Mismatch		●			±10	%
$t_{ON(UVL)}$	V_{CC} Exits Undervoltage to GATE High	ON High	●	25	50	100	ms
	Channel-to-Channel $t_{ON(UVL)}$ Mismatch		●			±10	%
$t_{D(COOL)}$	Auto-Retry Delay	LTC4226-2 Only	●	0.25	0.5	1	s

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

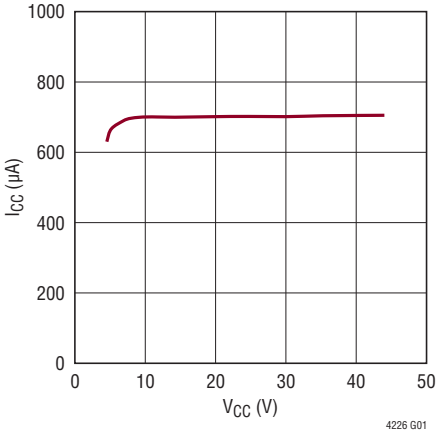
Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3: Limits on maximum rating is defined as whichever limit occurs first. Internal clamps limit the GATE pin to a minimum of 12V above OUT, a diode voltage drop below OUT, or a diode voltage drop below GND. Driving the GATE to OUT pin voltage beyond the clamp may damage the device.

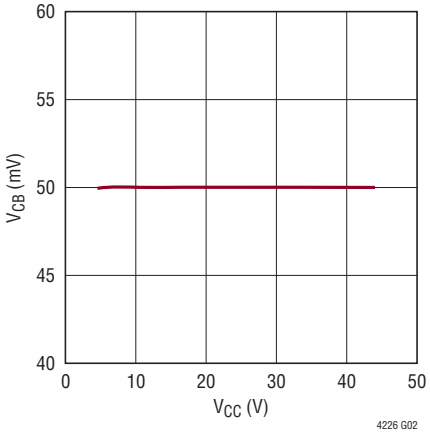
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 12V, unless otherwise noted.

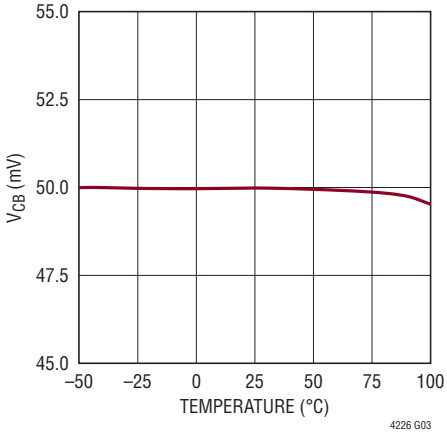
Supply Current vs Supply Voltage



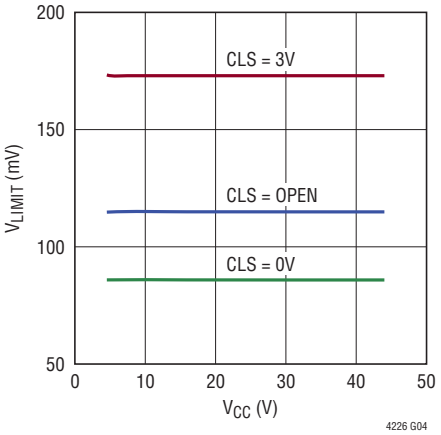
Circuit Breaker Voltage vs Supply Voltage



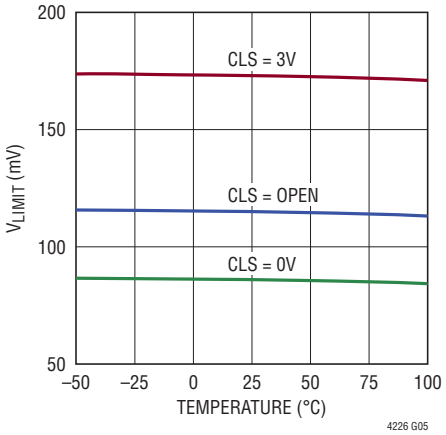
Circuit Breaker Voltage vs Temperature



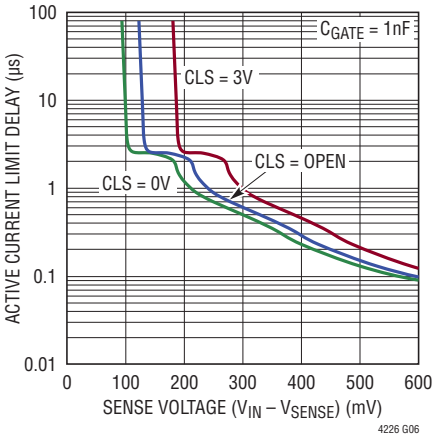
Current Limit Voltage vs Supply Voltage



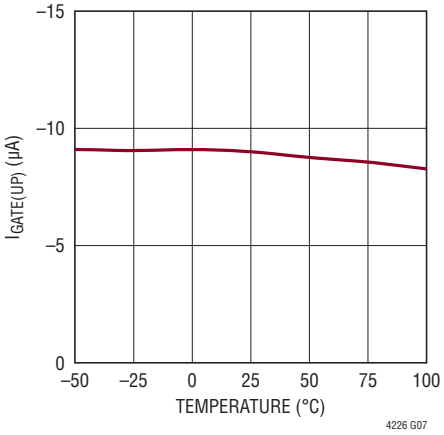
Current Limit Voltage vs Temperature



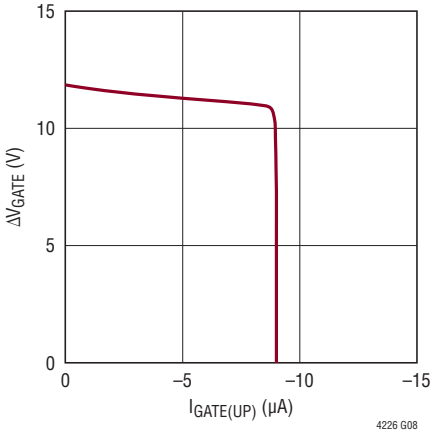
Active Current Limit Delay vs Sense Voltage



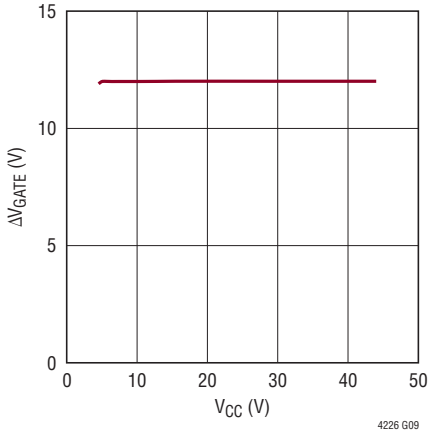
Gate Pull-Up Current vs Temperature



Gate Voltage vs Gate Pull-Up Current



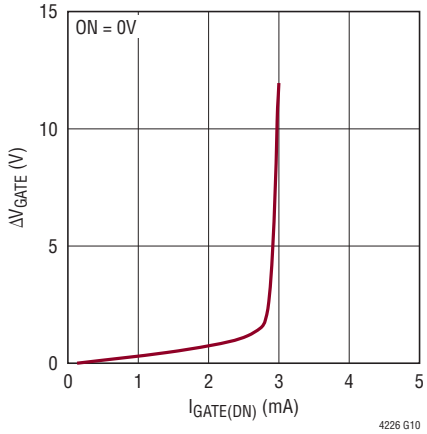
Gate Voltage vs Supply Voltage



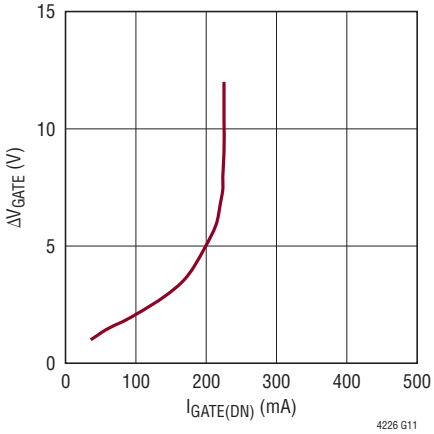
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 12V, unless otherwise noted.

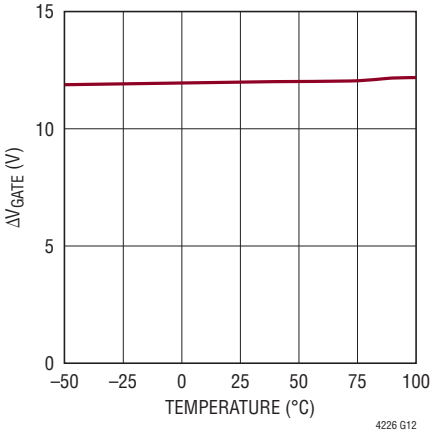
Gate Voltage vs Gate Pull-Down Current



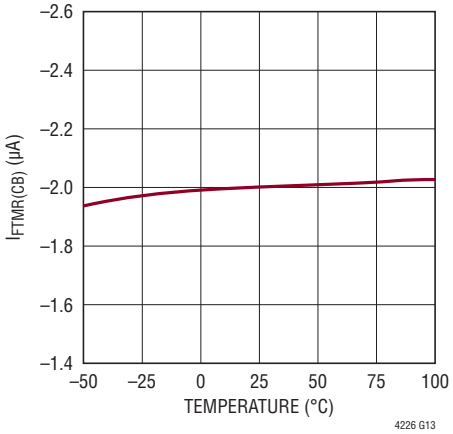
Gate Voltage vs Severe Fault Gate Pull-Down Current



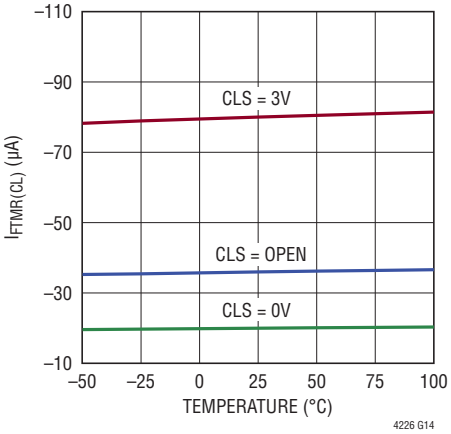
Gate Voltage vs Temperature



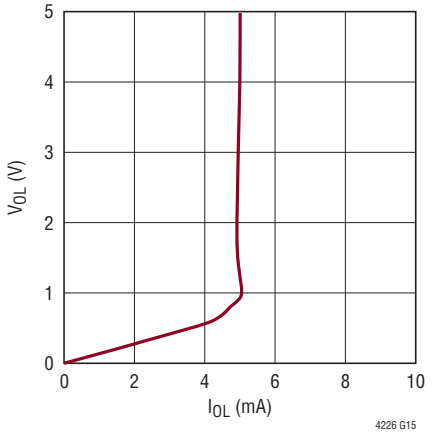
Circuit Breaker Timer Current vs Temperature



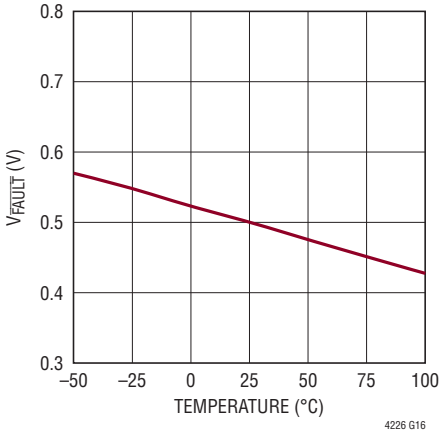
Current Limit Timer Current vs Temperature



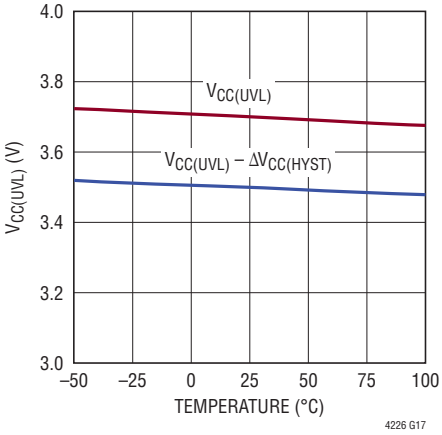
Fault Output Low Voltage vs Current



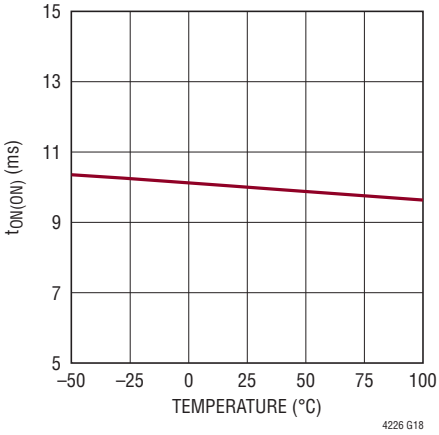
Fault Input Threshold Voltage vs Temperature



Supply Undervoltage Lockout vs Temperature



ON Turn-On Time vs Temperature



PIN FUNCTIONS

CLS: Three-State Current Limit Select Input. Tying this pin low enables 1.5× current limit; opening this pin enables 2× current limit and tying this pin high (above 2V) enables 3× current limit. A higher current limit selection permits larger current transients to pass without invoking current limiting. The CLS pin permits dynamic current limit selection. The three input states configure the preset current limit voltage V_{LIMIT} to approximately 1.5×, 2× or 3× of 1.15 • V_{CB}.

Exposed Pad: The exposed pad may be left open or connected to device ground.

$\overline{\text{FAULT1}}$, $\overline{\text{FAULT2}}$: $\overline{\text{FAULT}}$ Input/Output Status. When the FTMR pin has reached the $V_{FTMR(H)}$ threshold, the fault status is set active and the $\overline{\text{FAULT}}$ pin output pulls low. When fault is inactive, a 10µA current source pulls this pin up to a diode below its internal supply voltage. Pulling the $\overline{\text{FAULT}}$ pin low turns off the external MOSFET without affecting the FTMR pin status. The $\overline{\text{FAULT}}$ pin is not latched.

FTMR1, FTMR2: Fault Timer. A capacitor sets the dual-rate fault timer durations: circuit breaker CB timeout and current limit CL timeout. The FTMR pin pulls up with $I_{FTMR(CB)}$ when the sense resistor voltage is between V_{CB} and V_{LIMIT}. The FTMR pin pulls up with $I_{FTMR(CL)}$ when the sense resistor voltage is at or above V_{LIMIT}. FTMR pulls low with $I_{FTMR(DEF)}$ when the sense resistor voltage falls below V_{CB}. When the FTMR voltage reaches the $V_{FTMR(H)}$ threshold, the fault status is activated. To reset FTMR, the ON pin can be pulled low or the corresponding supply voltage can be pulled below the undervoltage lockout threshold. The capacitor on the FTMR pin is pulled to GND with $I_{FTMR(RST)}$ to clear the fault status. For the LTC4226-1 latchoff option, the MOSFET remains off until faults are cleared by cycling the ON pin or by an undervoltage condition on the corresponding supply. For the LTC4226-2 auto-retry option, after a $t_{D(COOL)}$ delay, FTMR is reset, the fault status is cleared, and the GATE begins to ramp up. The LTC4226-2 can be forced to restart by cycling the ON pin or by an undervoltage condition on the corresponding supply.

GATE1, GATE2: Gate Drive for External MOSFET. The gate driver controls the external N-channel MOSFET switch by applying a voltage across the GATE and OUT pins which connect to the MOSFET gate and source pins. A charge pump sources 9µA at the GATE pin to turn on the external MOSFET. When the MOSFET is on, the GATE pin voltage is clamped at ΔV_{GATE} above the OUT pin. During turn-off, the GATE pin is discharged by a 3mA pull-down with about 2.85mA of current flowing to the OUT pin. In a severe fault, the GATE pin is discharged to the OUT pin with a minimum of 100mA. When the MOSFET is off, the GATE pin is pulled towards ground with 150µA and a voltage clamps limits the GATE voltage to a diode drop below the OUT pin.

GND: Device ground

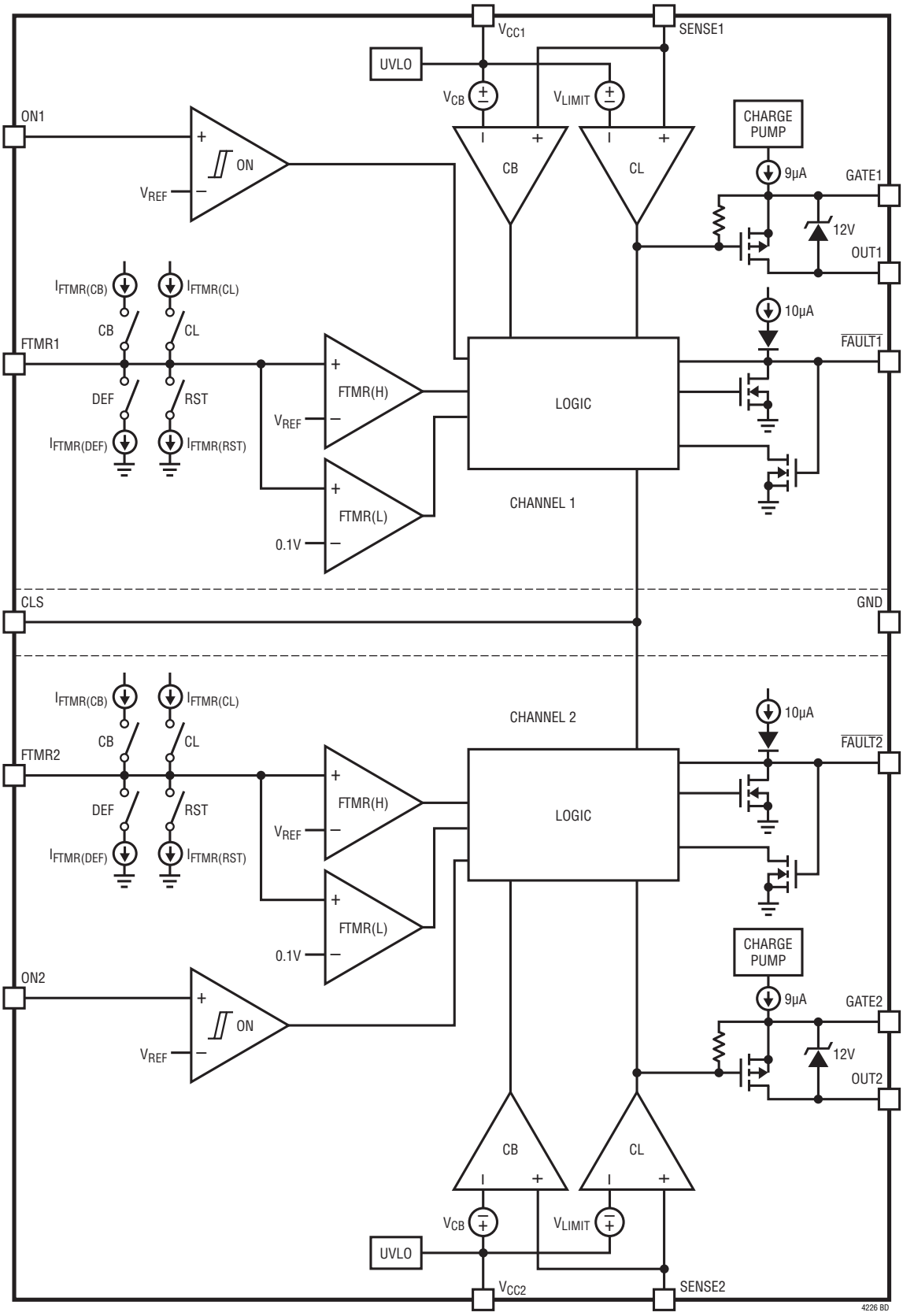
ON1, ON2: ON Control Inputs. The ON pins have a 1.23V threshold with 50mV of hysteresis. A high input turns on the external MOSFET with a 10ms delay. A low input turns off the external MOSFET and resets circuit breaker faults.

OUT1, OUT2: Gate Drive Return. Connect this pin to the source of the external N-channel MOSFET switch. This pin provides a return for the gate pull-down circuit. When the GATE pin is below the OUT pin, the internal clamp diode draws current from this OUT pin.

SENSE1, SENSE2: Current Sense Negative Input. The circuit breaker comparator and the current limit amplifier monitor the voltage across the sense resistor. The current limiting amplifier controls the GATE of the external MOSFET to keep the sense resistor voltage at V_{LIMIT}. The current limit is set higher than the circuit breaker to accommodate noisy loads that momentarily exceed the circuit breaker comparator threshold.

V_{CC1}, V_{CC2}: Supply Voltage and Current Sense Positive Input. An undervoltage lockout circuit disables the MOSFET switch until V_{CC} is above the lockout voltage $V_{CC(UVL)}$ for 50ms.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

The LTC4226 controls two independent Hot Swap channels. It is designed to turn each supply voltage on and off in a controlled manner, allowing live insertion into a powered connector or backplane.

The LTC4226 powers-up the output of a channel when that channel's V_{CC} pin has remained above the 3.7V undervoltage lockout threshold $V_{CC(UVL)}$ for more than 50ms and its ON pin has remained above the V_{ON} threshold for more than 10ms. During normal operation, a charge pump turns on the external N-channel MOSFET providing power to the load. Each channel's charge pump derives its power from its own V_{CC} supply pin. To protect the MOSFET, the GATE voltage is clamped at about 12V above the OUT pin. It is also clamped a diode voltage below the OUT pin and a diode voltage below GND.

The current flowing through the MOSFET is measured by the external sense resistor. The sense voltage across the sense resistor is measured between the V_{CC} and SENSE pins. The LTC4226 has a circuit breaker (CB) comparator to detect the sense current above circuit breaker threshold and a current limit (CL) amplifier to actively clamp the sense current at the current limit threshold. Both the CB comparator and the CL amplifier monitor the sense resistor voltage between the V_{CC} and SENSE pins. When the sense voltage exceeds V_{CB} but is below V_{LIMIT}, the CB comparator enables a 2µA $I_{FTMR(CB)}$ current source that ramps up the voltage on the FTMR pin. If the sense resistor voltage exceeds V_{LIMIT}, the CL amplifier limits the current in the MOSFET by reducing the GATE-to-OUT voltage with an active control loop. The fast response CL amplifier can quickly gain control of the GATE-to-OUT voltage in the event of an OUT-to-GND short circuit. The FTMR pin is ramped up by the larger $I_{FTMR(CL)}$ current source during active current limiting. If the sense voltage falls below V_{CB}, the FTMR is ramped down by the default 2µA $I_{FTMR(DEF)}$ pull-down current.

A fault timeout occurs when an overcurrent condition persists above V_{CB} that causes the FTMR pin to ramp to the $V_{FTMR(H)}$ threshold. When this occurs, the MOSFET is turned off and the $\overline{FAULT}$ pin asserts low. The FTMR has two timeout durations: a longer circuit breaker (CB) timeout with a lower current $I_{FTMR(CB)}$ ramp up when the current limit is not activated and a shorter current limit (CL) timeout with a higher current $I_{FTMR(CL)}$ ramp up if current limit is active. The CLS input state sets the higher current $I_{FTMR(CL)}$ at 20µA when CLS = 0V; 36µA when CLS = open; 80µA when CLS > 2V.

During current limit, the sense voltage is at V_{LIMIT}. There can be significant MOSFET power dissipation while in current limit due to the substantial drain-to-source voltage. The CL timeout duration should be selected based on the external MOSFET safe-operating-area to prevent MOSFET damage. The CL timeout is set by the FTMR capacitor C_T and the $I_{FTMR(CL)}$ pull-up to the $V_{FTMR(H)}$ threshold. Setting the current limit higher than the circuit breaker threshold allows momentary current load spikes as long as the average current remains below the circuit breaker limit.

Both channels share a common current limit select, CLS pin. This pin has three input states: low, open and high. The three input states configure the preset current limit V_{LIMIT} to approximately 1.5×, 2× or 3× of 1.15 • V_{CB}.

After a fault timeout, the auto-retry (LTC4266-2) version waits 0.5 seconds before resetting FTMR. After the FTMR capacitor is discharged, the GATE pin is free to ramp up again after the $\overline{FAULT}$ pin resets high. For the latchoff (LTC4266-1) version, there is no 0.5 second restart delay. For both versions, FTMR can be reset by cycling the ON pin low and then high or by cycling V_{CC} below and then above UVLO.

The $\overline{FAULT}$ pin pulls low when active with a 5mA current limit. The pin can drive a low-current 2mA LED with a series resistor connected to V_{CC}. The $\overline{FAULT}$ pin has an internal 10µA pull-up current to a diode below its internal V_{CC} when signaling no fault. Pulling the $\overline{FAULT}$ pin below the $V_{\overline{FAULT}}$ threshold causes the external MOSFET to turn off without affecting FTMR status. The $\overline{FAULT}$ pin can be wire-OR'ed with other open-drain outputs.

The output voltage of the Hot Swap circuit is ramped down when the ON pin transitions low or V_{CC} falls below the 3.7V undervoltage lockout. The gate driver discharges the GATE pin with 3mA (including 2.85mA to the OUT pin) when GATE > OUT and 150µA to GND when GATE < OUT.

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The typical LTC4226 application is in high availability systems that distribute positive voltage supplies between 4.5V to 44V to hot-swappable ports or cards. It can also be used in daisy chain port applications like FireWire to provide instant current limit.

The basic two channel applications are shown in Figure 1 and Figure 2. Figure 1 shows the LTC4226 in a card resident application with an upstream connector. Figure 2 shows the LTC4226 on a backplane or motherboard with a downstream connector. Each Hot Swap channel has a power path controlled by an external MOSFET switch and a sense resistor for monitoring current.

Turn-On Sequence

During turn-on, a 9µA current charges the gate of the MOSFET switch: Q1 for channel 1. The current limit amplifier monitors the current in the channel 1 power path by sensing the voltage across the resistor, R_{S1}.

At start-up, the switch current is typically dominated by the current charging the load capacitor, C_{L1}. If the sense voltage reaches V_{LIMIT}, the current limit amplifier controls the gate of the MOSFET in a closed loop. This keeps the start-up inrush current at the current limit.

Several conditions must be present before the external MOSFET can be turned on. The fault timer FTMR is reset by either UVLO or ON low status. The external supply V_{CC} must exceed its undervoltage lockout level $V_{CC(UVL)}$ for more than 50ms. The ON pin must be high for more than 10ms and the $\overline{FAULT}$ pin must be high before the external MOSFET turns on with no additional delay.

If the channel is not in UVLO, the ON pin low to high assertion delay is 10ms. The $\overline{FAULT}$ pin must be high before the external switch turns on. When the channel is not in UVLO and the ON pin is high, there is no delay from the $\overline{FAULT}$ low to high transition to turn on of the external switch.

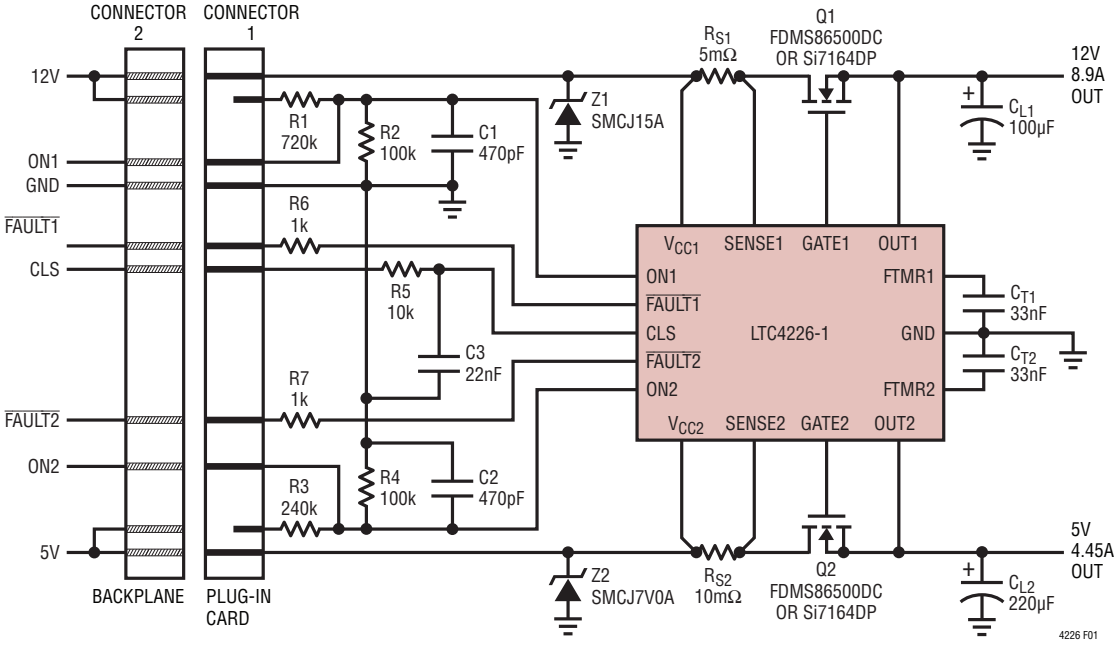

Figure 1. 2-Channel Card Resident Controller with Upstream Connector

APPLICATIONS INFORMATION

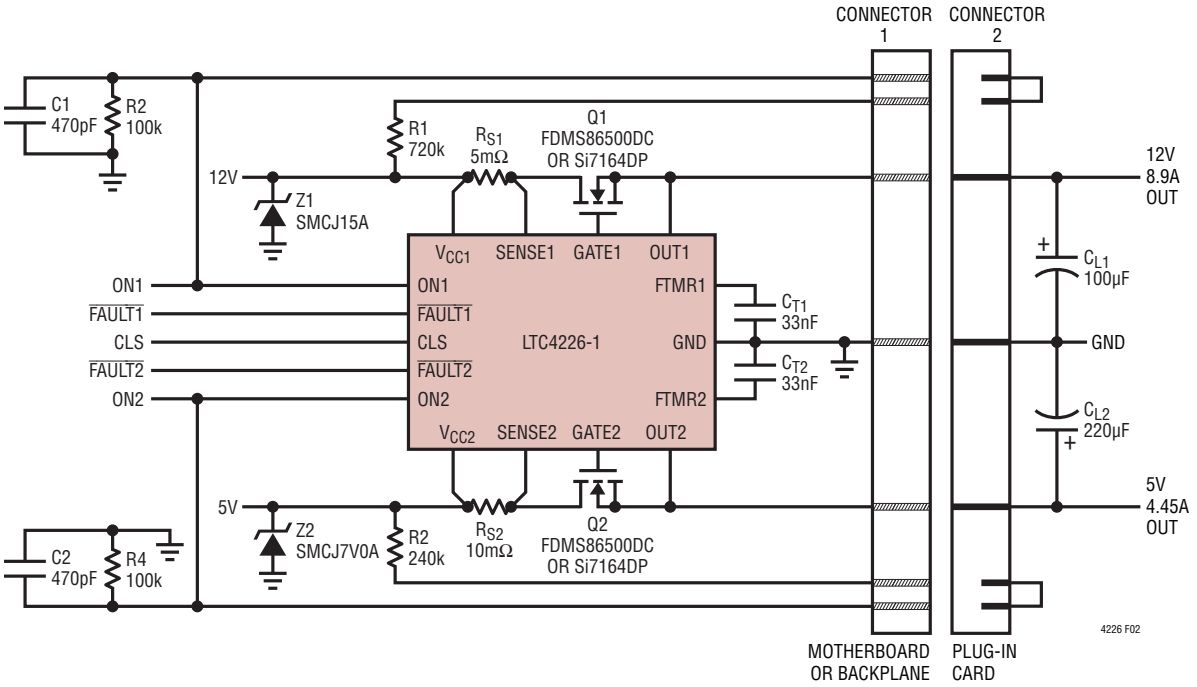

Figure 2. 2-Channel Backplane Resident Controller with Downstream Connector

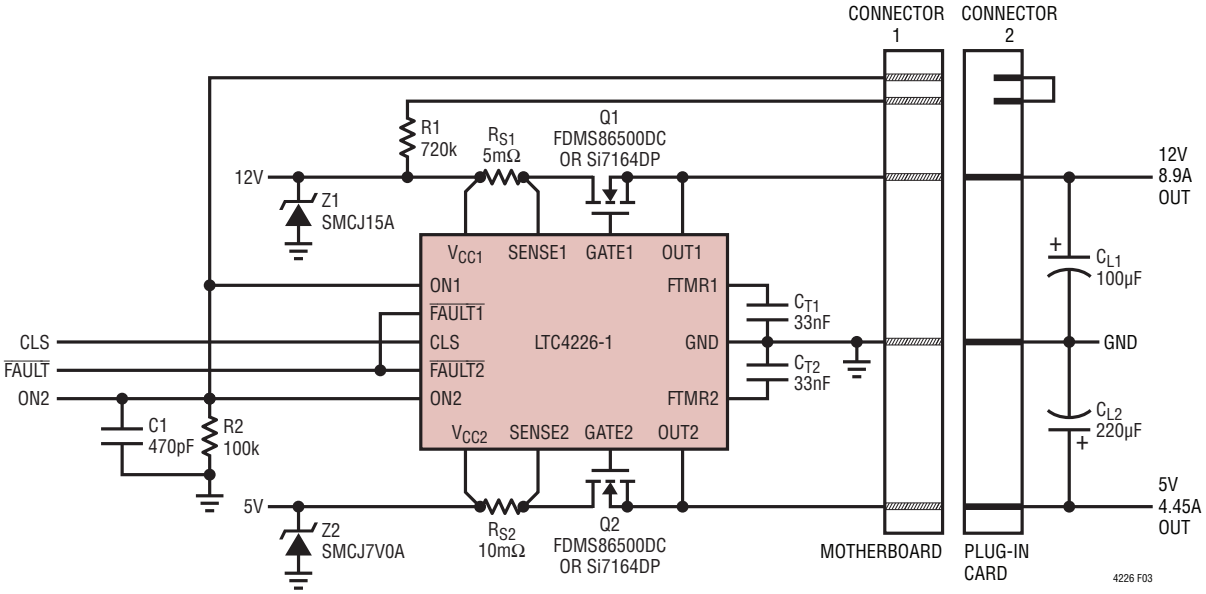

Figure 3. 2-Channel Controller with a Common ON/OFF Connection

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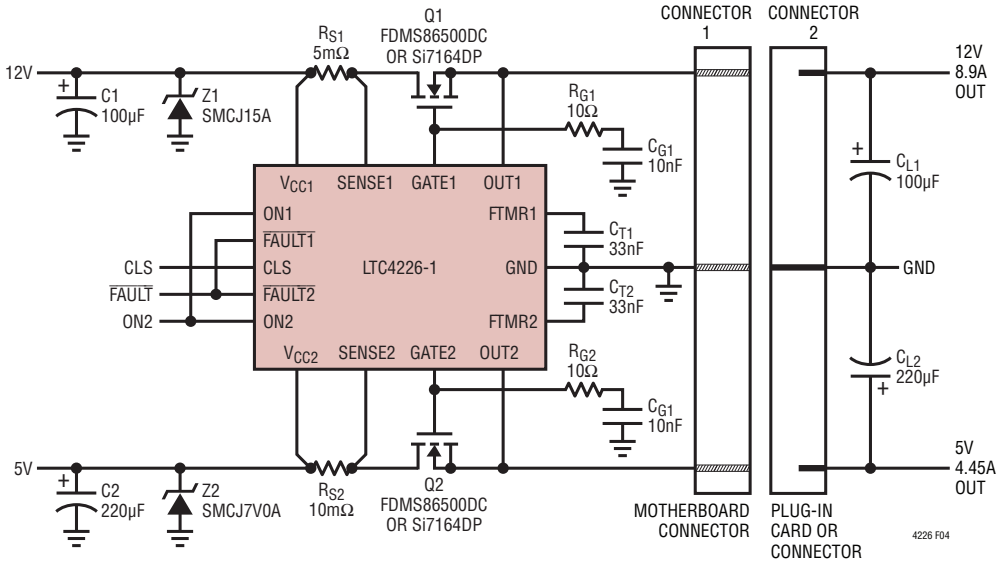

Figure 4. 2-Channel Controller with Inrush Current Control but without Connector Enable

Turn-Off Sequence

The MOSFET switch can be turned off by a variety of conditions. A normal turn-off is initiated by the ON pin going low. Additionally, a circuit breaker/current limit timeout will cause the MOSFET to turn off, as will V_{CC} dropping below its undervoltage lockout potential $V_{CC(UVL)}$. Alternatively, the $\overline{FAULT}$ pin can be externally pulled low to force the gate shutdown. Under any of these conditions, the MOSFET is turned off with a 3mA current pulling down from GATE. About 2.85mA of that current flows from GATE to OUT and the remainder flows to GND. When the GATE voltage is below the OUT pin, the GATE is pulled towards GND by a 150µA current source.

Inrush Current Control

In most applications, keeping the inrush current at current limit is an acceptable start-up method if it does not trip the fault timer FTMR and the MOSFET has an adequate safe operating margin. To keep the inrush sense resistor voltage below the circuit breaker threshold voltage V_{CB}, a resistor R_G and a capacitor C_G can be inserted between the GATE pin and ground as shown in Figure 4. The capacitor C_G with a grounded terminal and interconnect inductance can lead to parasitic MOSFET oscillations. A resistor R_G between 10Ω and 100Ω is typically adequate to prevent parasitic oscillation. R_G also allows C_G to act as a charge reservoir during current limit while preserving the fast pull-down of the gate. The capacitor C_G should be sized to limit the inrush current below the circuit breaker trip current. For leaded MOSFET with heatsink, an additional 10Ω resistor (as shown with R1 in Figure 13) can be added close to the MOSFET gate pin to prevent possible parasitic oscillation due to more trace/wire inductance and capacitance.

The MOSFET is turned on by a 9µA current source charging up the GATE. When the GATE voltage reaches the MOSFET threshold voltage, the MOSFET turns on and the SOURCE voltage follows the GATE voltage as it increases. The GATE voltage rises with a slope 9µA/C_G and the supply inrush current is:

$$I_{INRUSH} = \frac{C_L}{C_G} \bullet 9\mu A \quad (1)$$

Note that the voltage across the MOSFET switch can be large during inrush current control. If the inrush current is below the circuit breaker threshold, the fault timer FTMR is not activated. In some applications like Firewire where a large supply voltage step up transient can occur, the current limit amplifier is momentarily activated and the GATE is partially discharged. Once the switch current falls below the current limit, the GATE will continue to charge up at the supply inrush control rate.

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Overcurrent Fault

The LTC4226 manages overcurrent faults by differentiating between circuit breaker faults and current limit faults. Typical applications have a load capacitor to filter the load current. A large load capacitor is an effective filter, but it can increase MOSFET switch power dissipation at start-up or during step up supply transients.

When the MOSFET is fully enhanced and the current is below the current limit, the MOSFET power dissipation is low and is determined by the R_{DSON} and the switch current. If the current is above the circuit breaker threshold but below current limit, the circuit breaker CB comparator activates a $I_{FTMR(CB)}$ pull-up current source at the FTMR pin.

When the channel current exceeds the current limit, the CL amplifier activates the gate driver pull-down in a closed loop manner. The excess GATE overdrive voltage is abruptly discharged to the OUT pin until the sense voltage between V_{CC} and SENSE drops below V_{LIMIT}. This brief interval is kept short by the fast responding amplifier to reduce the excessive channel current. Next the CL amplifier servos the GATE pin to maintain the sense voltage at V_{LIMIT}. During this current limit interval, the power dissipation in the MOSFET increases. The worst case switch power dissipation occurs during a load short where the current is set by the current limit with the entire supply voltage appearing across the MOSFET. During active current limiting, the FTMR pin is pulled up with $I_{FTMR(CL)}$.

Dual-Rate Fault Timer

The fault timer pin FTMR, as illustrated in Figure 5 timing waveforms, has a dual-rate fault pull-up that extends the allowable duration of peak currents that are above the circuit breaker threshold but below the current limit level. When the load current exceeds the current limit threshold, the power dissipation in the MOSFET may be high due to the potentially large drain-to-source voltage. In this condition, the FTMR pull-up current increases to reduce the fault timer duration. When the load current is below the current limit threshold, the power dissipation in the MOSFET is less since the MOSFET is fully enhanced and the drain-to-source voltage is small. Therefore, when the current is below the current limit threshold but above the circuit breaker threshold, the FTMR pull-up current is reduced. The MOSFET will turn off in a fault condition where the average current is above the circuit breaker threshold, but the dual-rate timer extends the allowable duration for peak currents that remain below the current limit level.

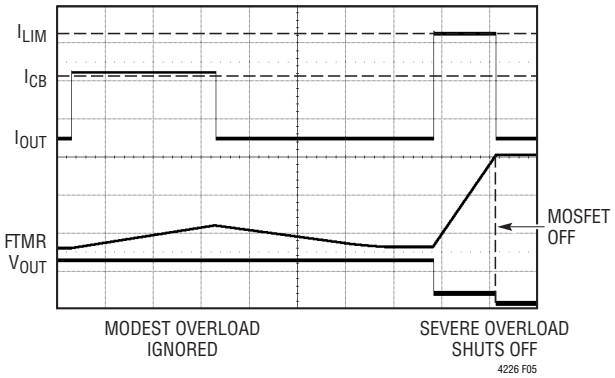

Figure 5. Dual-Rate Fault Timing

The FTMR pin has comparators and four current sources connected to an external capacitor C_T. The four current sources are: the default pull-down current $I_{FTMR(DEF)}$, the circuit breaker pull-up current source $I_{FTMR(CB)}$, the higher current limit pull-up current source $I_{FTMR(CL)}$ and the reset pull-down current source $I_{FTMR(RST)}$. When the FTMR pin voltage exceeds the $V_{FTMR(H)}$ threshold, the FTMR comparator signals a fault timeout.

The FTMR pin is held low in default normal mode whenever the circuit breaker comparator, the current limit amplifier and the reset are all inactive. The default mode has the $I_{FTMR(DEF)}$ pull-down current source activated. When the sense voltage exceeds the circuit breaker threshold V_{CB} but is below V_{LIMIT}, the circuit breaker comparator enables the $I_{FTMR(CB)}$ pull-up current source and disables the $I_{FTMR(DEF)}$ current source. When the sense voltage reaches the V_{LIMIT} threshold, the current limit amplifier activates the higher $I_{FTMR(CL)}$ pull-up current source.

When the FTMR pin ramps up to $V_{FTMR(H)}$, the FTMR(H) comparator trips. The $\overline{FAULT}$ pin is asserted low and the GATE to OUT voltage is discharged to turn off the MOSFET. For the Auto-Retry option, the Auto-Retry internal timing is initiated. The FTMR pin is asserted high at $V_{FTMR(H)}$ until the FTMR(L) comparator is reset low at $V_{FTMR(L)}$ by the $I_{FTMR(RST)}$ pull-down source, which is activated by ON low or UVLO or at the end of the Auto-Retry interval of typically 0.5s. The $\overline{FAULT}$ pin goes high when the FTMR

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pin is pulled below $V_{FTMR(L)}$. The GATE to OUT voltage can ramp up for Auto-Retry mode if the ON pin is high and V_{CC} is not in UVLO.

When the MOSFET current exceeds the circuit breaker threshold but remains below the current limit the fault time is given by:

$$t_{CB} = C_T \bullet \frac{1.23V}{I_{FTMR(CB)}} \quad (2)$$

When the current limit is active the fault time is given by:

$$t_{LIMIT} = C_T \bullet \frac{1.23V}{I_{FTMR(CL)}} \quad (3)$$

During active current limiting, a large MOSFET drain to source voltage can appear, and t_{LIMIT} should be selected appropriately based on the worst MOSFET safe-operating-area with the OUT pin shorted to ground.

A $I_{FTMR(RST)}$ pull-down source is active when resetting the fault status. The current sources at the FTMR pin can be overdriven externally. The FTMR pin can be pulled high externally above $V_{FTMR(H)}$ to force a fault status or the FTMR pin can be pulled low externally towards ground to force a reset status. Both the $\overline{FAULT}$ and GATE pins behave the same way for externally driven FTMR as described above for internal mode. A prolonged external pull-down is not recommended as it may mask normal FTMR operation.

Selecting Current Limit to Circuit Breaker Ratio

The ratio of the current limit voltage V_{LIMIT} and circuit breaker voltage V_{CB} can be configured to allow low duty cycle, high crest factor load events like hard drive spin up to operate above the maximum average load current without invoking current limit. Avoiding current limit events is a good practice as the load voltage is not glitched unnecessarily by the current limit amplifier and the MOSFET power dissipation is kept low. The unlatched CLS pin has three input states (low, open and high). This pin configures both Hot Swap channels simultaneously the preset current limit voltage V_{LIMIT} to approximately 1.5×, 2× or 3× of 1.15 • V_{CB}. However, higher current limit settings will result in higher MOSFET power dissipation in the event of a load short. Proper choice of the MOSFET must accommodate high MOSFET power dissipation under the worst case short-circuit. There are three $I_{FTMR(CL)}$, each corresponds with a V_{LIMIT} selected by the CLS input. The typical MOSFET SOA (safe operating area) has a constant P^2t characteristic for single narrow (<10ms) pulse dissipation. An increase in current (V_{LIMIT}) for constant MOSFET drain/source voltage results in square reduction in allowed stress duration t_{LIMIT} (or square increase in $I_{FTMR(CL)}$).

The CLS pin is internally pulled to 1.23V. If it is driven by a three-state output, the maximum allowable open-circuit leakage is ±2µA. The driving output must source or sink more than 10µA in the high or low state. If the CLS trace crosses noisy digital signal lines, an RC filter close to the CLS pin will filter noise pickup (as shown in Figure 1: R5/C3).

Auto-Retry vs Latchoff

The LTC4226-2 (automatic retry) version resets the FTMR pin after a 0.5 second delay following a FTMR(H) comparator timeout if the V_{CC} voltage remains above the 4V undervoltage lockout threshold $V_{CC(UVL)}$ and the ON pin remains above its 1.23V V_{ON} threshold. This retry delay can be terminated to force a 50ms delay restart by cycling V_{CC} below the $V_{CC(UVL)}$ undervoltage threshold or a 10ms delay restart by cycling the ON pin below the V_{ON} threshold. The latchoff option (LTC4226-1) does not reset FTMR(L) comparator automatically. It requires voltage cycling at either the ON pin or the V_{CC} pin to reset FTMR pin.

Resetting Faults

The circuit breaker fault can be reset by cycling the ON pin below and then above the ON comparator threshold. There is a turn on delay of 10ms after the ON pin transitions high.

Alternatively, the V_{CC} pin can be cycled below and then above the undervoltage lockout threshold to reset faults. There is a turn on delay of 50ms after the V_{CC} pin exits the undervoltage lockout.

The FTMR pin reset begins with the FTMR pin pulled down with 100µA to ground. This is followed by a start-up with a 10µA $\overline{FAULT}$ pin pull-up and a 9µA GATE pin pull-up.

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Fault Status

The $\overline{FAULT}$ status pin is active low with a 10µA current source pull-up to a diode below its internal supply voltage, typically 5V for any V_{CC} >7V. When a fault occurs, the $\overline{FAULT}$ pin pulls to ground with a 5mA limit. Although the $\overline{FAULT}$ pin has the same voltage rating as the supply pin, sinking LED current as in Figure 9 requires a series resistor to reduce pin power dissipation.

The $\overline{FAULT}$ pin is also an unlatched input to synchronize the MOSFET GATE. Pulling this pin externally below 0.3V causes the GATE to shutoff immediately. This pin can optionally be wire-ORed with other LTC4226's $\overline{FAULT}$ pins to turn off their GATEs when one of the LTC4226 has a circuit breaker fault with the FTMR pin asserted at $V_{FTMR(H)}$. The other LTC4226's FTMR pin is unaffected by the low external $\overline{FAULT}$ input. When the LTC4226 with fault is reset (see section on auto-retry and resetting faults), the wire-ORed $\overline{FAULT}$ pins return high and the GATEs revert to their prior states. It is not recommended to connect an LED to wire-ORed $\overline{FAULT}$ pins.

Daisy Chained Ports

Figure 7, illustrates FireWire power distribution with LTC4226 Hot Swap circuits and supply diode-ORing. The Firewire devices can be power providers or power consumers and can be daisy chained together.

In Figure 8, a 2-port device allows either port to be powered internally through diode D1 or to be powered from the opposite port. The higher voltage source delivers power to the external port devices and the internal FireWire controller interface. This permits the host power to be shutdown while the FireWire controller remains active with external power provided by the port. The port can relay actively current limited power as long as there are power sources in the chain. More than two ports per device are possible permitting power consumption or distribution among multiple ports. The ports allow live plugging and unplugging with port load capacitances as large as 1mF at 33V for Figure 8. The output port step up surge current is actively limited.

Figure 9 shows a 12V host power source application that can drive a remote load capacitance up to 100µF with a small MOSFET like the Si2318DS. 2mA rated LEDs can be used as $\overline{FAULT}$ indicators with resistors to reduce power dissipation at the $\overline{FAULT}$ pins.

V_{CC} Overvoltage Detection

The FTMR pin can be used to detect a V_{CC} overvoltage condition with a Zener diode Z2 as shown in Figure 6. Resistor R5 and Zener Z3 protect the FTMR pin from excessive voltage while R6 provides a ground path. An overvoltage at V_{CC} beyond 35V will pull the FTMR pin above 1.23V through diode D2A and force a fault status. If V_{CC} has a transient suppressor as shown in Figure 10, the overvoltage threshold should be set at 35V which is below the transient suppressor SMCJ33A minimum breakdown voltage of 36.7V.

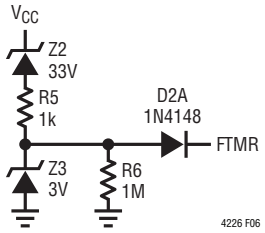

Figure 6. V_{CC} Overvoltage Detection

Supply Transient Protection

All pins on the LTC4226 are tested for 44V operation with the exception of FTMR and GATE. The GATE pins are voltage clamped either to OUT or GND while the FTMR pins are low voltage. If greater than 44V supply transients are possible, 33V transient suppressors are highly recommended at the V_{CC} pins to clamp the voltage below the 55V absolute maximum voltage rating of the pins.

Output Positive Overvoltage Isolation

Transient voltage suppressors are adequate for clamping short overvoltage pulses at the ports, but they may overheat if forced to sink large currents for extended periods. Figure 10 shows how series MOSFETs can be used to isolate positive port voltages up to the MOSFET V_{BVDSS}. Q3 and Q4 are turned off when the overvoltage detection Zener Z2 pulls both FTMR1 and FTMR2 high through D2A and D2B. The resistors R7 and R8 with MOSFETs Q5 and Q6 facilitate restart by pulling up through the body diodes of Q1 and Q2, respectively.

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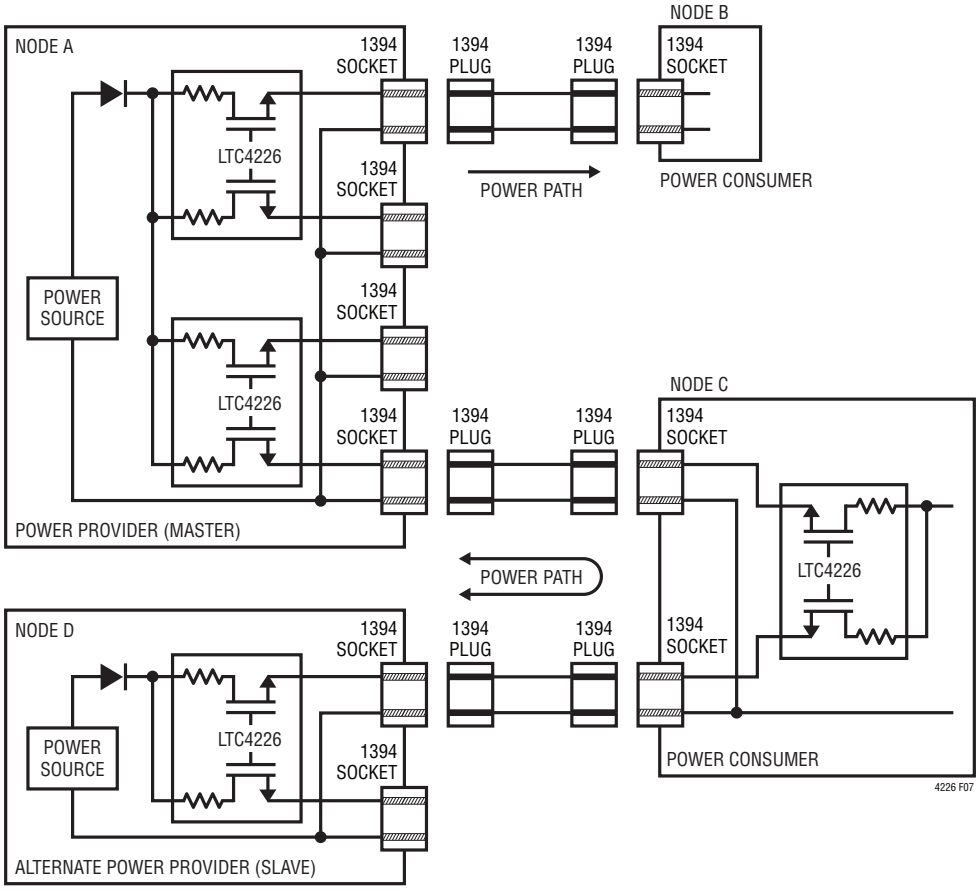

Figure 7. FireWire Power Distribution Example

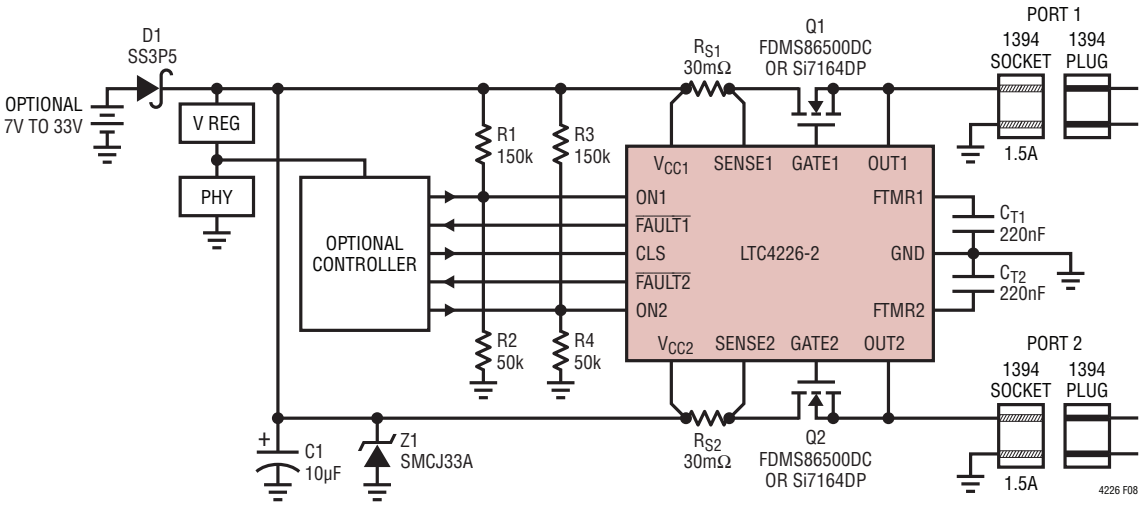

Figure 8. 2-Port FireWire Master or Slave Application

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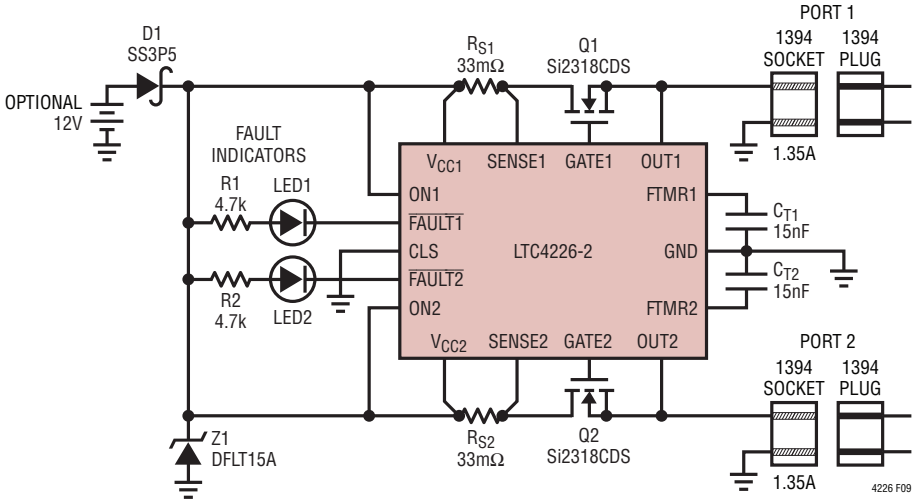

Figure 9. 12V FireWire Ports with LED Fault Indicators

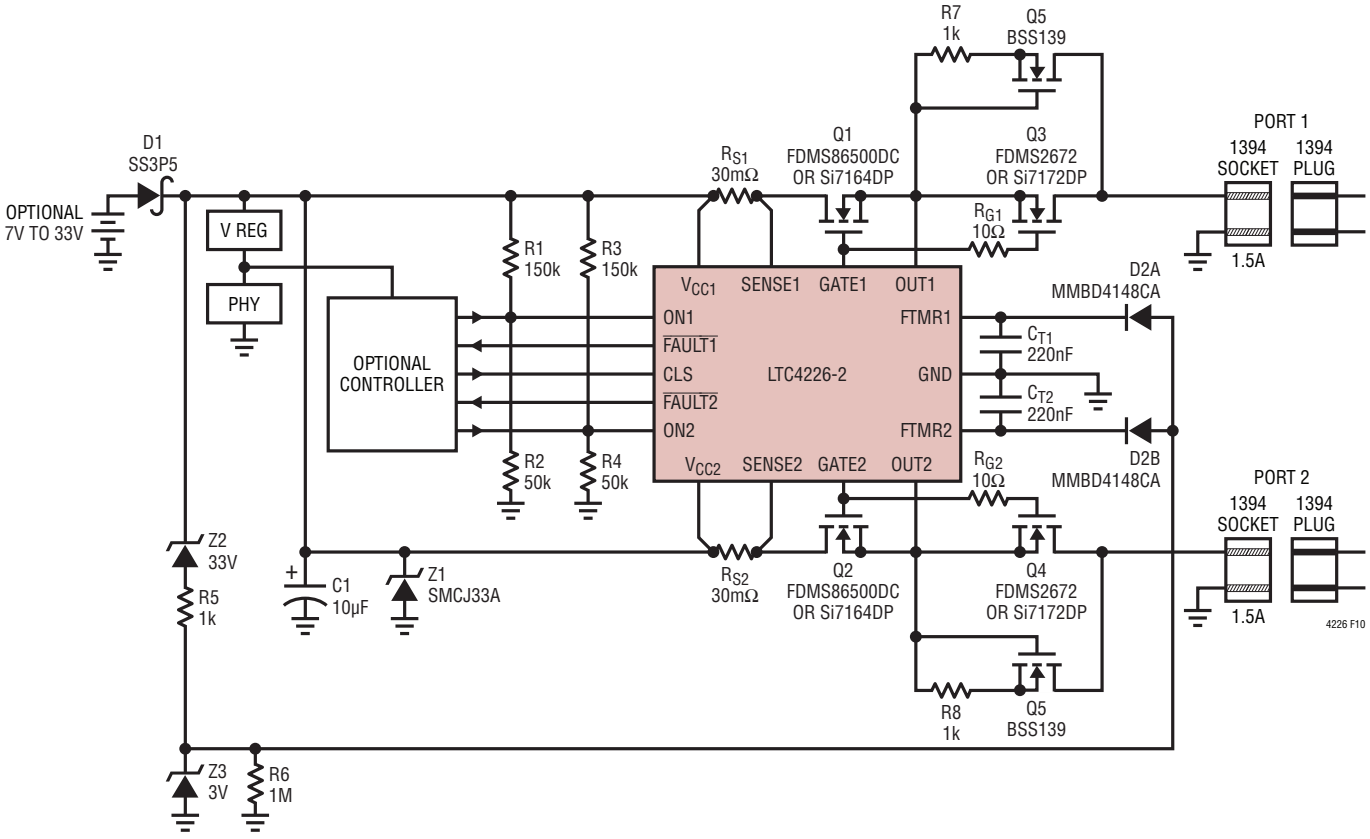

Figure 10. 2 FireWire Ports with Positive Overvoltage Isolation

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Design Example

As a design example, take the following specifications for Figure 8 with a load capacitor C_{OUT} of 1mF (not shown on schematic) at the cable end of port 1:

The channel is rated for a maximum V_{CC} of 33V at 1.5A, C_{OUT} = 1mF and current limit at 1.5× of circuit breaker current.

Circuit breaker current plus a 15% margin:

I_{CB} = 1.5A • 1.15 = 1.725A,

Sense resistor:

$$R_S = \frac{50mV}{1.5A \bullet 1.15} \approx 29m\Omega$$

Start-up in current limit with CLS low,

V_{LIMIT} = 1.5 • 1.15 • V_{CB}

and

I_{LIMIT} = 1.5 • 1.15 • I_{CB} ≈ 2.98A

Calculate the time it takes to charge up C_{OUT} in current limit:

$$t_{CHARGE} = \frac{C_{OUT} \bullet V_{CC}}{I_{LIMIT}} \approx 11ms$$

During a normal start-up where all of the current charges C_{OUT}, the average power dissipation in the MOSFET is given by:

$$P_{DISS} = \frac{V_{CC} \bullet I_{LIMIT}}{2} = 49.2W$$

If the output is shorted to ground, the average power dissipation in MOSFET doubles:

P_{DISS} = V_{CC} • I_{LIMIT} = 98.4W

The SOA (safe operating area) curve for the FDMS86500DC MOSFET shows 100W for 35ms. During a normal start-up the MOSFET dissipates 49.2W for 11ms at 33V with adequate SOA margin.

Setting the current limit fault timeout at about 14ms gives:

$$C_T = \frac{t_{LIMIT} \bullet 20\mu A}{1.23V} = 228nF$$

Choose a standard value of 220nF. The resulting FTMR timeout in current limit is:

t_{LIMIT} = 13.5ms

The FTMR circuit breaker timeout is:

t_{CB} = 135ms

The resistor pair R1 and R2 sets the ON threshold voltage for both channels. In this case R1 = 150k, R2 = 50k:

$$V_{CC}\ ON\ Threshold = \frac{(R1+R2) \bullet 1.23}{R2} = 4.92V$$

Layout Considerations

To achieve accurate current sensing, Kelvin connections for the sense resistor are recommended. The PCB layout of Kelvin sensing traces should be balanced, symmetrical and minimized to reduce error. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for device power dissipation such as vias and wide metal area. A recommended PCB layout for the sense resistor and power MOSFET is illustrated in Figure 11. To avoid the need for the additional MOSFET GATE pin resistor (R1 in Figure 13), the GATE trace over ground plane should have minimized trace length and capacitance.

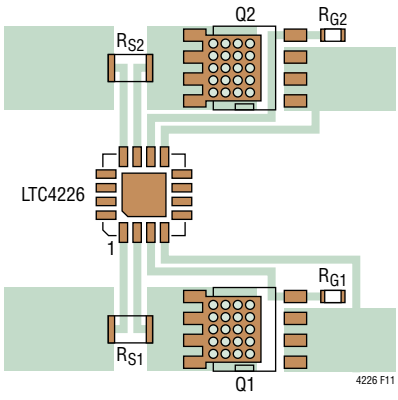

Figure 11. Recommended Layout

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In Hot Swap applications where load currents can be 5A, narrow PCB tracks exhibit more resistances than wide tracks and operate at elevated temperatures. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 0.5mΩ/square. The use of vias allow multi-copper planes to be used to improve both electrical conduction and thermal dissipation. Thicker top and bottom copper such as 3oz or more can improve electrical conduction and reduce PCB trace dissipation.

It is important to minimize noise pickup on PCB traces for ON, FTMR, $\overline{\text{FAULT}}$, CLS and GATE. If an R_G resistor is used, place the resistor as close to the MOSFET gate as possible to limit the parasitic trace capacitance that leads to MOSFET self-oscillation.

Bidirectional Current Limiting

Figure 16 shows an application with bidirectional current limiting with a common sense resistor. Figure 12 shows an asymmetric bidirectional current limiter for operating voltage between 7V and 30V using two separate sense resistors. Separate resistors allow different current limit in each direction to be set. The transient suppressor at the sense pins allow the circuit breaker to trip when either the input or output voltage exceeds the suppressor breakdown voltage. When the OUT voltage exceeds the suppressor breakdown, GATE2 shuts down after FTMR2 time-out and this can prevent suppressor blow out. The timing capacitor at FTMR2 can be selected to keep the suppressor within safe operating area.

High Current Applications

Figure 13 and Figure 14 show 44A and 89A continuous current applications for bus power distribution. The bus connection inductance causes a supply dip at the sense resistor when there is a load transient. The worst transient is a short at the output or the sudden connection of an uncharged load capacitor. Without capacitors C1 and C2 for channel 1, V_{CC1} voltage can dip below the LTC4226 undervoltage lockout threshold resulting in a channel 1 UVLO reset. The low ESR electrolytic capacitor C1 and ceramic capacitor C2 should be placed very close to the sense resistor V_{CC1} terminal and the ground plane to minimize inductance.

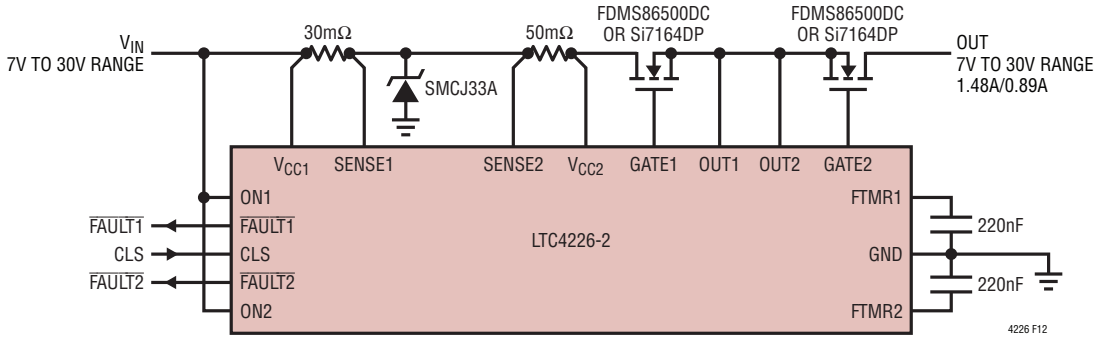


Figure 12. 7V to 30V Asymmetric Bidirectional Current-Limiter

APPLICATIONS INFORMATION

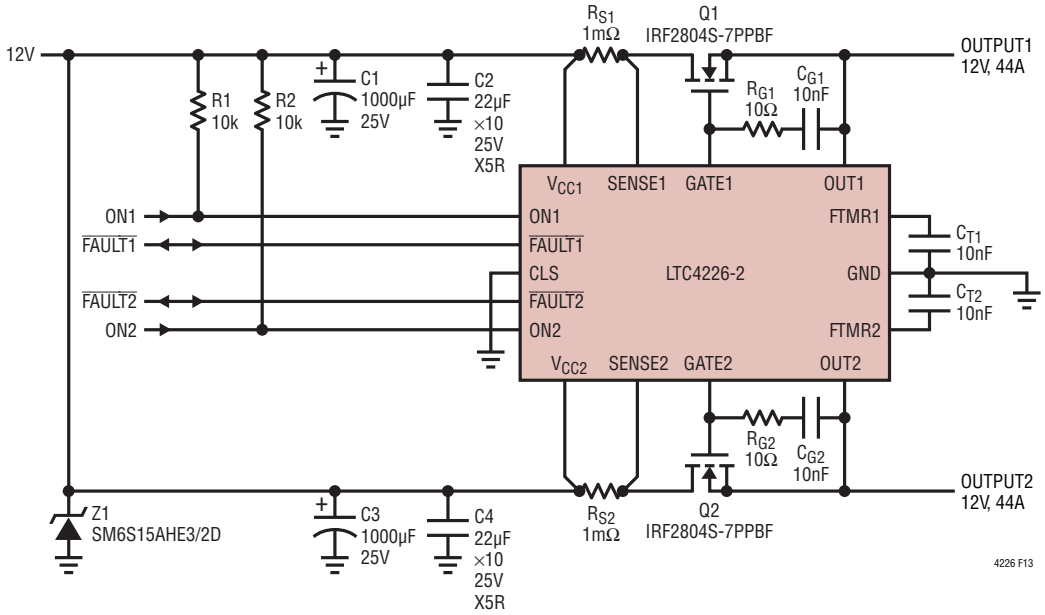


Figure 13. Dual Continuous 44A Typical Output

At the occurrence of severe load transient, the GATE1 voltage undershoots the voltage needed for current limit regulation. The R_{G1} and C_{CG1} network between GATE1 and OUT1 help restore GATE1 voltage quickly to the voltage needed for current limit regulation. When a heatsink is a used and gate interconnect has significant capacitance and inductance, optional resistors R1 and R2 can be inserted close to the MOSFET's gate to prevent parasitic oscillation. The product of R1 and MOSFET C_{ISS} add delay to the current limit response. For short PCB gate interconnection, these optional resistors are not needed.

Two Hot Swap channels with identical sense resistors and MOSFETs can have their outputs connected together to almost double the current output capability without significant improvement in MOSFET's SOA. OUTPUT1 in Figure 14 can be connected to OUTPUT2 to give 178A. FTMR1 and FTMR2 should be kept separate as capacitors C_{T1} and C_{T2} individually monitor the sense voltages across R_{S1} and R_{S2} respectively. In the event of a current fault, one channel may time out earlier than the adjacent channel due to mismatch. If $\overline{FAULT1}$ and $\overline{FAULT2}$ are kept separate, the current in the channel of the first fault is diverted to the adjacent channel with a second fault time out occurring later.

Now consider the case where $\overline{FAULT1}$ and $\overline{FAULT2}$ are tied together during a current fault. First fault channel $\overline{FAULT1}$ pulls low and this causes an input low at $\overline{FAULT2}$ with GATE2 pulling low immediately. FTMR2 does not time out due to the common $\overline{FAULT}$ connection with GATE2 disabled earlier than the case of separate $\overline{FAULT}$ connection. The MOSFET Q1 where the first occurrence of current fault occurs would not be stressed as much as Q2 since the fully enhanced Q2 determines the parallel channels V_{CC} and OUT voltage drop. Common ON pin connections are preferred for parallel channel applications.

APPLICATIONS INFORMATION

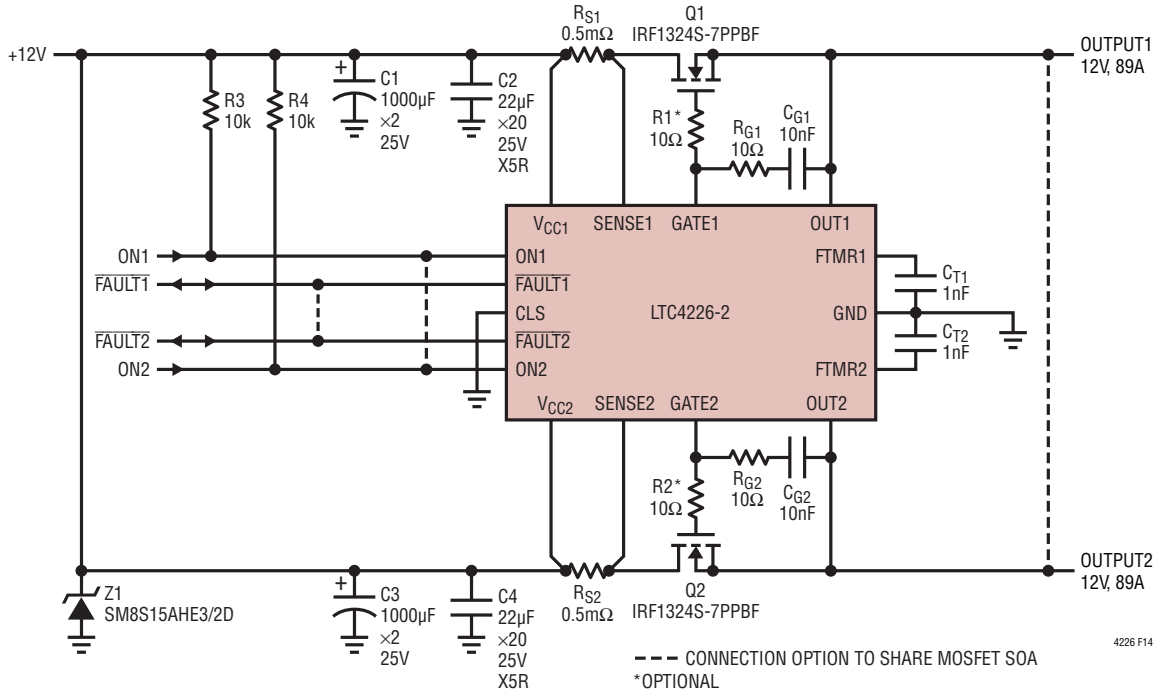


Figure 14. Dual Continuous 89A Typical Output

One drawback of the separate FTMR scheme for parallel channels is that one timer may ramp up in current limit mode before the other channel, resulting in shorter circuit breaker timer duration and/or a reduction in the combined circuit breaker current threshold due to $R_{DS(ON)}$ mismatch. These issues are solved by using two cross-coupled PNP clamps connected between the FTMR pins as shown in Figure 15. The $\overline{FAULT}$ pins are shorted together and connected to an external open drain pull-down which is controlled by a gate synchronization signal. The PNPs prevent a current limited channel's FTMR from ramping up too fast while the other channel is still in circuit breaker mode. If only one of the channels is in current limit mode, the clamp from the other channel will slow down the current limited channel's FTMR ramp rate as shown in Figure 15's accompanying waveforms. This scheme assumes common V_{CC} and ON pins, and both channels should be on the same chip. Channel to channel matching is 6% for V_{CB}, 6% for V_{LIMIT}, and GATE high skew delay timing for both ON and V_{CC} are 10%. The GATE pins must be synchronized by asserting the $\overline{FAULT}$ inputs low to mask out $t_{ON(UVL)}$ skew. Asserting the $\overline{FAULT}$ pins low for at least 100ms at power-up will ensure that the MOSFETs turn on together.

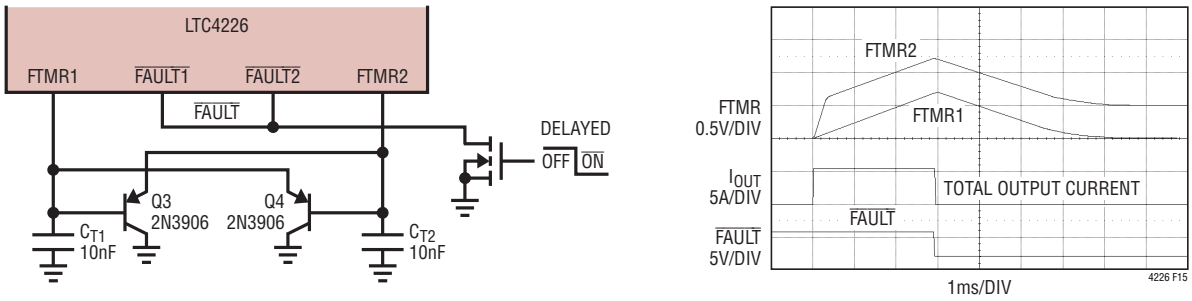
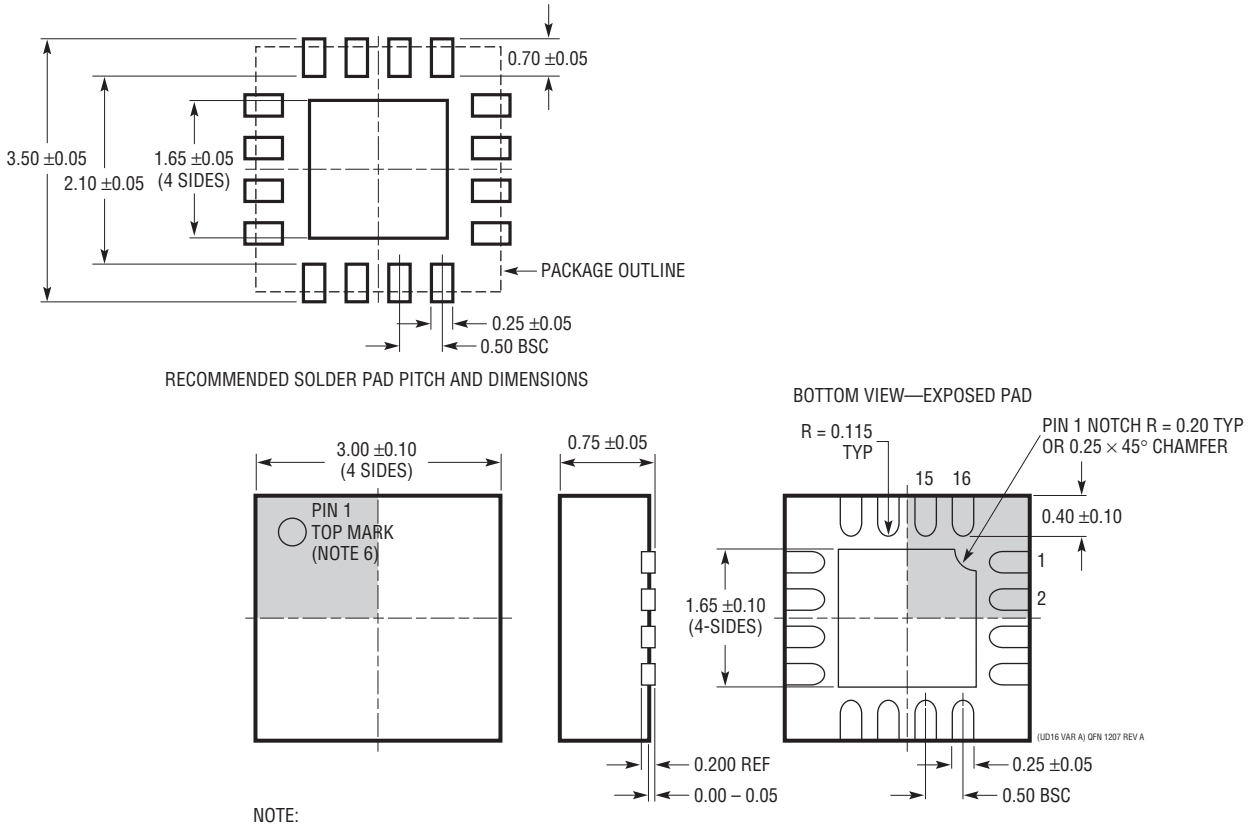


Figure 15. PNP Connected FTMR for 2 Parallel Channels

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1700 Rev A)
Exposed Pad Variation AA

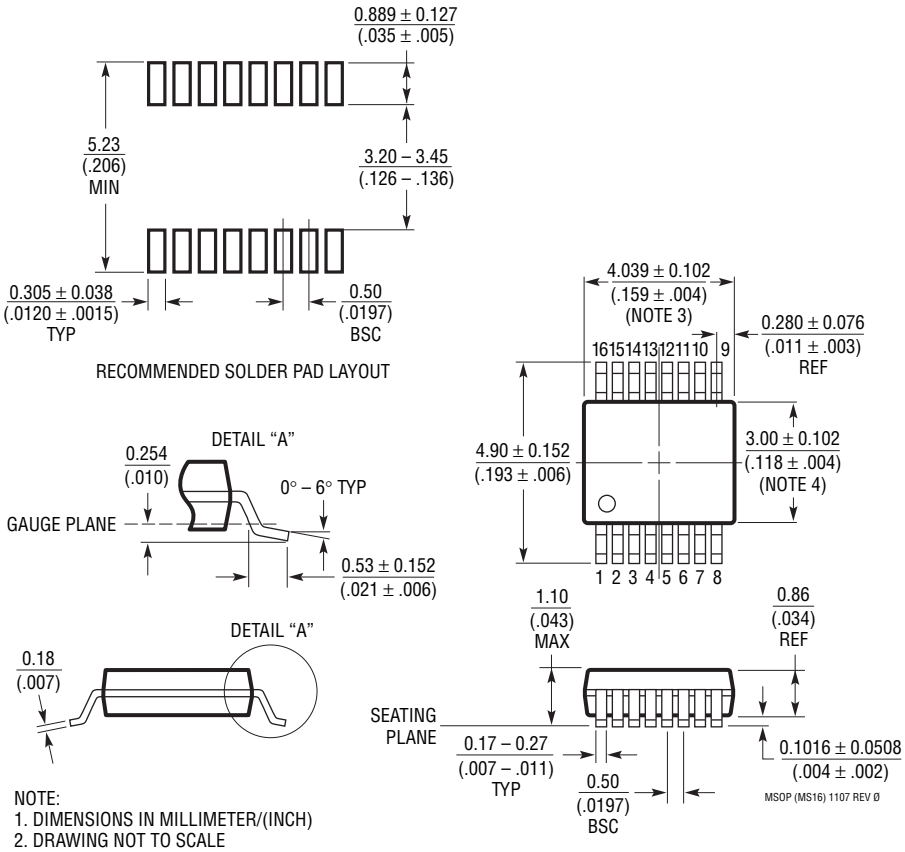


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX