Ideal Diode and Hot Swap Controller

FEATURES

- **Ideal Diode and Inrush Current Control for Redundant Supplies**
- **Low Loss Replacement for Power Schottky Diode**
- **Protects Output Voltage from Input Brownouts**
- **Allows Safe Hot Swapping from a Live Backplane**
- **2.9V to 18V Operating Range**
- Controls Back-to-Back N-Channel MOSFETs
- Limits Peak Fault Current in ≤1µs
- Adjustable Current Limit with Foldback
- Adjustable Start-Up and Current Limit Fault Delay
- 0.5µs Ideal Diode Turn-On and Turn-Off Time
- Undervoltage and Overvoltage Protection
- Status, Fault and Power Good Outputs
- Pin Selectable Latch Off or Automatic Retry After Fault
- 24-Lead 4mm × 5mm QFN and SSOP Packages

APPLICATIONS

- Redundant Power Supplies
- Supply Holdup
- High Availability Systems and Servers
- Telecom and Network Infrastructure
- Power Prioritizer

DESCRIPTION

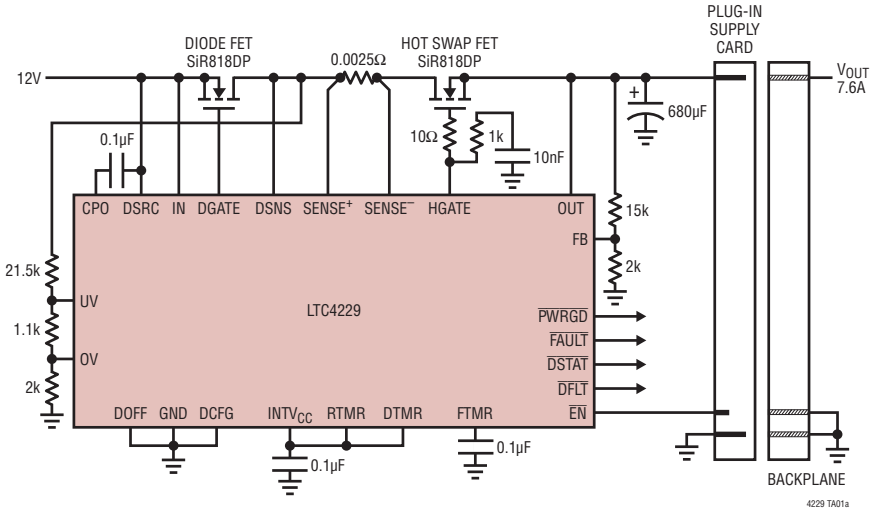
The LTC®4229 offers ideal diode and Hot Swap™ functions for a power rail by controlling two external N-channel MOSFETs. The MOSFET acting as an ideal diode replaces a high power Schottky diode and the associated heat sink, saving power and board area. The Hot Swap MOSFET control allows a board to be safely inserted and removed from a live backplane by limiting inrush current. The supply output is also protected against short-circuit faults with a fast acting foldback current limit and electronic circuit breaker.

The LTC4229 regulates the forward voltage drop across the external MOSFET to ensure smooth current transfer in diode-OR applications. The ideal diode turns on quickly to reduce the load voltage droop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse-current transients.

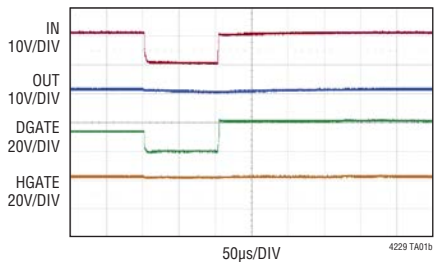
The LTC4229 provides adjustable start-up delay, undervoltage and overvoltage protection, and reports fault and power good status for the supply. It can be configured for latch off or automatic retry after a fault.

TYPICAL APPLICATION

Plug-In Supply Card Application



Diode FET Protects Output Voltage from Input Brownout



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages
- IN ..... –0.3V to 24V
- $INTV_{CC}$ ..... –0.3V to 7V

Input Voltages
- FB, DCFG ..... –0.3V to 7V
- FTMR, DTMR, RTMR ..... –0.3V to $INTV_{CC}$ + 0.3V
- UV, OV, $\overline{EN}$, DOFF ..... –0.3V to 24V
- $SENSE^+$, $SENSE^-$, DSNS, DSRC ..... –0.3V to 24V

Output Voltages
- $\overline{FAULT}$, $\overline{PWRGD}$, $\overline{DSTAT}$, $\overline{DFLT}$, OUT ..... –0.3V to 24V
- CPO, DGATE (Note 3) ..... –0.3V to 35V
- HGATE (Note 4) ..... –0.3V to 35V

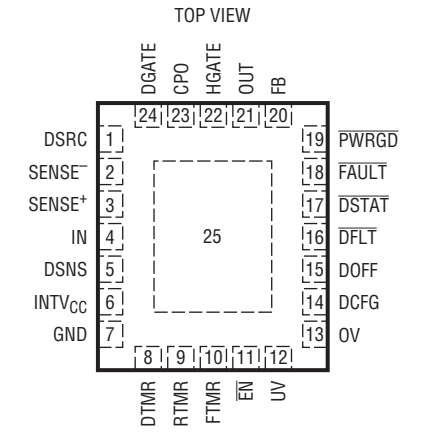
Average Currents
- $\overline{FAULT}$, $\overline{PWRGD}$, $\overline{DSTAT}$, $\overline{DFLT}$ 5mA
- $INTV_{CC}$ 1mA

Operating Ambient Temperature Range
- LTC4229C ..... 0°C to 70°C
- LTC4229I ..... –40°C to 85°C

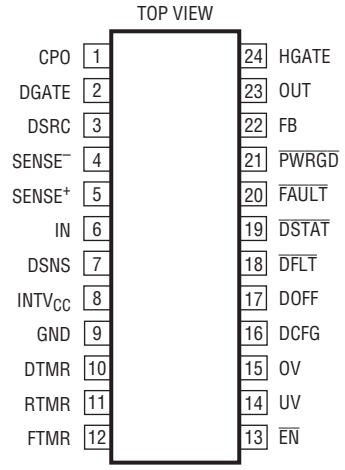
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- G Package ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W (Note 5)
EXPOSED PAD (PIN 25) PCB GND CONNECTION OPTIONAL



G PACKAGE
24-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 88°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4229CUFD#PBF	LTC4229CUFD#TRPBF	4229	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4229IUFD#PBF	LTC4229IUFD#TRPBF	4229	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4229CG#PBF	LTC4229CG#TRPBF	LTC4229G	24-Lead Plastic SSOP	0°C to 70°C
LTC4229IG#PBF	LTC4229IG#TRPBF	LTC4229G	24-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{IN}	Input Supply Range		●	2.9		18	V
I_{IN}	Input Supply Current		●		2	4	mA
V_{INTVCC}	Internal Regulator Voltage	I = 0, –500µA	●	4.5	5	5.5	V
$V_{INTVCC(UVL)}$	Internal V_{CC} Undervoltage Lockout	$INTV_{CC}$ Rising	●	2.1	2.2	2.3	V
$\Delta V_{INTVCC(HYST)}$	Internal V_{CC} Undervoltage Lockout Hysteresis		●	30	60	90	mV
Ideal Diode Control							
$\Delta V_{FWD(REG)}$	Forward Regulation Voltage ($V_{IN} – V_{DSNS}$)		●	35	50	65	mV
ΔV_{DGATE}	External N-Channel Gate Drive ($V_{DGATE} – V_{DSRC}$) ($V_{DGATE} – V_{DSRC}$)	IN < 7V, ΔV_{FWD} = 0.15V; I = 0, –1µA IN = 7V to 18V, ΔV_{FWD} = 0.15V; I = 0, –1µA	● ●	5 10	7 12	14 14	V V
$\Delta V_{DGATE(ST)}$	Diode MOSFET On Detect Threshold ($V_{DGATE} – V_{DSRC}$)	$\overline{DSTAT}$ Pulls Low, ΔV_{FWD} = 75mV	●	0.3	0.7	1.1	V
$\Delta V_{FWD(FLT)}$	Open Diode MOSFET Threshold ($V_{IN} – V_{DSNS}$)	$\overline{DFLT}$ Pulls Low	●	200	250	300	mV
I_{DSNS}	DSNS Pin Current	DSNS = 12V	●	50	150	300	µA
I_{DSRC}	DSRC Pin Current	DSRC = 0V	●		–95	–150	µA
$I_{CPO(UP)}$	CPO Pull-Up Current	CPO = DSRC = IN = 2.9V CPO = DSRC = IN = 18V	● ●	–70 –60	–105 –95	–130 –120	µA µA
$I_{DGATE(FPU)}$	DGATE Fast Pull-Up Current	ΔV_{FWD} = 0.2V, ΔV_{DGATE} = 0V, CPO = 17V			–1.5		A
$I_{DGATE(FPD)}$	DGATE Fast Pull-Down Current	ΔV_{FWD} = –0.2V, ΔV_{DGATE} = 5V			1.5		A
$I_{DGATE(DN)}$	DGATE Off Pull-Down Current	DOFF = 2V, ΔV_{DGATE} = 2.5V	●	50	100	200	µA
$t_{ON(DGATE)}$	DGATE Turn-On Delay	ΔV_{FWD} = 0.2V , C_{DGATE} = 10nF	●		0.25	0.5	µs
$t_{OFF(DGATE)}$	DGATE Turn-Off Delay	ΔV_{FWD} = –0.2V, C_{DGATE} = 10nF	●		0.2	0.5	µs
$t_{PLH(DGATE)}$	DOFF Low to DGATE High		●		50	100	µs
Hot Swap Control							
$\Delta V_{SENSE(TH)}$	Current Limit Sense Voltage Threshold ($V_{SENSE^+} – V_{SENSE^-}$) ($V_{SENSE^+} – V_{SENSE^-}$)	FB = 1.23V FB = 0V	● ●	22.5 6	25 8.3	27.5 10.6	mV mV
$V_{SENSE^+(UVL)}$	$SENSE^+$ Undervoltage Lockout	$SENSE^+$ Rising	●	1.8	1.9	2	V
$\Delta V_{SENSE^+(HYST)}$	$SENSE^+$ Undervoltage Lockout Hysteresis		●	10	50	90	mV
I_{SENSE^+}	$SENSE^+$ Pin Current	$SENSE^+$ = 11V, IN = 12V, OUT = 0V $SENSE^+$ = 13V, IN = 12V, OUT = 0V	● ●	150	300 2	450 4	µA mA
I_{SENSE^-}	$SENSE^-$ Pin Current	$SENSE^-$ = 12V	●	10	40	100	µA
ΔV_{HGATE}	External N-Channel Gate Drive ($V_{HGATE} – V_{OUT}$) IN = 7V to 18V; I = 0, –1µA	IN < 7V; I = 0, –1µA	● ●	5 10	7 12	14 14	V V
$\Delta V_{HGATE(H)}$	Gate High Threshold ($V_{HGATE} – V_{OUT}$)		●	3.6	4.2	4.8	V
$I_{HGATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, HGATE = 0V	●	–7	–10	–13	µA
$I_{HGATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, HGATE = OUT + 5V	●	1	2	4	mA
$I_{HGATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, HGATE = OUT + 5V	●	100	200	350	mA
$t_{PHL(SENSE)}$	Sense Voltage ($SENSE^+ – SENSE^-$) High to HGATE Low	ΔV_{SENSE} = 200mV, C_{HGATE} = 10nF	●		0.5	1	µs
$t_{OFF(HGATE)}$	OV High to HGATE Low UV Low to HGATE Low $\overline{EN}$ High to HGATE Low $SENSE^+$ Low to HGATE Low		● ● ● ●		10 10 20 10	20 20 40 20	µs µs µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{D(HGATE)}$	UV High, $\overline{EN}$ Low to HGATE Turn-On Delay	DTMR = $INTV_{CC}$	●	50	100	150	ms
$t_{P(HGATE)}$	UV to HGATE Propagation Delay	UV = Step 0.8V to 2V	●		10	20	µs
Input/Output Pin							
$V_{DOFF(H,TH)}$	DOFF Pin High Threshold	DOFF Rising	●	1.21	1.235	1.26	V
$V_{DOFF(L,TH)}$	DOFF Pin Low Threshold	DOFF Falling	●	1.19	1.215	1.24	V
$\Delta V_{DOFF(HYST)}$	DOFF Pin Hysteresis		●	10	20	30	mV
$V_{IN(TH)}$	UV, OV, FB Pin Threshold Voltage	Voltage Rising	●	1.21	1.235	1.26	V
$\Delta V_{UV(HYST)}$	UV Pin Hysteresis		●	40	80	120	mV
$\Delta V_{OV(HYST)}$	OV Pin Hysteresis		●	10	20	30	mV
$\Delta V_{FB(HYST)}$	FB Pin Hysteresis		●	10	20	30	mV
$V_{UV(RESET)}$	UV Pin Fault Reset Threshold Voltage	UV Falling	●	0.57	0.6	0.63	V
$I_{IN(LEAK)}$	Input Leakage Current (UV, OV, FB, DOFF)	V = 5V	●		0	±1	µA
$V_{\overline{EN}(TH)}$	$\overline{EN}$ Pin Threshold Voltage	$\overline{EN}$ Rising	●	1.185	1.235	1.284	V
$\Delta V_{\overline{EN}(HYST)}$	$\overline{EN}$ Pin Hysteresis		●	60	110	160	mV
$I_{\overline{EN}(UP)}$	$\overline{EN}$ Pull-Up Current	$\overline{EN}$ = 1V	●	–7	–10	–13	µA
$V_{TMR(H)}$	FTMR, DTMR, RTMR Pin High Threshold		●	1.198	1.235	1.272	V
$V_{TMR(L)}$	FTMR, DTMR, RTMR Pin Low Threshold		●	0.15	0.2	0.25	V
$I_{FTMR(UP)}$	FTMR Pull-Up Current	FTMR = 1V, In Fault Mode	●	–80	–100	–120	µA
$I_{FTMR(DN)}$	FTMR Pull-Down Current	FTMR = 2V, No Faults	●	1.3	2	2.6	µA
$I_{FTMR(RATIO)}$	FTMR Current Ratio $I_{FTMR(DN)}/I_{FTMR(UP)}$		●	1.3	2	2.7	%
$I_{TMR(UP)}$	DTMR, RTMR Pull-Up Current	V = 0V	●	–8	–10	–12	µA
$I_{TMR(DN)}$	DTMR, RTMR Pull-Down Current	V = 1.5V	●	1	5	10	mA
V_{IH}	Input High Voltage (DTMR, RTMR)		●	$INTV_{CC}$ – 0.1		$INTV_{CC}$ + 0.1	V
$V_{DCFG(TH)}$	Logic Input Threshold (DCFG)		●	0.5		2	V
I_{OUT}	OUT Pin Current	OUT = 11V, IN = 12V, $SENSE^+$ = 11.5V OUT = 13V, IN = 12V, $SENSE^+$ = 11.5V	● ●		40 1.7	100 4	µA mA
V_{OL}	Output Low Voltage ($\overline{PWRGD}$, $\overline{FAULT}$, $\overline{DSTAT}$, $\overline{DFLT}$)	I = 1mA I = 3mA	● ●		0.15 0.4	0.4 1.2	V V
V_{OH}	Output High Voltage ($\overline{PWRGD}$, $\overline{FAULT}$, $\overline{DFLT}$)	I = –1µA	●	$INTV_{CC}$ – 1	$INTV_{CC}$ – 0.5		V
I_{OH}	Input Leakage Current ($\overline{PWRGD}$, $\overline{FAULT}$, $\overline{DSTAT}$, $\overline{DFLT}$)	V = 18V	●		0	±1	µA
I_{PU}	Output Pull-Up Current ($\overline{PWRGD}$, $\overline{FAULT}$, $\overline{DFLT}$)	V = 1.5V	●	–7	–10	–13	µA
$t_{RST(UV)}$	UV Low to $\overline{FAULT}$ High		●		20	40	µs
$t_{PG(FB)}$	FB Low to $\overline{PWRGD}$ High		●		20	40	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the DGATE and CPO pins to a minimum of 10V above and a diode below DSRC. Driving these pins to voltages beyond the clamp may damage the device.

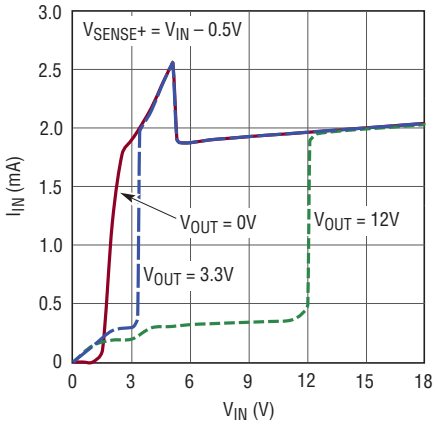
Note 4: An internal clamp limits the HGATE pin to a minimum of 10V above and a diode below OUT. Driving this pin to voltages beyond the clamp may damage the device.

Note 5: Thermal resistance is specified when the exposed pad is soldered to a 3" × 4.5", four layer, FR4 board.

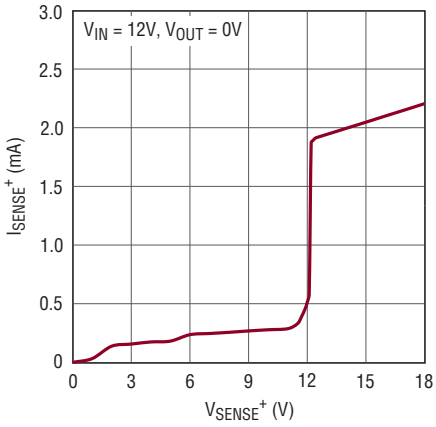
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, unless otherwise noted.

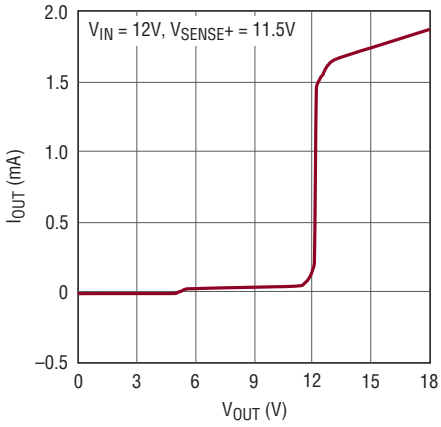
IN Supply Current vs Voltage



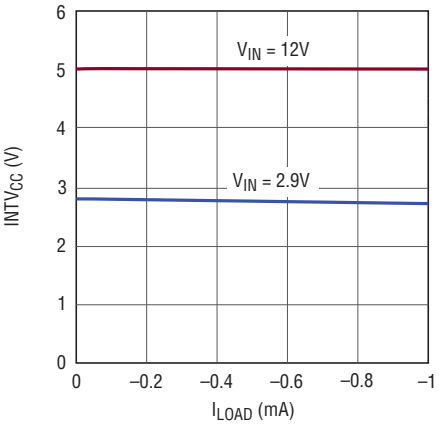
SENSE+ Current vs Voltage



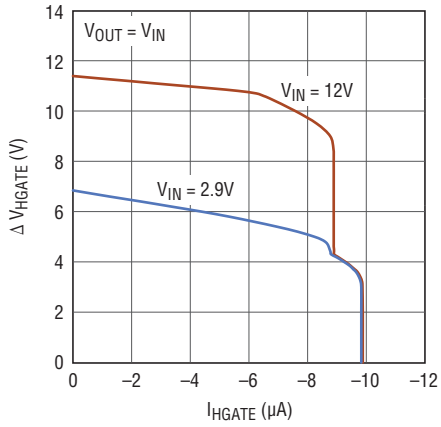
OUT Current vs Voltage



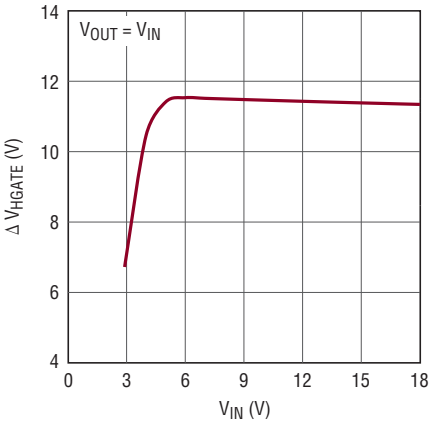
INTVCC Load Regulation



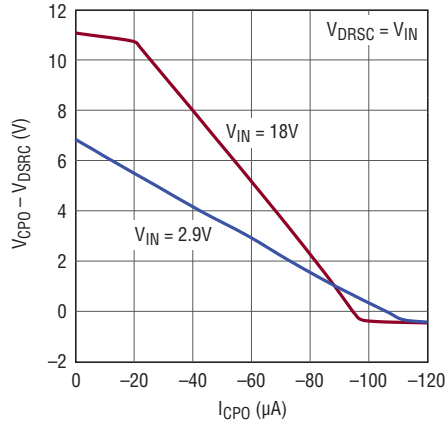
Hot Swap Gate Voltage vs Current



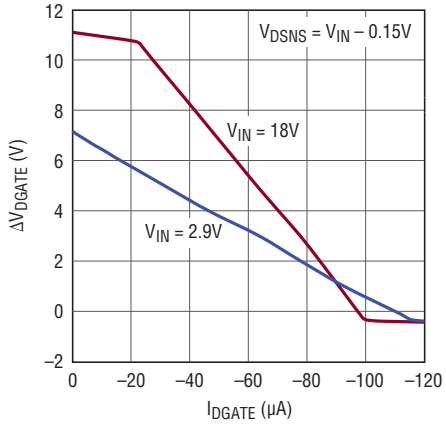
Hot Swap Gate Voltage vs IN Voltage



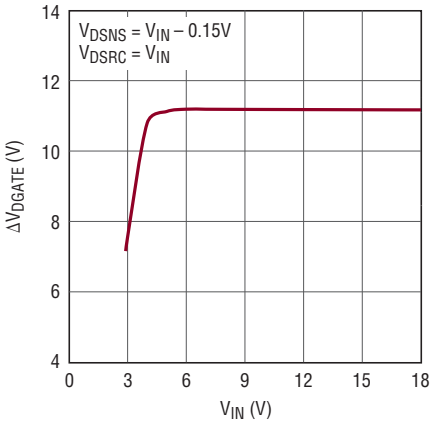
CPO Voltage vs Current



Diode Gate Voltage vs Current

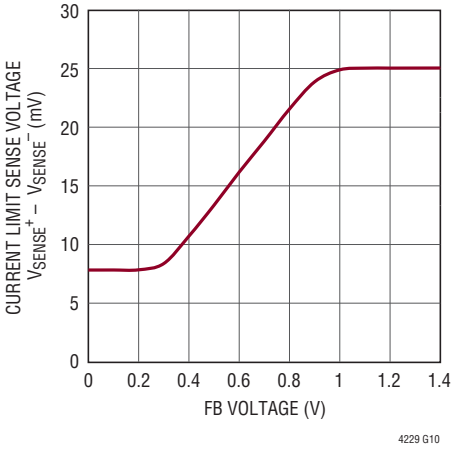


Diode Gate Voltage vs IN Voltage

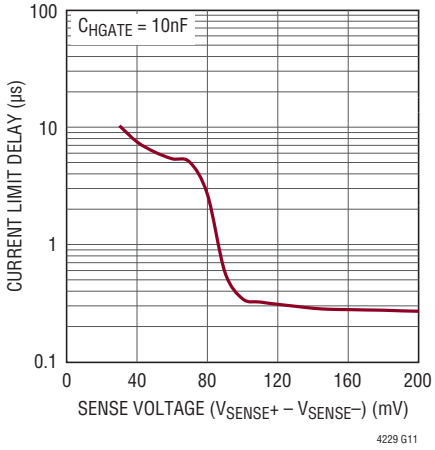


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{IN} = 12V, unless otherwise noted.

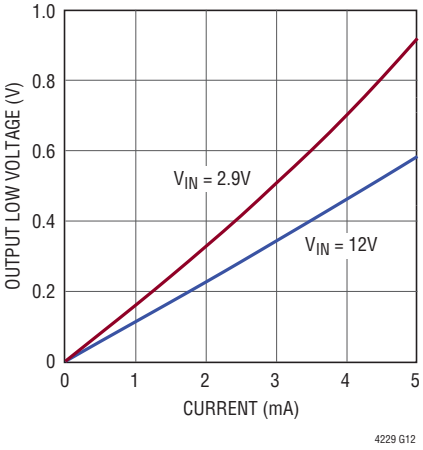
Current Limit Threshold Foldback



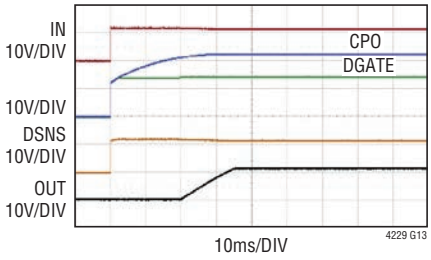
Current Limit Delay vs Sense Voltage



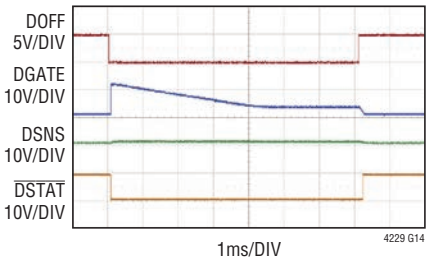
PWRGD, FAULT, DSTAT, DFLT Output Low Voltage vs Current



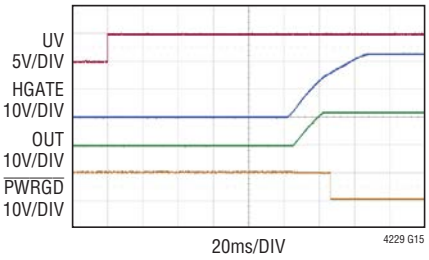
Ideal Diode Start-Up Waveform on IN Power-Up



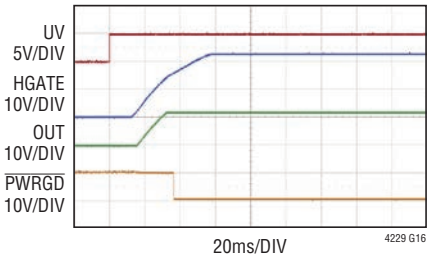
Ideal Diode Turn-On and Turn-Off Waveform



100ms HGATE Start-Up Delay with DTMR Pin Connected to $INTV_{CC}$



Adjustable HGATE Start-Up Delay with 0.1µF Capacitor at DTMR Pin



PIN FUNCTIONS

CPO: Charge Pump Output. Connect a capacitor from CPO to the DSRC pin. The value of this capacitor is approximately 10× the gate capacitance (C_{ISS}) of the external MOSFET for ideal diode control. The charge stored on this capacitor is used to pull up the ideal diode MOSFET gate during a fast turn-on. Leave this pin open if fast ideal diode turn-on is not needed.

DCFG: Logic Input. Configures status indication of $\overline{DFLT}$ output depending on diode sense (DSNS) connection. Connect this pin to GND when the diode sense is only across the ideal diode MOSFET. Connect to $INTV_{CC}$ when the diode sense is across the ideal diode MOSFET, sense resistor and Hot Swap MOSFET.

$\overline{DFLT}$: Diode MOSFET Fault Status Output. This pin is pulled low by an internal switch when the voltage between IN and DSNS exceeds 250mV. The external ideal diode MOSFET is not turned off during the fault. An internal 10µA current source pulls this pin up to a diode below $INTV_{CC}$. It may be pulled above $INTV_{CC}$ using an external pull-up. Leave open if unused.

DGATE: Ideal Diode MOSFET Gate Drive Output. Connect this pin to the gate of an external N-channel MOSFET for ideal diode control. An internal clamp limits the gate voltage to 12V above and a diode voltage below DSRC. During fast turn-on, a 1.5A pull-up charges DGATE from CPO. During fast turn-off, a 1.5A pull-down discharges DGATE to DSRC.

DOFF: Control Input. A rising edge above 1.235V turns off the external ideal diode MOSFET and a falling edge below 1.215V allows the MOSFET to be turned on.

DSNS: Ideal Diode Output Voltage Sense Input. Connect this pin to the output of either the ideal diode MOSFET or the Hot Swap MOSFET for diode output sense. The voltage sensed at this pin is used to control DGATE for forward voltage regulation and reverse turn-off.

DSRC: Ideal Diode's MOSFET Gate Drive Return. Connect this pin to the source of the external N-channel MOSFET switch. The gate fast pull-down current returns through this pin when DGATE is discharged.

$\overline{DSTAT}$: Diode MOSFET Status Output. Open drain output that pulls low when the MOSFET gate drive voltage between DGATE and DSRC exceeds 0.7V. Otherwise it goes high impedance and requires an external pull-up resistor to a positive supply as there is no internal 10µA current source at this pin. Leave open if unused.

DTMR: Debounce Timer Capacitor Terminal. Connect this pin to either $INTV_{CC}$ for fixed 100ms delay or an external capacitor to ground for adjustable start-up delay (123ms/µF) when $\overline{EN}$ toggles low.

$\overline{EN}$: Enable Input. Ground this pin to enable Hot Swap control. If this pin is pulled high, the MOSFET is not allowed to turn on. A 10µA current source pulls this pin up to a diode below $INTV_{CC}$. Upon $\overline{EN}$ going low when UV is high and OV is low, there is a start-up delay for debounce as configured at the DTMR pin, after which the fault is cleared.

Exposed Pad (UFD Package): The exposed pad may be left open or connected to device ground.

$\overline{FAULT}$: Overcurrent Fault Status Output. Output that pulls low when the fault filter times out during an overcurrent fault. Otherwise it is pulled high by a 10µA current source to a diode below $INTV_{CC}$. It may be pulled above $INTV_{CC}$ using an external pull-up. Leave open if unused.

FB: Foldback and Power Good Comparator Input. Connect this pin to an external resistive divider from OUT. If the voltage falls below 1.215V, the $\overline{PWRGD}$ pin pulls high to indicate the power is bad. If the voltage falls below 0.9V, the output power is considered bad and the current limit is reduced. Tie to $INTV_{CC}$ to disable foldback.

FTMR: Fault Timer Capacitor Terminal. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the external Hot Swap MOSFET is turned off. The duration of the off time is 11s/µF, resulting in a 0.1% duty cycle.

GND: Device Ground.

PIN FUNCTIONS

HGATE: Hot Swap MOSFET Gate Drive Output. Connect this pin to the gate of the external N-channel MOSFET for Hot Swap control. An internal 10µA current source charges the MOSFET gate. An internal clamp limits the gate voltage to 12V above and a diode voltage below OUT. During an undervoltage or overvoltage generated turn-off, a 2mA pull-down discharges HGATE to ground. During an output short or $INTV_{CC}$ undervoltage lockout, a fast 200mA pull-down discharges HGATE to OUT.

IN: Positive Supply Input. The 5V $INTV_{CC}$ supply is generated from IN, $SENSE^+$ and OUT via an internal diode-OR. The voltage sensed at this pin is used to control DGATE.

$INTV_{CC}$: Internal 5V Supply Decoupling Output. This pin must have a 0.1µF or larger capacitor. An external load of less than 500µA can be connected at this pin. An undervoltage lockout threshold of 2.2V will turn off both MOSFETs.

OUT: Hot Swap's MOSFET Gate Drive Return. Connect this pin to the output side of the external MOSFET. The gate fast pull-down current returns through this pin when HGATE is discharged.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider from IN or $SENSE^+$ to monitor the supply overvoltage condition. If the voltage at this pin rises above 1.235V, an overvoltage fault is detected and the Hot Swap MOSFET turns off. Tie to GND if unused.

$\overline{PWRGD}$: Power Status Output. Output that pulls low when the FB pin rises above 1.235V and the MOSFET gate drive between HGATE and OUT exceeds 4.2V. Otherwise it is pulled high by a 10µA current source to a diode below $INTV_{CC}$. It may be pulled above $INTV_{CC}$ using an external pull-up. Leave open if unused.

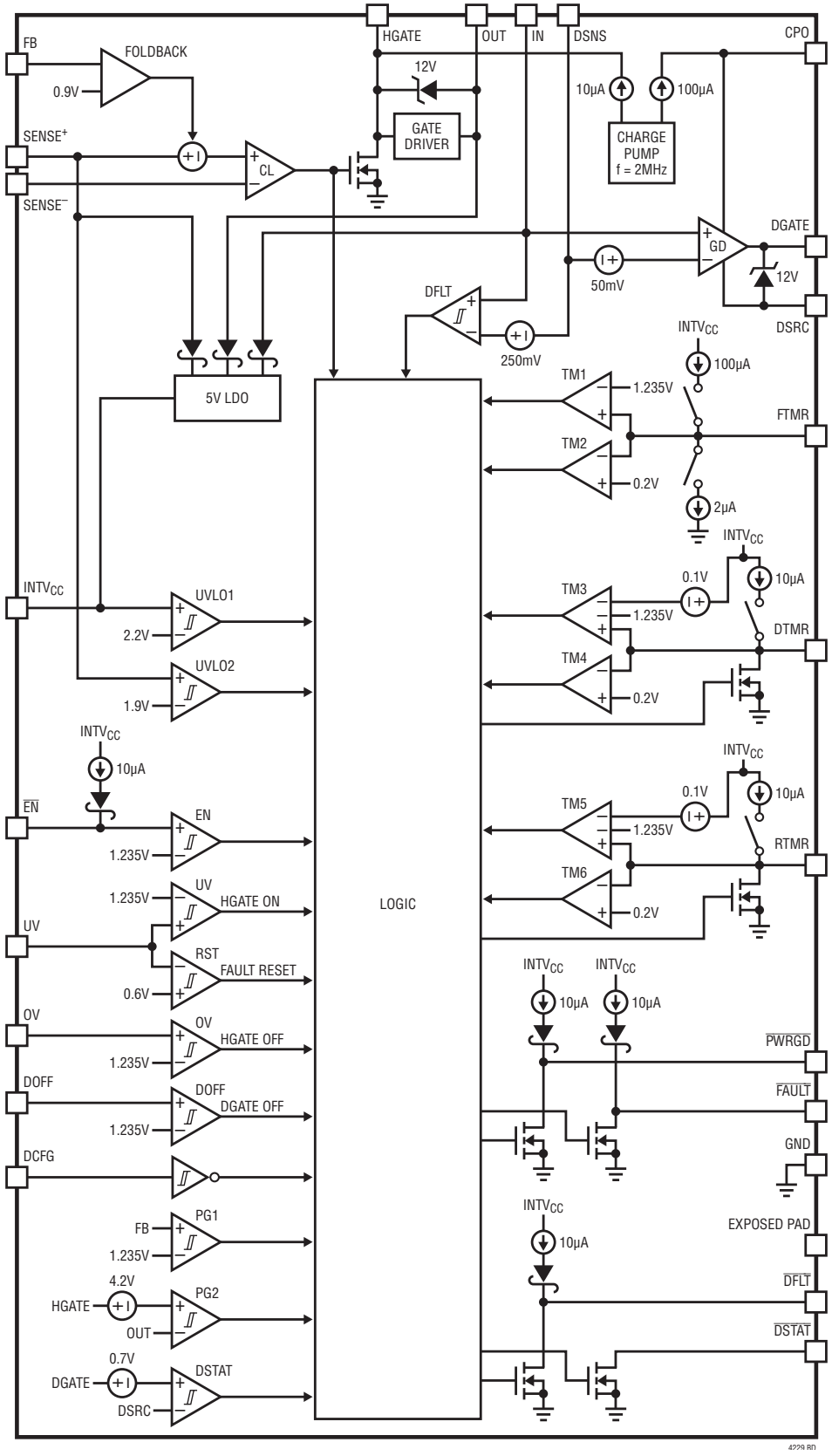
RTMR: Auto-Retry Timer Capacitor Terminal. Connect this pin to $INTV_{CC}$ for fault latch off. Leave open for auto-retry with 0.1% duty cycle after a fault. Connect an external capacitor to extend the Hot Swap MOSFET off time set by the FTMR pin capacitor to less than 0.1% auto-retry duty cycle after a fault.

$SENSE^+$: Positive Current Sense Input. Connect this pin to the input of the current sense resistor. The voltage sensed at this pin is used for monitoring the current limit. This pin has an undervoltage lockout threshold of 1.9V that will turn off the Hot Swap MOSFET.

$SENSE^-$: Negative Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls HGATE to limit the voltage between $SENSE^+$ and $SENSE^-$ to 25mV or less depending on the voltage at the FB pin.

UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider from IN or $SENSE^+$ to monitor the supply undervoltage condition. If the voltage at this pin falls below 1.155V, an undervoltage fault is detected and the Hot Swap MOSFET turns off. Pulling the UV pin below 0.6V resets the fault latch after an overcurrent fault. Tie to $INTV_{CC}$ if unused.

BLOCK DIAGRAM



OPERATION

The LTC4229 functions as an ideal diode with inrush current limiting and overcurrent protection. It controls two external N-channel MOSFETs on a supply path, a diode MOSFET (M_D) and a Hot Swap MOSFET (M_H).

When the LTC4229 is first powered up, the gates of the external MOSFETs are held low, keeping them off. The gate drive amplifier (GD) monitors the voltage between the IN and DSNS pins and drives the DGATE pin. The amplifier quickly pulls up the DGATE pin, turning on the MOSFET for ideal diode control, when it senses a large forward voltage drop. An external capacitor connected between the CPO and DSRC pins provides the charge needed to quickly turn on the ideal diode MOSFET. An internal charge pump charges up this capacitor at device power-up. The DGATE pin sources current from the CPO pin and sinks current into the DSRC and GND pins. When the DGATE to DSRC voltage exceeds 0.7V, the $\overline{DSTAT}$ pin pulls low to indicate that the ideal diode MOSFET is turned on.

If the LTC4229 is out of undervoltage and overvoltage conditions, pulling the $\overline{EN}$ pin low initiates a debounce timing cycle that can be a fixed 100ms or adjustable delay as configured at the DTMR pin. After this timing cycle, a 10µA current source from the charge pump ramps up the HGATE pin. When the Hot Swap MOSFET turns on, the inrush current is limited at a level set by an external sense resistor (R_S) connected between the $SENSE^+$ and $SENSE^-$ pins. An active current limit amplifier (CL) servos the gate of the MOSFET to 25mV or less across the current sense resistor depending on the voltage at the FB pin. Inrush current can be further reduced, if desired, by adding a capacitor from HGATE to GND. When FB voltage rises above 1.235V and the MOSFET's gate drive (HGATE to OUT voltage) exceeds 4.2V, the $\overline{PWRGD}$ pin pulls low.

When both of the MOSFETs are turned on, the gate drive amplifier controls DGATE to servo the forward voltage drop ($V_{IN} – V_{DSNS}$) across the sense resistor and the two MOSFETs to 50mV if DSNS and OUT pins are connected together. If the load current causes more than 50mV of voltage drop, the DGATE voltage rises to enhance the MOSFET used for ideal diode control. For large output currents, the ideal diode MOSFET is driven fully on and the voltage drop across the MOSFETs is equal to the sum of the $I_{LOAD} • R_{DS(ON)}$ of the two MOSFETs in series. However, if DSNS and $SENSE^+$ pins are connected together, the gate drive amplifier attempts to regulate 50mV across the ideal diode MOSFET only regardless of the $I_{LOAD} • R_{DS(ON)}$ drop across the Hot Swap MOSFET.

In the case of an input supply short circuit when the MOSFETs are conducting, a large reverse current starts flowing from the load towards the input. The gate drive amplifier detects this failure condition and turns off the ideal diode MOSFET by pulling down the DGATE pin.

In the case where an overcurrent fault occurs on the supply output, the current is limited with foldback. After a delay set by 100µA charging the FTMR pin capacitor, the fault filter times out and pulls the HGATE pin low, turning off the Hot Swap MOSFET. The $\overline{FAULT}$ pin is also latched low. At this point, the DGATE pin continues to pull high and keeps the ideal diode MOSFET on.

Internal clamps limit both the DGATE to DSRC and CPO to DSRC voltages to 12V. The same clamps also limit the CPO and DGATE pins to a diode voltage below the DSRC pin. Another internal clamp limits the HGATE to OUT voltage to 12V and also clamps the HGATE pin to a diode voltage below the OUT pin.

Power to the LTC4229 is supplied from either the IN, $SENSE^+$ or OUT pins, through an internal diode-OR circuit to a low dropout regulator (LDO). That LDO generates a 5V supply at the $INTV_{CC}$ pin and powers the LTC4229's internal low voltage circuitry

APPLICATIONS INFORMATION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. Power ORing diodes are commonly used to connect these supplies at the point of load at the expense of power loss due to significant diode forward voltage drop. The LTC4229 minimizes this power loss by using an external N-channel MOSFET as the pass element, allowing for a low voltage drop from the supply to the load when the MOSFET is turned on. When an input source voltage drops below the output common supply voltage, the appropriate MOSFET is turned off, thereby matching the function and performance of an ideal diode. By adding a current sense resistor in between the two external MOSFETs that are separately controlled, the LTC4229 enhances the ideal diode performance with inrush current limiting and overcurrent protection (see Figure 1). This allows the board to be safely inserted and removed from a live backplane without damaging the connector.

Internal V_{CC} Supply

The LTC4229 operates with an input supply from 2.9V to 18V. The power supply to the device is internally regulated at 5V by a low dropout regulator (LDO) with an output at the $INTV_{CC}$ pin. An internal diode-OR circuit selects the highest of the supplies at the IN, $SENSE^+$ and OUT pins to power the device through the LDO. The diode-OR scheme permits the device's power to be kept alive by the OUT voltage when the IN and $SENSE^+$ supplies have collapsed or shut off.

An undervoltage lockout circuit prevents all of the MOSFETs from turning on until the $INTV_{CC}$ voltage exceeds 2.2V. A 0.1µF capacitor is recommended between the $INTV_{CC}$ and GND pins, close to the device for bypassing. No external supply should be connected at the $INTV_{CC}$ pin so as not to affect the LDO's operation. A small external load of less than 500µA can be connected at the $INTV_{CC}$ pin.

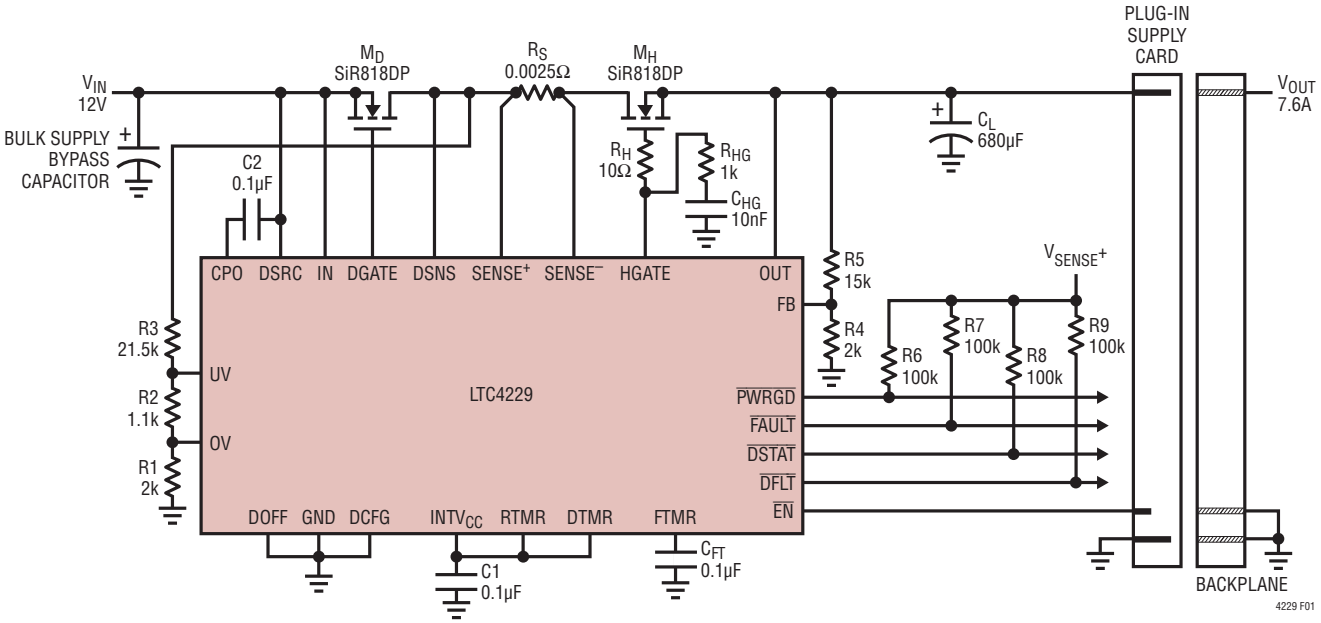


Figure 1. Plug-In Card Supplying 12V Power to Backplane

APPLICATIONS INFORMATION

DSNS and DCFG Configuration

The LTC4229 features the DSNS and DCFG pins that allow a diode-OR circuit output to be configured either at the SENSE+ or OUT pin (see Figure 2). If DSNS is connected to SENSE+, the forward voltage is sensed across the ideal diode MOSFET M_D. As the Hot Swap MOSFET M_H is not part of the diode sensing, connect the DCFG pin to GND so that the Hot Swap MOSFET gate overdrive will not be considered as a criterion for the ideal diode MOSFET fault status indication at the $\overline{DFLT}$ pin. If DSNS is connected to OUT, the forward voltage is sensed across the ideal diode MOSFET, sense resistor and Hot Swap MOSFET. Since the Hot Swap MOSFET is part of the diode sensing and is turned off at start-up, the $\overline{DFLT}$ pin may be falsely pulled low to indicate an open ideal diode MOSFET fault when the forward voltage exceeds 250mV. For such a configuration, connect DCFG pin to $INTV_{CC}$ so that the Hot Swap MOSFET gate overdrive condition will be considered to avoid false indication of the $\overline{DFLT}$ output status.

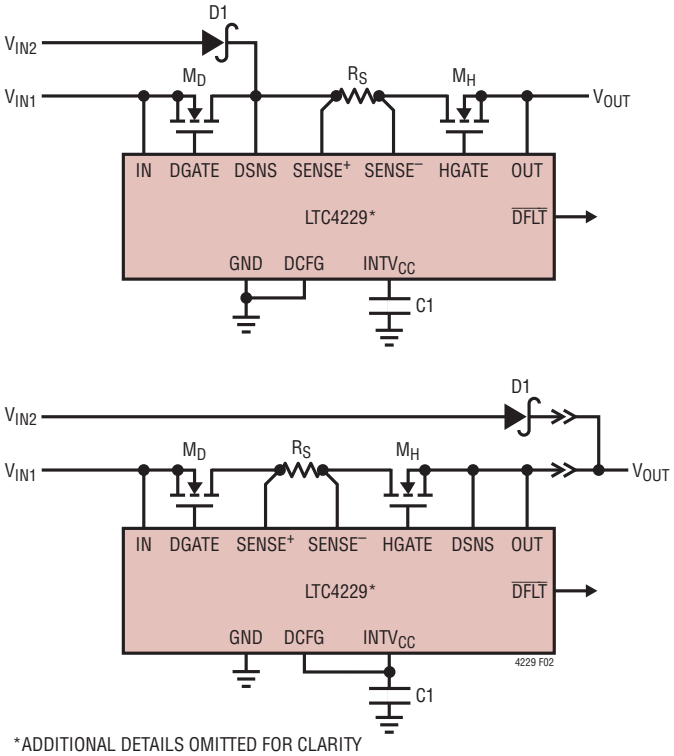


Figure 2. DSNS and DCFG Configurations

Turn-On Sequence

The board power supply at the OUT pin is controlled with two external N-channel MOSFETs (M_D, M_H) in Figure 1. The MOSFET M_D on the supply side functions as an ideal diode, while M_H on the load side acts as a Hot Swap controlling the power supplied to the output load. The sense resistor R_S monitors the load current for overcurrent detection. The HGATE capacitor C_{HG} controls the gate slew rate to limit the inrush current. Resistor R_{HG} with C_{HG} compensates the current control loop, while R_H prevents high frequency oscillations in the Hot Swap MOSFET.

During a normal power-up, the ideal diode MOSFET turns on first. As soon as the internally generated supply, $INTV_{CC}$, rises above its 2.2V undervoltage lockout threshold, the internal charge pump is allowed to charge up the CPO pin. The gate drive amplifier controls the gate of the ideal diode MOSFET, to servo its forward voltage drop between the IN and DSNS pins to 50mV. If the forward drop is large, the gate drive amplifier will cause DGATE to be pulled up to the CPO pin voltage and drive the MOSFET gate fully on.

Before the Hot Swap MOSFET can be turned on, the UV and OV pin voltage requirements should be met and $\overline{EN}$ must remain low for a debounce cycle as configured at the DTMR pin, to ensure that any contact bounces during the insertion have ceased. At the end of the debounce cycle, the internal fault latch is cleared. The Hot Swap MOSFET is then allowed to turn on by charging up HGATE with a 10µA current source from the charge pump. The voltage at the HGATE pin rises with a slope equal to $10\mu A/C_{HG}$ and the supply inrush current flowing into the load capacitor C_L is limited to:

$$I_{INRUSH} = \frac{C_L}{C_{HG}} \bullet 10\mu A$$

The OUT voltage follows the HGATE voltage when the Hot Swap MOSFET turns on. If the voltage across the current sense resistor R_S becomes too high based on the FB pin voltage, the inrush current will be limited by the internal current limiting circuitry. Once the MOSFET gate overdrive exceeds 4.2V and the FB pin voltage is above 1.235V, the $\overline{PWRGD}$ pin pulls low to indicate that the power is good.

APPLICATIONS INFORMATION

Once OUT reaches the input supply voltage, HGATE continues to ramp up. An internal 12V clamp limits the HGATE voltage above OUT.

Turn-Off Sequence

The external MOSFETs can be turned off by a variety of conditions. A normal turn-off for the Hot Swap MOSFET is initiated by pulling the UV pin below its 1.155V threshold (80mV UV pin hysteresis), or pulling the $\overline{EN}$ pin above its 1.235V threshold. Additionally, an overvoltage fault or overcurrent fault that exceeds the fault filter time-out also turns off the Hot Swap MOSFET. Normally, the LTC4229 turns off the MOSFET by pulling the HGATE pin to ground with a 2mA current sink.

All of the MOSFETs turn off when $INTV_{CC}$ falls below its undervoltage lockout threshold (2.2V). The DGATE pin is pulled down with a 100µA current to one diode voltage below the DSRC pin, while the HGATE pin is pulled down to the OUT pin by a 200mA current.

The gate drive amplifier controls the ideal diode MOSFET to prevent reverse current when the input supply falls below DSNS (connects to either $SENSE^+$ or OUT). If the input supply collapses quickly, the gate drive amplifier turns off the ideal diode MOSFET with a fast pull-down circuit. If the input supply falls at a more modest rate, the gate drive amplifier controls the MOSFET to maintain DSNS at 50mV below IN.

Board Presence Detect with $\overline{EN}$

After the input has settled to within the OV and UV limits, and the $\overline{EN}$ pin goes low indicating a board presence, the LTC4229 initiates a timing cycle as configured at the DTMR pin for contact debounce. It defaults to internal 100ms delay if DTMR is tied to $INTV_{CC}$. If an external capacitor C_{DT} is connected from the DTMR pin to GND, the delay is given by charging the capacitor to 1.235V with a 10µA current. Thereafter, the capacitor is discharged to ground by a 5mA current. For a given debounce delay, the equation for setting the external capacitor C_{DT} value is:

$$C_{DT} = t_{DB} \bullet 0.0081\ [\mu F/ms]$$

Upon board insertion, any bounces on the $\overline{EN}$ pin restart the timing cycle. When the debounce timing cycle is done, the internal fault latch is cleared. If the $\overline{EN}$ pin remains low at the end of the timing cycle, HGATE is charged up with a 10µA current source to turn on the Hot Swap MOSFET.

If the $\overline{EN}$ pin goes high, indicating a board removal, the HGATE pin is pulled low with a 2mA current sink after a 20µs delay, turning off the Hot Swap MOSFET without clearing any latched fault.

Overcurrent Fault

The LTC4229 features an adjustable current limit with foldback that protects the external MOSFET against short circuits or excessive load current. The voltage across the external sense resistor R_S is monitored by an active current limit amplifier. The amplifier controls the gate of the Hot Swap MOSFET to reduce the load current as a function of the output voltage sensed by the FB pin during active current limit. A graph in the Typical Performance Characteristics shows the current limit sense voltage versus FB voltage.

An overcurrent fault occurs when the output has been in current limit for longer than the fault filter delay configured at the FTMR pin. Current limiting begins when the sense voltage between the $SENSE^+$ and $SENSE^-$ pins reaches 8.3mV to 25mV depending on the FB pin voltage. The gate of the Hot Swap MOSFET is brought under control by the current limit amplifier and the output current is regulated to limit the sense voltage to less than 25mV. At this point, the fault filter starts the timeout with a 100µA current charging the FTMR pin capacitor. If the FTMR pin voltage exceeds its 1.235V threshold, the external MOSFET turns off with HGATE pulled to ground by 2mA, and $\overline{FAULT}$ pulls low.

After the Hot Swap MOSFET turns off, the FTMR pin capacitor is discharged with a 2µA pull-down current until its threshold reaches 0.2V. This is followed by a cool-off period of 14 timing cycles as described in the FTMR Pin Functions. Figure 3 shows an overcurrent fault on the 12V output.

APPLICATIONS INFORMATION

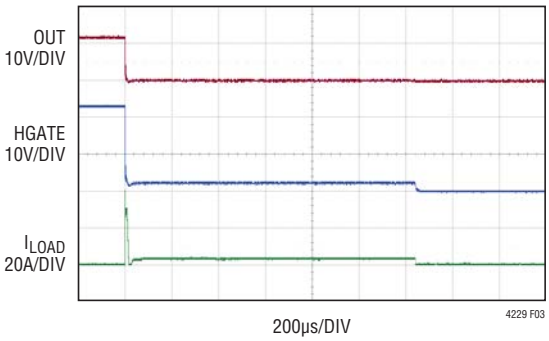


Figure 3. Overcurrent Fault on 12V Output

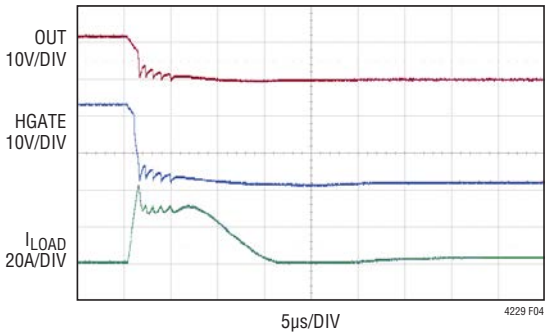


Figure 4. Severe Short-Circuit on 12V Output

In the event of a severe short-circuit fault on the 12V output as shown in Figure 4, the output current can surge to tens of amperes. The LTC4229 responds within 1µs to bring the current under control by pulling the HGATE to OUT voltage down to zero volts. Almost immediately, the gate of the Hot Swap MOSFET recovers rapidly due to the charge stored in the R_{HG} and C_{HG} network, and current is actively limited until the fault filter times out. Due to parasitic supply lead inductance, an input supply without any bypass capacitor may collapse during the high current surge and then spike upwards when the current is interrupted. Figure 13 shows the input supply transient suppressors consisting of Z1, R_{SNUB} and C_{SNUB} for the supply if there is no input capacitance.

FTMR Pin Functions

An external capacitor C_{FT} connected from the FTMR pin to GND serves as fault filtering when the supply output is in active current limit. When the voltage across the sense resistor exceeds the foldback current limit threshold (from 25mV to 8.3mV), FTMR pulls up with 100µA. Otherwise, it pulls down with 2µA. The fault filter times out when the 1.235V FTMR threshold is exceeded, causing the $\overline{FAULT}$ pin to pull low. For a given fault filter delay, the equation for setting the external capacitor C_{FT} value is:

$$C_{FT} = t_{FF} \bullet 0.083\ [\mu F/ms]$$

After the fault filter timeout, the FTMR pin capacitor pulls down with 2µA from the 1.235V FTMR threshold until it reaches 0.2V. Then, it completes 14 cooling cycles consisting of the FTMR pin capacitor charging to 1.235V with a 100µA current and discharging to 0.2V with a 2µA current. At that point, the HGATE pin voltage is allowed to start up if the fault has been cleared as described in the Resetting Fault section. When the latched fault is cleared during the cool-off period, the $\overline{FAULT}$ pin pulls high. The total cool-off time for the MOSFET after an overcurrent fault is:

$$t_{COOL} = C_{FT} \bullet 11\ [s/\mu F]$$

After the cool-off period, the HGATE pin is only allowed to pull up if the fault has been cleared for the latchoff configuration. For the auto-retry configuration, the latched fault is cleared automatically following the extended cool-off period and the HGATE pin voltage is allowed to restart.

Resetting Fault

For the latchoff configuration with the RTMR pin tied to $INTV_{CC}$, an overcurrent fault is latched after fault filter times out, and the $\overline{FAULT}$ pin is asserted low. To reset a latched fault and restart the output, pull the UV pin below 0.6V for more than 100µs and then high above 1.235V. The fault latch resets and the $\overline{FAULT}$ pin deasserts on the falling edge of the UV pin. When UV goes high again, a debounce timing cycle is initiated before the HGATE pin voltage restarts. Toggling the $\overline{EN}$ pin high and then low again also resets a fault, but the $\overline{FAULT}$ pin pulls high at the end of the debounce cycle before the HGATE pin voltage starts up. Bringing the supply below the $INTV_{CC}$ undervoltage lockout threshold (2.2V) shuts off all the MOSFETs and resets the fault latch. A debounce cycle is initiated before a normal start-up when the supply is restored above the $INTV_{CC}$ UVLO threshold.

APPLICATIONS INFORMATION

Auto-Retry After a Fault

For the auto-retry configuration, if the RTMR pin is left open, the latched fault is reset automatically at the end of the cool-off period as described in the FTMR Pin Functions section. In this case, the auto-retry duty cycle is equal to 0.1%, irrespective of C_{FT}. If an external capacitor C_{RT} is connected from the RTMR pin to GND, the cool-off time can be further extended by another 15 cooling cycles consisting of the RTMR pin capacitor charging to 1.235V with a 10µA current and discharging to 0.2V with a 5mA current. For a given additional cool-off time for the MOSFET, the equation for setting the external capacitor C_{RT} value is:

$$C_{RT} = t_{XCOOL} \bullet 0.54\ [\mu F/s]$$

At the end of the extended cool-off period, the fault latch is cleared and $\overline{FAULT}$ pulls high. The HGATE pin voltage is allowed to start up and turn on the Hot Swap MOSFET. If the output short persists, the supply powers up into a short with active current limiting until the fault filter times out and $\overline{FAULT}$ again pulls low. A new extended cool-off cycle begins with FTMR ramping down with a 2µA current. The whole process repeats itself until the output short is removed.

The auto-retry duty cycle is given by:

$$\text{Duty Cycle} = \frac{t_{FF}}{t_{COOL} + t_{XCOOL}} \bullet 100\%$$

For example, if C_{FT} = 0.1µF, C_{RT} = 1µF and t_{FF} = 1.2ms, the auto-retry duty cycle is calculated as 0.04%. Figure 5 shows an auto-retry sequence after an overcurrent fault.

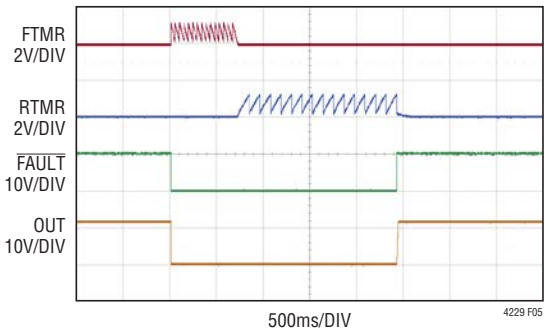


Figure 5. Auto-Retry Sequence After a Fault

Monitor Overvoltage and Undervoltage Faults

Both the OV and UV pins function as an input supply monitor while UV pin also functions as a turn-on control. A resistive divider connected between the input supply (IN or SENSE+) and GND at the OV and UV pins monitors the supply for overvoltage and undervoltage conditions. The overvoltage and undervoltage thresholds are set by proper selection of the resistors at their respective OV and UV rising threshold voltage (1.235V).

For Figure 1, if R1 = 2k, R2 = 1.1k and R3 = 21.5k, the input supply overvoltage and undervoltage thresholds are set to 15.2V and 9.8V respectively.

An overvoltage fault occurs if the input supply rises above its overvoltage threshold. The Hot Swap MOSFET is turned off by a 2mA pull-down from HGATE to ground. If the input supply subsequently falls below its overvoltage threshold, the Hot Swap MOSFET is allowed to turn on immediately. The OV pin voltage is 1.215V when falling out of overvoltage.

An undervoltage fault occurs if the input supply falls below its undervoltage threshold. If the UV pin voltage falls below 1.155V but remains above 0.6V, the Hot Swap MOSFET is turned off by a 2mA pull-down from HGATE to ground. The Hot Swap MOSFET turns back on instantly without the debounce cycle when the input supply rises above its undervoltage threshold. However, if the UV pin voltage drops below 0.6V, it turns off the Hot Swap MOSFET and clears the fault latch. The Hot Swap MOSFET turns back on only after a debounce cycle when the input supply is restored above its undervoltage threshold.

During the overvoltage and undervoltage fault conditions, $\overline{FAULT}$ will not be pulled low but $\overline{PWRGD}$ will be pulled high as HGATE is pulled low. The ideal diode function controlled by the ideal diode MOSFET is not affected by the OV and UV fault conditions.

Power Good Monitor

Internal circuitry monitors the MOSFET gate overdrive between the HGATE and OUT pins. Also, the FB pin that connects to OUT through a resistive divider is used to determine a power good condition. The power good

APPLICATIONS INFORMATION

comparator drives high when the FB pin rises above 1.235V, and drives low when FB falls below 1.215V. The power good status for the input supply is reported via an open-drain output, $\overline{PWRGD}$. It is normally pulled high by an external pull-up resistor or the internal 10µA pull-up.

The $\overline{PWRGD}$ pin pulls low when the FB power good comparator is high and the HGATE drive exceeds 4.2V. The $\overline{PWRGD}$ pin goes high when the HGATE is turned off by the UV, OV or $\overline{EN}$ pins, or when the FB power good comparator drives low, or when $INTV_{CC}$ enters undervoltage lockout.

CPO and DGATE Start-Up

In applications where a single ideal diode MOSFET is placed on the supply side, CPO is initially pulled up to a diode below the DSRC pin when first powered up (see Figure 13). In back-to-back MOSFETs applications, CPO starts off at 0V, since DSRC is near ground (see Figure 14). CPO starts ramping up 7µs after $INTV_{CC}$ clears its undervoltage lockout level. Another 40µs later, DGATE also starts ramping up with CPO. The CPO ramp rate is determined by the CPO pull-up current into the combined CPO and DGATE pin capacitances. An internal clamp limits the CPO pin voltage to 12V above the DSRC pin, while the final DGATE pin voltage is determined by the gate drive amplifier. An internal 12V clamp limits the DGATE pin voltage above DSRC.

CPO Capacitor Selection

The recommended value of the capacitor between the CPO and DSRC pins is approximately 10× the input capacitance C_{ISS} of the ideal diode MOSFET. A larger capacitor takes a correspondingly longer time to charge up by the internal charge pump. A smaller capacitor suffers more voltage drop during a fast gate turn-on event as it shares charge with the MOSFET gate capacitance.

MOSFET Selection

The LTC4229 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are on-resistance $R_{DS(ON)}$, the maximum drain-source voltage BV_{DSS} and the threshold voltage.

The gate drive for the ideal diode and Hot Swap MOSFET is guaranteed to be greater than 5V when the supply voltage at IN is between 2.9V and 7V. When the supply voltage at IN is greater than 7V, the gate drive is guaranteed to be greater than 10V. The gate drive is limited to 14V. An external Zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 14V.

The maximum allowable drain-source voltage BV_{DSS} must be higher than the supply voltage including supply transients as the full supply voltage can appear across the MOSFET. If an input or output is connected to ground, the full supply voltage will appear across the MOSFET. The $R_{DS(ON)}$ should be small enough to conduct the maximum load current, and also stay within the MOSFET's power rating.

Supply Transient Protection

When the capacitances at the input and output are very small, rapid changes in current during input or output short-circuit events can cause transients that exceed the 24V absolute maximum ratings of the IN and OUT pins. To minimize such spikes, use wider traces or heavier trace plating to reduce the power trace inductance. Also, bypass locally with a 10µF electrolytic and 0.1µF ceramic, or alternatively clamp the input with a transient voltage suppressor Z1. A 100Ω, 0.1µF snubber damps the response and eliminates ringing (see Figure 13).

Design Example

As a design example for selecting components, consider a 12V system with a 7.6A maximum load current for the input supply (see Figure 1).

First, select the appropriate value of the current sense resistor R_S for the 12V supply. Calculate the sense resistor value based on the maximum load current $I_{LOAD(MAX)}$ and the lower limit for the current limit sense voltage threshold $\Delta V_{SENSE(TH)(MIN)}$.

$$R_S = \frac{\Delta V_{SENSE(TH)(MIN)}}{I_{LOAD(MAX)}} = \frac{22.5mV}{7.6A} = 2.9m\Omega$$

Choose a 2.5mΩ sense resistor with a 1% tolerance.

Next, calculate the $R_{DS(ON)}$ of the ideal diode MOSFET to achieve the desired forward drop at maximum load.

APPLICATIONS INFORMATION

Assuming a forward drop, ΔV_{FWD} of 50mV across the ideal diode MOSFET:

$$R_{DS(ON)} \leq \frac{\Delta V_{FWD}}{I_{LOAD(MAX)}} = \frac{50mV}{7.6A} = 6.5m\Omega$$

The SiR818DP offers a good choice with a maximum $R_{DS(ON)}$ of 2.8mΩ at V_{GS} = 10V. The input capacitance C_{ISS} of the SiR818DP is about 3660pF. Slightly exceeding the 10× recommendation, a 0.1µF capacitor is selected for C2 at the CPO pin.

Next, verify that the thermal ratings of the selected Hot Swap MOSFET are not exceeded during power-up or an overcurrent fault.

Assuming the MOSFET dissipates power due to inrush current charging the load capacitor C_L at power-up, the energy dissipated in the MOSFET is the same as the energy stored in the load capacitor, and is given by:

$$E_{CL} = \frac{1}{2} \bullet C_L \bullet V_{IN}^2$$

For C_L = 680µF, the time it takes to charge up C_L is calculated as:

$$t_{CHARGE} = \frac{C_L \bullet V_{IN}}{I_{INRUSH}} = \frac{680\mu F \bullet 12V}{1A} = 8ms$$

The inrush current is set to 1A by adding capacitance C_{HG} at the gate of the Hot Swap MOSFET.

$$C_{HG} = \frac{C_L \bullet I_{HGATE(UP)}}{I_{INRUSH}} = \frac{680\mu F \bullet 10\mu A}{1A} = 6.8nF$$

Choose a practical value of 10nF for C_{HG}.

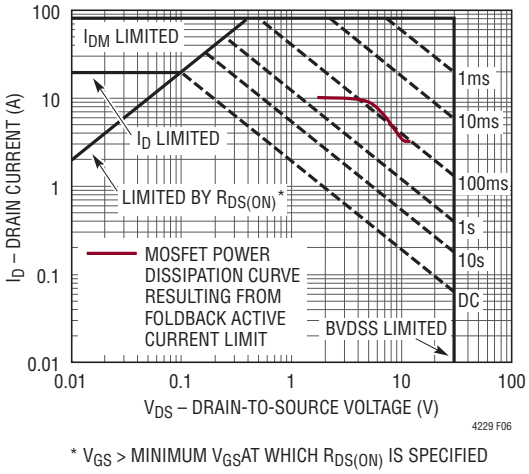
The average power dissipated in the MOSFET is calculated as:

$$P_{AVG} = \frac{E_{CL}}{t_{CHARGE}} = \frac{1}{2} \bullet \frac{680\mu F \bullet (12V)^2}{8ms} = 6W$$

The MOSFET selected must be able to tolerate 6W for 8ms during power-up. The SOA curves of the SiR818DP provide 45W (1.5A at 30V) for 100ms. This is sufficient to satisfy the requirement. The increase in junction temperature due to the power dissipated in the MOSFET is $\Delta T = P_{AVG} \bullet Zth_{JC}$ where Zth_{JC} is the junction-to-case thermal impedance. Under this condition, the SiR818DP data sheet indicates that the junction temperature will increase by 3°C using Zth_{JC} = 0.5°C/W (single pulse).

Next, the power dissipated in the MOSFET during an overcurrent fault must be safely limited. The fault timer capacitor (C_{FT}) is used to prevent power dissipation in the MOSFET from exceeding the SOA rating during active current limit. A good way to determine a suitable value for C_{FT} is to superimpose the foldback current limit profile shown in the Typical Performance Characteristics on the MOSFET data sheet's SOA curves.

For the SiR818DP MOSFET, this exercise yields the plot in Figure 6.



* V_{GS} > MINIMUM V_{GS} AT WHICH $R_{DS(ON)}$ IS SPECIFIED

Figure 6. SiR818DP SOA with Design Example MOSFET Power Dissipation Superimposed

As can be seen, the LTC4229's foldback current limit profile roughly coincides with the 100ms SOA contour. Since this SOA plot is for an ambient temperature of 25°C only, a maximum fault filter time of much less than 100ms should be considered, such as 10ms or less. Selecting a 0.1µF ± 10% value for C_{FT} yields a maximum fault filter time of 1.75ms which should be small enough to protect the MOSFET during any overcurrent fault scenario.

Next, select the values for the resistive divider at the OV and UV pins that define the overvoltage and undervoltage threshold of 15.2V and 9.8V respectively for the 12V input supply. Since the leakage currents for the OV and UV pins can be as high as ±1µA each, the total resistance in the divider should be low enough to minimize the resulting

APPLICATIONS INFORMATION

offset errors. Calculate the bottom resistor R1 based on the following equation to obtain less than ±0.5% error due to leakage current.

$$R1 = \left(\frac{V_{OV(TH)}}{2 \bullet I_{IN(LEAK)}}\right) \bullet 0.5\% = \left(\frac{1.235V}{2\mu A}\right) \bullet 0.5\% = 3k$$

Choose R1 to be 2k to achieve less than ±0.5% error and calculating R2/R3 yields:

$$R2 = \left(\frac{V_{IN(OV)}}{V_{IN(UV)}} - 1\right) \bullet R1 = \left(\frac{15.2V}{9.8V} - 1\right) \bullet 2k = 1.1k$$

$$R3 = \left(\frac{V_{IN(UV)}}{V_{UV(TH)}} - 1\right) \bullet (R1 + R2)$$

$$R3 = \left(\frac{9.8V}{1.235V} - 1\right) \bullet (2k + 1.1k) = 21.5k$$

The worst case OV and UV threshold offset voltage errors resulting from the total UV and OV pin leakage current ($2 \bullet I_{IN(LEAK)}$) that flows into R3, are calculated as ±0.29% and ±0.44% respectively.

It remains to select the values for the FB pin resistive divider in order to set a power good threshold of 10.5V. Keeping in mind the FB pin's ±1µA leakage current, choose a value of 2k for the bottom resistor R4. Calculating the top resistor R5 value yields:

$$R5 = \left(\frac{V_{OUT(PG)}}{V_{FB(TH)}} - 1\right) \bullet R4 = \left(\frac{10.5V}{1.235V} - 1\right) \bullet 2k = 15k$$

The subsequent offset error due to the FB pin leakage current will be less than ±0.14%.

The final component to consider is a 0.1µF bypass (C1) at the $INTV_{CC}$ pin.

PCB Layout Considerations

To achieve accurate current sensing, a Kelvin connection for the sense resistor is recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor and the power MOSFET should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout is illustrated in Figure 7.

Connect the IN and OUT pin traces as close as possible to the MOSFET's terminals. Keep the traces to the MOSFETs wide and short to minimize resistive losses. The PCB traces associated with the power path through the MOSFETs should have low resistance. The suggested trace width for

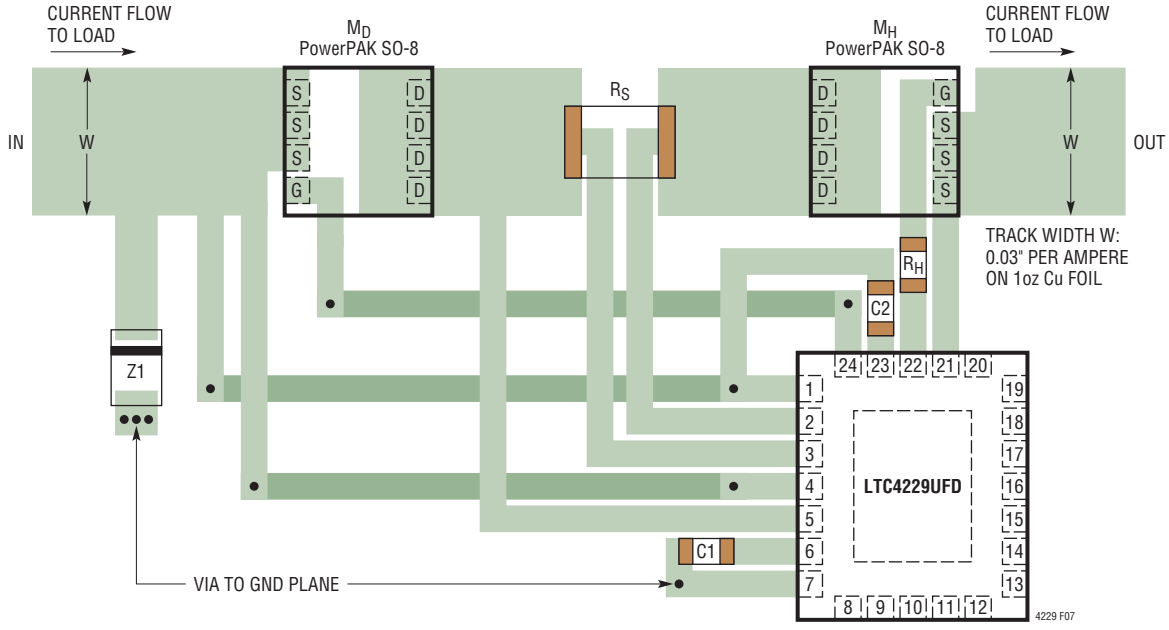


Figure 7. Recommended PCB Layout for Power MOSFETs and Sense Resistor

APPLICATIONS INFORMATION

1oz copper foil is 0.03" for each ampere of DC current to keep PCB trace resistance, voltage drop and temperature rise to a minimum. Note that the sheet resistance of 1oz copper foil is approximately 0.5mΩ/square, and voltage drops due to trace resistance add up quickly in high current applications.

It is also important to place the bypass capacitor C1 for the $INTV_{CC}$ pin, as close as possible between $INTV_{CC}$ and GND. Also place C2 near the CPO and DSRC pins. The transient voltage suppressor Z1, when used, should be mounted close to the LTC4229 using short lead lengths.

Flexible Configuration for Ideal Diode and Hot Swap MOSFET

The LTC4229 offers the flexibility to swap the ordering of the M_D and M_H N-channel MOSFETs for the ideal diode and Hot Swap control respectively between the supply and load side.

Figure 8 shows a configuration that allows two input supplies to be diode-ORed at $SENSE^+$ pin followed by Hot Swap control for a card-resident application. For applications where the LTC4229 resides on the backplane, the two supplies are diode-ORed at the output as shown in Figures 9 and 10. Figure 11 depicts an application where placing the M_D MOSFET downstream of the M_H MOSFET allows a dedicated bypass capacitor to keep alive its small load after power is removed at the input. Unlike the circuit in Figure 9 where the $SENSE^+$ pin is protected from momentary negative input transients by the ideal diode, the loads in Figures 10 and 11 are much more susceptible to brownouts. This is because input transients that dip below the $SENSE^+$ pin's 1.9V UVLO threshold can cause the HGATE pin to pull low thus discharging the M_H MOSFET's gate capacitance as well as any external capacitance which can result in a lengthy recovery time for the Hot Swap controller.

Since the LTC4229's ideal diode and Hot Swap controllers operate independently, the M_D and M_H MOSFETs can also be configured to operate on two different supplies at the same time as shown in Figure 12. If one of the supplies is not available, the LTC4229 will continue to operate with the remaining supply since the internal $INTV_{CC}$ regulator is powered from an internal diode-OR of the IN, $SENSE^+$ and OUT pins.

Power Prioritizer

Figure 14 shows an application where either of two supplies is passed to the output on the basis of priority, rather than simply allowing the highest voltage to prevail. The 5V primary supply (V_{IN1}) is passed to the output whenever it is available; power is drawn from the 12V backup supply (V_{IN2}) only when the primary supply is unavailable. As long as V_{IN1} is above the 4.7V threshold set by the R6-R7 divider at the DOFF pin, back-to-back ideal diode MOSFETs, M_{D1} and M_{D2}, are turned off, allowing V_{IN1} to be connected to the output through M_{D3} that is controlled by another ideal diode controller LTC4352. The common source terminals of M_{D1} and M_{D2} are connected to DSRC pin, which allows the body-diode of M_{D1} to reverse block the current flow from the higher backup supply (V_{IN2}) to the output. If the primary supply fails and V_{IN1} drops below 4.3V, DOFF is allowed to turn on M_{D1} and M_{D2}, and connect the V_{IN2} to the output. When V_{IN1} returns to a viable voltage, M_{D1} and M_{D2} turn off, and the output is connected to V_{IN1}. Adding R8 in the R6-R7 divider and bypassing it with $\overline{DSTAT}$ pin control, allows the DOFF pin hysteresis to be increased from 20mV to 100mV. The resistive divider at OV and UV pins set the $SENSE^+$ overvoltage and undervoltage thresholds to 15V and 4.1V respectively.

Hot Swap Followed by Ideal Diode Application

Figure 15 shows an application whereby the Hot Swap MOSFET is placed on the supply side and the ideal diode MOSFET on the load side with the source terminals connected together. The ideal diode voltage is sensed across M_D at IN and DSNS pins. If the 12V power supply is connected, it supplies power to the load and also charges up the standby battery cell at $SENSE^+$ through M_H and R6 as M_D is turned off. If the power supply is disconnected, the power to the load is provided by the standby battery as M_D turns on. Since the LTC4229's internal 12V clamp only limits the HGATE-to-OUT pin voltage, the gate-to-source breakdown voltage of the Hot Swap MOSFET can be exceeded when the input is connected to ground. An external Zener diode clamp is required between the GATE and SOURCE pins of the MOSFET to prevent it from breaking down.

APPLICATIONS INFORMATION

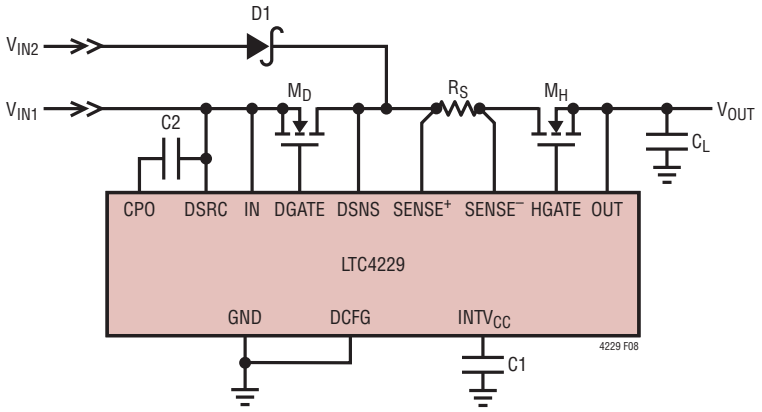


Figure 8. Ideal Diode Followed by Hot Swap Configuration with Diode Sense Across M_D

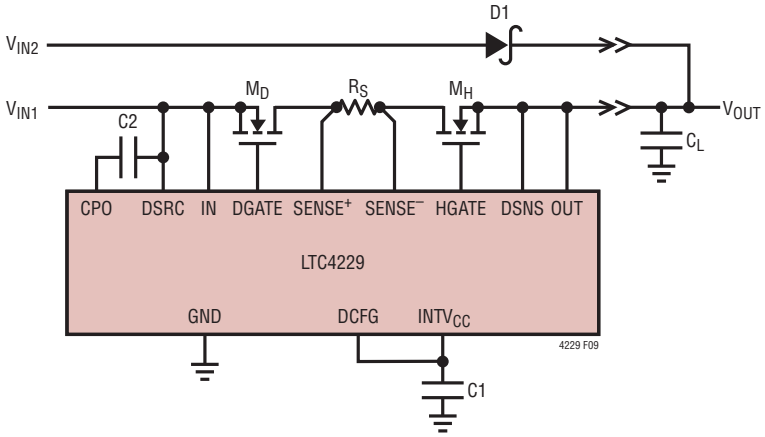


Figure 9. Ideal Diode Followed by Hot Swap Configuration with Diode Sense Across M_D, R_S and M_H

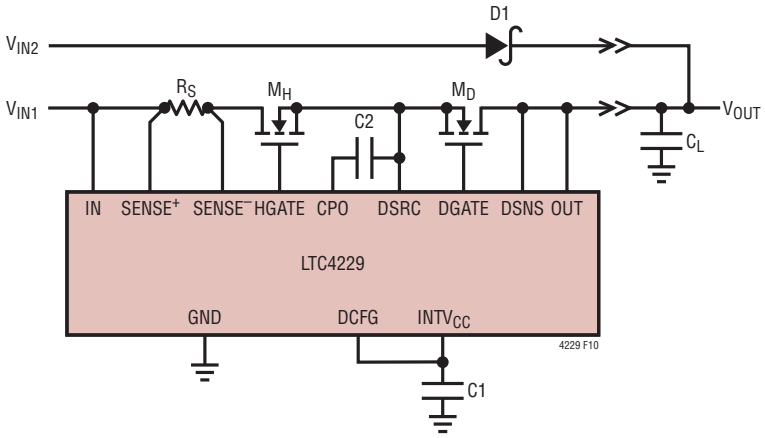


Figure 10. Hot Swap Followed by Ideal Diode Configuration with Diode Sense Across R_S, M_H and M_D

APPLICATIONS INFORMATION

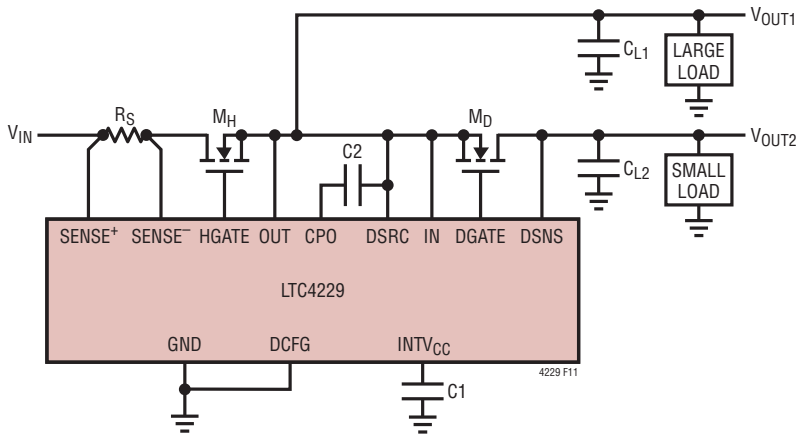


Figure 11. Hot Swap Followed by Ideal Diode Configuration with Diode Sense Across M_D

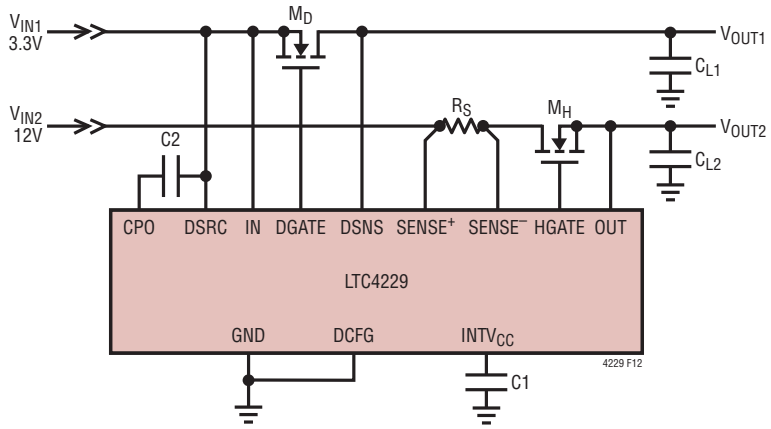


Figure 12. Separate Ideal Diode and Hot Swap Configuration with Diode Sense Across M_D

APPLICATIONS INFORMATION

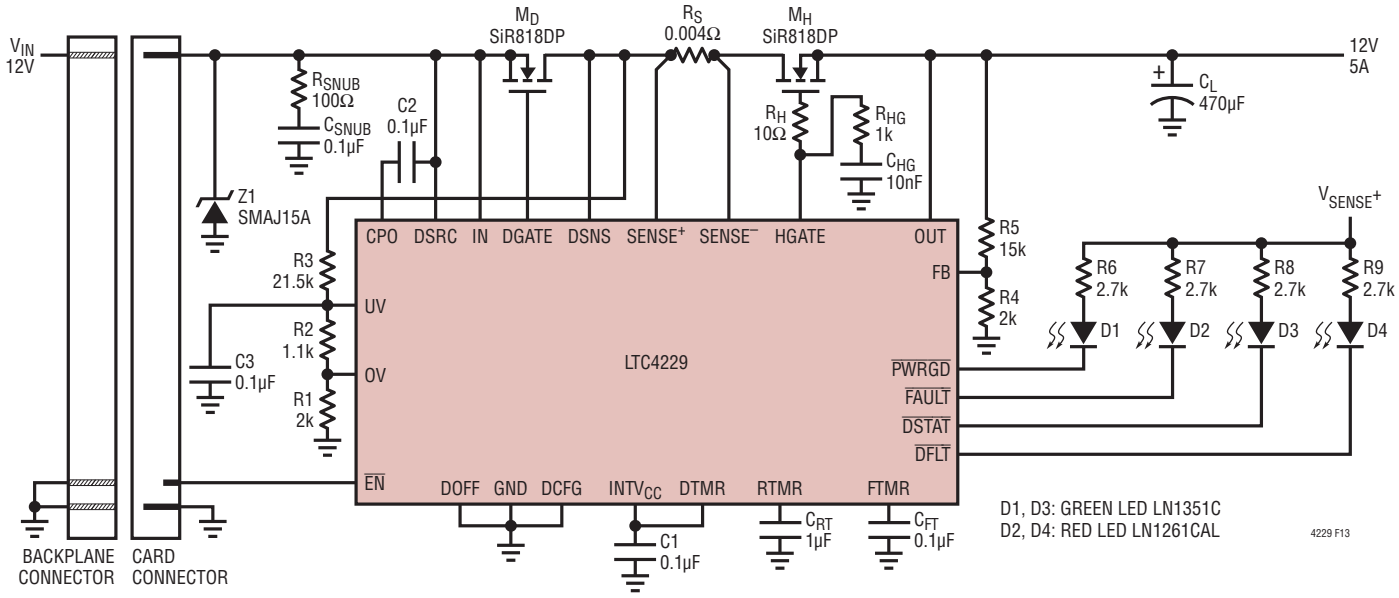


Figure 13. Plug-In Card Supply Holdup Using Ideal Diode at Input

APPLICATIONS INFORMATION

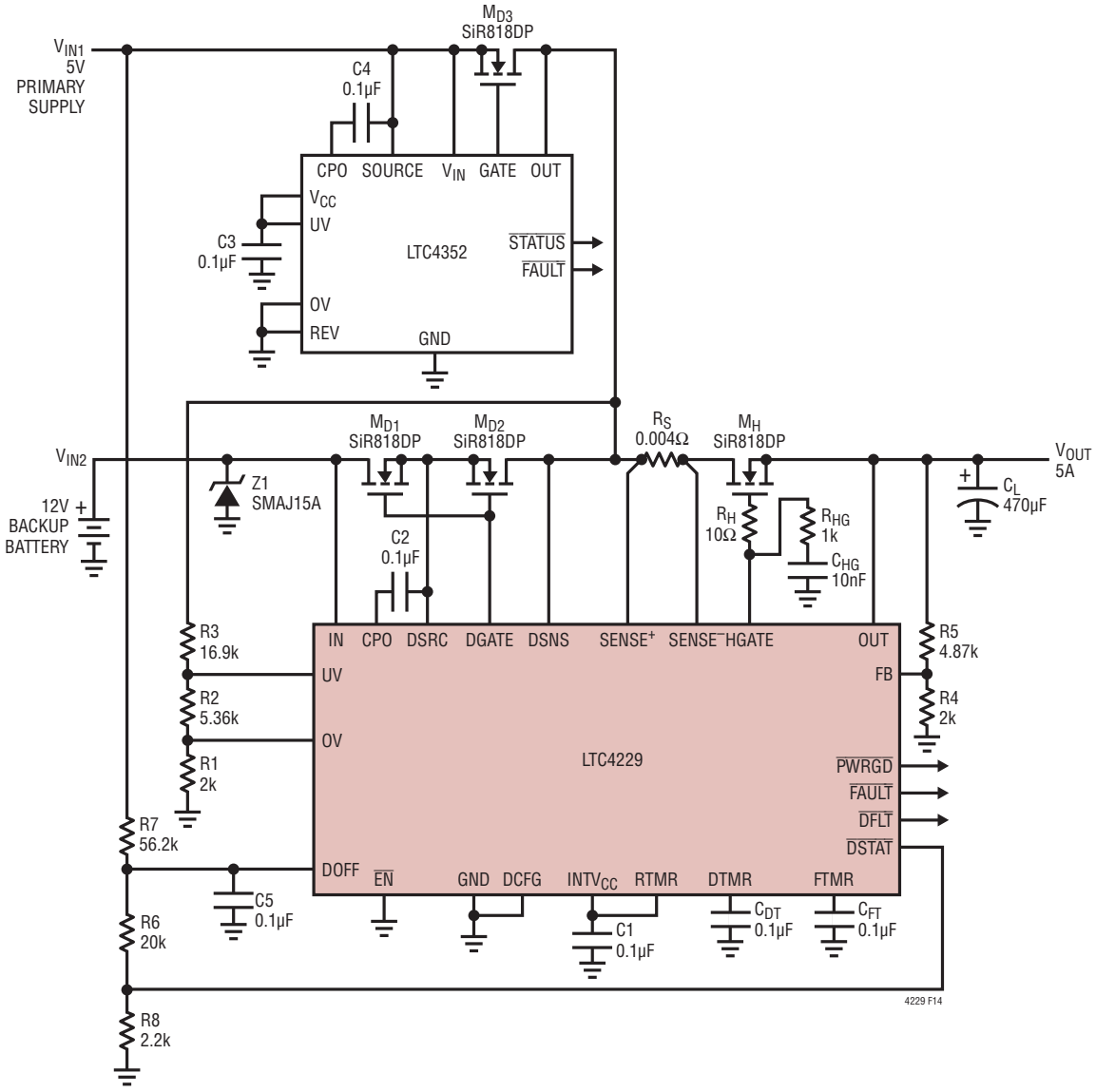


Figure 14. 2-Channel Power Prioritizer

APPLICATIONS INFORMATION

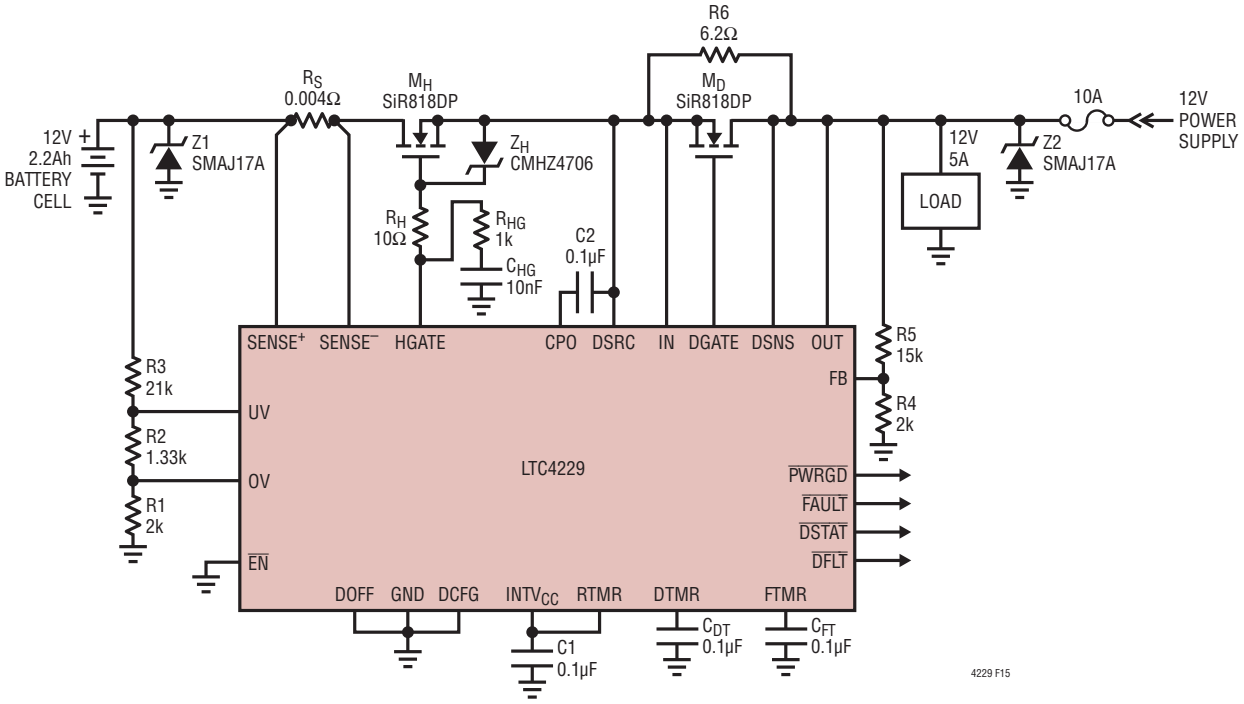


Figure 15. Battery Application with Hot Swap MOSFET on the Supply Side and Ideal Diode MOSFET on the Load Side

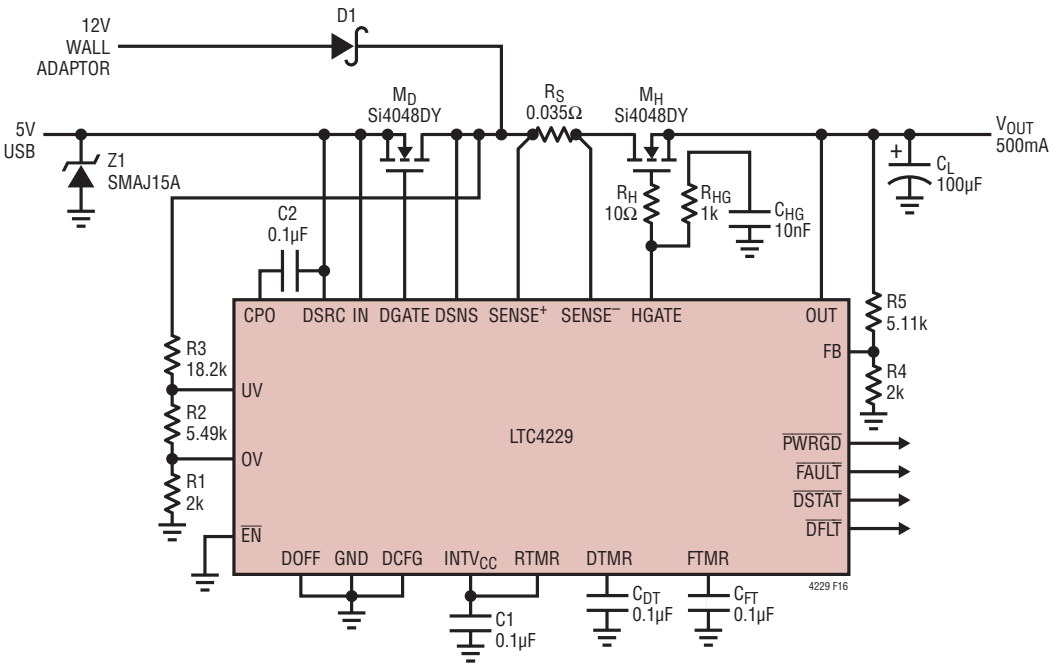
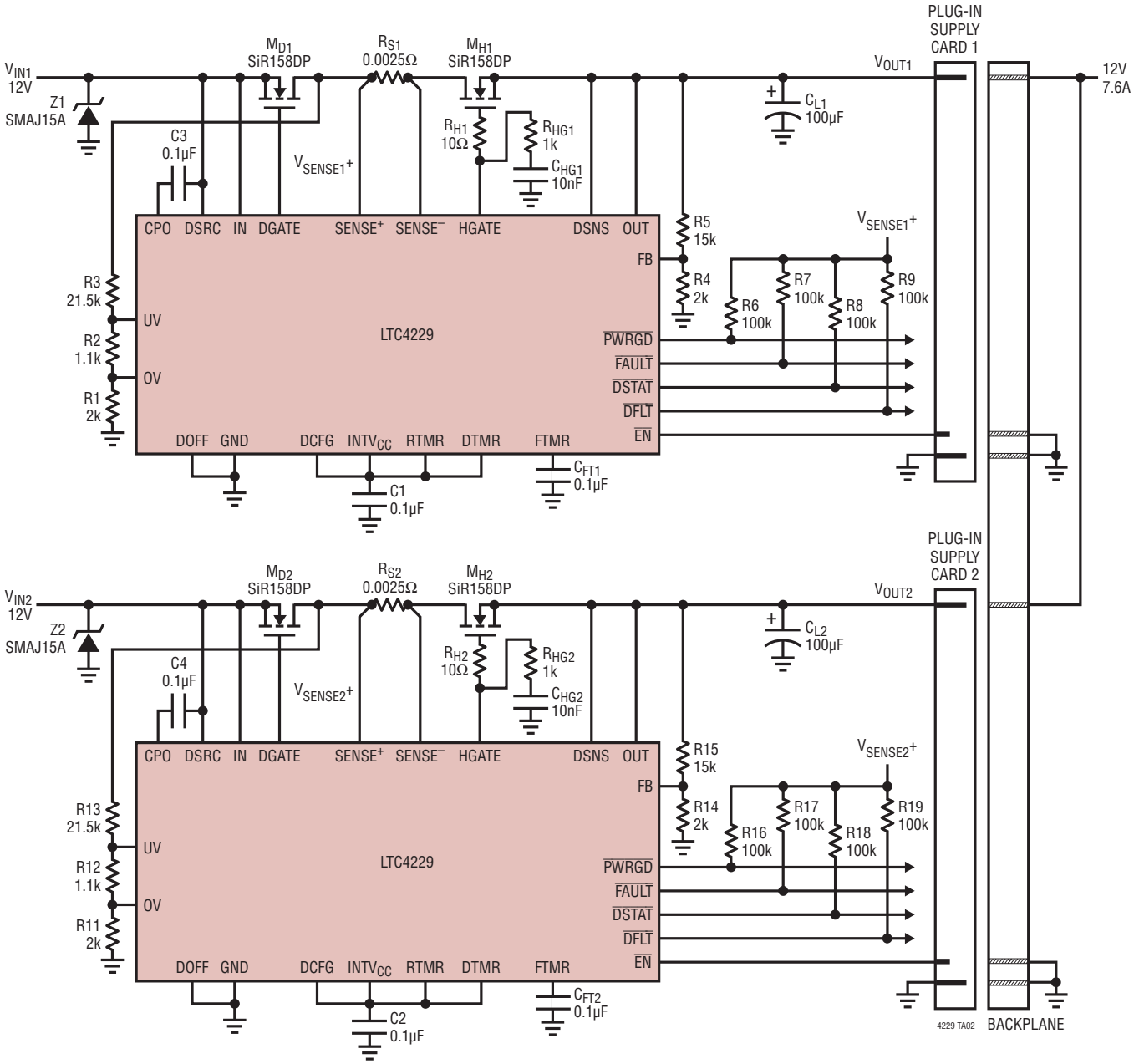


Figure 16. USB Power Combined with Wall Adaptor

TYPICAL APPLICATION

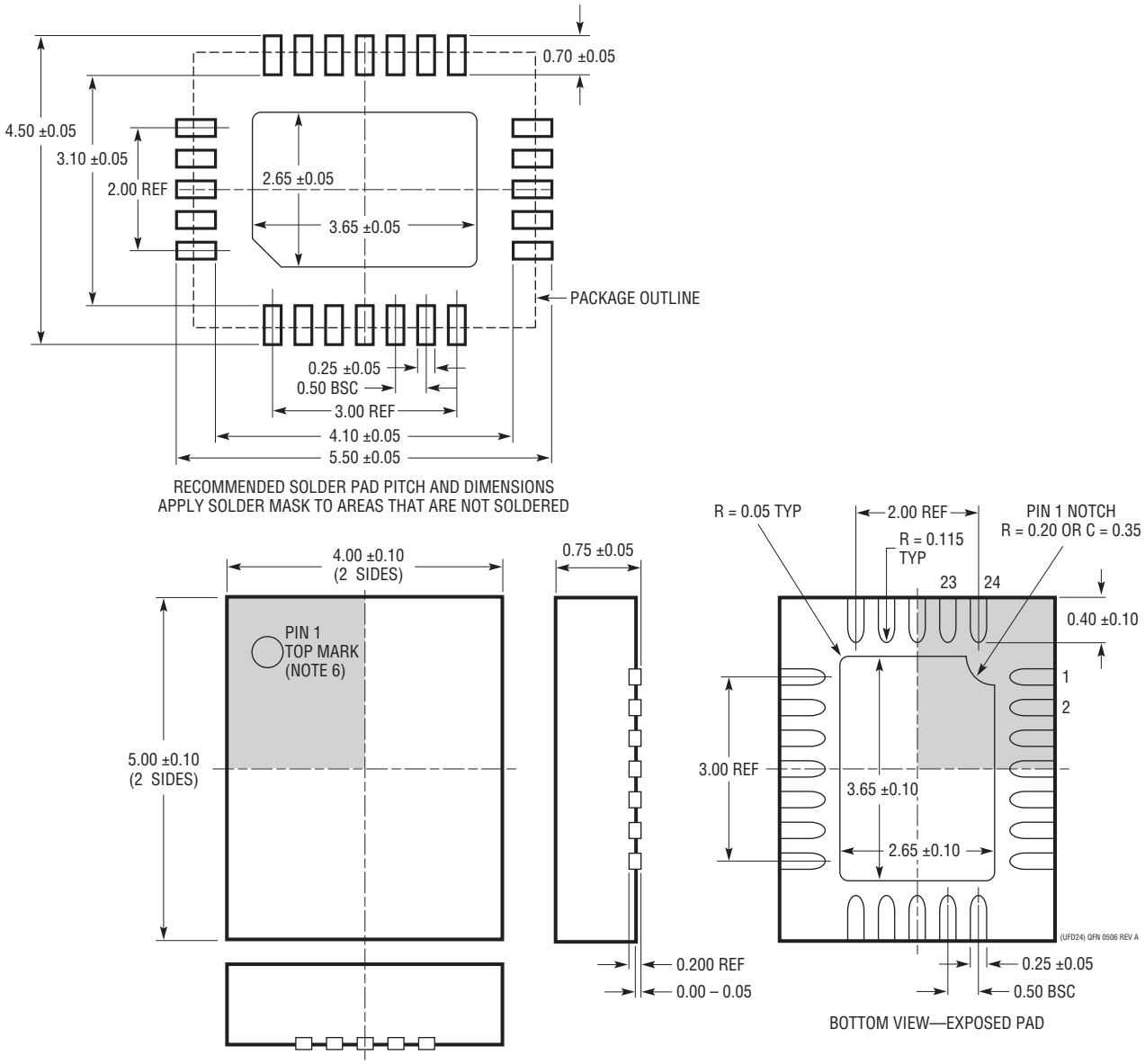
Diode-ORing on Backplane Application with Ideal Diode First Followed by Hot Swap Control



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)

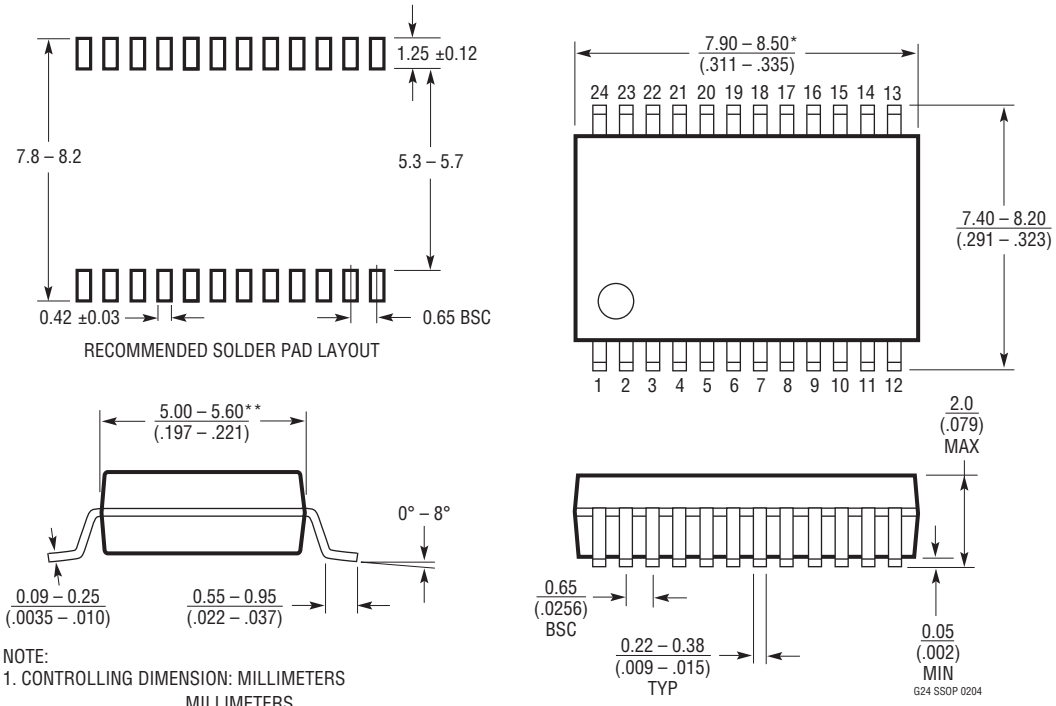


NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

G Package
24-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE