Dual Slot Hot Swap Controller for PCI Express

FEATURES

- **Allows Live Insertion into PCI Express® Backplane**
- **Controls Two Independent PCI Express Slots**
- **Independent Control of Main and Auxiliary Supplies**
- **20V Rating for 12V Supply Input Pins**
- **Integrated 0.25Ω AUX Switches**
- Limits Fault Current in ≤1µs
- Force On Test Mode
- Adjustable Supply Voltage Power-Up Rate
- High Side Drivers for N-Channel MOSFETs
- Thermal Shutdown Protection
- Available in 38-Lead QFN and 36-Lead SSOP Packages

APPLICATIONS

- PCI Express-Based PC and Servers
- Hot Swap Application for Triple Supply Systems

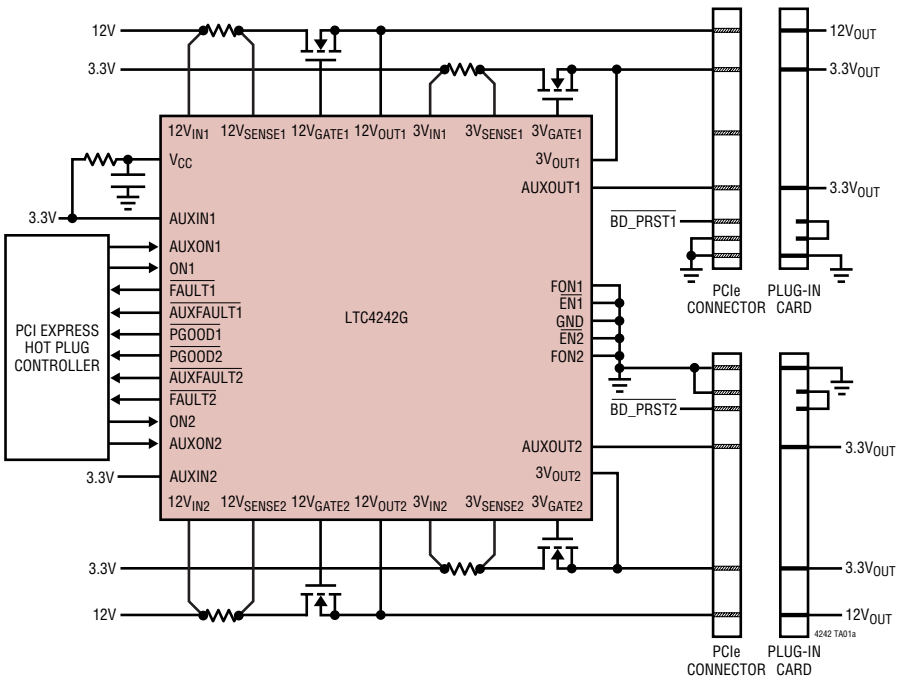
DESCRIPTION

The LTC®4242 Hot Swap™ controller allows safe board insertion and removal for two independent slots on a PCI Express backplane. External N-channel transistors control the 12V and 3.3V supplies while integrated switches control the 3.3V auxiliary supplies. Both 12V and 3.3V supplies can be ramped up at an adjustable rate. Dual level circuit breakers and fast active current limiting protect all supplies against overcurrent faults.

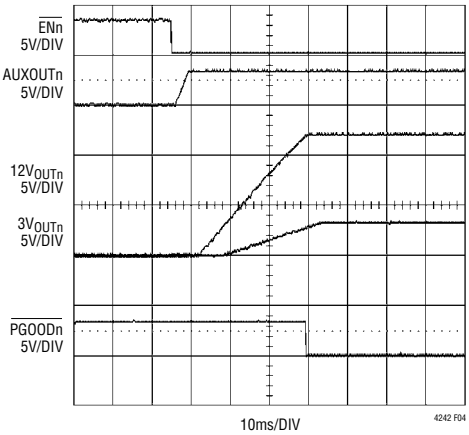
A supply filter at the V_{CC} pin allows the LTC4242 to endure supply transients. The $\overline{EN}$ input detects the presence of a card in the PCI Express slot. The $\overline{FAULT}$ and $\overline{AUXFAULT}$ outputs alert the system of overcurrent conditions on the main and auxiliary supplies, respectively. $\overline{PGOOD}$ and $\overline{AUXPGOOD}$ outputs indicate proper main and auxiliary supply outputs.

TYPICAL APPLICATION

PCI Express Application



Normal Power-Up Sequence



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages
- V_{CC} ..... –0.3V to 7V
- $12V_{INn}$ ..... –0.3V to 20V
- $3V_{INn}$ ..... –0.3V to 10V
- AUXINn ..... –0.3V to 10V

Input Voltages
- $\overline{ONn}$, AUXONn, FONn ..... –0.3V to 7V
- $\overline{ENn}$ ..... –0.3V to 7V

Output Voltages
- $\overline{FAULTn}$, $\overline{PGOODn}$, $\overline{AUXFAULTn}$, $\overline{AUXPGOODn}$ ..... –0.3V to 7V

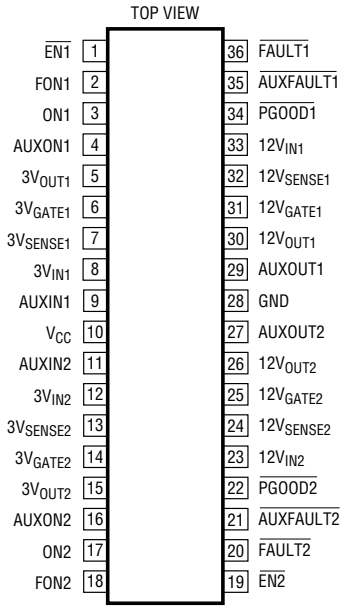
Analog Voltages
- $12V_{SENSEn}$ ..... –0.3V to 20V
- $12V_{GATEn}$ ..... –0.3V to 25V
- $12V_{OUTn}$ (Note 3) .. $12V_{GATEn}$ – 5V to $12V_{GATEn}$ + 0.3V
- AUXOUTn, $3V_{SENSEn}$ ..... –0.3V to 10V
- $3V_{GATEn}$ ..... –0.3V to 14V
- $3V_{OUTn}$ (Note 3) ..... $3V_{GATEn}$ – 5V to $3V_{GATEn}$ + 0.3V

Operating Temperature Range
- LTC4242C ..... 0°C to 70°C
- LTC4242I ..... –40°C to 85°C

Storage Temperature Range
- SSOP ..... –65°C to 150°C
- QFN ..... –65°C to 125°C

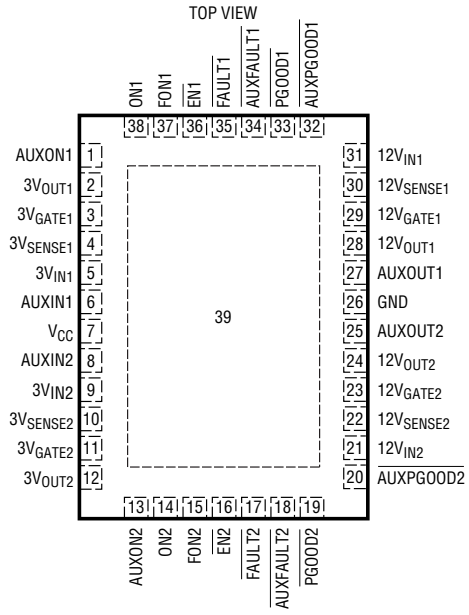
Lead Temperature (Soldering, 10 sec)
- SSOP ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W

EXPOSED PAD (PIN 39) IS GND, PCB ELECTRICAL CONNECTION OPTIONAL

ORDER PART NUMBER	ORDER PART NUMBER	UHF PART MARKING*
LTC4242CG LTC4242IG	LTC4242CUHF LTC4242IUHF	4242 4242

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3V, V_{12VINn} = 12V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{IN}	Operating Voltage	V_{CC}	●	2.7		6.0	V
		$12V_{INn}$	●	10.1		14.4	V
		$3V_{INn}$	●	3.0		6.0	V
		AUXINn	●	3.0		6.0	V
I_{DD}	Input Supply Current	V_{AUXONn} = 2V, V_{ONn} = 2V					
	V_{CC}		●		1.6	4	mA
	$12V_{INn}$		●		0.5	1	mA
	$3V_{INn}$		●		0.35	1	mA
V_{UVL}	Supply Undervoltage Lockout	V_{CC} Rising	●	2.3	2.45	2.6	V
		$12V_{INn}$ Rising	●	9.48	9.78	10.08	V
		$3V_{INn}$ Rising	●	2.57	2.67	2.77	V
		AUXINn Rising	●	2.57	2.67	2.77	V
$\Delta V_{LKO(HYST)}$	Supply Undervoltage Lockout Hysteresis	V_{CC}	●	30	100	200	mV
		$12V_{INn}$	●	90	130	170	mV
		$3V_{INn}$	●	20	35	50	mV
		AUXINn	●	20	35	50	mV
Current Limit							
$\Delta V_{SENSE(CB)}$	Circuit Breaker Trip Sense Voltage						
	$12V_{INn} – 12V_{SENSEn}$		●	45	50	55	mV
	$3V_{INn} – 3V_{SENSEn}$		●	45	50	55	mV
$\Delta V_{SENSE(ACL)}$	Active Current Limit Sense Voltage						
	$12V_{INn} – 12V_{SENSEn}$		●	75	100	125	mV
	$3V_{INn} – 3V_{SENSEn}$		●	75	100	125	mV
I_{CBAUX}	Circuit Breaking Current for AUX Supply		●	385	550	715	mA
t_{CB}	Circuit Breaker Response Time		●	10	20	40	µs
Switch Resistance							
R_{AUX}	Internal Switch Resistance	(Note 4)					
	$R_{AUX} = (V_{AUXINn} – V_{AUXOUTn})/I$	I = 375mA	●		0.25	0.4	Ω
External Gate Drive							
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On					
		$V_{12VGATEn}$ = 1V	●	–5	–9	–13	µA
		$V_{3VGATEn}$ = 1V	●	–5	–9	–13	µA
$I_{GATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off					
		$V_{12VGATEn}$ = 17V, $V_{12VOUTn}$ = 12V	●	0.5	1	2	mA
		$V_{3VGATEn}$ = 8.3V, V_{3VOUTn} = 3.3V	●	0.5	1	2	mA
$I_{GATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn Off					
		$V_{12VGATEn}$ = 17V, $V_{12VOUTn}$ = 12V	●	150	250	400	mA
		$V_{3VGATEn}$ = 8.3V, V_{3VOUTn} = 3.3V	●	150	250	400	mA
ΔV_{GATE}	External N-Channel Gate Drive	I_{GATE} = 1µA (Note 3)					
	$12V_{GATEn} – 12V_{OUTn}$		●	4.5	5.5	7.9	V
	$3V_{GATEn} – 3V_{OUTn}$		●	4.5	5.5	7.9	V
Input Pins							
$V_{PG(TH)}$	Power Good Threshold Voltage	$12V_{OUTn}$ Falling	●	10.08	10.38	10.68	V
		$3V_{OUTn}$ Falling	●	2.772	2.855	2.937	V
		AUXOUTn Falling (Note 5)	●	2.772	2.855	2.937	V
$V_{PG(HYST)}$	Power Good Hysteresis	$12V_{OUTn}$	●	20	70	110	mV
		$3V_{OUTn}$	●	5	20	30	mV
		AUXOUTn (Note 5)	●	5	20	30	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3V, V_{12VINn} = 12V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{ON(TH)}$	ONn, AUXONn Pin Threshold Voltage	Rising Edge	●	1.173	1.235	1.297	V
$\Delta V_{ON(TH)}$	ONn, AUXONn Pin Hysteresis		●	30	70	120	mV
$V_{ON(RTH)}$	ONn, AUXONn Pin Reset Threshold Voltage	Falling Edge	●	0.5	0.6	0.7	V
$I_{ON(IN)}$	ONn, AUXONn Pin Input Current	V_{ONn} = V_{AUXONn} = 1.2V	●			±1	µA
$V_{\overline{EN}(TH)}$	$\overline{ENn}$ Pin Threshold Voltage	$\overline{ENn}$ Rising	●	1.173	1.235	1.297	V
$\Delta V_{\overline{EN}(HYST)}$	$\overline{ENn}$ Pin Hysteresis		●	30	70	120	mV
$I_{\overline{EN}(UP)}$	$\overline{ENn}$ Pull-Up Current	$V_{\overline{ENn}}$ = 1V	●	–5	–9	–13	µA
V_{FON}	FONn Pin Logic Threshold		●	0.7		2.6	V
I_{SENSE}	SENSE Pin Input Current						
	$12V_{SENSEn}$	$V_{12VSENSEn}$ = 12V	●		40	100	µA
	$3V_{SENSEn}$	$V_{3VSENSEn}$ = 3.3V	●		40	100	µA
I_{OUT}	OUT Pin Input Current	Gate Drive On					
	$12V_{OUTn}$	$V_{12VOUTn}$ = 12V	●		45	90	µA
	$3V_{OUTn}$	V_{3VOUTn} = 3.3V	●		27	60	µA
$R_{OUT(DIS)}$	OUT Pin Discharge Resistance	Gate Drive Off					
	$12V_{OUTn}$	$V_{12VOUTn}$ = 6V	●	350	700	1400	Ω
	$3V_{OUTn}$	V_{3VOUTn} = 2V	●	165	330	660	Ω
	AUXOUTn	$V_{AUXOUTn}$ = 2V	●	375	750	1500	Ω
Output Pins							
V_{OL}	Output Low Voltage $\overline{FAULTn}$, $\overline{AUXFAULTn}$, $\overline{PGOODn}$, $\overline{AUXPGOODn}$ (Note 5)	I_{PIN} = 3mA	●		0.14	0.4	V
I_{PU}	Pull-Up Current $\overline{FAULTn}$, $\overline{AUXFAULTn}$, $\overline{PGOODn}$, $\overline{AUXPGOODn}$ (Note 5)	V_{PIN} = 1.5V	●	–5	–9	–13	µA
Slew Rate							
SR_{AUXOUT}	AUXOUTn Slew Rate		●		1.25	1.7	V/ms
Delays							
$t_{PLH(GATE)}$	Input High (ONn) to GATEs High Prop Delay		●		7	14	µs
$t_{PLH(UVL)}$	Input Supply Low ($12V_{INn}$, $3V_{INn}$) to GATEs Low Prop Delay		●		18	36	µs
$t_{PLH(PG)}$	Out Low ($12V_{OUTn}$, $3V_{OUTn}$) to $\overline{PGOOD}$ High Prop Delay		●		20	40	µs
$t_{PHL(SENSE)}$	Sense Voltage High to GATE Low	ΔV_{SENSE} = 200mV, C_{GATE} = 10nF	●		0.4	1	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All current into device pins is positive, all current out of the device pins is negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pins to a minimum of 5V above V_{OUT}. Driving this pin to voltages beyond the clamp may damage the device.

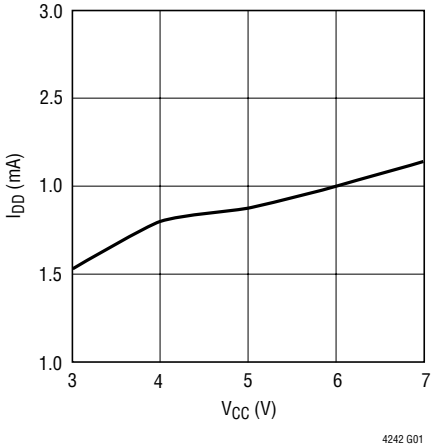
Note 4: For the QFN package, the AUX FET on resistance is guaranteed by correlation to wafer level measurements.

Note 5: Available on QFN package only.

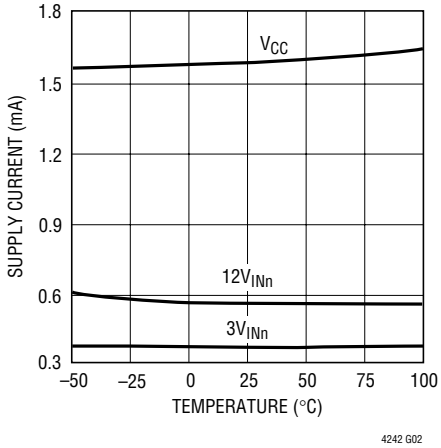
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3V, V_{12VINn} = 12V, unless otherwise noted. (Note 2)

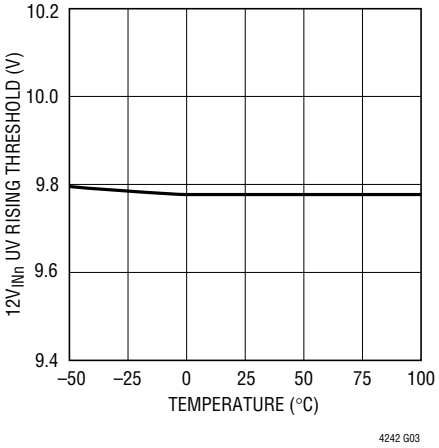
I_{DD} vs V_{CC}



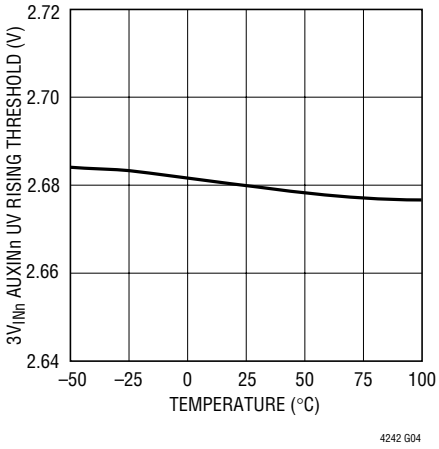
V_{CC}, $12V_{INn}$ and $3V_{INn}$ Supply Current vs Temperature



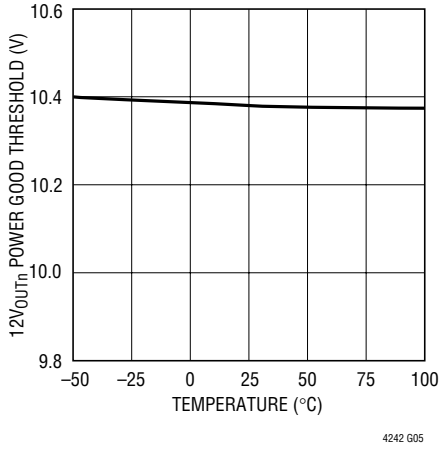
$12V_{INn}$ UV Rising Threshold vs Temperature



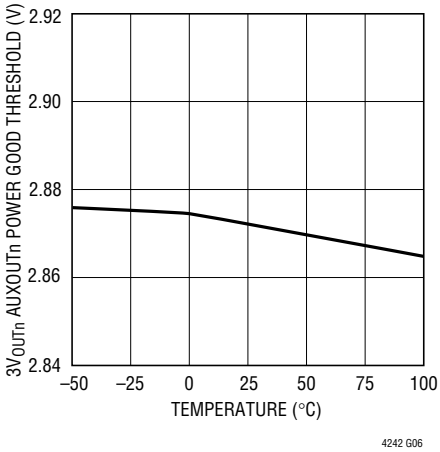
$3V_{INn}$, AUXINn Rising Threshold vs Temperature



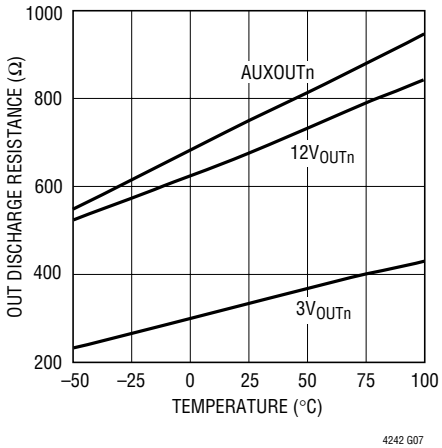
$12V_{OUTn}$ Power Good Threshold vs Temperature



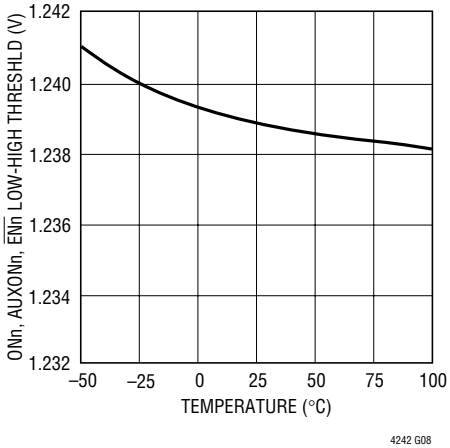
$3V_{OUTn}$, AUXOUTn Power Good Threshold vs Temperature



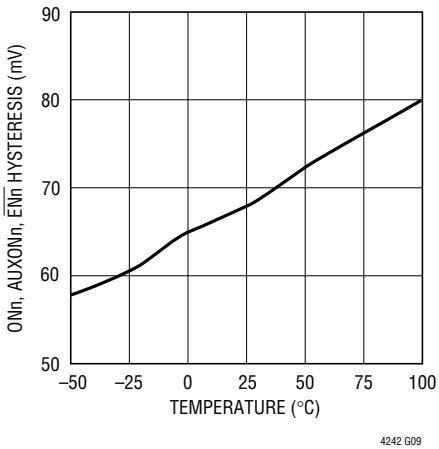
OUT Discharge Resistance vs Temperature



ONn, AUXONn, $\overline{ENn}$ Low-to-High Threshold vs Temperature



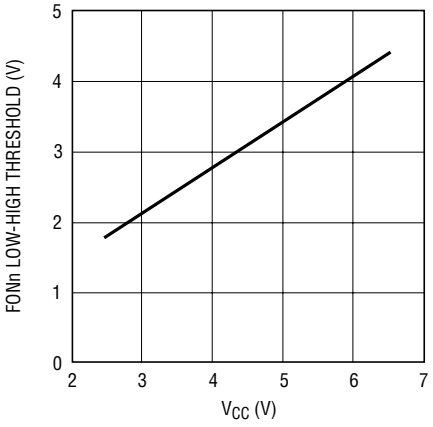
ONn, AUXONn, $\overline{ENn}$ Hysteresis vs Temperature



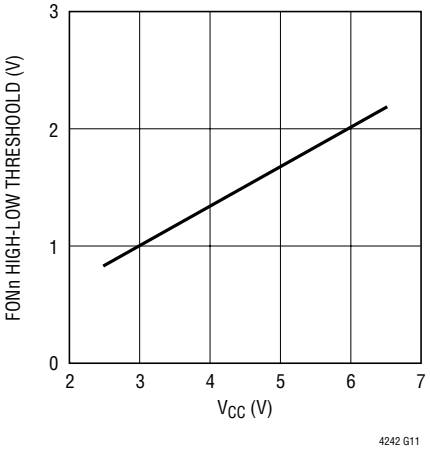
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3V, V_{12VINn} = 12V, unless otherwise noted. (Note 2)

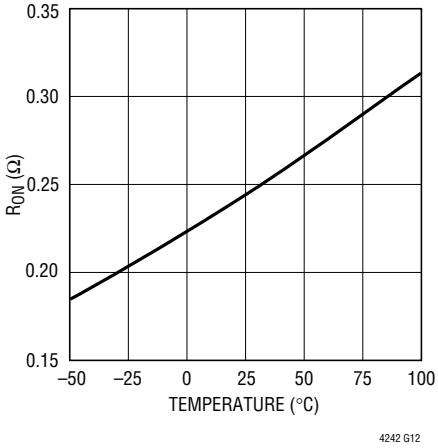
FONn Low-to-High Threshold vs V_{CC}



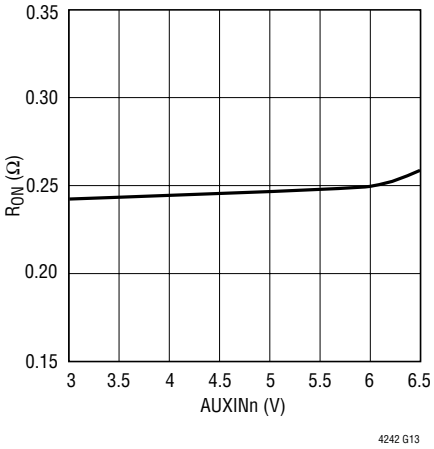
FONn High-to- Low Threshold vs V_{CC}



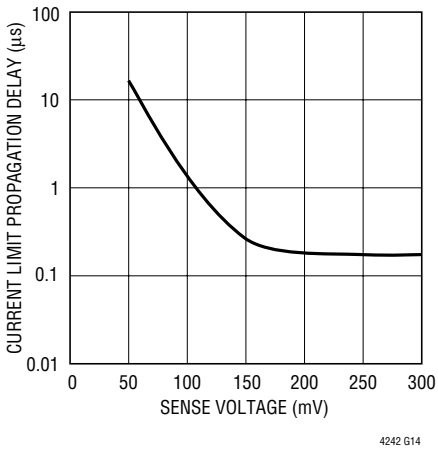
R_{ON} vs Temperature



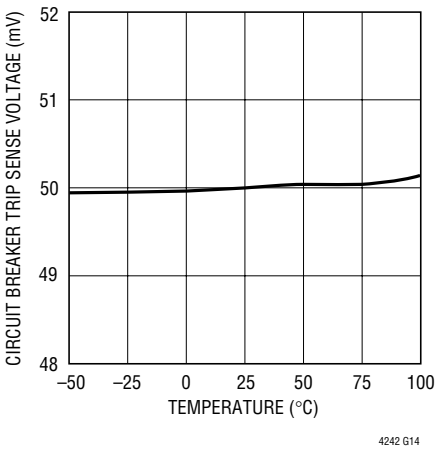
R_{ON} vs AUXINn



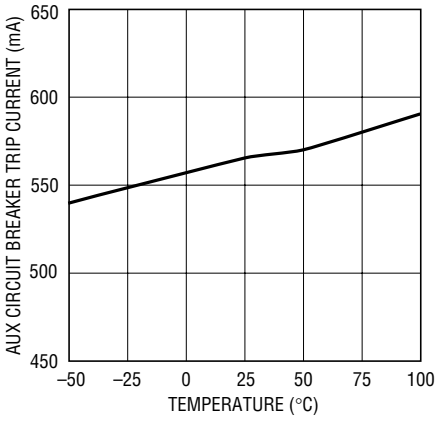
Current Limit Propagation Delay vs Sense Voltage



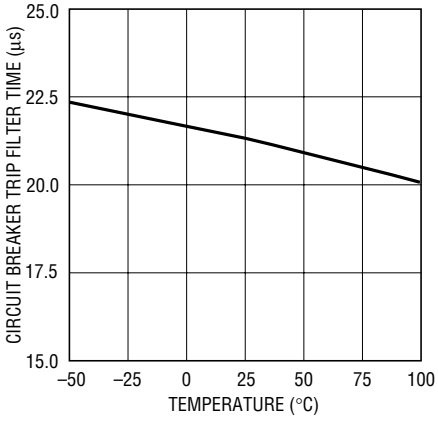
Circuit Breaker Trip Sense Voltage vs Temperature



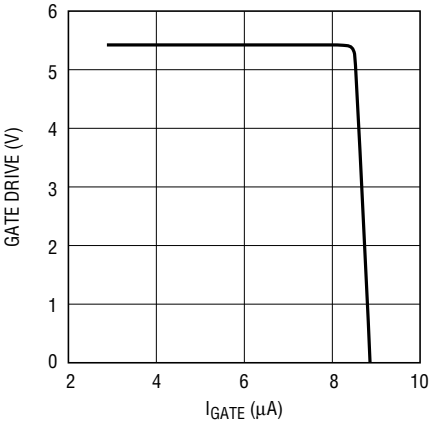
Aux Circuit Breaker Trip Current vs Temperature



Circuit Breaker Trip Filter Time vs Temperature



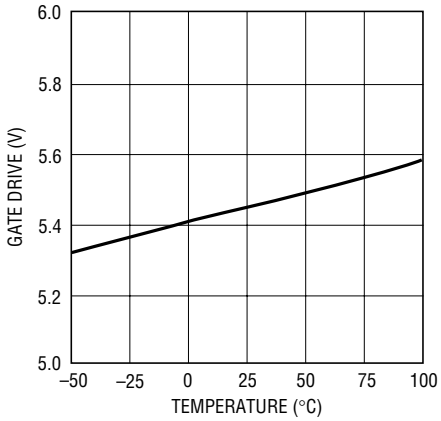
Gate Drive vs I_{GATE}



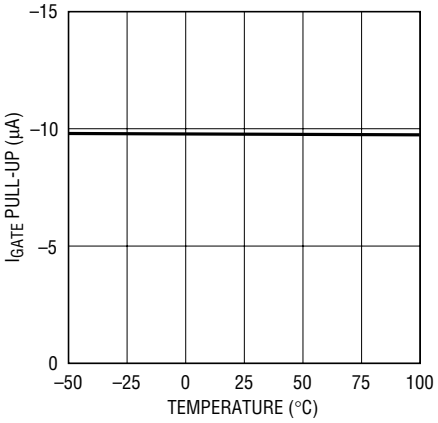
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3V, V_{12VINn} = 12V, unless otherwise noted. (Note 2)

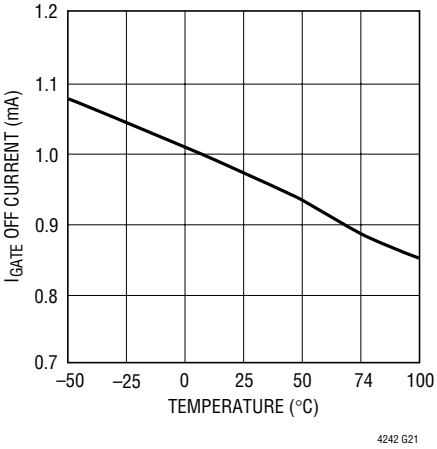
Gate Drive vs Temperature



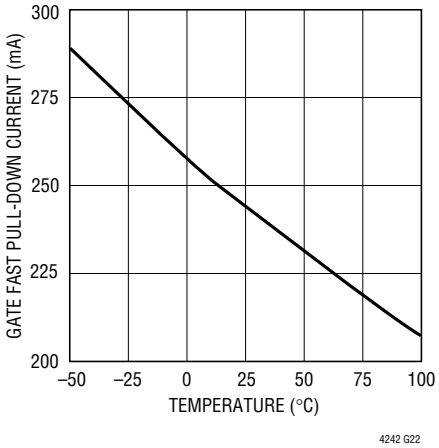
I_{GATE} Pull-Up vs Temperature



I_{GATE} Off Current vs Temperature



Gate Fast Pull-Down Current vs Temperature



PIN FUNCTIONS

$12V_{GATE1}/12V_{GATE2}$: Gate Drive for 12V Supply External N-Channel MOSFET. An internal charge pump provides a 9µA pull-up current to ramp up $12V_{GATEn}$. During turn off, a 1mA pull-down current source discharges $12V_{GATEn}$ to ground. $12V_{GATEn}$ is internally clamped to 5.5V above $12V_{OUTn}$. During an overcurrent fault, a 250mA pull-down current source between $12V_{GATEn}$ and $12V_{OUTn}$ is activated. An external RC network is required at the pin for optimum current limit response.

$12V_{SENSE1}/12V_{SENSE2}$: 12V Supply Current Limit Sense Input. A sense resistor is placed in the supply path between $12V_{INn}$ and $12V_{SENSEn}$ to sense the 12V channel's load current. The voltage across the sense resistor is monitored for active current limit and circuit breaker fault detection. To disable the circuit breaker function for the 12V channel, connect $12V_{SENSEn}$ to $12V_{INn}$.

$12V_{IN1}/12V_{IN2}$: 12V Supply Input. An undervoltage lockout circuit disables the 12V and 3.3V supplies when $12V_{INn}$ voltage is less than 9.78V.

$12V_{OUT1}/12V_{OUT2}$: 12V Output Connection. Connect this pin to the source of the 12V supply external N-channel MOSFET for gate drive return. PGOOD1/PGOOD2 cannot pull low until this pin goes above 10.38V. A 700Ω active pull-down discharges $12V_{OUTn}$ to ground when the external MOSFET is turned off.

$3V_{GATE1}/3V_{GATE2}$: Gate Drive for 3.3V Supply External N-Channel MOSFET. An internal charge pump provides a 9µA pull-up current to ramp up $3V_{GATEn}$. During turn off, a 1mA pull-down current source discharges $3V_{GATEn}$ to ground. $3V_{GATEn}$ is internally clamped to 5.5V above $3V_{OUTn}$. During an overcurrent fault, a 250mA pull-down current source between $3V_{GATEn}$ and $3V_{OUTn}$ is activated. An external RC network is required at the pin for optimum current limit response.

$3V_{SENSE1}/3V_{SENSE2}$: 3.3V Supply Current Limit Sense Input. A sense resistor is placed in the supply path between $3V_{INn}$ and $3V_{SENSEn}$ to sense 3.3V channel's load current. The voltage across the sense resistor is monitored for active current limit and circuit breaker fault detection. To disable the circuit breaker function for the 3.3V channel, connect $3V_{SENSEn}$ to $3V_{INn}$.

$3V_{IN1}/3V_{IN2}$: 3.3V Supply Input. An undervoltage lockout circuit disables the 3.3V and 12V supplies when $3V_{INn}$ voltage is less than 2.67V.

$3V_{OUT1}/3V_{OUT2}$: 3.3V Output Connection. Connect this pin to the source of the 3.3V supply external N-channel MOSFET for gate drive return. PGOOD1/PGOOD2 cannot pull low until this pin goes above 2.855V. A 375Ω active pull-down discharges $3V_{OUTn}$ to ground when the external MOSFET is turned off.

$\overline{AUXFAULT1}/\overline{AUXFAULT2}$: AUX Supply Fault Status Output. $\overline{AUXFAULTn}$ is normally pulled high by an internal 9µA pull-up. It asserts low if the AUX channel shuts off due to an overcurrent fault or due to the device temperature rising above 150°C. Indicates switch ON status when FONn and ENn are high.

AUXON1/AUXON2: AUX Supply On Control Input. A rising edge turns on the internal FET, while a falling edge turns it off. Pulling this pin below 0.6V for more than 3.5µs clears the fault on the AUX channel.

AUXIN1/AUXIN2: AUX Supply Input. An undervoltage lockout circuit disables the AUX supply when the voltage at AUXINn is less than 2.67V. AUXINn is the input to the internal pass FET.

AUXOUT1/AUXOUT2: AUX Supply Output. AUXOUTn is the output from the internal pass FET. AUXPGOOD1/AUXPGOOD2 cannot pull low until this pin goes above 2.855V. A 750Ω active pull-down discharges AUXOUTn to ground when the internal FET is turned off.

PIN FUNCTIONS

$\overline{\text{AUXPGOOD1}}$/$\overline{\text{AUXPGOOD2}}$ (QFN): AUX Supply Power Status Output. This open-drain pin is pulled high by an internal 9µA pull-up when AUXOUTn is below power good threshold, when $\overline{\text{ENn}}$ is high, during thermal shutdown, AUXONn is low or when V_{CC} or AUXINn are in UVLO.

$\overline{\text{EN1}}$/$\overline{\text{EN2}}$: Card Presence/Slot Insert Detect Input. $\overline{\text{ENn}}$ pin must be pulled below 1.235V to enable the system. An internal 9µA pull-up current source is present on this pin.

Exposed Pad (QFN): Power Ground. PCB electrical connection is optional.

$\overline{\text{FAULT1}}$/$\overline{\text{FAULT2}}$: Main Supplies Fault Status Output. $\overline{\text{FAULTn}}$ is pulled high by an internal 9µA pull-up. When an overcurrent fault occurs at either the 12V or 3.3V supply, $\overline{\text{FAULTn}}$ is latched low.

FON1/FON2: Force On Digital Input. For diagnostic purposes, a high input overrides undervoltage and overcurrent faults on 12V, 3.3V and AUX channels and input commands on the ONn and AUXONn pins. However, UVLO on V_{CC} would shut off the switches. Caution! There is no current limit mechanism in this mode. Connect FONn to ground to disable the fault override feature.

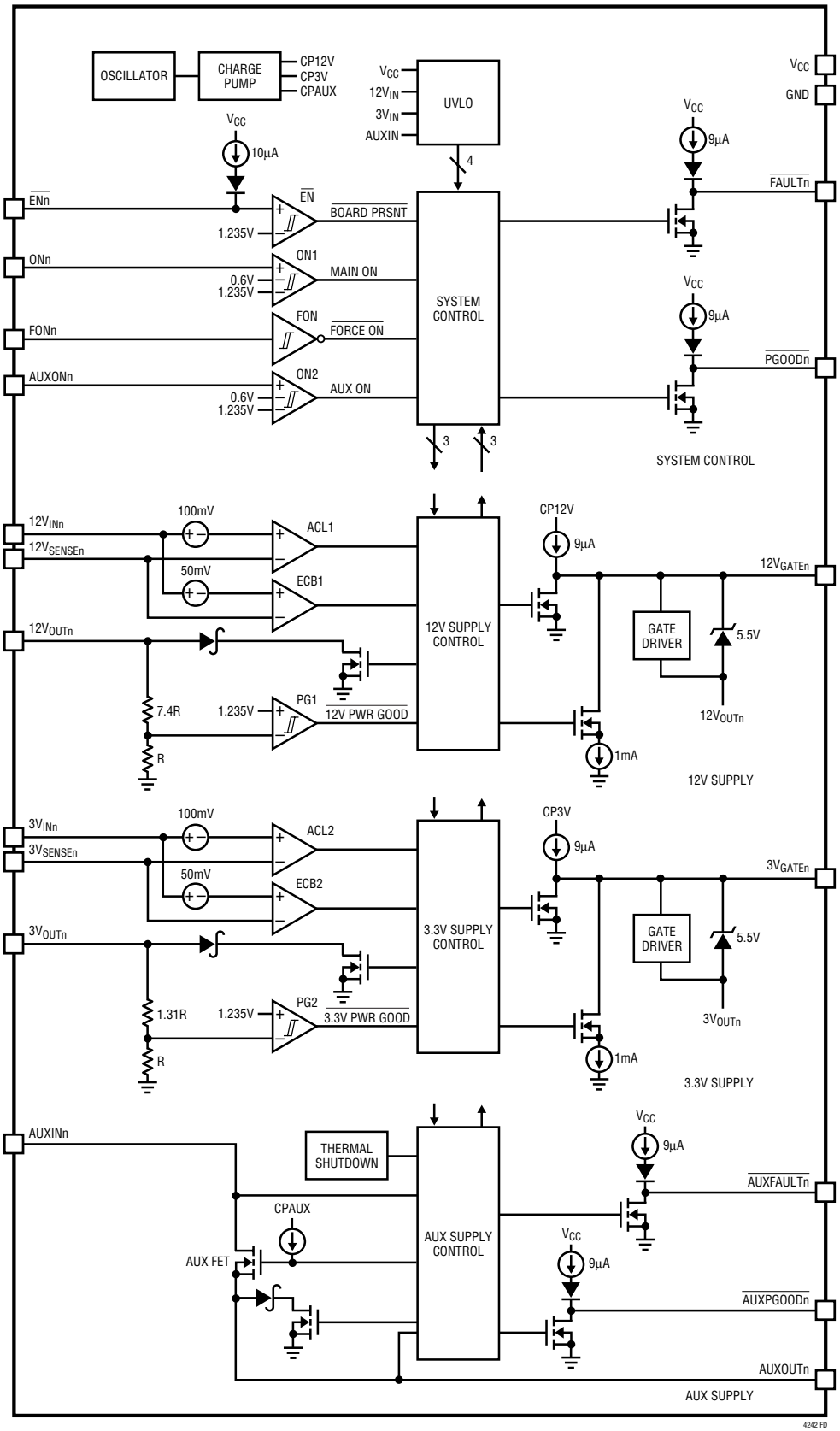
GND: Device Ground. Connect to a ground plane.

ON1/ON2: Main Supply On Control Input. A rising edge turns on the external MOSFETs for the 12V and 3.3V supplies, while a falling edge turns them off. Pull this pin below 0.6V to clear the faults on 12V and 3.3V channels.

$\overline{\text{PGOOD1}}$/$\overline{\text{PGOOD2}}$: Main Supply Power Status Output. This open-drain pin is pulled high by an internal 9µA pull-up when $12V_{OUTn}$ or $3V_{OUTn}$ is below power good threshold, when $\overline{\text{ENn}}$ is high, ONn is low or when V_{CC} or any of the main supplies are in UVLO.

V_{CC}: Device Supply Input. Operates from 2.7V to 6V. An internal undervoltage lockout circuit disables the part until the voltage at V_{CC} exceeds 2.45V.

FUNCTIONAL DIAGRAM



OPERATION

The Functional Diagram displays the main functional elements of this device. The LTC4242 is designed to control the power for two independent slots on a PCI Express backplane, allowing two boards to be safely inserted and removed. During normal operation, the charge pump sources 9µA to turn on the gate of the external N-channel MOSFETs to pass power to the load. The gates of the external MOSFETs are clamped about 5.5V above their sources. The gates of the AUX FETs rise at a slew rate of about 1.25V/ms to control the inrush current.

The electronic circuit breaker (ECB) comparator and analog current limit (ACL) amplifier monitor the load current using the difference between the V_{IN} and SENSE voltage. The threshold of the ACL is set at 2x the ECB threshold. The ACL amplifier limits the current in the load by reducing the gate-to-source voltage of the external MOSFETs in an active control loop. When an overcurrent condition persists for more than 20µs, the MOSFETs are shut off to prevent overheating. FAULT is latched low to signal that an overcurrent condition has occurred on the external MOSFETs controlling the main channels.

The AUX FET's control circuitry has a circuit breaker that trips at 550mA after 20µs. It also incorporates an active current limit amplifier that would limit the current flowing in the AUX FET to about 1.65A. A thermal shutdown circuit shuts off the AUX FET when the die temperature rises above 150°C. AUXFAULT is latched low to signal an overcurrent conditon on the internal FET or thermal shutdown has occurred.

When the switches are off (both internal and external), the OUT pins are discharged to ground through internal N-channel transistors.

The output voltages are monitored using the OUT pins and the PG comparators to determine if the voltage is valid. The power good conditon is signaled by the PGOOD/AUXPGOOD pins using open-drain pull-down transistors.

The Functional Diagram shows the monitoring blocks of the LTC4242. The group of comparators in the system control includes the UVLO, ON and EN comparators. These comparators are used to determine if the external conditions are valid prior to turning on the switches. But first the undervoltage lockout circuit (UVLO) must validate the input supplies and the main supply V_{CC} and generate the power up initialization to the logic circuits.

The FON inverter in the system control is used for operating the LTC4242 in diagnostic mode. In this mode of operation, all pass transistors are forced to turn on, ignoring the undervoltage, circuit breaker/current limiting status and input commands. However, if V_{CC} drops below its UVLO voltage, all switches would be shut off, regardless of FON.

APPLICATIONS INFORMATION

The typical LTC4242 application is in a backplane or motherboard that controls power to two PCI Express slots. The device reports fault and power good status to the system hot plug controller (HPC).

The basic LTC4242 application circuit is shown in Figure 1. Discussion begins with board presence detection in a PCI Express system, the normal turn on and off sequence, the various fault conditons and recovery from fault situations. The force on operation is discussed next followed by the considerations for PCB layout. External component selection is discussed in detail in the Design Example section.

Board Presence Detect

In PCI Express systems, the system board connector uses two signals, PRSNT1 and PRSNT2, to detect the presence of a board and ensure a fully inserted board in the connector as shown in Figure 2. PRSNT2 is routed to the system HPC. Upon a board insertion into the connector, a turn-on command is generated by the HPC to LTC4242 after a programmed HPC debounce delay, as shown in Figure 1. Another method to generate the debounce delay is through the delay network shown in Figure 3.

APPLICATIONS INFORMATION

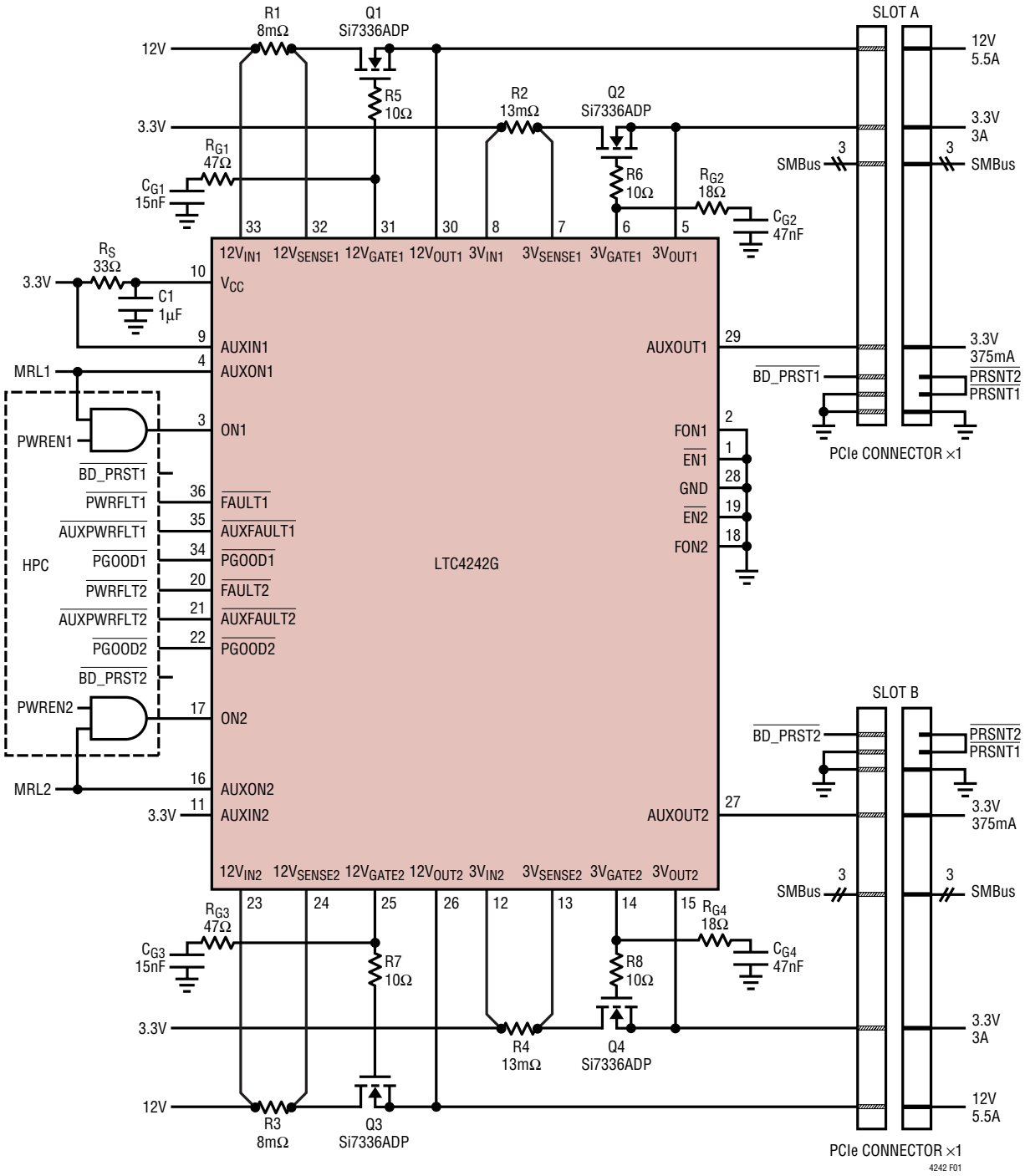


Figure 1. Typical PCI Express Application

APPLICATIONS INFORMATION

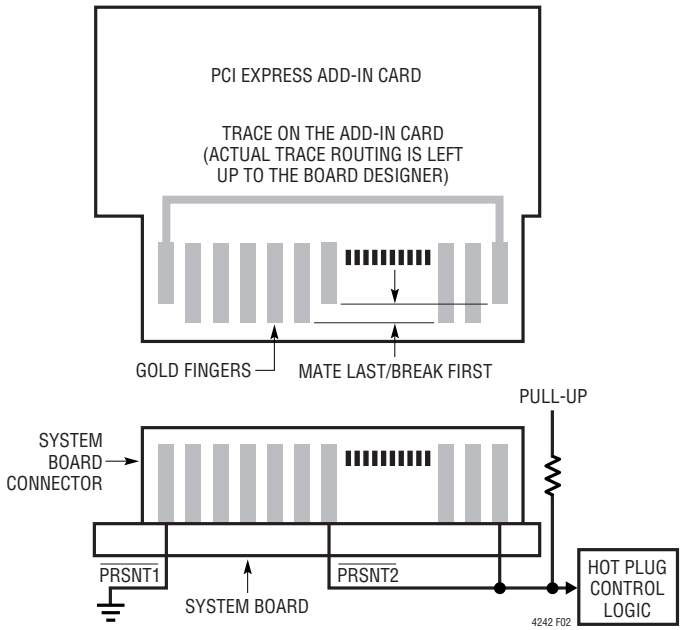


Figure 2. Plug-In Card Insertion/Removal

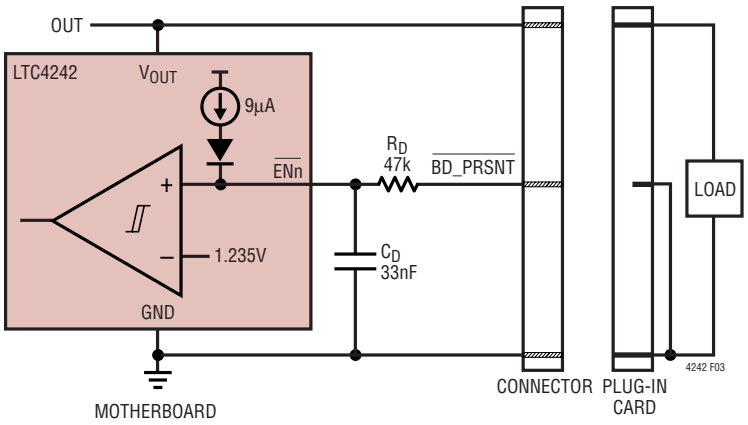


Figure 3. RC Network to Generate Delay During Card Plug-In

When $\overline{PRSNT2}$ pulls low after insertion of a board, the $\overline{ENn}$ pin goes low after a delay as determined by the values of C_D and R_D. For plug-in debounce delay of 1ms and R_D of 47k:

$$C_D = \frac{t_{DELAY1}\ (ms)}{43.5}\ \mu F = 0.023\mu F$$

Choose C_D to be 33nF.

When the board is removed, the power to the slot is disabled after a delay of:

$$t_{DELAY2} = \frac{0.765C_D}{9}\ s = 2.8ms$$

Turn-On Sequence

The PCI Express power supplies are controlled by the external N-channel pass transistors, Q1 through Q4, in the 12V and 3.3V power paths, and internal pass transistors

APPLICATIONS INFORMATION

for the 3.3V auxiliary power paths. Sense resistors R1 to R4 provide input for current fault detection. Resistors R_{G1} to R_{G4} and capacitors C_{G1} to C_{G4} compensate the current control loops. Capacitors C_{G1} to C_{G4} also control the output power-up rate and the inrush current while resistors R5 to R8 prevent high frequency oscillations in N-channel MOSFETs, Q1 to Q4 respectively.

The following conditions must be satisfied before the external and internal switches can be turned on.

1. The device's power supply, V_{CC}, must exceed its undervoltage lockout threshold. To turn on the external/internal switches, the main/auxiliary input supplies must exceed their UVLO thresholds.
2. The $\overline{EN}$ pin must be pulled low to begin the start-up sequence.

When these initial conditions are satisfied, the ON pins are checked. The LTC4242 features per slot ON pins, the AUXON and ON, to allow independent control of the main input supplies (12V and 3.3V) and the 3.3V auxiliary supplies. If the ON pin is high, the switches turn on. If ON is low, the switches turn on when the ON pin is brought high. Figure 4 shows all supplies turning on after $\overline{EN}$ goes low.

Each of the external switches is turned on by charging the GATE with a 9µA current source. The voltage at the GATE pins rises with a slope equal to $9\mu A/C_G$ and the supply inrush current is set at $C_L/C_G \bullet 9\mu A$, where C_L is the capacitance at the supply output.

The gate of the internal switch is slewed resulting in the $3.3V_{AUX}$ supply output powering up at an internally set rate of about 1.25V/ms.

The circuit breaker (ECB) of the input supplies is armed after the input supplies clear UVLO. Once the supplies have been turned on and the outputs are within tolerance, $\overline{PGOOD}$ for the main input supplies and $\overline{AUXPGOOD}$ for the auxiliary input supplies (available for the QFN only) are pulled low.

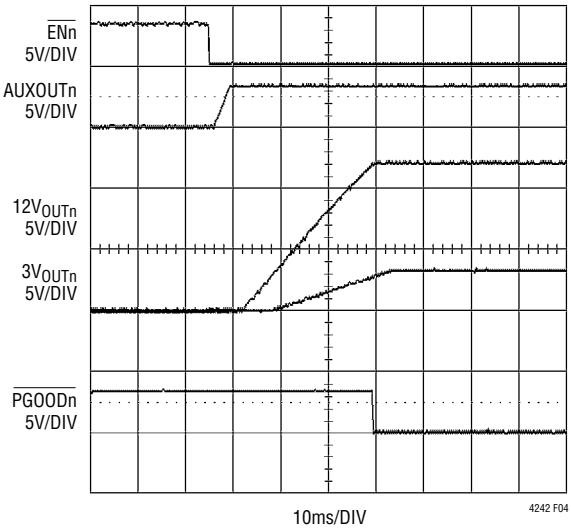


Figure 4. Normal Power-Up Sequence

Turn-Off Sequence

The switches can be turned off by a variety of conditions.

1. The ON/AUXON pin going low would turn off the main/internal switches.
2. $\overline{EN}$ going high turns off all switches.
3. A variety of fault conditions will turn off the switches. These include supply undervoltage and overcurrent circuit breaker faults.
4. When thermal shutdown activates, the internal switch is shut off.

When ON goes low, the main switches are turned off with a 1mA current pulling down the gate to ground. When the main supplies are shut off, the $\overline{PGOOD}$ signal pulls high and the outputs are discharged to ground through internal switches. Similarly, when an auxiliary supply is turned off, the $\overline{AUXPGOOD}$ signal pulls high and its output is discharged to ground through internal switches. Figure 5 shows all supplies being turned off by $\overline{EN}$ going high.

APPLICATIONS INFORMATION

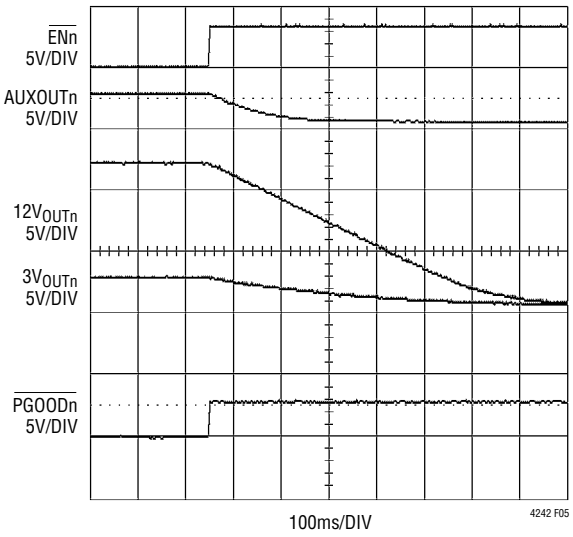


Figure 5. Normal Power-Down Sequence

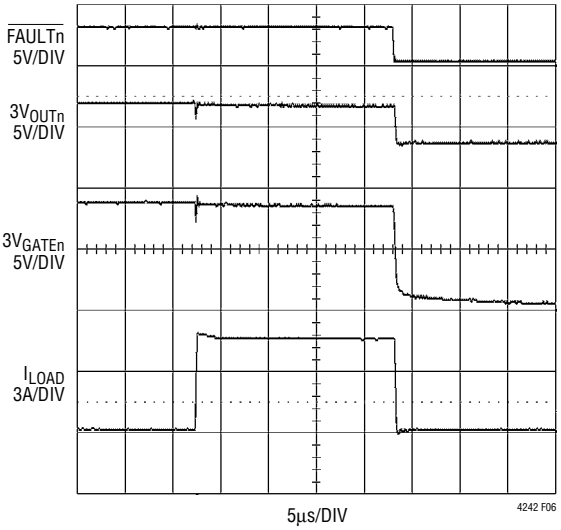


Figure 6. Overcurrent Fault on 3.3V Output

Thermal Shutdown

Each of the two internal switches for the 3.3V auxiliary supplies is protected by an independent thermal shutdown circuit. If the temperature of an internal switch reaches 150°C, the switch shuts down immediately and AUXFAULT is latched low. All other power switches are not affected. The switch is allowed to turn on again by recycling the AUXON pin low then high with the temperature falling below 120°C.

Overcurrent Fault

The LTC4242 features dual level glitch tolerant protection against overcurrent faults for all the supplies. The sense resistor (both internal and external) voltage drop is monitored by an electronic circuit breaker (ECB) comparator and an active current limit (ACL) amplifier. In the event that a supply's current exceeds the ECB threshold, an internal timer is started. If the supply is still overcurrent after 20µs, the ECB trips and the MOSFET turns off immediately, as shown in Figure 6.

During start-up, a supply output could be shorted to ground in the worst case. The inrush current would be limited to the ACL threshold, which is 2x the ECB threshold, and the part will latch off after 20µs.

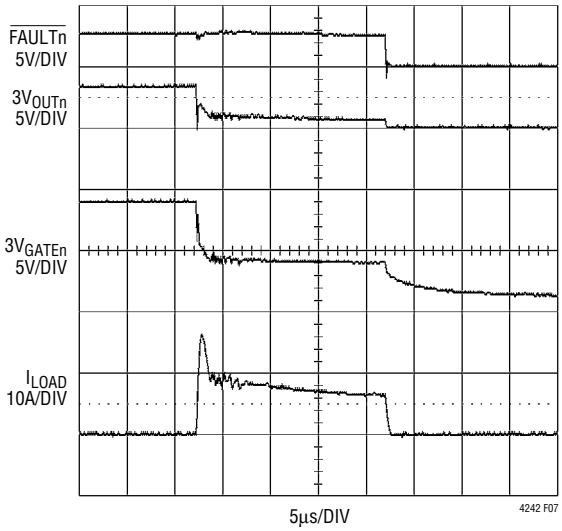


Figure 7. Short-Circuit Fault on 3.3V Output

During an output short circuit, the surge current must be brought to a controlled level within the shortest amount of time to protect the system. The LTC4242's active current limit enters a high current protection mode that immediately turns off the output MOSFET by pulling its gate-to-source voltage to zero. Current in the output MOSFET drops from tens of amps to zero in a few hundred nanoseconds. The input voltage drops during the high current and then spikes upwards due to lead parasitic inductances as the

APPLICATIONS INFORMATION

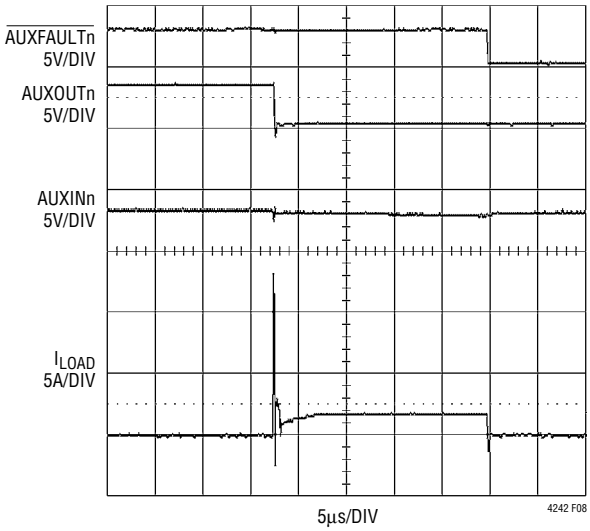


Figure 8. Short-Circuit Fault on 3.3V_{AUX} Output

MOSFET shuts off (see Supply Transients). The compensation network R_G/C_G assists the gate voltage recovery. The ACL limits the current level to 2x the ECB threshold by regulating the gate voltage.

For the internal switch, the ACL limits the supply current to about 3x the circuit breaker current level of 550mA.

The ECB has a 20µs filter delay before latching off to prevent unnecessary resets of the system due to minor transient surges. An overcurrent fault on any of the main outputs (12V or 3.3V) latches off both main outputs without affecting the 3.3V auxiliary output. Similarly, an overcurrent fault on the 3.3V auxiliary output latches off the auxiliary output, without affecting the main outputs.

When there is a shorted load with significant supply lead inductance, the supply pin voltage could collapse before the ACL brings down the gate of the external MOSFET. In this case, the undervoltage lockout circuit, with 18µs filter time, turns off the pass MOSFETs.

Undervoltage Fault

An undervoltage fault occurs when any of the input supplies, $12V_{IN}$, $3V_{IN}$ or AUXIN, falls below its undervoltage threshold for more than 18µs. This turns off the switches immediately. An undervoltage on the 3.3V auxiliary supply will not cause the main supplies to shut off and vice versa. An undervoltage fault on any of the main supplies shuts off both main supply switches. If V_{CC} falls below its UVLO threshold for more than 38µs, all switches are turned off. The switches are allowed to turn on when the supply voltages and V_{CC} rise above their respective undervoltage thresholds.

Power Good Fault

A power good fault occurs when any supply output drops below its power good threshold for more than 20µs. A power good fault on the main/AUX supplies causes the $\overline{PGOOD}/\overline{AUXPGOOD}$ to be pulled high. There are a variety of conditions which must be satisfied for $\overline{PGOOD}/\overline{AUXPGOOD}$ to be asserted low:

1. The output voltage is above power good threshold
2. $\overline{EN}$ pin is low
3. The input voltage is above the undervoltage threshold
4. ON pin is high
5. Thermal shutdown not activated

Resetting Faults

To reset an overcurrent fault on the main outputs, bring ON low or the faulting supply below its undervoltage lockout (UVLO) threshold. To reset an overcurrent or thermal shutdown fault on the auxiliary output, bring AUXON low or the auxiliary suppy below its UVLO threshold. Bringing V_{CC} below its UVLO threshold resets all overcurrent and thermal shutdown faults. The part cannot be reset when fault overide, FON, is high.

Auto-Retry After a Fault

As shown in Figure 9, the LTC4242 can be configured to automatically retry after a fault condition by connecting both the $\overline{FAULT}$ and ON pins together with an RC network. The auto-retry circuit will attempt to restart the LTC4242 after a circuit breaker trip, as shown in the timing diagram of Figure 10.

$$t_{OFF} \approx \frac{R_{AUTO} \bullet C_{AUTO} \bullet (1.235 - V_{OL})}{2.065 + R_{AUTO} \bullet 9\mu A}$$

For the component values shown, t_{OFF} = 3.3ms. Since the duration of a short is less than 40µs in the worst case, the auto-retry duty cycle is 1.3%.

APPLICATIONS INFORMATION

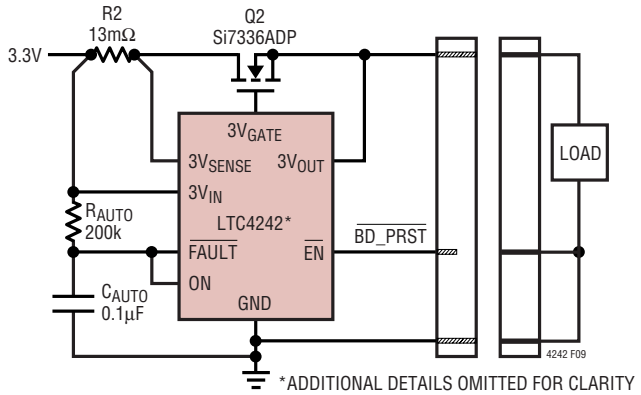


Figure 9. Auto-Retry Application

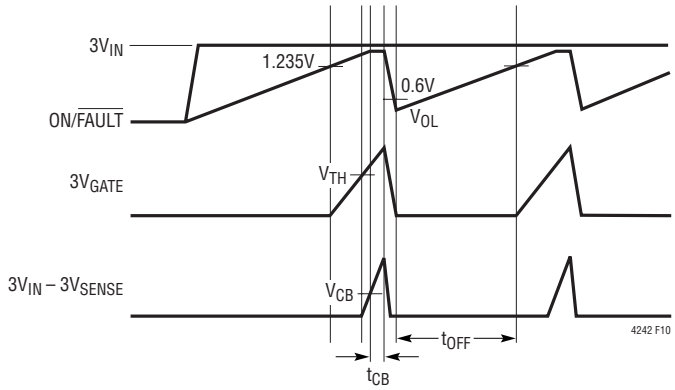


Figure 10. Auto-Retry Timing

GATE Pin Voltage

The minimum gate drive voltage is 4.5V, therefore, logic level N-channel MOSFETs should be used for the external switches to maintain adequate gate enhancement. The GATE pins are clamped at a typical value of 5.5V above the respective OUT pins.

Compensating the Active Current Loop

The active current limit circuit is compensated using the resistor R_G and the slew rate control capacitor C_G. The value of C_G is selected based on the inrush current allowed. The R_G value should be experimentally determined. A suggested value range for R_G is between 10Ω and 100Ω.

V_{CC} Power Supply

The LTC4242 derives its power from V_{CC}. A bypass capacitor of 1µF should be connected between this pin and ground. If V_{CC} is derived from the input supplies of $3V_{IN}$ or AUXIN, a lowpass filter shown in Figure 11 should be used.

This RC network allows the LTC4242 to ride through a $3V_{IN}$/AUXIN short-circuit transient without collapsing below the V_{CC} UVLO threshold. AUXIN or $3V_{IN}$ may have narrow but high glitches due to parasitic inductance. Since the absolute maximum rating for V_{CC} is 7V compared to 10V for AUXIN and $3V_{IN}$, the R_S and C1 values should be chosen to damp the peak voltage seen by V_{CC} below 7V.

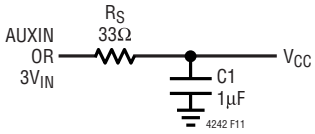


Figure 11. RC Network for V_{CC} Filtering

Force ON Operation

When the FON pin is pulled high and $\overline{EN}$ is low, the LTC4242 operates in the diagnostic mode. All the input supplies' power switches are forced to turn on, regardless of undervoltage conditions on the input supplies, status of the ON pins and the fault latch. The contents in the fault latch would be preserved during this time and no change of state would occur after the part is configured to operate in the diagnostic mode. If the output current exceeds the ECB threshold, $\overline{FAULT}$/$\overline{AUXFAULT}$ is pulled low immediately, but does not latch. The undervoltage lockout on V_{CC} turns off all the switches, regardless of the status of FON. During thermal shutdown, the internal switch is shut off to prevent overheating, even if FON is high. The main power switches remain on as FON is high. Care must be taken to ensure the outputs are not short circuited since there is no current limit mechanism in diagnostic mode.

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Yet another mode of operation is the Force ON with current limit mode. To enter this mode, pull both FON and EN high. In this mode of operation, the ACLs are enabled with the 20µs filter time disabled. The fault latch of the AUX supply can be latched if the AUX's I_{CBAUX} is exceeded. AUXFAULT indicates whether the AUX channel FET is on or off. To enter normal operation, pull FON and EN low and recycle the ON and AUXON pins.

PCB Layout Considerations

For proper operation of the LTC4242's circuit breaker, a Kelvin connection to the sense resistors is required. The Kelvin sense PCB layout traces should be minimum length, closed together, balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout for the 12V sense resistor and the power MOSFET is illustrated in Figure 12.

In Hot Swap applications where load currents can be 10A, narrow PCB tracks exhibit more resistance than wider tracks and hence, operate at higher temperatures. Since the sheet resistance of 1oz copper foil is approximately 0.5mΩ/square, track resistances and voltage drops add up quickly in high current applications. Thus, to keep PCB track resistance, voltage drop and temperature rise to a minimum, the suggested trace width in these applications for 1oz copper foil is 0.03" for each ampere of DC current.

In the majority of applications, it will be necessary to use plated-through vias to make circuitry connections from components layers to power and ground layers internal to the PCB. For 1oz copper foil plating, a general rule is 1A of DC current per via making sure the via is properly dimensioned so that solder completely fills any void. Check with your PCB fabrication facility for via current specifications.

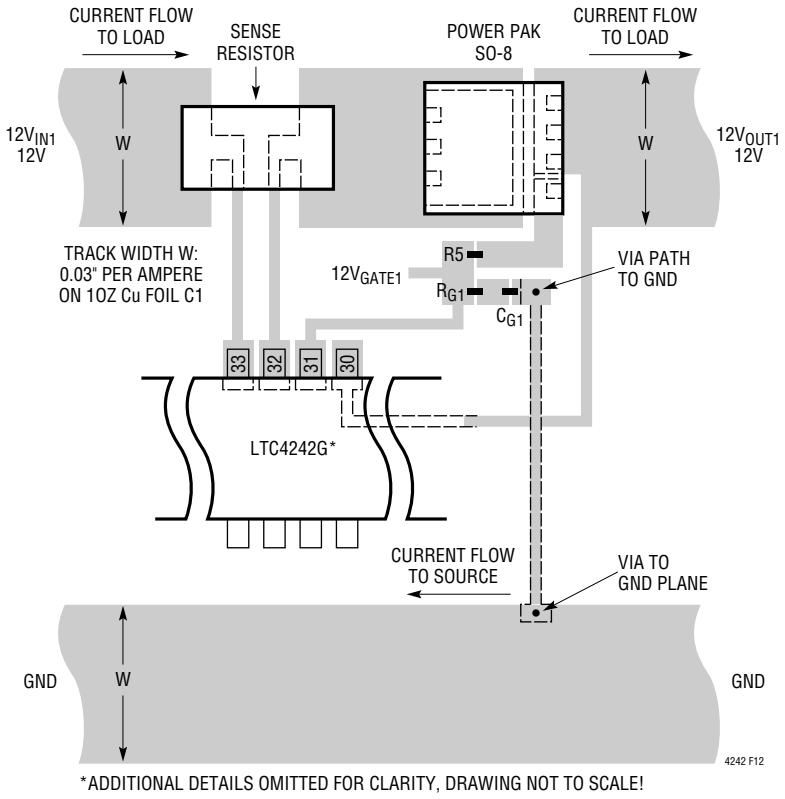


Figure 12. Recommended Layout for Power MOSFET, Sense Resistor and GATE Components for the 12V Rail

APPLICATIONS INFORMATION

In system board applications, large bypass capacitors (≥10µF) are recommended at each of the system input supplies to minimize supply glitches as a result of large inrush or fault currents.

It is important to put C1, the bypass capacitor for the V_{CC} pin as close as possible between the V_{CC} and GND pins.

Design Example

Consider a PCI Express Hot Swap application example with the following power supply requirements:

Table 1. PCI Express Power Supply Requirements

SUPPLY VOLTAGE	MAXIMUM SUPPLY CURRENT	MAXIMUM LOAD CAPACITANCE
12V	5.5A	2000µF
3.3V	3.0A	1000µF
$3.3V_{AUX}$	375mA	150µF

1. Select an R_{SENSE} value for each supply. Calculate the R_{SENSE} value based on the maximum load current and the lower circuit breaker threshold limit, $\Delta V_{SENSE(CB)(MIN)}$. In a PCI Express connector, five pins are allocated for the 12V supply, three pins for the 3.3V supply and one pin for $3.3V_{AUX}$. The current rating of a connector pin is 1.1A. If a 1% tolerance is assumed for the sense resistors, then the following values of resistances should suffice:

Table 2. Sense Resistance Values

VOLTAGE SUPPLY	R_{SENSE} (1%)	$I_{TRIP(MIN)}$	$I_{TRIP(MAX)}$
12V	8mΩ	5.6A	6.9A
3.3V	13mΩ	3.4A	4.3A

2. Assume no load current at start-up and the inrush current charges the load capacitance. Compute gate capacitance with:

$$C_{GATE} = \frac{I_{GATE(UP)} \bullet t_1}{V_{OUT}} \quad (2)$$

t_1 is the time to charge up the load capacitor.

With $I_{GATE(UP)(MAX)}$ = 13µA and t_1 = 10ms:

a. For 12V Supply, C_{GATE} = 11nF

b. For 3.3V Supply, C_{GATE} = 39nF

So a value of 15nF and 47nF (±10%) should suffice for the 12V and 3.3V supplies respectively. The worst-case t_1 and inrush currents are tabulated in Table 3.

Table 3. Worst-Case t_1 and Inrush Current

VOLTAGE SUPPLY	$t_{1(MIN)}$	$t_{1(MAX)}$	MAX I_{INRUSH}
12V	13ms	40ms	2.4A
3.3V	11ms	34ms	0.4A

For the internal switch, the slew rate (SR) at the $3.3V_{AUX}$ supply output is limited to 1.7V/ms max. The inrush current can then be calculated according to:

$$I_{INRUSH(MAX)} = C_{LOAD} \bullet SR_{MAX} \quad (3)$$

The inrush current must be lower than 385mA ($I_{CBAUX(MIN)}$) for proper start-up. Assuming a tolerance of 30% for the load capacitance, the value of C_{LOAD} should not exceed 170µF.

3. Next is the selection of MOSFETs for the 12V and 3.3V main input supplies. The Si7336ADP's on resistance is less than 4mΩ at V_{GS} = 4.5V, 25°C and it is a good choice for 3.3V and 12V main supplies.

Since the maximum load for the 3.3V supply is 3A, the MOSFET may dissipate up to 36mW. The Si7336ADP has a maximum junction-to-ambient thermal resistance of 50°C/W. This gives a junction temperature of 51.8°C when operating at a case temperature of 50°C. According to the Si7336ADP's Normalized On-Resistance vs Junction Temperature curve, the device's on resistance can be expected to increase by about 12% over its room temperature value. Recalculation for steady-state R_{ON} and junction temperature yield approximately 4.5mΩ and 52°C, respectively. The voltage drop across the 3.3V sense resistor and series MOSFET at 3A and at 50°C PCB temperature is less than 53mV.

The MOSFET dissipates power during inrush charging of the output load capacitor. Assuming no load current, the MOSFET's dissipated power equals the final load capacitor stored energy. Therefore, average MOSFET dissipated power is:

$$P_{ON} = \frac{C_L \bullet V_{OUT}^2}{2 \bullet t_1} \quad (4)$$

APPLICATIONS INFORMATION

Using P_{ON} and t_1 to look up the MOSFETs' single pulse $\theta_{JA(MAX)}$ from the manufacturer's Transient Thermal Impedance Graph, the worst-case junction-to-ambient temperature rise occurs for the 12V MOSFET.

Table 4. MOSFET Power-Up Temperature Rise Calculation

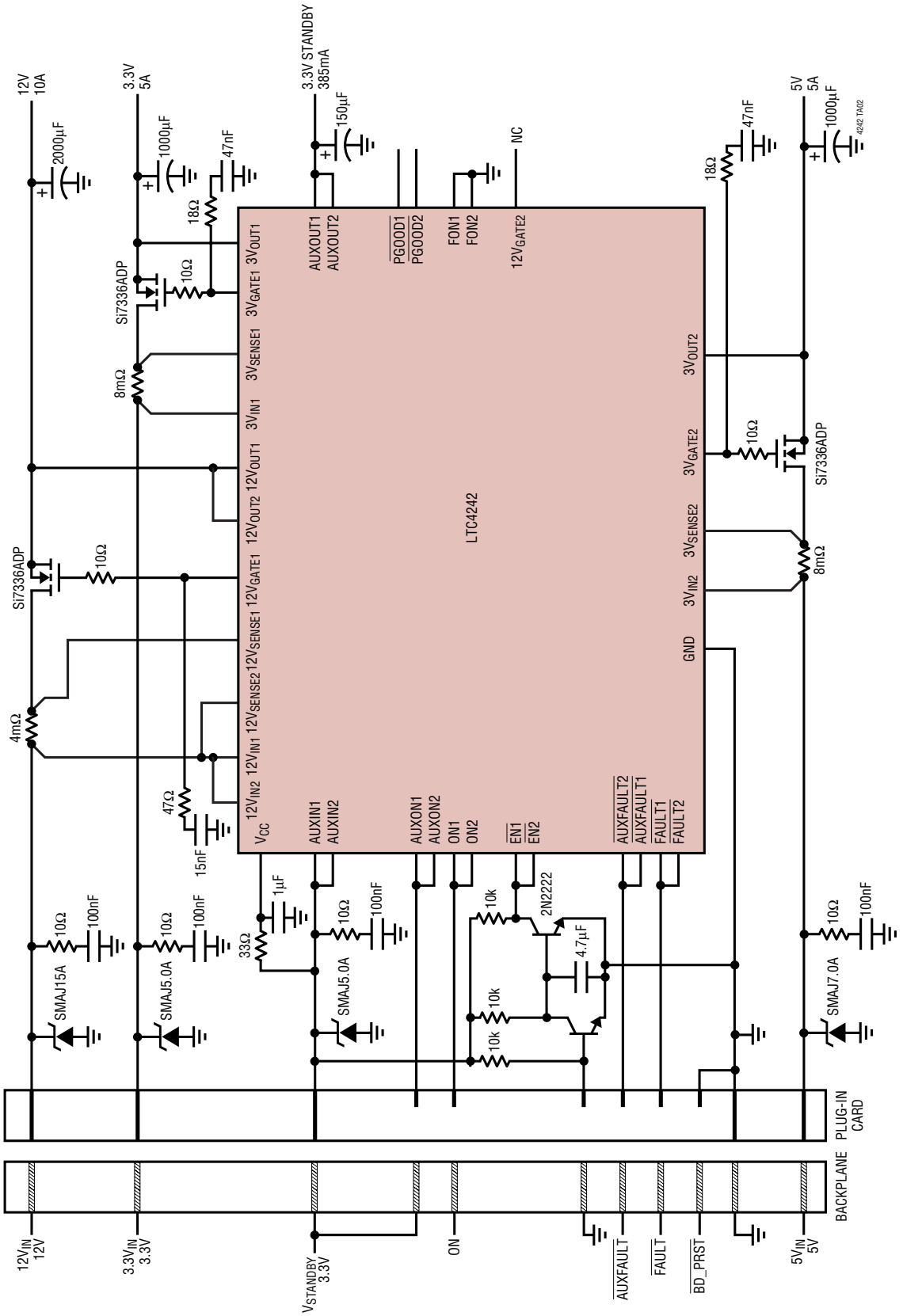
VOLTAGE SUPPLY	P_{ON}	$\theta_{JA(MAX)}$	ΔT
12V	11W	0.75°C/W	8.3°C
3.3V	0.5W	0.6°C/W	0.3°C

There is a 20µs filter time when large current of 2x circuit breaker's threshold can flow in the switches. This time is short enough to cause minimal increase in the junction-to-ambient temperature of the MOSFETs, in the event of powering up into short circuit or short circuiting after power up. Therefore, in these events, it can be safely assumed that the MOSFETs would have minimal thermal stress on them.

If the LTC4242 operates in the diagnostic mode, user must ensure a safe joule heating limit of the external MOSFET. The internal switch will be disabled once the temperature reaches 150°C, thereby preventing overheating.

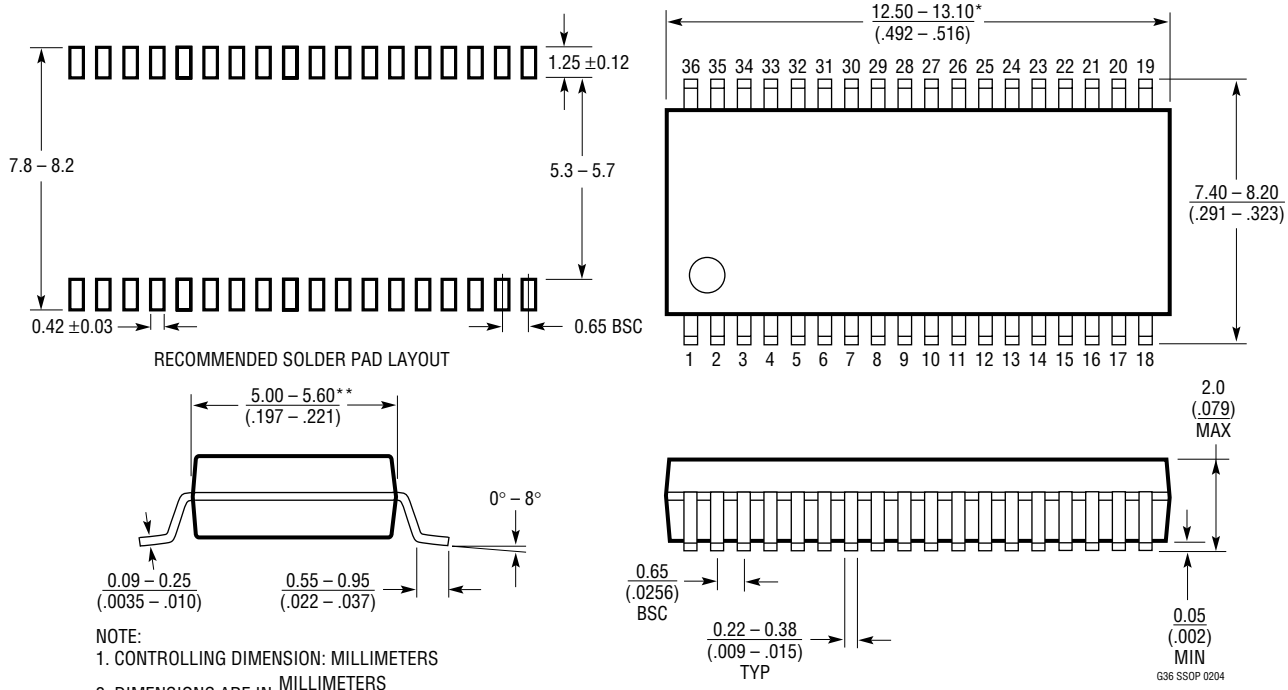
TYPICAL APPLICATION

Standalone Hot Swap Application for Four Supplies: 12V, 5V, 3.3V and 3.3V Standby



PACKAGE DESCRIPTION

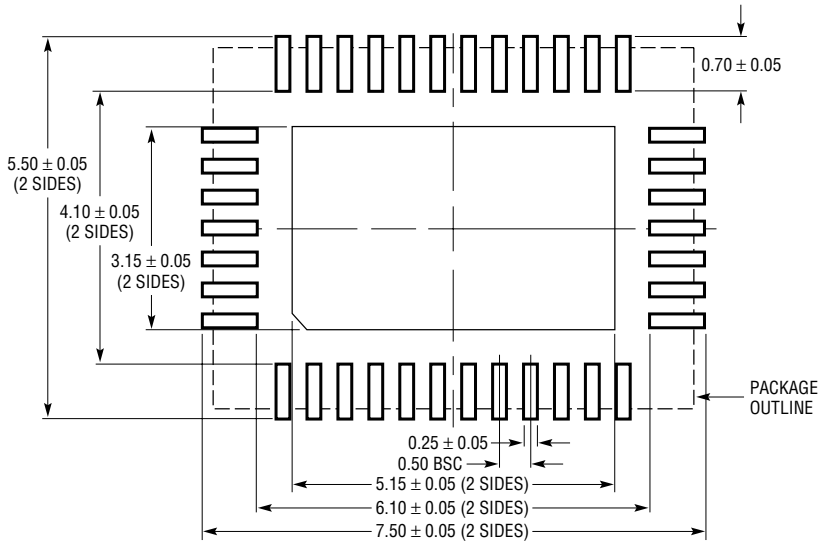
G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



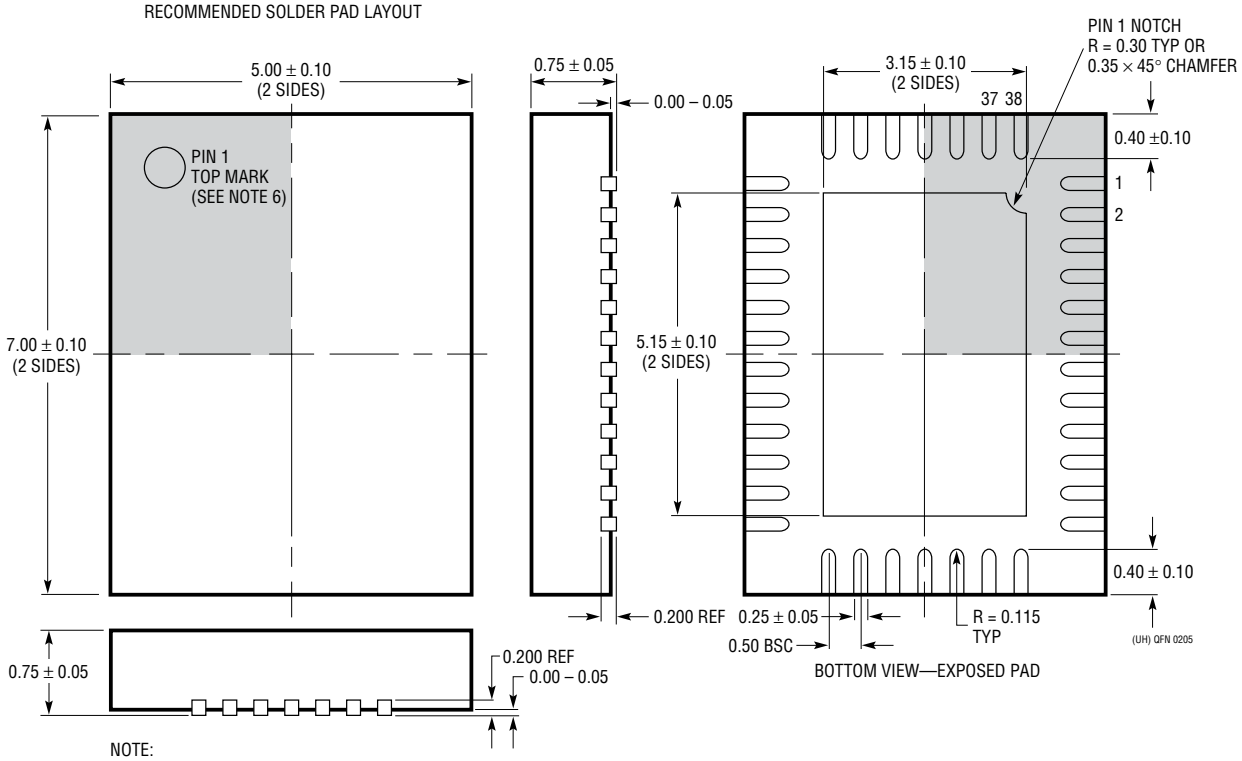
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701)



RECOMMENDED SOLDER PAD LAYOUT



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE