Rugged, CompactPCI Bus Hot Swap Controllers

FEATURES

- **Controls –12V, 3.3V, 5V and 12V Supplies**
- **±14.4V Absolute Maximum Rating for $12V_{IN}$ and $–12V_{IN}$ Input Pins**
- **Insensitive to Supply Voltage Transients**
- Adjustable Foldback Current Limit with Circuit Breaker
- LOCAL_PCI_RST# Logic On-Chip
- PRECHARGE Output Biases I/O Pins During Card Insertion and Extraction
- LTC4244-1 Designed for Applications without –12V
- Available in 20-Lead Narrow SSOP Package

APPLICATIONS

- Hot Board Insertion into CompactPCI Bus

DESCRIPTION

The LTC®4244/LTC4244-1 are Hot Swap™ controllers that allow a board to be safely inserted into and removed from a CompactPCI™ bus slot. External N-channel transistors control the 5V and 3.3V supplies while on-chip switches control the ±12V supplies. The 3.3V and 5V supplies can be ramped up at an adjustable rate. Electronic circuit breakers protect all four supplies against overcurrent faults. After the power-up cycle is complete, the TIMER pin capacitor serves as auxiliary V_{CC} allowing the LTC4244/LTC4244-1 to function without interruption in the presence of voltage spikes on the $12V_{IN}$ supply. The $\overline{PWRGD}$ output indicates when all four supplies are within tolerance. The OFF/$\overline{ON}$ pin is used to cycle board power or reset the circuit breaker. The PRECHARGE output can be used to bias the bus I/O pins during card insertion and extraction. PCI_RST# is combined on-chip with HEALTHY# in order to generate LOCAL_PCI_RST#.

TYPICAL APPLICATION

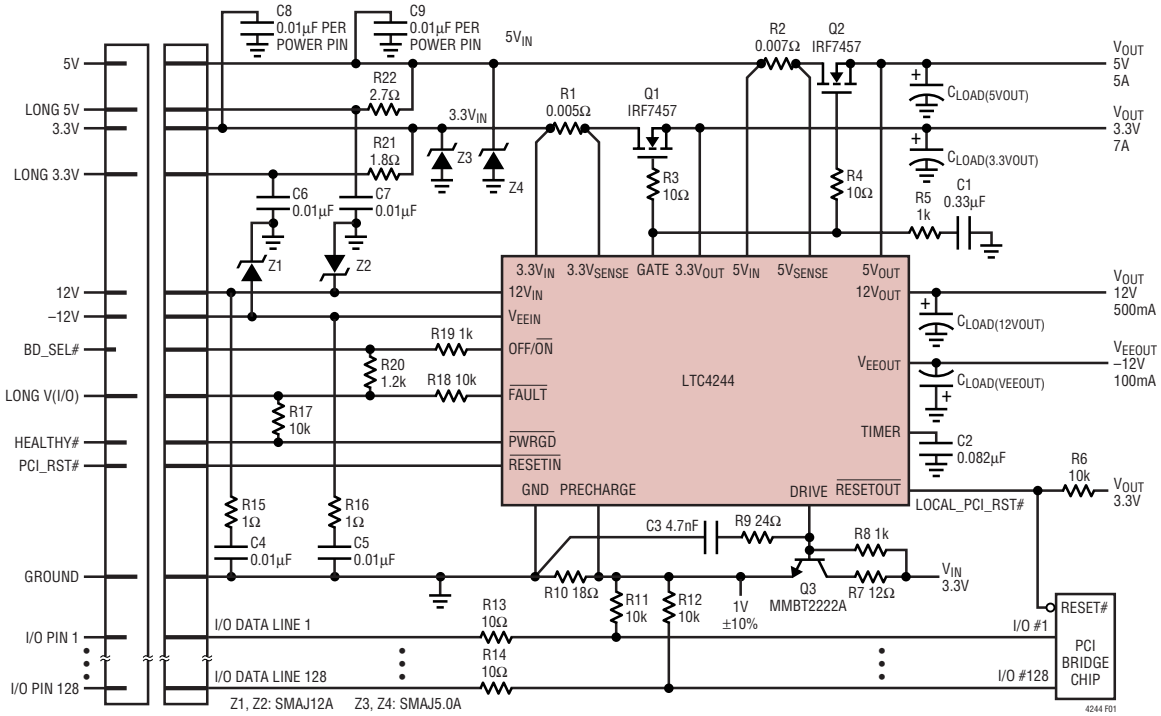


Figure 1. Typical Compact PCI Application

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

Supply Voltages
- $12V_{IN}$ 14.4V
- V_{EEIN} ..... –14.4V

Input Voltages (OFF/$\overline{ON}$, $\overline{RESETIN}$) .....–0.3V to 13.5V

Output Voltages ($\overline{FAULT}$, $\overline{PWRGD}$, $\overline{RESETOUT}$) .....–0.3V to 13.5V

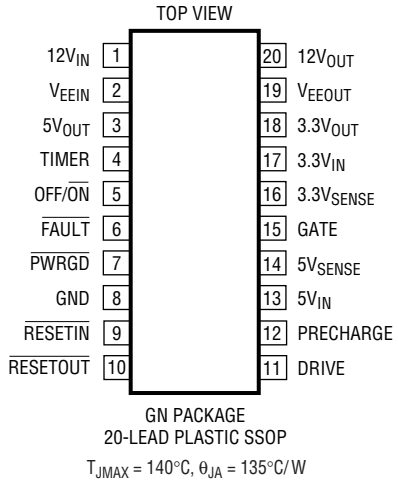
Analog Voltages and Currents
- $5V_{OUT}$, DRIVE, $5V_{IN}$, $3.3V_{SENSE}$, $3.3V_{IN}$, $3.3V_{OUT}$, $5V_{SENSE}$ .....–0.3V to 13.5V
- PRECHARGE, GATE ..... ±20mA
- V_{EEOUT} .....–14.4V to 0.3V
- TIMER, $12V_{OUT}$ .....–0.3V to 14.4V

Operation Temperature Range
- LTC4244C/LTC4244C-1 ..... 0°C to 70°C
- LTC4244I/LTC4244I-1 ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 140°C, θ_{JA} = 135°C/W

ORDER PART NUMBER
LTC4244CGN
LTC4244CGN-1
LTC4244IGN
LTC4244IGN-1

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{EEIN} = –12V, $V_{3.3VIN}$ = 3.3V, V_{5VIN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD}	V_{12VIN} Supply Current	OFF/$\overline{ON}$ = 0V	●		4	10	mA
V_{LKO}	Undervoltage Lockout	$12V_{IN}$, Ramping Down	●	8	9	10	V
		$5V_{IN}$, Ramping Down	●	4	4.25	4.5	V
		$3.3V_{IN}$, Ramping Down	●	2.25	2.5	2.75	V
		V_{EEIN}, Ramping Up (LTC4244 Only)	●	–8.25	–9.25	–10.25	V
		TIMER, Ramping Down, V_{12VIN} = 6V	●	8.25	9.25	10.25	V
V_{FB}	Foldback Current Limit Voltage	$V_{FB} = (V_{5VIN} – V_{5VSENSE})$, V_{5VOUT} = 0V, TIMER = 0V	●	11	16	21	mV
		$V_{FB} = (V_{5VIN} – V_{5VSENSE})$, V_{5VOUT} = 3V, TIMER = 0V	●	46	51	56	mV
		$V_{FB} = (V_{3.3VIN} – V_{3.3VSENSE})$, $V_{3.3VOUT}$ = 0V, TIMER = 0V	●	11	16	21	mV
		$V_{FB} = (V_{3.3VIN} – V_{3.3VSENSE})$, $V_{3.3VOUT}$ = 2V, TIMER = 0V	●	46	51	56	mV
V_{CB}	Circuit Breaker Trip Voltage	$V_{CB} = (V_{5VIN} – V_{5VSENSE})$, TIMER = FLOAT	●	45	52	57	mV
		$V_{CB} = (V_{3.3VIN} – V_{3.3VSENSE})$, TIMER = FLOAT	●	45	52	57	mV
t_{OC}	Overcurrent Fault Response Time	$(V_{5VIN} – V_{5VSENSE})$ = 100mV, TIMER = FLOAT	●	17	25	35	µs
		$(V_{3.3VIN} – V_{3.3VSENSE})$ = 100mV, TIMER = FLOAT	●	17	25	35	µs
$I_{GATE(UP)}$	GATE Pin Output Current	OFF/$\overline{ON}$ = 0V, V_{GATE} = 2V, TIMER = 0V	●	–20	–67	–100	µA
$I_{GATE(DN)}$		V_{GATE} = 5V, OFF/$\overline{ON}$ = 4V	●	20	60	100	µA
$I_{GATE(\overline{FAULT})}$		OFF/$\overline{ON}$ = 0V, V_{GATE} = 2V, TIMER = FLOAT, $\overline{FAULT}$ = 0V	●	4	8	16	mA
ΔV_{GATE}	External Gate Voltage	$\Delta V_{GATE} = (V_{12VIN} – V_{GATE})$, I_{GATE} = –1µA	●		0.6	1	V
ΔV_{12V}	Internal Switch Voltage Drop	$\Delta V_{12V} = (V_{12VIN} – V_{12VOUT})$, I = 500mA	●		225	600	mV
ΔV_{VEE}		$\Delta V_{VEE} = (V_{EEOUT} – V_{EEIN})$, I_{EE} = 100mA	●		110	250	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{EEIN} = –12V, $V_{3.3VIN}$ = 3.3V, V_{5VIN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CL}	Current Foldback	$12V_{IN}$ = 12V, $12V_{OUT}$ = 0V, TIMER = 0V	●	–100	–360	–1000	mA
		$12V_{IN}$ = 12V, $12V_{OUT}$ = 10V, TIMER = 0V	●	–550	–850	–1500	mA
		V_{EEIN} = –12V, V_{EEOUT} = 0V, TIMER = 0V	●	50	225	350	mA
		V_{EEIN} = –12V, V_{EEOUT} = –10V, TIMER = 0V	●	350	610	870	mA
T_{TS}	Thermal Shutdown Temperature	Junction Temperature, Ramping Up			150		°C
V_{TH}	Power Good Threshold Voltage	$12V_{OUT}$, Ramping Down	●	10.8	11.1	11.4	V
		$5V_{OUT}$, Ramping Down	●	4.50	4.61	4.75	V
		$3.3V_{OUT}$, Ramping Down	●	2.80	2.90	3.00	V
		V_{EEOUT}, Ramping Up, LTC4244 Only	●	–10.8	–11.1	–11.4	V
V_{IL}	Logic Input Low Voltage	OFF/$\overline{ON}$, $\overline{RESETIN}$, $\overline{FAULT}$	●			0.8	V
V_{IH}	Logic Input High Voltage	OFF/$\overline{ON}$, $\overline{RESETIN}$, $\overline{FAULT}$	●	2			V
I_{IN}	OFF/$\overline{ON}$, $\overline{RESETIN}$ Input Current	OFF/$\overline{ON}$, $\overline{RESETIN}$ = 0V	●			±10	µA
		OFF/$\overline{ON}$, $\overline{RESETIN}$ = 12V	●			±10	µA
	$\overline{RESETOUT}$, $\overline{FAULT}$ Leakage Current	$\overline{RESETOUT}$, $\overline{FAULT}$ = 5V, OFF/$\overline{ON}$ = 0V, $\overline{RESETIN}$ = 3.3V	●			±10	µA
	$\overline{PWRGD}$ Output Current	$\overline{PWRGD}$ = 5V, OFF/$\overline{ON}$ = 4V	●			±10	µA
	$5V_{SENSE}$ Input Current	$5V_{SENSE}$ = 5V, $5V_{OUT}$ = 0V	●		57	100	µA
	$3.3V_{SENSE}$ Input Current	$3.3V_{SENSE}$ = 3.3V, $3.3V_{OUT}$ = 0V	●		56	100	µA
	$5V_{IN}$ Input Current	$5V_{IN}$ = 5V, TIMER = 0V	●		0.8	1.5	mA
	$3.3V_{IN}$ Input Current	$3.3V_{IN}$ = 3.3V, TIMER = FLOAT	●		510	700	µA
		$3.3V_{IN}$ = 3.3V, TIMER = 0V	●		400	550	µA
	$5V_{OUT}$ Input Current	$5V_{OUT}$ = 5V, OFF/$\overline{ON}$ = 0V, TIMER = 0V	●		107	200	µA
	$3.3V_{OUT}$ Input Current	$3.3V_{OUT}$ = 3.3V, OFF/$\overline{ON}$ = 0V, TIMER = 0V	●		170	300	µA
	PRECHARGE Input Current	$V_{PRECHARGE}$ = 1V	●		0.1	10	µA
I_{TIMER}	TIMER Pin Current	OFF/$\overline{ON}$ = 0V, V_{TIMER} = 0V	●	16	21	26	µA
		OFF/$\overline{ON}$ = 5V, V_{TIMER} = 5V	●	25	45	70	mA
V_{TIMER}	TIMER Threshold Voltage	TIMER_HI, (V_{12VIN} – V_{TIMER}), $\overline{FAULT}$ = 0V, Ramping Up	●	1.3	1.6	1.9	V
		TIMER_LO, V_{TIMER}, Ramping Down	●	0.5	0.8	1.1	V
ΔV_{TIMER}	External Timer Voltage	ΔV_{TIMER} = (V_{12VIN} – V_{TIMER}), I_{TIMER} = –1µA	●			1	V
R_{DIS}	$12V_{OUT}$ Discharge Resistance	OFF/$\overline{ON}$ = 4V	●		440	1000	Ω
	$5V_{OUT}$ Discharge Resistance	OFF/$\overline{ON}$ = 4V	●		200	500	Ω
	$3.3V_{OUT}$ Discharge Resistance	OFF/$\overline{ON}$ = 4V	●		200	500	Ω
	V_{EEOUT} Discharge Resistance	OFF/$\overline{ON}$ = 4V	●		390	1000	Ω
V_{OL}	Output Low Voltage	$\overline{PWRGD}$, $\overline{RESETOUT}$, $\overline{FAULT}$, I = 1mA	●			0.4	V
V_{PXG}	PRECHARGE Reference Voltage	V_{DRIVE} = 2V	●	0.95	1	1.05	V

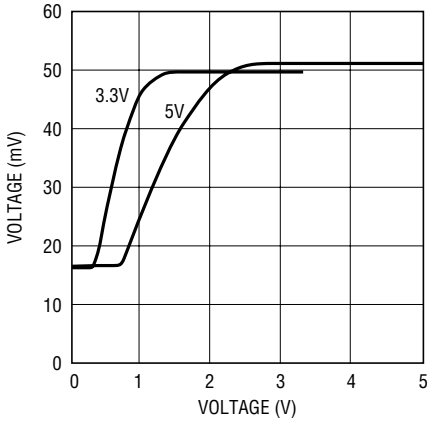
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

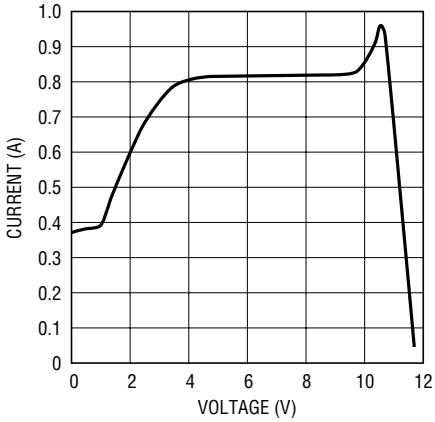
Note 3: The $12V_{IN}$ and V_{EEIN} pins will withstand transient surges up to ±15V, respectively, upon hot insertion.

TYPICAL PERFORMANCE CHARACTERISTICS

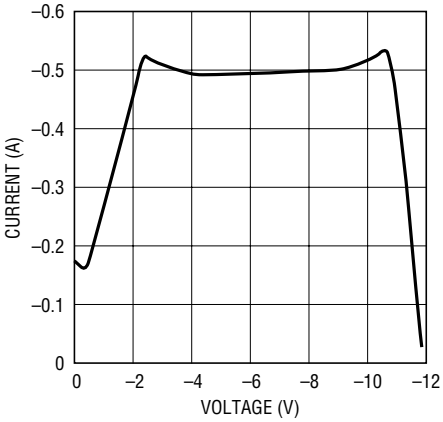
3.3V and 5V Current Foldback Profile



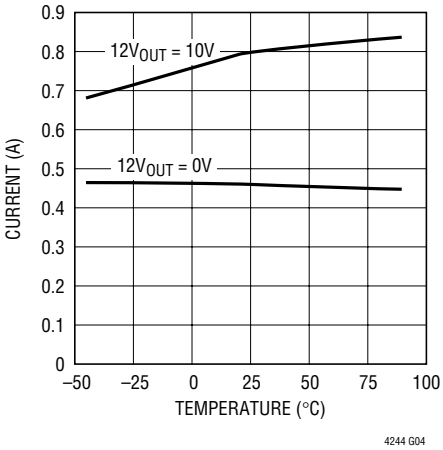
$12V_{OUT}$ Current vs $12V_{OUT}$ Voltage



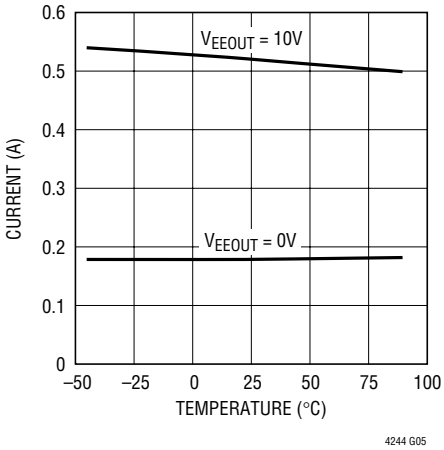
V_{EEOUT} Current vs V_{EEOUT} Voltage



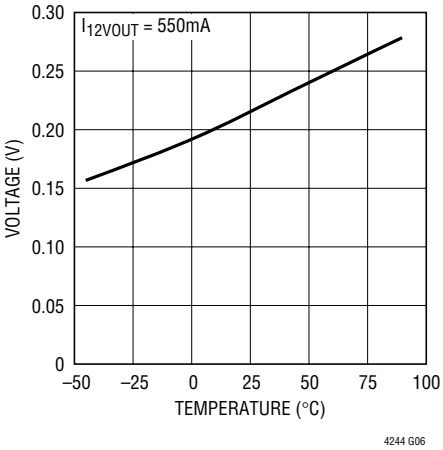
12V Foldback Current Limit vs Temperature



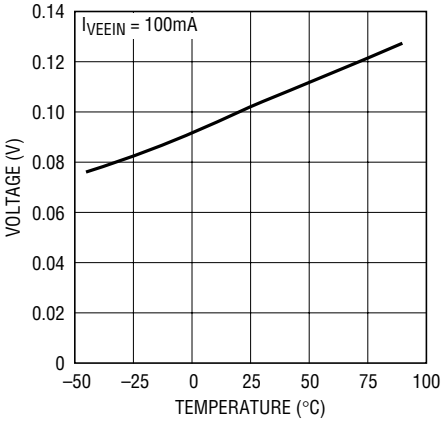
V_{EE} Foldback Current Limit vs Temperature



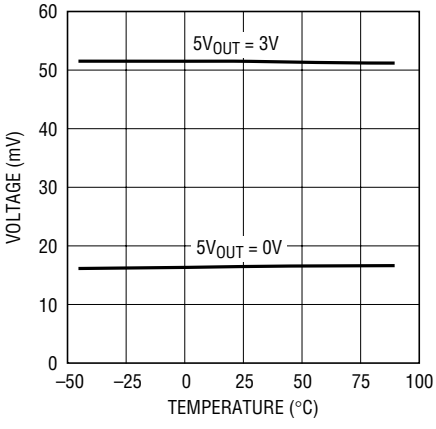
12V Internal Switch Voltage Drop vs Temperature



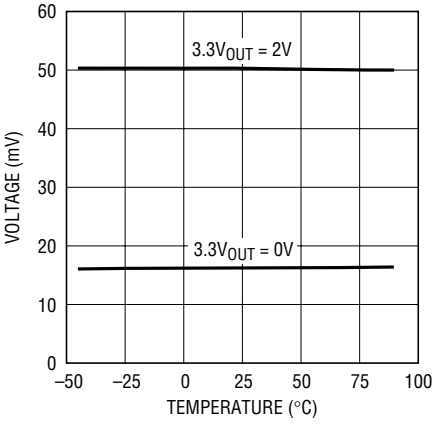
V_{EE} Internal Switch Voltage Drop vs Temperature



$5V_{IN}$ Foldback Current Limit Voltage vs Temperature

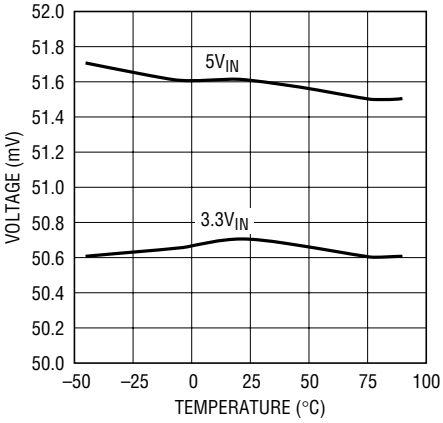


$3.3V_{IN}$ Foldback Current Limit Voltage vs Temperature

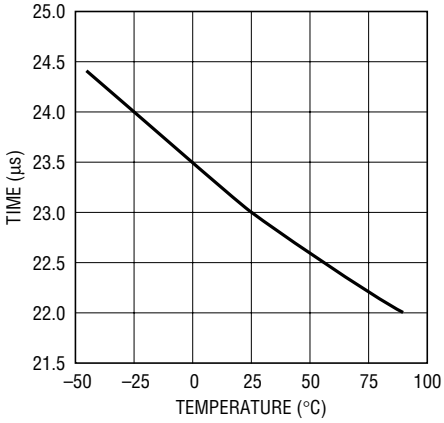


TYPICAL PERFORMANCE CHARACTERISTICS

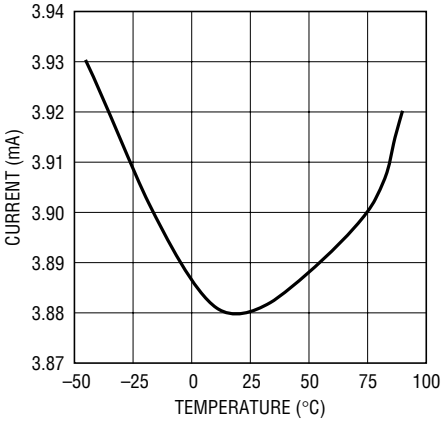
3.3V_{IN} and 5V_{IN} Circuit Breaker Trip Voltage vs Temperature



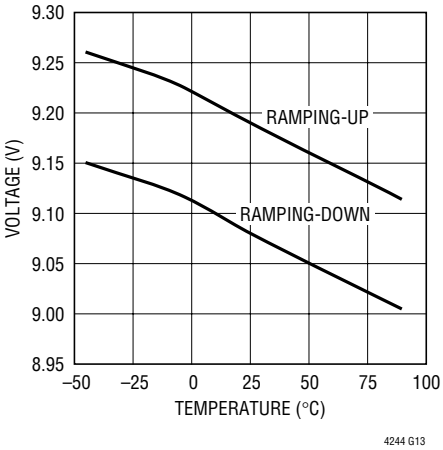
3.3V_{IN} and 5V_{IN} Circuit Breaker Trip Filter Time vs Temperature



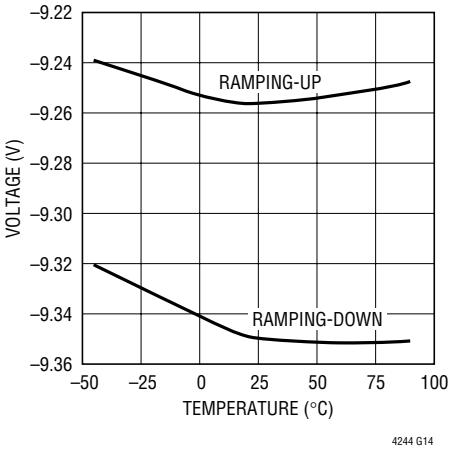
12V_{IN} Supply Current vs Temperature



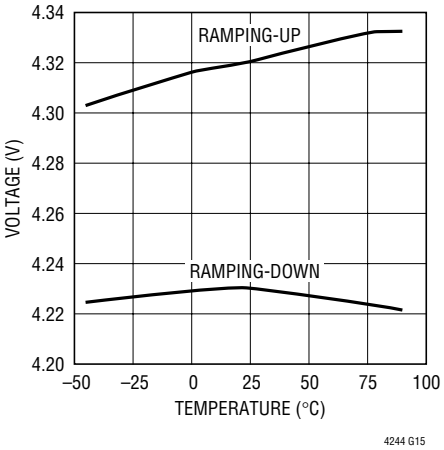
12V_{IN} Undervoltage Lockout vs Temperature



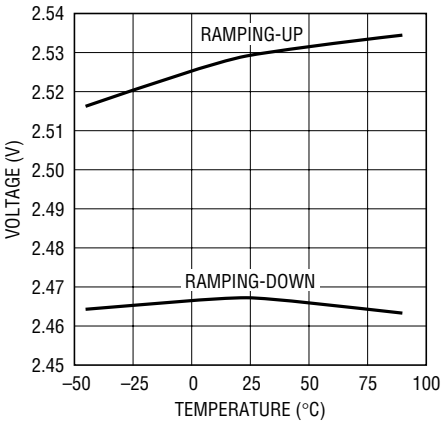
V_{EEIN} Undervoltage Lockout vs Temperature



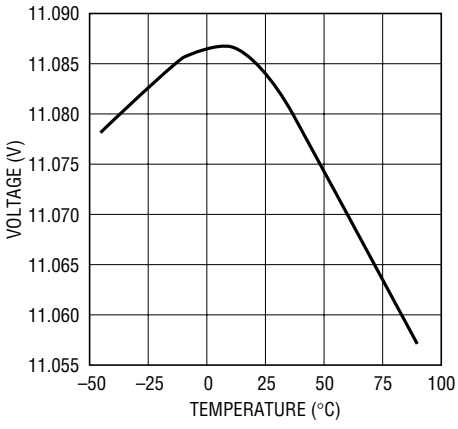
5V_{IN} Undervoltage Lockout vs Temperature



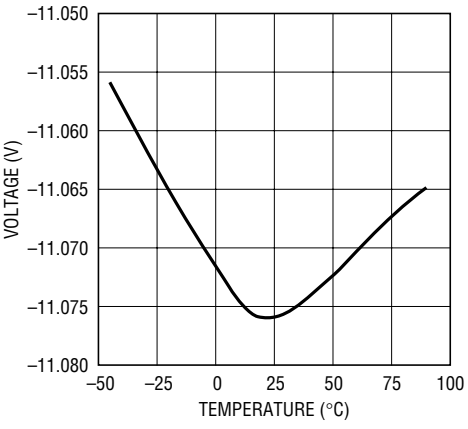
3.3V_{IN} Undervoltage Lockout vs Temperature



12V_{OUT} Powergood Threshold Voltage vs Temperature

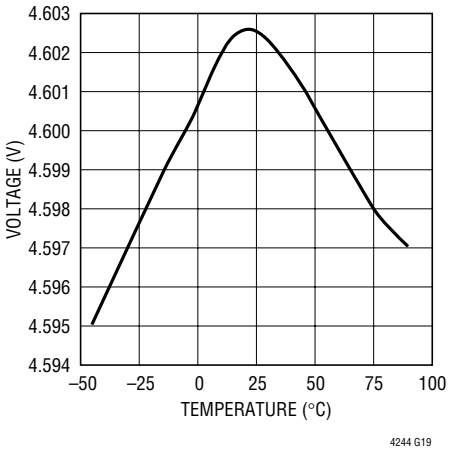


V_{EEIN} Powergood Threshold Voltage vs Temperature

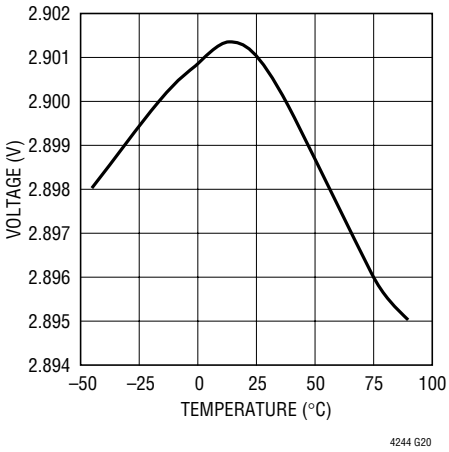


TYPICAL PERFORMANCE CHARACTERISTICS

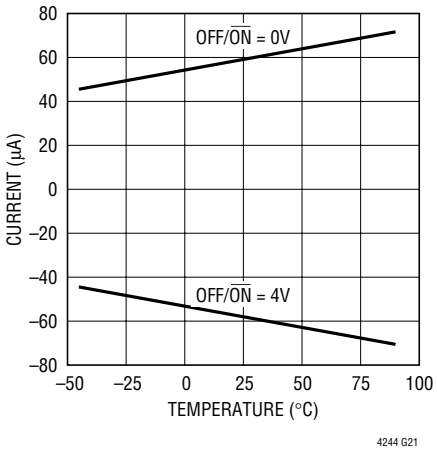
$5V_{OUT}$ Powergood Threshold Voltage vs Temperature



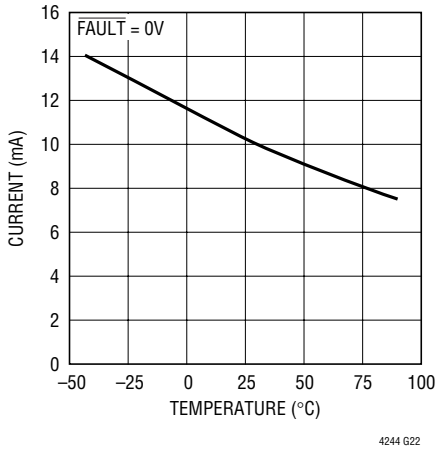
$3.3V_{OUT}$ Powergood Threshold Voltage vs Temperature



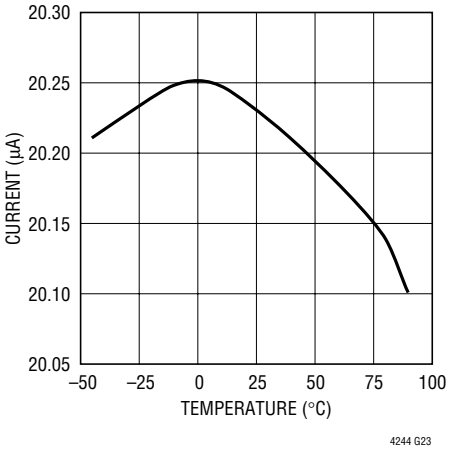
Gate Pin Current vs Temperature



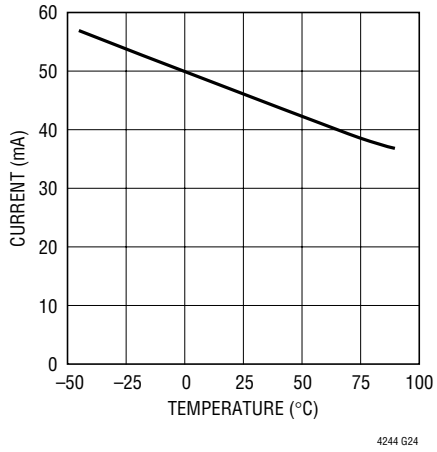
Gate Pin Fault Current vs Temperature



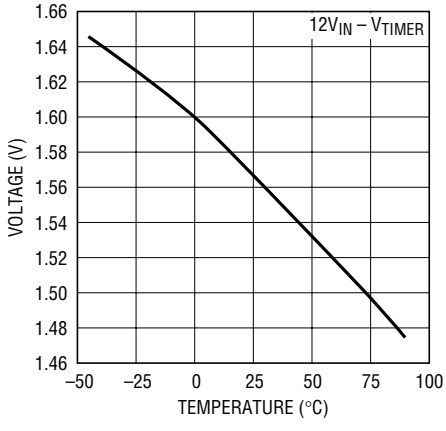
Timer Pin On Current vs Temperature



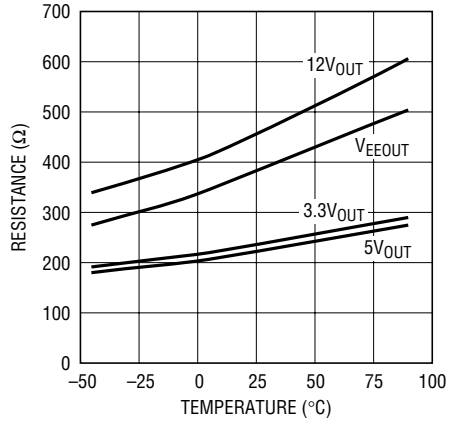
Timer Pin Off Current vs Temperature



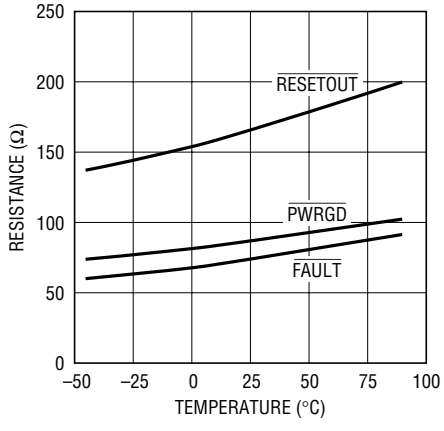
Timer Threshold Voltage vs Temperature



Discharge Resistance vs Temperature



V_{OL} vs Temperature



PIN FUNCTIONS

$12V_{IN}$ (Pin 1): 12V Supply Input. A 0.5Ω switch is connected between $12V_{IN}$ and $12V_{OUT}$ with a foldback current limit. An undervoltage lockout circuit prevents the switches from turning on while the $12V_{IN}$ pin voltage is less than 9V. $12V_{IN}$ also provides power to the LTC4244's internal V_{CC} node.

V_{EEIN} (Pin 2): –12V Supply Input. A 1Ω switch is connected between V_{EEIN} and V_{EEOUT} with a foldback current limit. An undervoltage lockout circuit prevents the switches from turning on while the V_{EEIN} pin voltage is greater than –9.25V. The V_{EEIN} undervoltage lockout function is disabled for the LTC4244-1.

$5V_{OUT}$ (Pin 3): 5V Output Sense. The $\overline{PWRGD}$ pin will not pull low until the $5V_{OUT}$ pin voltage exceeds 4.61V. A 200Ω active pull-down discharges $5V_{OUT}$ to ground when the power switches are turned off.

TIMER (Pin 4): Current Fault Inhibit Timing Input and Auxiliary V_{CC}. Connect a capacitor from TIMER to GND. When the LTC4244 is turned on, a 21μA pull-up current source is connected to TIMER. Current limit faults will be ignored until the voltage at the TIMER pin rises to within 1.6V of $12V_{IN}$. After the TIMER pin has completed ramping up, the TIMER capacitor serves as an auxiliary charge reservoir for V_{CC} in the event the $12V_{IN}$ pin voltage momentarily drops below the undervoltage lockout threshold voltage. When the LTC4244 is turned off ($OFF/\overline{ON}$ > 2V), the TIMER pin is pulled down to GND. After the TIMER pin voltage drops to within 0.8V of GND, the TIMER latch is reset and the part is ready for another power cycle.

$OFF/\overline{ON}$ (Pin 5): Digital Input. Connect the CPCI BD_SEL# signal to the $OFF/\overline{ON}$ pin. When the $OFF/\overline{ON}$ pin is pulled low, the GATE pin is pulled high by a 67μA current source and the internal 12V and –12V switches are turned on. When the $OFF/\overline{ON}$ pin is pulled high, the GATE pin will be pulled to ground by a 60μA current source and the 12V and –12V switches turn off.

$\overline{FAULT}$ (Pin 6): Open-Drain Digital I/O. $\overline{FAULT}$ is pulled low when a current limit fault is detected. Current limit faults are ignored until the voltage at the TIMER pin is within 1.6V of $12V_{IN}$. Once the TIMER cycle is complete, $\overline{FAULT}$ will pull low and the LTC4244 latches off in the event of an overcurrent fault. The part will remain in the latched off state until the $OFF/\overline{ON}$ pin is cycled high then low. Forcing the $\overline{FAULT}$ pin low with an external pull-down will cause the part to latch into the off state after a 25μs deglitching time.

$\overline{PWRGD}$ (Pin 7): Open-Drain Digital Power Good Output. Connect the CPCI HEALTHY# signal to the $\overline{PWRGD}$ pin. $\overline{PWRGD}$ remains low while $V_{12VOUT} \geq 11.1V$, $V_{3.3VOUT} \geq 2.9V$, $V_{5VOUT} \geq 4.61V$, and $V_{EEOUT} \leq -11.1V$. When any of the supplies falls below its power good threshold voltage, $\overline{PWRGD}$ will go high after a 14μs deglitching time.

GND (Pin 8): Device Ground.

$\overline{RESETIN}$ (Pin 9): Digital Input. Connect the CPCI PCI_RST# signal to the $\overline{RESETIN}$ pin. Pulling the $\overline{RESETIN}$ pin low will cause $\overline{RESETOUT}$ to pull low. $\overline{RESETOUT}$ will also pull low when $\overline{PWRGD}$ is high.

PIN FUNCTIONS

$\overline{\text{RESETOUT}}$ (Pin 10): Open-Drain Digital Output. Connect the CPCI_LOCAL_RST# signal to the $\overline{\text{RESETOUT}}$ pin. $\overline{\text{RESETOUT}}$ is the logical combination of the $\overline{\text{RESETIN}}$ and $\overline{\text{PWRGD}}$.

DRIVE (Pin 11): Precharge Base Drive Output. Provides base drive for an external NPN emitter-follower that in turn biases the PRECHARGE node.

PRECHARGE (Pin 12): Precharge Monitor Input. An internal error amplifier servos the DRIVE pin voltage to keep the PRECHARGE node at 1V. See Applications Information for generating voltages other than 1V. If not used, tie the PRECHARGE pin to ground.

$5V_{IN}$ (Pin 13): 5V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the $5V_{IN}$ pin is less than 4.25V.

$5V_{SENSE}$ (Pin 14): 5V Current Limit Sense. With a sense resistor placed in the supply path between $5V_{IN}$ and $5V_{SENSE}$, the GATE pin voltage will be adjusted to maintain a constant 51mV across the sense resistor and a constant current through the switch while the TIMER pin is low. A foldback feature makes the current limit decrease as the voltage at the $5V_{OUT}$ pin approaches GND. When the TIMER pin is high, the circuit breaker function is enabled. If the voltage across the sense resistor exceeds 52mV, the circuit breaker is tripped after a 25µs time delay. In the event of a short-circuit or large overcurrent transient condition, the GATE pin voltage will be adjusted to maintain a constant 150mV across the sense resistor and a constant current through the switch.

GATE (Pin 15): High Side Gate Drive for the External 3.3V and 5V N-Channel Pass Transistors. An external series RC network is required for current limit loop compensation and setting the minimum ramp-up time. During power-up, the slope of the voltage rise at the GATE is set by the 67µA current source connected through a Schottky diode to $12V_{IN}$ and the external capacitor connected to GND (C1 in Figure 1) or by the 3.3V or 5V current limit and the bulk capacitance in the $3.3V_{OUT}$ or $5V_{OUT}$ supply lines. During power down, the slew rate of the GATE voltage is set by the 60µA current source connected to GND and the external GATE capacitor (C1 in Figure 1).

The voltage at the GATE pin will be modulated to maintain a constant current when either the 5V or 3.3V supplies go into current limit. In the event of an overcurrent fault, the GATE pin is immediately pulled to GND.

$3.3V_{SENSE}$ (Pin 16): 3.3V Current Limit Sense. With a sense resistor placed in the supply path between $3.3V_{IN}$ and $3.3V_{SENSE}$, the GATE pin voltage will be adjusted to maintain a constant 51mV across the sense resistor and a constant current through the switch while the TIMER pin is low. A foldback feature makes the current limit decrease as the voltage at the $3.3V_{OUT}$ pin approaches GND. When the TIMER pin is high, the circuit breaker function is enabled. If the voltage across the sense resistor exceeds 52mV, the circuit breaker is tripped after a 25µs time delay. In the event of a short-circuit or large overcurrent transient condition, the GATE pin voltage will be adjusted to maintain a constant 150mV across the sense resistor and a constant current through the switch.

If no 3.3V input supply is available, short the $3.3V_{SENSE}$ pin to the $5V_{IN}$ pin.

PIN FUNCTIONS

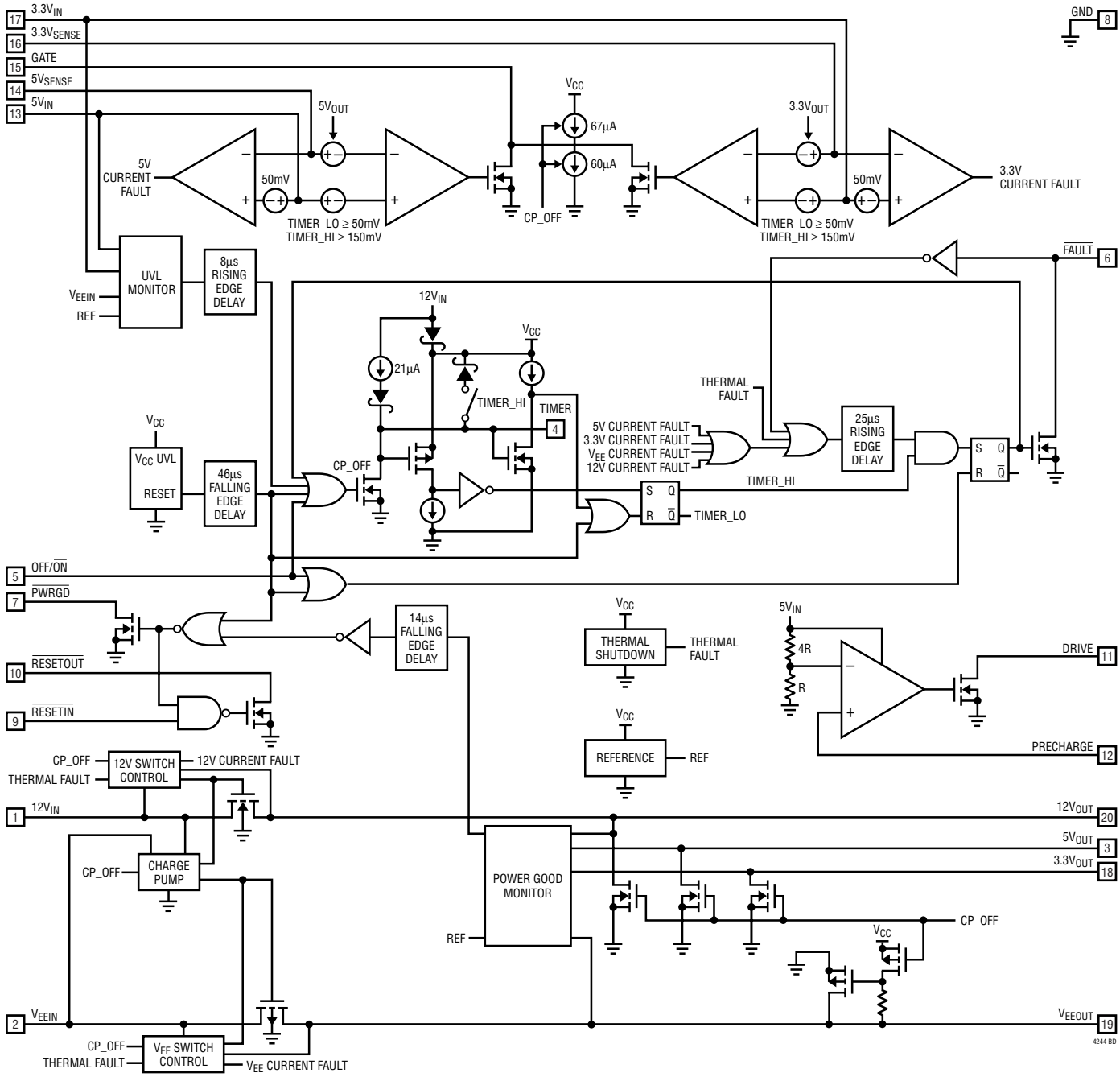
$3.3V_{IN}$ (Pin 17): 3.3V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the $3.3V_{IN}$ pin is less than 2.5V. If no 3.3V input supply is available, short the $3.3V_{IN}$ pin to the $5V_{IN}$ pin.

$3.3V_{OUT}$ (Pin 18): Analog Input Used to Monitor the 3.3V Output Supply Voltage. The $\overline{PWRGD}$ pin cannot pull low until the $3.3V_{OUT}$ pin voltage exceeds 2.9V. If no 3.3V input supply is available, tie the $3.3V_{OUT}$ pin to the $5V_{OUT}$ pin. A 200Ω active pull-down discharges $3.3V_{OUT}$ to ground when the power switches are turned off.

V_{EEOUT} (Pin 19): -12V Supply Output. A 1Ω switch is connected between V_{EEIN} and V_{EEOUT}. V_{EEOUT} must be less than –11.1V before the $\overline{PWRGD}$ pin pulls low. The V_{EEOUT} power good comparator is disabled for the LTC4244-1. A 390Ω active pull-up discharges V_{EEOUT} to ground when the power switches are turned off.

$12V_{OUT}$ (Pin 20): 12V Supply Output. A 0.5Ω switch is connected between $12V_{IN}$ and $12V_{OUT}$. $12V_{OUT}$ must exceed 11.1V before the $\overline{PWRGD}$ pin can pull low. A 440Ω active pull-down discharges $12V_{OUT}$ to ground when the power switches are turned off.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Hot Circuit Insertion

When a circuit board is inserted into a live CompactPCI (CPCI) bus, the supply bypass capacitors can draw huge inrush currents from the CPCI power bus as they charge up. These transient currents can create glitches on the power bus, causing other boards in the system to reset.

The LTC4244 is designed to turn a board's back-end supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live CPCI connector without glitching the system power supplies. It also protects the system supplies from shorts, precharges the bus I/O connector pins during hot insertion and extraction, and monitors the supply voltages.

The LTC4244 is specifically designed for CPCI applications where the Hot Swap controller resides on the plug-in board.

LTC4244 Feature Summary

- Allows safe insertion and removal from a CPCI backplane.
- Controls all four CPCI supplies: -12V, 12V, 3.3V and 5V.
- Adjustable foldback current limit for the 5V and 3.3V supplies: an adjustable analog current limit with a value that depends on the output voltage. If the output is shorted to ground the current limit drops to keep power dissipation and supply glitches to a minimum.
- 12V and –12V circuit breakers: if either supply remains in analog foldback current limit for more than 25µs, the circuit breakers will trip, the supplies are turned off and the $\overline{\text{FAULT}}$ pin is pulled low.
- Adjustable 5V and 3.3V circuit breakers: if either supply exceeds its current limit for more than 25µs, the circuit breaker will trip, the supplies will be turned off and the $\overline{\text{FAULT}}$ pin is asserted low. In the event of a short circuit on either supply, an analog current limit will prevent the supply current from exceeding three times the circuit breaker threshold current.
- Current limit during power up: the supplies are allowed to power up in current limit. This allows the LTC4244 to power up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is adjustable using the TIMER pin capacitor.
- Internal 12V and –12V power switches.
- $\overline{\text{PWRGD}}$ output: monitors the voltage status of the four back-end supply voltages.
- PCI_RST# combined on chip with HEALTHY# to create LOCAL_PCI_RST# output. Simply connect the PCI_RST# signal to the $\overline{\text{RESETIN}}$ pin and the LOCAL_PCI_RST# signal to the open-drain $\overline{\text{RESETOUT}}$ pin.
- Precharge output: on-chip reference and error amplifier provide 1V for biasing bus I/O connector pins during CPCI card insertion and extraction.
- TIMER/AUX. V_{CC}: After power-up, the TIMER pin capacitor serves as auxiliary V_{CC}, thus enabling the LTC4244 to ride out large voltage spikes on the $12V_{IN}$ supply without interruption.
- Undervoltage lockout: All four input voltages are protected by undervoltage lockouts.
- Space saving 20-pin SSOP package.

LTC4244 vs LTC1644

The LTC4244 is pin-for-pin compatible with the LTC1644. There are, however, some important differences between the two parts:

- TIMER: The LTC4244's TIMER pin threshold voltage is 1.6V below V_{12VIN} vs 1V for the LTC1644. After power-up, the LTC4244's TIMER pin also doubles as auxiliary V_{CC}.
- V_{EEIN} UVL: The LTC4244 has a –9.5V UVL threshold protecting the V_{EEIN} supply. The LTC1644 has no V_{EEIN} UVL feature.

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- $5V_{IN}$ UVL Threshold Voltage: The LTC4244's $5V_{IN}$ UVL threshold voltage is 4.25V vs. 2.5V for the LTC1644.
- V_{EEOUT} $\overline{PWRGD}$ Threshold Voltage: The LTC4244 V_{EEOUT} power good threshold voltage is –11.1V vs –10.5V for the LTC1644.
- Absolute Maximum Ratings: The LTC4244's absolute maximum ratings for the $12V_{IN}$ and V_{EEIN} pins are ±14.4V, respectively, vs ±13.2V for the LTC1644.
- 5V/3.3V Circuit Breakers: If a short-circuit occurs after power-up, the LTC4244 actively limits the voltage dropped across the external 5V and 3.3V sense resistors to 150mV for 25µs before tripping the circuit breaker. In the event either the 5V or 3.3V sense resistor voltage exceeds 150mV, the LTC1644 trips the circuit breaker without delay.
- 5V/3.3V Circuit Breaker Threshold Voltage: The LTC4244 threshold voltage is 52mV ±5mV vs 55mV ±15mV for the LTC1644.
- External Gate Voltage: After power-up, the voltage drop from the $12V_{IN}$ pin to the GATE pin is 0.6V for the LTC4244 vs 50mV for the LTC1644.

Hot Plug Power-Up Sequence

The LTC4244 is specifically designed for hot plugging CPCI boards. The typical application circuit is shown in Figure 1.

CPCI Connector Pin Sequence

The staggered lengths of the CPCI male connector pins ensure that all power supplies are physically connected to the LTC4244 before back-end power is allowed to ramp up (BD_SEL# asserted low). The long pins, which include 5V, 3.3.V, V(I/O) and GND, mate first. The short BD_SEL# pin mates last. At least one long 5V power pin must be connected to the LTC4244 in order for the PRECHARGE voltage to be available during the insertion sequence.

The following is a typical hot insertion sequence:

1. ESD clips make contact.
2. Long power and ground pins make contact and Early Power is established. The 1V precharge voltage becomes valid at this stage of insertion. Power is also applied to the pull-up resistors connected to the $\overline{FAULT}$, $\overline{PWRGD}$ and OFF/$\overline{ON}$ pins. All power switches are held off at this stage of insertion.
3. Medium length pins make contact. Both $\overline{FAULT}$ and $\overline{PWRGD}$ continue to be pulled up high at this stage in the hot plug sequence, and the power switches are still held off. The 12V and –12V connector pins also make contact at this stage. Zener clamps Z1 and Z2 plus shunt RC snubbers R16-C5 and R15-C4 help protect the V_{EEIN} and $12V_{IN}$ pins, respectively, from large voltage transients during hot insertion.

   The signal pins also connect at this point. These include the HEALTHY# signal (which is connected to the $\overline{PWRGD}$ pin), the PCI_RST# signal (which is connected to the $\overline{RESETIN}$ pin) and the I/O connector pins (which are biased at 1V by the LTC4244's precharge circuit).
4. Short pins make contact. The BD_SEL# signal is connected to the OFF/$\overline{ON}$ pin. If the BD_SEL# signal is grounded on the backplane, the plug-in card power-up cycle begins immediately. System backplanes that do not ground the BD_SEL# signal will instead have circuitry that detects when BD_SEL# makes contact with the plug-in board. The system logic can then control the power up process by pulling BD_SEL# low.

Power-Up Sequence

The back-end $3.3V_{OUT}$ and $5V_{OUT}$ power planes are isolated from the $3.3V_{IN}$ and $5V_{IN}$ power planes by external N-channel pass transistors Q1 and Q2, respectively. Internal pass transistors isolate the back-end $12V_{OUT}$ and V_{EEOUT} power planes from the $12V_{IN}$ and V_{EEIN} power planes.

APPLICATIONS INFORMATION

Sense resistors R1 and R2 provide current fault detection and R5 and C1 provide current control loop compensation as well as ramp rate control for the GATE pin voltage. Resistors R3 and R4 prevent high frequency oscillations in MOSFET's Q1 and Q2.

A power-up sequence begins when the OFF/$\overline{ON}$ pin is pulled low (Figure 2). This enables the pass transistors to turn on and an internal 21µA current source is connected to TIMER. Once the pass transistors begin to conduct current, the supplies will start to power up. Current limit faults are ignored while the TIMER pin voltage is ramping up and is less than ($12V_{IN}$ – 1.6V). When all four supply voltages are within tolerance, HEALTHY# will pull low and LOCAL_PCI_RST# is free to follow PCI_RST#.

Power-Down Sequence

When the BD_SEL# signal is pulled high, a power-down sequence begins (Figure 3).

Internal switches are connected to each of the output voltage supply pins to discharge the bypass capacitors to ground. The TIMER pin is immediately pulled low. The GATE pin is pulled down by a 60µA current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously and glitching the power supply voltages. When any of the output voltages dips below its threshold, the HEALTHY# signal pulls high and LOCAL_PCI_RST# will be asserted low.

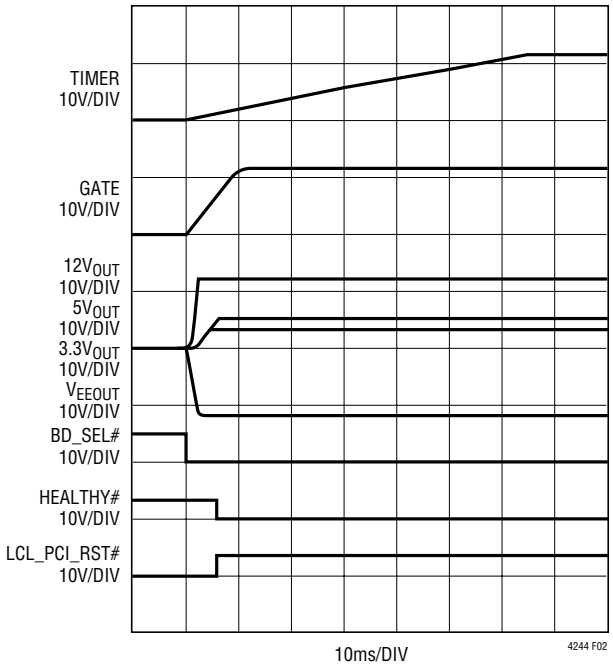

Figure 2. Normal Power-Up Sequence

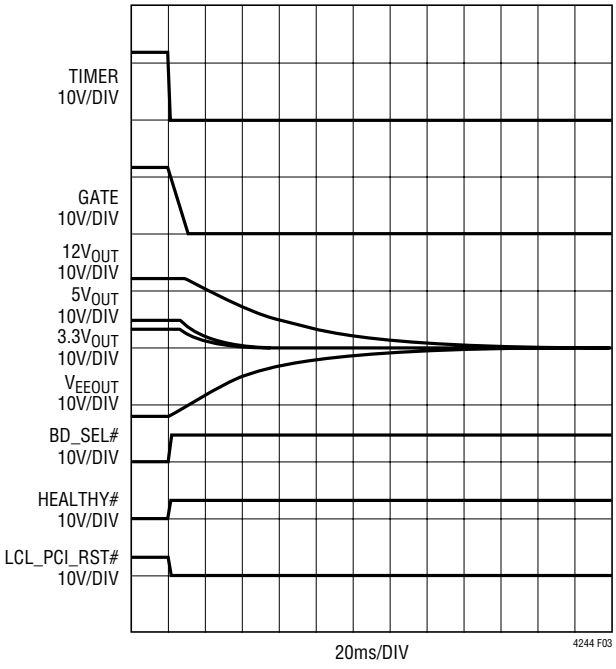

Figure 3. Normal Power-Down Sequence

APPLICATIONS INFORMATION

Once the power-down sequence is complete, the CPCI card may be removed from the slot. During extraction, the precharge circuit continues to bias the bus I/O connector pins at 1V until the long 5V and 3.3V connector pin connections are broken.

GATE Pin Capacitor Selection

Both the load capacitance and the LTC4244's GATE pin capacitor (C1 in Figure 1) affect the ramp rate of the $5V_{OUT}$ and $3.3V_{OUT}$ voltages. The precise relationship can be expressed as:

$$\frac{dV_{OUT}}{dt} = \frac{I_{GATE}}{C1} \text{ or } = \frac{I_{LIMIT(5V)} - I_{LOAD(5V)}}{C_{LOAD(5VOUT)}} \text{ or } = \frac{I_{LIMIT(3.3V)} - I_{LOAD(3.3V)}}{C_{LOAD(3.3VOUT)}} \quad (1)$$

whichever is slowest. The power-up time for any of the LTC4244's outputs where the inrush current is constrained by that supply's foldback current limit can be approximated as:

$$t_{on(nVOUT)} < \frac{2 \bullet C_{LOAD} \bullet nV_{OUT}}{I_{LIMIT(nVOUT)} - I_{LOAD(nVOUT)}} \quad (2)$$

Where nV_{OUT} = $5V_{OUT}$, $3.3V_{OUT}$, $12V_{OUT}$ or V_{EEOUT}. For example, if C_{LOAD}=2000µF, $I_{LIMIT(5VOUT)}$ = 6A and $I_{LOAD(5VOUT)}$ = 5A, the $5V_{OUT}$ turn-on time will be less than 20ms.

If the value of C1 is large enough that it alone determines the output voltage ramp rate, then the magnitude of the inrush current initially charging the load capacitance is:

$$I_{INRUSH} = \frac{C_{LOAD}}{C1} \bullet I_{GATE} \quad (3)$$

The maximum power-up time for this condition can be approximated by:

$$t_{ON} < \frac{\left(V_{OUT} + V_{TH,MOSFET(MAX)}\right) \bullet C1(MAX)}{I_{GATE(MIN)}} \quad (4)$$

where $V_{TH,MOSFET(MAX)}$ is the maximum threshold voltage of the external 5V or 3.3V MOSFET.

In general, the edge rate (dI/dt) at which the back-end 5V and 3.3V supply currents are turned on can be limited by increasing the size of C1. Applications that are sensitive to the edge rate should characterize how varying the size of C1 reduces dI/dt for the external MOSFET selected for a particular design.

In the event of a short-circuit or overcurrent condition, the LTC4244's GATE pin can be pulled down within 2µs since a 1kΩ (R5 in Figure 1) decouples C1 from the gates of the external MOSFET's (Q1 and Q2 in Figure 1).

TIMER Pin Capacitor Selection

During a power-up sequence, a 21µA current source is connected to the TIMER pin and current limit faults are ignored until the voltage ramps to within 1.6V of $12V_{IN}$. This feature allows the part to power up large capacitive loads using its foldback current limit. The TIMER inhibit period can be expressed as:

$$t_{TIMER} = \frac{C_{TIMER} \bullet \left(12V_{IN} - V_{TIMER}\right)}{I_{TIMER}} \quad (5)$$

The timer period should be set longer than the duration of any inrush current that exceeds the LTC4244's foldback current limit but yet be short enough not to exceed the maximum, safe operating area of the external 5V and 3.3V pass transistors in the event of a short circuit (see Design Example). As a design aid, the TIMER period as a function of the timing capacitor using standard values from 0.1µF to 0.82µF is shown in Table 1.

APPLICATIONS INFORMATION

Table 1. t_{TIMER} vs C_{TIMER}

C_{TIMER} (±10%)	$t_{TIMER(MIN)}$	$t_{TIMER(MAX)}$
0.1µF	35ms	74ms
0.22µF	77ms	162ms
0.33µF	115ms	243ms
0.47µF	164ms	346ms
0.68µF	238ms	500ms
0.82µF	287ms	603ms

The TIMER pin is immediately pulled low when the BD_SEL# pin signal goes high.

Thermal Shutdown

The internal switches for the 12V and –12V supplies are protected by a thermal shutdown circuit. When the junction temperature of the die reaches 150°C, all switches will be latched off and the $\overline{FAULT}$ pin will be pulled low.

Short-Circuit Protection

During a normal power-up sequence, if the TIMER pin is done ramping and any supply is still in current limit all of the pass transistors will be immediately turned off and $\overline{FAULT}$ will be pulled low as shown in Figure 4.

In order to prevent excessive power dissipation in the pass transistors and prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function where large currents can flow before the breaker trips, the current foldback feature guarantees that the supply current will be kept at a safe level.

If either the 12V or –12V supply exceeds current limit after power-up, the shorted supply's current will drop

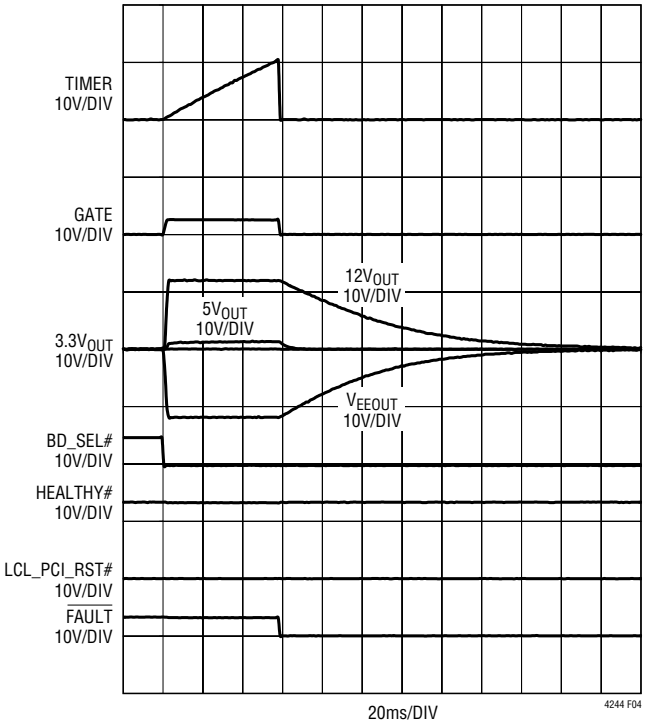

Figure 4. Power-Up Into a Short on a 3.3V Output

APPLICATIONS INFORMATION

immediately to its I_{LIMIT} value. If that supply remains in current limit for more than 25µs, all of the supplies will be latched off. The 25µs prevents quick current spikes—for example, from a fan turning on—from causing false trips of the circuit breaker.

After power-up, the 5V and 3.3V supplies are protected from short circuits by dual-level circuit breakers. In the event that either supply's current exceeds the nominal current limit, an internal timer is started. If the supply is still overcurrent after 25µs, the circuit breaker trips and all the supplies are turned off (Figure 5). An analog current limit loop prevents the supply current from exceeding 3× the nominal current limit in the event of a short circuit (Figure 6). The LTC4244 will stay in the latched off state until the OFF/$\overline{ON}$ pin is cycled high then low or the $12V_{IN}$ power supply is cycled low then high.

The current limit and the foldback current level for the 5V and 3.3V outputs are both a function of the external sense resistor. As shown in Figure 1, a sense resistor is connected between $5V_{IN}$ and $5V_{SENSE}$ for the 5V supply. For the 3.3V supply, a sense resistor is connected between $3.3V_{IN}$ and $3.3V_{SENSE}$. The typical current limit and the foldback current levels are given by Equations 6 and 7:

$$I_{LIMIT(nVOUT)} = \frac{51mV}{R_{SENSE(nVOUT)}} \quad (6)$$

$$I_{FOLDBACK(nVOUT)} = \frac{16mV}{R_{SENSE(nVOUT)}} \quad (7)$$

where nV_{OUT} = $5V_{OUT}$ or $3.3V_{OUT}$.

The current limit for the internal 12V switch is set at 850mA folding back to 360mA and the –12V switch at 610mA folding back to 225mA.

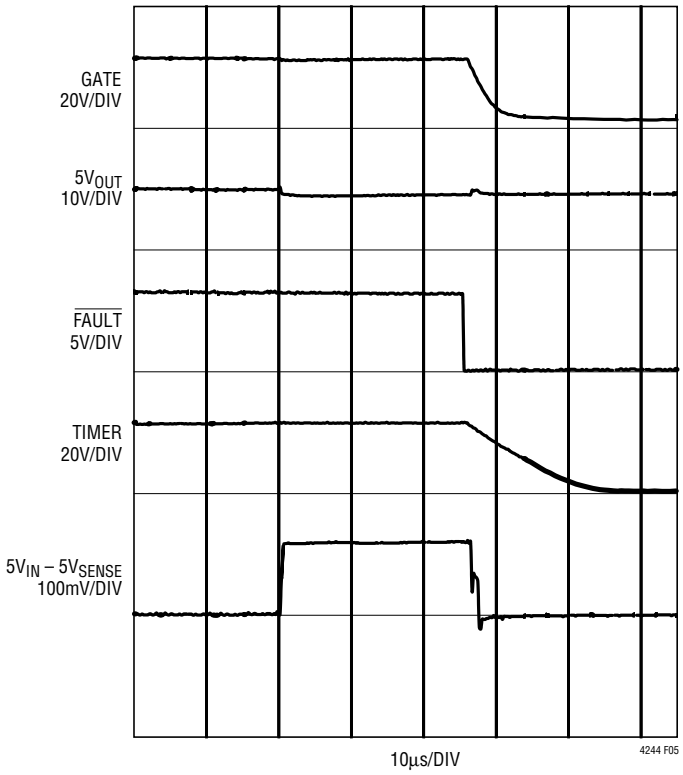

Figure 5. Overcurrent Fault on 5V Output

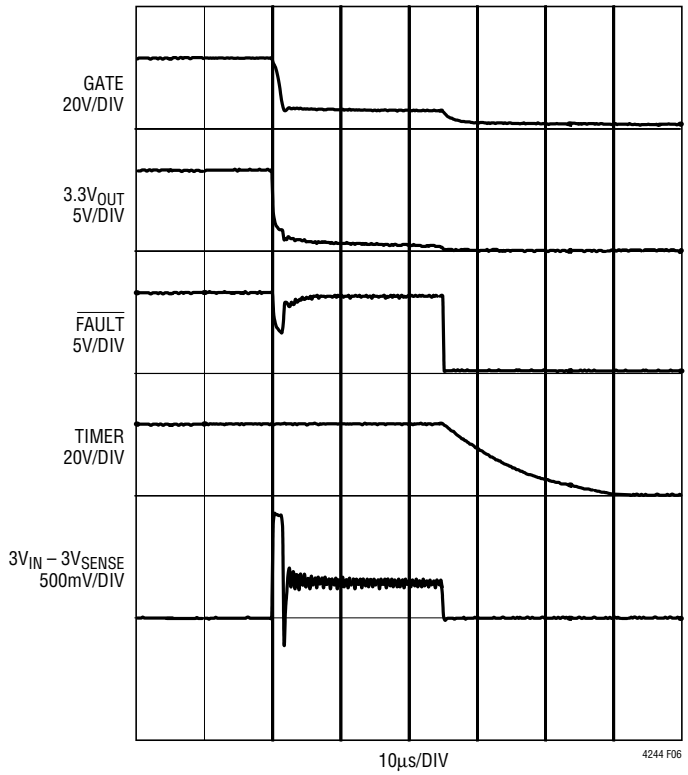

Figure 6. Short-Circuit Fault on 3.3V Output

APPLICATIONS INFORMATION

Calculating R_{SENSE}

Determining the most appropriate value for the sense resistor first requires knowing the maximum current needed by the load under worst-case conditions. Two other parameters affect the value of the sense resistor. First is the tolerance of the LTC4244's circuit breaker threshold voltage. The LTC4244's nominal circuit breaker threshold voltage is $V_{CB(NOM)}$ = 52mV; however it exhibits ±5mV tolerance over process and temperature. Second is the tolerance (RTOL) of the sense resistor. Sense resistors are available in RTOL's of ±1%, ±2% and ±5% and exhibit temperature coefficients of resistance (TCR's) between ±75ppm/°C and ±100ppm/°C. How the sense resistor changes as a function of temperature depends on the $I^2 \bullet R$ power being dissipated by it. The power rating of the sense resistor should accommodate steady-state fault current levels so that the component is not damaged before the circuit breaker trips.

Table 2 lists $I_{TRIP(MIN)}$ and $I_{TRIP(MAX)}$ versus some suggested values of R_{SENSE}. Table 7 lists manufacturers and part numbers for these resistor values.

Table 2. I_{TRIP} vs R_{SENSE}

R_{SENSE} (1% RTOL)	$I_{TRIP(MIN)}$	$I_{TRIP(MAX)}$
0.005Ω	9.31A	11.5A
0.007Ω	6.6A	8.2A
0.011Ω	4.2A	5.2A

Output Voltage Monitor

The status of all four output voltages is monitored by the power good function. In addition, the PCI_RST# signal is logically combined on-chip with the HEALTHY# signal to create LOCAL_PCI_RST# (see Table 3). As a result, LOCAL_PCI_RST# will be pulled low whenever HEALTHY# is pulled high independent of the state of the PCI_RST# signal.

If any of the output voltages drop below the power good threshold for more than 14µs, the $\overline{PWRGD}$ pin will be pulled high and the LOCAL_PCI_RST# signal will be asserted low.

Table 3. LOCAL_PCI_RST# Truth Table

PCI_RST#	HEALTHY#	LOCAL_PCI_RST#
LO	LO	LO
LO	HI	LO
HI	LO	HI
HI	HI	LO

Precharge

The PRECHARGE input and DRIVE output pins are intended for use in generating the 1V precharge voltage that is used to bias the bus I/O connector pins during board insertion and extraction. The LTC4244 is also capable of generating precharge voltages other than 1V. Figure 7 shows a circuit that can be used in applications requiring a precharge voltage of less than 1V. The circuit in Figure 8 can be used for applications that need precharge voltages greater than 1V.

Precharge resistors are used to connect the 1V bias voltage to the I/O lines with minimal disturbance. Figure 1 shows the precharge application circuit for 5V signaling. The precharge resistor requirements are more stringent for 3.3V and Universal Hot Swap boards. If the total leakage current on the I/O line is less 2µA, then a 50k resistor can be connected directly from the 1V bias voltage to the I/O line. However, many ICs connected to the I/O lines can have leakage currents up to 10µA. For these applications, a 10k resistor is used but must be disconnected when the board is seated as determined by the state of the BD_SEL# signal. Figure 9 shows a precharge circuit that uses a bus switch to connect the individual 10k precharge resistors to the LTC4244's 1V PRECHARGE pin. The electrical connection is made (bus switches closed) when the voltage on the BD_SEL# pin of the plug-in card is pulled-up to $5V_{IN}$, which occurs just after the long pins have made contact. The bus switches are electrically disconnected when the short, BD_SEL# connector pin makes contact and the

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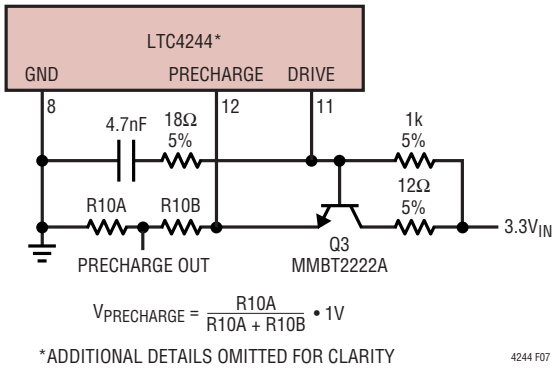

Figure 7. Precharge Voltage <1V Application Circuit

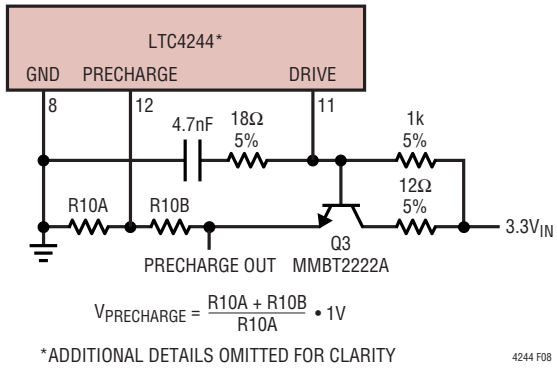

Figure 8. Precharge Voltage >1V Application Circuit

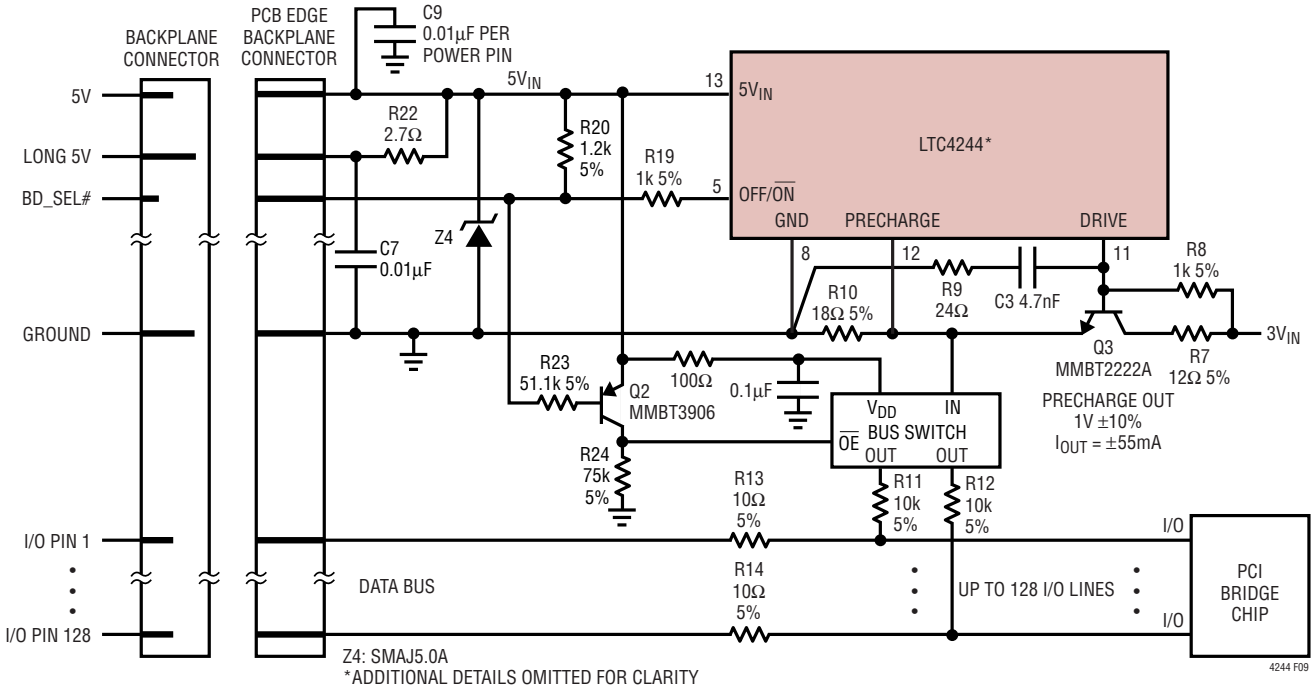

Figure 9. Precharge Bus Switch Application Circuit for 3.3V and Universal Hot Swap Boards

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BD_SEL# voltage drops below 4.4V thus causing the bus switch $\overline{OE}$ to be pulled high by Q2.

The CompactPCI specification assumes that there is a diode to 3.3V on the circuit that is driving the BD_SEL# pin. The 1.2k resistor pull-up to $5V_{IN}$ on the plug-in card will be clamped by the diode to 3.3V. If the BD_SEL# pin is being driven high, the actual voltage on the pin will be approximately 3.9V. This is still above the high TTL threshold of the LTC4244 $\overline{OFF}$/ON pin, but low enough for Q2 to disable the bus switches and thus disconnect the 10k precharge resistors from the I/O lines. Since the power to the bus switch is derived from a front-end power plane, a 100Ω resistor should be placed in series with the power supply of the bus switch.

When the plug-in card is removed from the connector, the BD_SEL# connection is broken first, and the BD_SEL# voltage pulls up to $5V_{IN}$. This causes Q2 to turn off, which re-enables the bus switch, and the precharge resistors are again connected to the LTC4244 PRECHARGE pin for the remainder of the extraction process.

TIMER/Auxiliary V_{CC}

Once the TIMER pin voltage has ramped to within 1.6V of $12V_{IN}$, the auxiliary V_{CC} function is enabled. In the event the $12V_{IN}$ supply voltage collapses, the LTC4244 will continue to draw power from the charge stored on the TIMER pin capacitor until the internal V_{CC} node drops below its undervoltage lockout threshold or the $12V_{IN}$ supply voltage recovers, whichever happens first.

Other CompactPCI Applications

The LTC4244-1 is designed for CompactPCI designs where the –12V supply is not being used on the plug-in board. The V_{EEOUT} power good comparator, V_{EEIN} UVL, and V_{EE} circuit breaker functions are disabled. The V_{EEIN} pin should be connected to GND and the V_{EEOUT} pin left floating if a –12V output is not needed.

If no 3.3V supply input is required, Figure 10 illustrates how the LTC4244 should be configured: $3.3V_{SENSE}$ and $3.3V_{IN}$ are connected to $5V_{IN}$ and $3.3V_{OUT}$ is connected to $5V_{OUT}$.

For applications where the BD_SEL# connector pin is typically connected to ground on the backplane, the circuit in Figure 11 allows the LTC4244 to be reset simply by pressing a pushbutton switch on the CPCI plug in board. This arrangement eliminates the requirement to extract and reinsert the CPCI board in order to reset the LTC4244's circuit breaker.

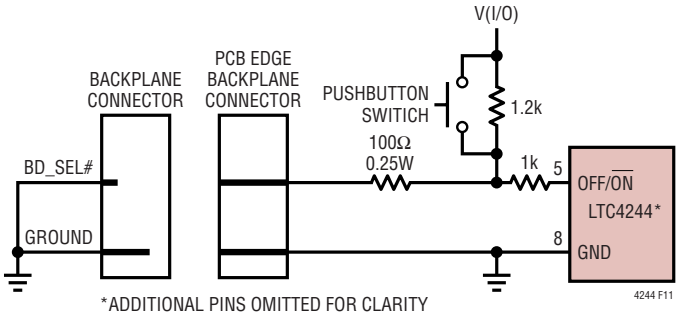

Figure 11. BD_SEL# Pushbutton Toggle Switch

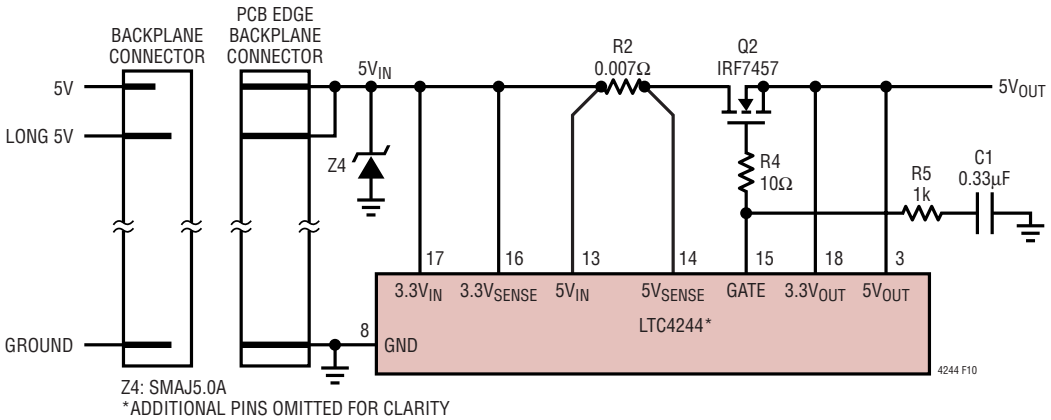

Figure 10. No 3.3V Supply Application Circuit

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Power MOSFET Selection Criteria

The LTC4244 uses external MOSFETs to limit the 5V and 3.3V supply currents. The following criteria should be used when selecting these MOSFET's:

1. The on resistance should be low enough to prevent an excessive voltage drop across the sense resistor and the series MOSFET at rated load current given the amount of gate to source voltage provided by the LTC4244.
2. The drain-to-source breakdown voltage should be high enough for the device to survive overvoltage transients that may occur during fault conditions (the 5V and 3.3V transient voltage limiters shown in Figure 1 will limit the maximum drain-source voltage seen by these MOSFET's during fault conditions).
3. The MOSFET package must be able to handle the maximum, steady state power dissipation for the ON state without exceeding the device's rated maximum junction temperature. The MOSFET's steady-state, dissipated power can be expressed as:

$$P_{ON} = I_{MAX}^2 \bullet R_{DS(ON)} \quad (8)$$

The increase in steady-state junction-to-ambient temperature is given by:

$$T_J - T_A = P_{ON} \bullet R_{\theta JA} \quad (9)$$

4. The MOSFET package must be able to dissipate the heat resulting from the power pulse during the transition from off to on. A worst-case approximation for the magnitude of the power pulse is:

$$P_{OFF\text{-}ON} < \frac{nV_{OUT} \bullet (I_{INRUSH} + I_{LOAD})}{2} \quad (10)$$

where $nV_{OUT} = 5V_{OUT}$ or $3.3V_{OUT}$, I_{INRUSH} is the transient current initially charging the load capacitance and I_{LOAD} is the steady-state load current. The duration, t_{ON}, of the power pulse can be expressed as:

$$t_{ON} = \frac{C_{LOAD} \bullet V_{OUT}}{I_{INRUSH}} \quad (11)$$

5. The MOSFET package must be able to sustain the maximum pulse power that occurs in the event the LTC4244 attempts to power-up either the 5V or 3.3V back-end supply into a short circuit (see Design Example for a sample calculation).

Table 8 lists some power MOSFET's that can be used with the LTC4244.

Input Overvoltage Transient Protection

Hot plugging a board into a backplane generates inrush currents from the backplane power supplies due to the charging of the plug-in board capacitance. To reduce this transient current to a safe level, the CPCI Hot Swap specification restricts the amount of unswitched capacitance used on the input side of the plug-in board. Each medium or long power pin connected to the CPCI female connector on the plug-in board is required to have a 10nF ceramic bypass capacitor to ground. Bulk capacitors are only allowed on the switched output side of the LTC4244 ($5V_{OUT}$, $3.3V_{OUT}$, $12V_{OUT}$, V_{EEOUT}). Some bulk capacitance is allowed on the $5V_{IN}$ and $3.3V_{IN}$ Early Power planes, but only because a current limiting resistor is assumed to decouple the connector pin from the bulk capacitance. Circuits normally placed on the unswitched side Early Power plane (PCI Bridge, for example) need to to be decoupled by a current limiting resistor.

Disallowing bulk capacitors on the input power pins mitigates the inrush current during Hot Swap. However, it also tends to create a resonant circuit formed by the inductance of the backplane power supply trace in series with the inductance of the connector pin and the parasitic capacitance of the plug-in board (mainly due to the large power FET). Upon board insertion, the ringing of this circuit can exhibit a peak overshoot of 2.5 times the steady-state voltage (>30V for $12V_{IN}$).

There are two methods for abating the effects of these high voltage transients: using voltage limiters to clip the transient to a safe level and snubber networks. Snubber networks are series RC networks whose time constants

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are experimentally determined based on the board's parasitic resonance circuits. As a starting point, the capacitors in these networks are chosen to be 10× to 100× the power MOSFET's C_{OSS} under bias. The series resistor is a value determined experimentally that ranges from 1Ω to 50Ω, depending on the parasitic resonance circuit. Note that in all LTC4244 circuit schematics, *both* transient voltage limiters and snubber networks have been added to the $12V_{IN}$ and V_{EEIN} supply rails and should always be used. Snubber networks are not necessary on the $3.3V_{IN}$ or the $5V_{IN}$ supply lines since their absolute maximum voltage ratings are 13.5V. Transient voltage limiters, however, are recommended as these devices provide large-scale transient protection for the LTC4244 in the event of abrupt changes in supply current. All protection networks should be mounted very close to the LTC4244's supply pins using short lead lengths to minimize trace resistance and inductance. This is shown schematically in Figures 12 and 13 and a recommended layout of the transient protection devices around the LTC4244 is shown in Figure 14.

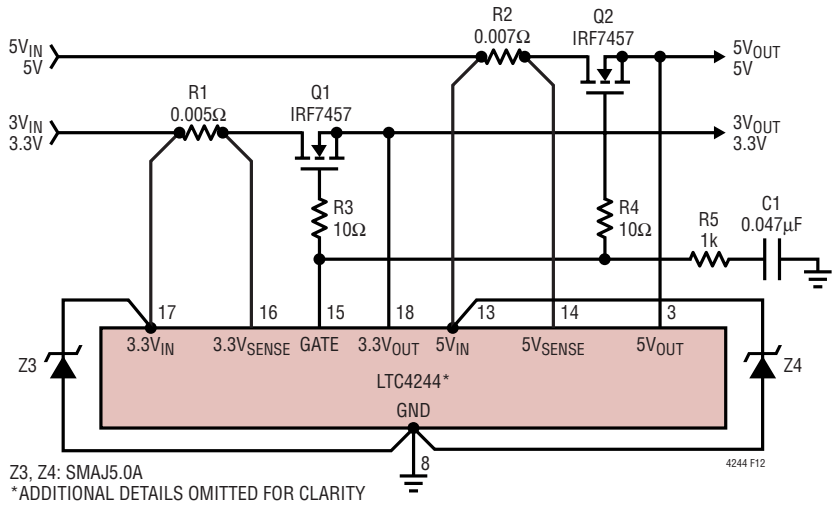

Figure 12. Place Transient Protection Devices Close to LTC4244's $5V_{IN}$ and $3.3V_{IN}$ Pins

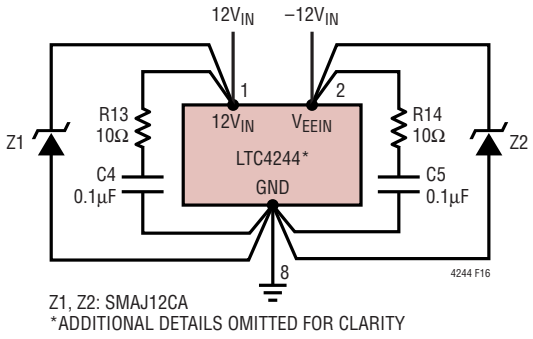

Figure 13. Place Transient Protection Devices Close to LTC4244's $12V_{IN}$ and V_{EEIN} Pins

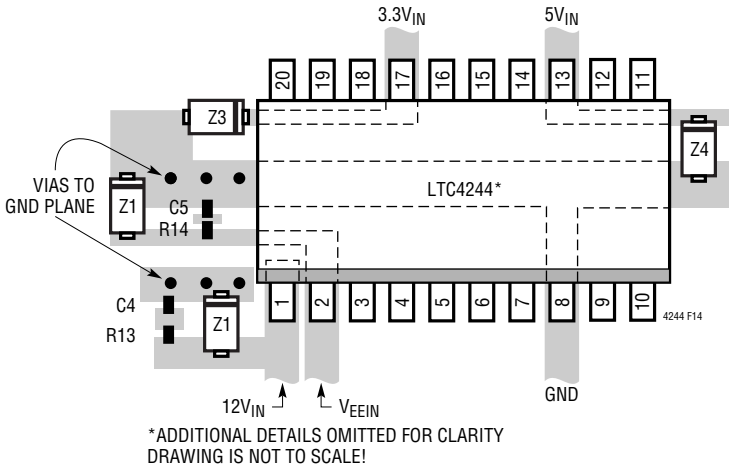

Figure 14. Recommended Layout for Transient Protection Components

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PCB Layout Considerations

For proper operation of the LTC4244's circuit breaker, 4-wire Kelvin sense connections between the sense resistor and the LTC4244's $5V_{IN}$ and $5V_{SENSE}$ pins and $3.3V_{IN}$ and $3.3V_{SENSE}$ pins are strongly recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout for the sense resistor, the power MOSFET and the GATE drive components around the LTC4244 is illustrated in Figure 15. In Hot Swap applications where load currents can be 10A, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper foil is approximately 0.45mΩ/□, track resistance and voltage drops add up quickly in high current applications. Thus, to keep PCB track resistance, voltage drop and temperature to a minimum, the suggested trace width in these applications for 1 ounce copper foil is 0.03" for each ampere of DC current.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to

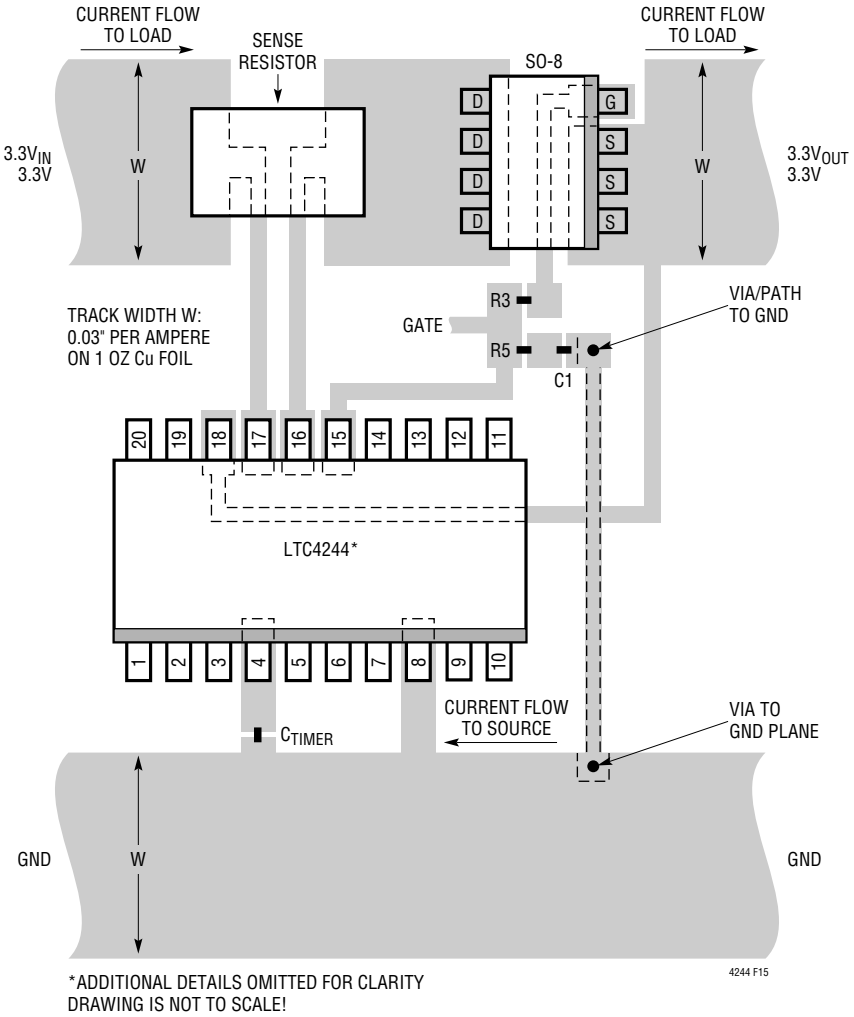

Figure 15. Recommended Layout for Power MOSFET, Sense Resistor and GATE Components for the 3.3V Rail

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the PC board. For 1 ounce copper foil plating, a general rule is 1 ampere of DC current per via making sure the via is properly dimensioned so that solder completely fills the void. For other plating thicknesses, check with your PCB fabrication facility.

Design Example

As a design example, consider a CPCI Hot Swap application with the following power supply requirements:

Table 4. Design Example Power Supply Requirements

VOLTAGE SUPPLY	MAXIMUM DC SUPPLY CURRENT	LOAD CAPACITANCE
12V	450mA	100µF
5V	5A	2200µF
3.3V	7A	2200µF
–12V	100mA	100µF

The first step is to select the appropriate values of R_{SENSE} for the 5V and 3.3V supplies. Calculating the value of R_{SENSE} is based on $I_{LOAD(MAX)}$ and the lower limit for the circuit breaker threshold voltage (47mV for both the 5V and 3.3V circuit breakers). If a 1% tolerance is assumed for the sense resistors, then 5mΩ and 7mΩ resistor values yield the following minimum and maximum I_{TRIP} values:

Table 5. I_{TRIP} vs R_{SENSE}

R_{SENSE} (1% RTOL)	$I_{TRIP(MIN)}$	$I_{TRIP(MAX)}$
5mΩ	9.3A	11.5A
7mΩ	6.6A	8.2A

So sense resistor values of 7mΩ and 5mΩ should suffice for the 5V and 3.3V supplies, respectively.

The second step is to select MOSFETs for the 5V and 3.3V supplies. The IRF7457's on resistance is less than 10.5mΩ for V_{GS} > 4.5V and a junction temperature of 25°C. Since the maximum load current requirement for the 3.3V supply is 7A, the steady-state power the device may be required to dissipate is 514mW. The IRF7457 has a junction-to-ambient thermal resistance of 50°C/Watt. If a maximum ambient temperature of 50°C is assumed, this yields a junction temperature of 75.7°C. According to the IRF7457's Normalized On-Resistance vs Junction Temperature curve, the device's on-resistance can be expected to increase by about 20% over its room temperature value. Recalculation of the steady-state values of R_{ON} and junction temperature yields approximately 12.6mΩ and 81°C, respectively. The I • R drop across the 3.3V sense resistor and series MOSFET at maximum load current under these conditions will be less than 124mV.

The next step is to select appropriate values for C1 and C_{TIMER}. Assuming that the total current for the 5V supply is constrained to less than 6A during power-up (6 × 5V medium length connector pins at 1A per pin), then the inrush current shouldn't exceed:

$$I_{INRUSH} < 6A - I_{LOAD(5VOUT)} = 6A - 5A = 1A \quad (12)$$

This yields:

$$C1 > \frac{I_{GATE(MAX)} \bullet 2200\mu F}{I_{INRUSH(MAX)}} \quad (13)$$

$$\Rightarrow C1 > \frac{100\mu A \bullet 2200\mu F}{1A} = 220nF$$

Hence a C1 value of 330nF ±10% should suffice. The value of C_{TIMER} for this design example will be constrained by the duration of the 12V supply inrush current, which according to Equation 2 is:

$$t_{ON(12VOUT)} < \frac{2 \bullet C_{LOAD} \bullet 12V}{I_{LIMIT(MIN)} - I_{LOAD(MAX)}} \quad (14)$$

$$\Rightarrow t_{ON(12VOUT)} < \frac{2 \bullet 100\mu F \bullet 12V}{550mA - 450mA} = 24ms$$

In order to guarantee that the LTC4244's TIMER fault inhibit period is greater than 24ms, the value of C_{TIMER} should be:

$$C_{TIMER} > \frac{24ms \bullet I_{TIMER(MAX)}}{12V - V_{TIMER(MAX)}} \quad (15)$$

$$\Rightarrow C_{TIMER} > \frac{24ms \bullet 26\mu A}{12V - 1.9V} = 61.8nF$$

So a value of 82nF (±10%) should suffice.

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The next step is to verify that the thermal ratings of the external 5V and 3.3V MOSFETs aren't being exceeded during power-up cycles into the designed loads or into a short circuit.

The amount of heating in the 5V and 3.3V MOSFETs during a normal power cycle depends on the LTC4244's GATE pin current (refer to Gate Current vs Temperature plot in the Typical Performance Characteristics section). The magnitude of the off-on power pulse that results in maximum heating of the MOSFETs is given by Equation 10 as:

$$P_{OFF\text{-}ON} = \frac{nV_{OUT} \bullet \left(I_{INRUSH(MIN)} + I_{LOAD(nVOUT)}\right)}{2} \quad (16)$$

where

$$I_{INRUSH(MIN)} = \frac{C_{LOAD}}{C1(MAX)} \bullet I_{GATE(MIN)} \quad (17)$$

The duration of the power-pulse is given by Equation 11 as:

$$t_{INRUSH} < \frac{C_{LOAD} \bullet nV_{OUT}}{I_{INRUSH(MIN)}} \quad (18)$$

Solving these equations for the 5V and 3.3V supplies yields:

Table 6

	$P_{OFF\text{-}ON}$	$t_{INRUSH(MAX)}$
5V MOSFET	12.8W	90ms
3.3V MOSFET	11.8W	60ms

Under these conditions, the IRF7457 datasheet's Thermal Response vs Pulse Duration curve indicates that the junction-to-ambient temperature will increase by 60°C for the 5V MOSFET and 46°C for the 3.3V MOSFET.

The duration and magnitude of the power pulse that results during a short-circuit condition on either the 5V or 3.3V outputs are a function of the TIMER capacitor and the LTC4244's foldback current limit. Figure 16 shows the worst-case power dissipated in the 5V and 3.3V external FETs vs V_{5VOUT} and $V_{3.3VOUT}$, respectively. In the case of the 3.3V external MOSFET, the maximum dissipated power is 24 Watts ($V_{3.3VOUT}$ = 0.9V). For the 5V external MOSFET, the maximum dissipated power is 22 Watts (V_{5VOUT} = 1.75V). The maximum duration of the short-circuit power-pulse is given by Equation 19 as:

$$t_{PULSE} < C_{TIMER(MAX)} \bullet \frac{12V - V_{TIMER(MIN)}}{I_{TIMER(MIN)}} \quad (19)$$

$$\Rightarrow t_{PULSE} < \frac{(82nF + 8.2nF) \bullet (12V - 1.3V)}{16\mu A}$$

$$\Rightarrow t_{PULSE} < 60.3ms$$

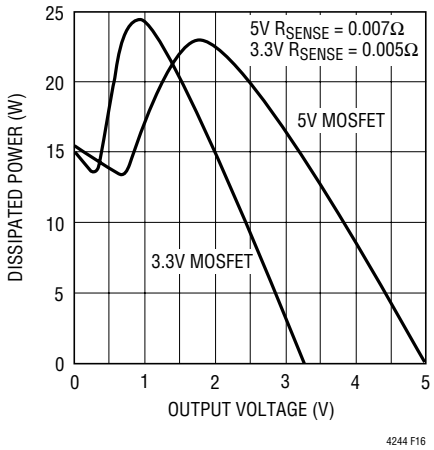

Figure 16. Worst-Case 5V and 3.3V MOSFET Dissipated Power vs Output Voltage

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The IRF7457's Thermal Response vs Pulse Duration curve indicates that the worst-case increase in junction-to-ambient temperature during a power-cycle for the 3.3V MOSFET is less than 96°C while the worst-case increase in junction-to-ambient temperature for the 5V MOSFET is less than 88°C.

Power MOSFET and Sense Resistor Selection

Tables 7 and 8 list current sense resistors and power MOSFET transistors, respectively, that can be used with the LTC4244's circuit breakers. Table 9 lists supplier web site addresses for discrete components mentioned throughout the LTC4244 data sheet.

Obtaining Information on Specific Parts

For more information or to request a copy of the CompactPCI specification, contact the PCI Industrial Computer Manufacturers Group at:

PCI Industrial Computer Manufacturers Group
Wakefield, MA 01880 USA
Phone: 01 (718) 224-1239
Web Site: http://www.picmg.com

Transient Voltage Suppressors SMAJ12A and SMAJ5.0A are supplied by:

Diodes, Incorporated
Westlake Village, CA 91362 USA
Phone: 01 (805) 446-4800
Web Site: http://www.vishay.com or
http://www.diodes.com

Transistors MMBT2222A and MMBT3906 are supplied by:

ON Semiconductor
Phoenix, AZ 85008 USA
Phone: 01 (602) 244-6600
Web Site: http://www.onsemi.com

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Table 7. Sense Resistor Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R055F WSL1206R055	0.055Ω, 0.5W, 1% Resistor	IRC-TT Vishay Dale
2A	LR120601R028F WSL1206R028	0.028Ω, 0.5W, 1% Resistor	IRC-TT Vishay Dale
5A	LR120601R011F WSL2010R011	0.011Ω, 0.5W, 1% Resistor	IRC-TT Vishay Dale
7.6A	WSL2512R007	0.007Ω, 1W, 1% Resistor	Vishay Dale
10A	WSL2512R005	0.005Ω, 1W, 1% Resistor	Vishay Dale

Table 8. N-Channel Power MOSFET Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
0A to 2A	MMDF3N02HD	Dual N-Channel SO-8, $R_{DS(ON)}$ = 0.1Ω	ON Semiconductor
2A to 5A	MMSF5N02HD	Single N-Channel SO-8, $R_{DS(ON)}$ = 0.025Ω	ON Semiconductor
5A to 10A	MTB50N06V	Single N-Channel DD-Pak, $R_{DS(ON)}$ = 0.028Ω	ON Semiconductor
5A to 10A	IRF7457	Single N-Channel SO-8, $R_{DS(ON)}$ = 0.007Ω	International Rectifier
5A to 10A	Si7880DP	Single N-Channel PowerPAK™, $R_{DS(ON)}$ = 0.003 Ω	Vishay Siliconix

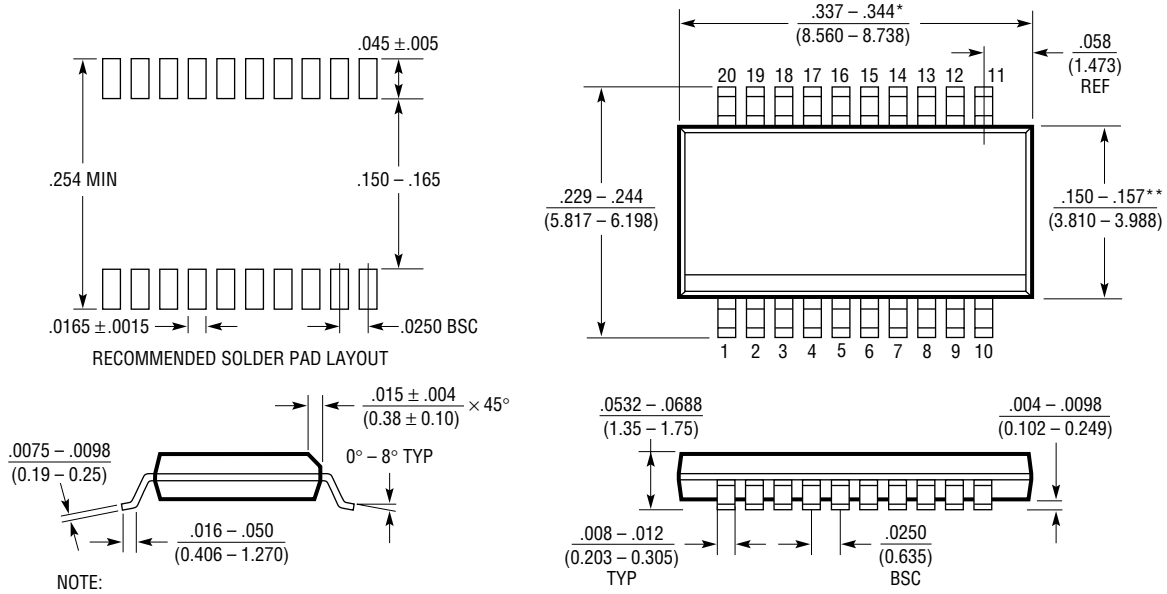
PowerPAK is a trademark of Vishay Siliconix

Table 9. Manufacturers' Web Site

MANUFACTURER	WEB SITE
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
IRC-TT	www.irctt.com
Vishay Dale	www.vishay.com
Vishay Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

PACKAGE DESCRIPTION

GN Package
20-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN20 (SSOP) 0204