Negative Voltage Hot Swap Controllers in SOT-23

FEATURES

- **Allows Safe Board Insertion and Removal from a Live –48V Backplane**
- **Floating Topology Permits Very High Voltage Operation**
- **Programmable Analog Current Limit with Circuit Breaker Timer**
- **Fast Response Time Limits Peak Fault Current**
- **Improved Ruggedness Shunt Regulator**
- Programmable Timer
- Programmable Undervoltage/Overvoltage Protection
- Low Profile 6-Lead SOT-23 (ThinSOT™) Package

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker
- –48V Distributed Power Systems
- Negative Power Supply Control
- Central Office Switching
- Programmable Current Limiting Circuit
- High Availability Servers
- Disk Arrays

DESCRIPTION

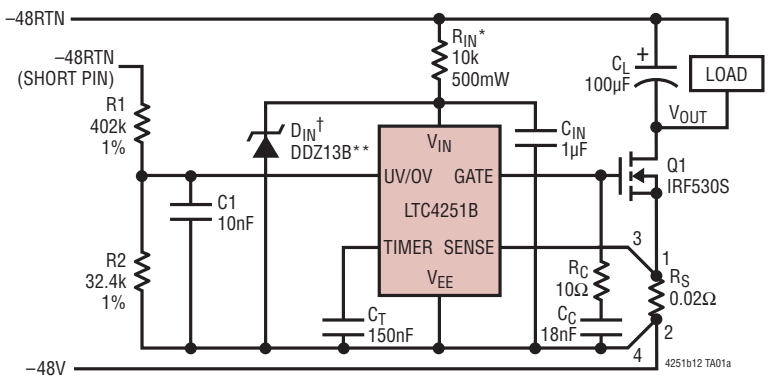
The LTC®4251B/LTC4251B-1/LTC4251B-2 negative voltage Hot Swap™ controllers allow a board to be safely inserted and removed from a live backplane. Output current is controlled by three stages of current limiting: a timed circuit breaker, active current limiting and a fast feedforward path that limits peak current under worst-case catastrophic fault conditions.

Programmable undervoltage and overvoltage detectors disconnect the load whenever the input supply exceeds the desired operating range. The supply input is shunt regulated, allowing safe operation with very high supply voltages. A multifunction timer delays initial start-up and controls the circuit breaker's response time.

The LTC4251B UV/OV thresholds are designed to match the standard telecom operating range of –43V to –75V. The LTC4251B-1 UV/OV thresholds extend the operating range to encompass –36V to –72V. The LTC4251B-2 implements a UV threshold of –43V only. The LTC4251B improves the ruggedness of the LTC4251 shunt regulator.

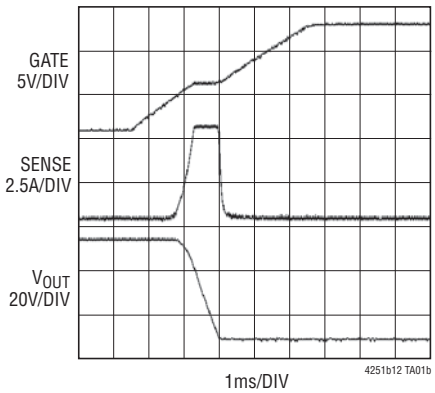
TYPICAL APPLICATION

–48V, 2.5A Hot Swap Controller



*TWO 0.25W RESISTORS IN SERIES FOR R_{IN} ON THE PCB ARE RECOMMENDED.
**DIODES, INC.
†RECOMMENDED FOR HARSH ENVIRONMENTS

Start-Up Behavior

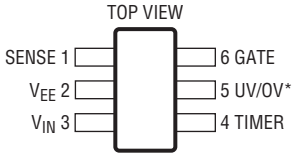


ABSOLUTE MAXIMUM RATINGS

(Note 1), All Voltages are Referred to V_{EE}

Current into V_{IN} (100µs Pulse) 100mA
Minimum V_{IN} Voltage..... –0.3V
Gate, UV/OV, Timer Voltage..... –0.3V to 16V
Sense Voltage ..... –0.6V to 16V
Current Out of Sense Pin (20µs Pulse)..... –200mA
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC4251BC/LTC4251BC-1/LTC4251BC-2....0°C to 70°C
LTC4251BI/LTC4251BI-1/LTC4251BI-2 .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



S6 PACKAGE
6-LEAD PLASTIC SOT-23
*UV FOR LTC4251B-2

T_{JMAX} = 125°C, θ_{JA} = 192°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4251BCS6#TRMPBF	LTC4251BCS6#TRPBF	LTGCT	6-Lead Plastic SOT-23	0°C to 70°C
LTC4251BIS6#TRMPBF	LTC4251BIS6#TRPBF	LTGCT	6-Lead Plastic SOT-23	–40°C to 85°C
LTC4251BCS6-1#TRMPBF	LTC4251BCS6-1#TRPBF	LTGDV	6-Lead Plastic SOT-23	0°C to 70°C
LTC4251BIS6-1#TRMPBF	LTC4251BIS6-1#TRPBF	LTGDV	6-Lead Plastic SOT-23	–40°C to 85°C
LTC4251BCS6-2#TRMPBF	LTC4251BCS6-2#TRPBF	LTGDW	6-Lead Plastic SOT-23	0°C to 70°C
LTC4251BIS6-2#TRMPBF	LTC4251BIS6-2#TRPBF	LTGDW	6-Lead Plastic SOT-23	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_Z	V_{IN} to V_{EE} Zener Voltage	I_{IN} = 2mA	●	11.5	13	14.5	V
r_Z	V_{IN} to V_{EE} Zener Dynamic Impedance	I_{IN} = 2mA to 30mA			5		Ω
I_{IN}	V_{IN} Supply Current	UV/OV = 4V, V_{IN} = (V_Z – 0.3V)	●		0.8	2	mA
V_{LKO}	V_{IN} Undervoltage Lockout	Coming Out of UVLO (Rising V_{IN})	●		9.2	11.5	V
V_{LKH}	V_{IN} Undervoltage Lockout Hysteresis				1		V
V_{CB}	Circuit Breaker Current Limit Voltage	V_{CB} = (V_{SENSE} – V_{EE})	●	40	50	60	mV
V_{ACL}	Analog Current Limit Voltage	V_{ACL} = (V_{SENSE} – V_{EE})	●	80	100	120	mV
V_{FCL}	Fast Current Limit Voltage	V_{FCL} = (V_{SENSE} – V_{EE})	●	150	200	300	mV
I_{GATE}	GATE Pin Output Current	UV/OV = 4V, V_{SENSE} = V_{EE}, V_{GATE} = 0V (Sourcing) UV/OV = 4V, V_{SENSE} – V_{EE} = 0.15V, V_{GATE} = 3V (Sinking) UV/OV = 4V, V_{SENSE} – V_{EE} = 0.3V, V_{GATE} = 1V (Sinking)	●	40	58 17 190	80	µA mA mA
V_{GATE}	External MOSFET Gate Drive	V_{GATE} – V_{EE}, I_{IN} = 2mA	●	10	12	V_Z	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{GATEL}	Gate Low Threshold	(Before Gate Ramp-Up)			0.5		V
V_{UVHI}	UV Threshold High	LTC4251B/LTC4251B-2 LTC4251B-1	● ●	3.075 2.300	3.225 2.420	3.375 2.540	V V
V_{UVLO}	UV Threshold Low	LTC4251B/LTC4251B-2 LTC4251B-1	● ●	2.775 2.050	2.925 2.160	3.075 2.270	V V
V_{UVHST}	UV Hysteresis	LTC4251B/LTC4251B-2 LTC4251B-1			0.30 0.26		V V
V_{OVHI}	OV Threshold High	LTC4251B LTC4251B-1	● ●	5.85 5.86	6.15 6.17	6.45 6.48	V V
V_{OVLO}	OV Threshold Low	LTC4251B LTC4251B-1	● ●	5.25 5.61	5.55 5.91	5.85 6.21	V V
V_{OVHST}	OV Hysteresis	LTC4251B LTC4251B-1			0.60 0.26		V V
I_{SENSE}	SENSE Input Current	UV/OV = 4V, V_{SENSE} = 50mV	●	–30	–15		µA
I_{INP}	UV/OV Input Current	UV/OV = 4V	●		±0.1	±1	µA
V_{TMRH}	Timer Voltage High Threshold				4		V
V_{TMRL}	Timer Voltage Low Threshold				1		V
I_{TMR}	Timer Current	Timer On (Initial Cycle, Sourcing), V_{TMR} = 2V Timer Off (Initial Cycle, Sinking), V_{TMR} = 2V Timer On (Circuit Breaker, Sourcing), V_{TMR} = 2V Timer Off (Cooling Cycle, Sinking), V_{TMR} = 2V			5.8 28 230 5.8		µA mA µA µA
t_{PLLUG}	UV Low to GATE Low				0.7		µs
t_{PHLOG}	OV High to GATE Low	LTC4251B/LTC4251B-1			1		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

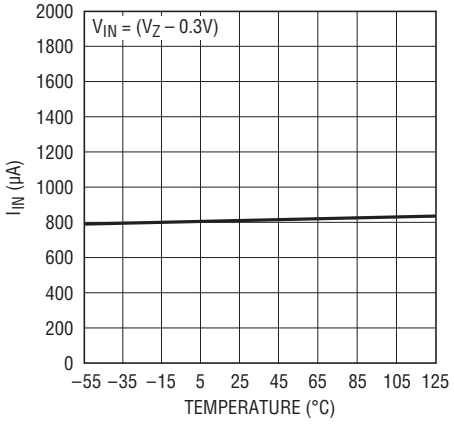
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE} unless otherwise specified.

Note 3: UV/OV = 4V refers to UV = 4V for the LTC4251B-2.

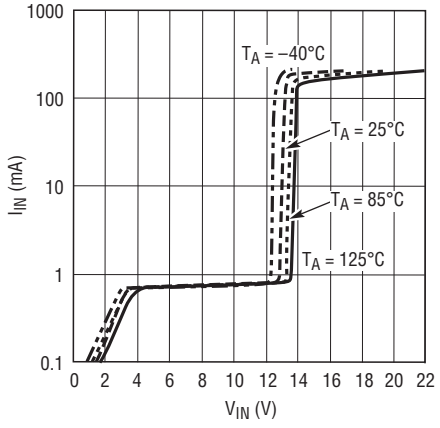
TYPICAL PERFORMANCE CHARACTERISTICS

UV/OV = 4V refers to UV = 4V for the LTC4251B-2.

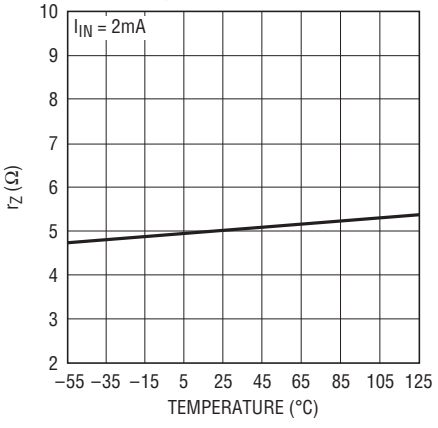
I_{IN} vs Temperature



I_{IN} vs V_{IN}



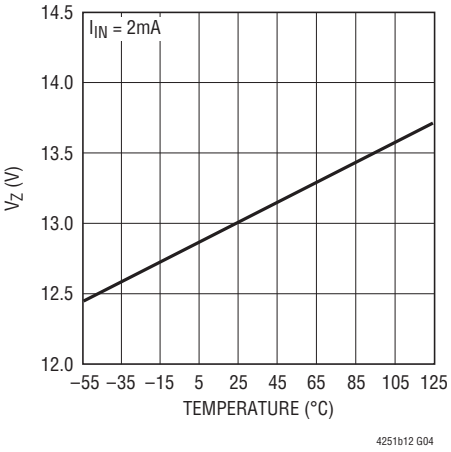
r_Z vs Temperature



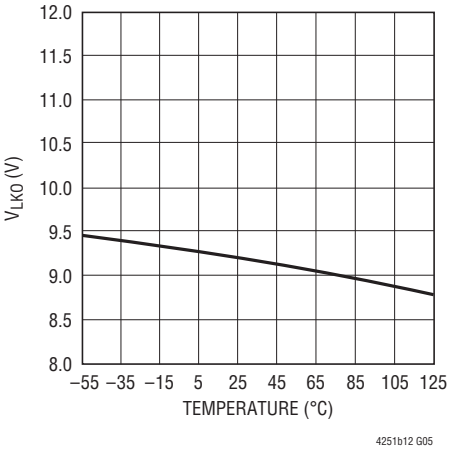
TYPICAL PERFORMANCE CHARACTERISTICS

UV/OV = 4V refers to UV = 4V for the LTC4251B-2.

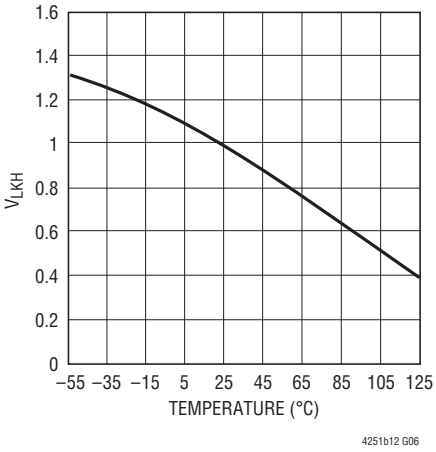
V_Z vs Temperature



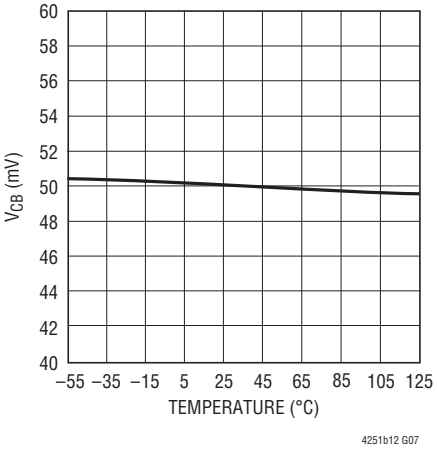
Undervoltage Lockout V_{LKO} vs Temperature



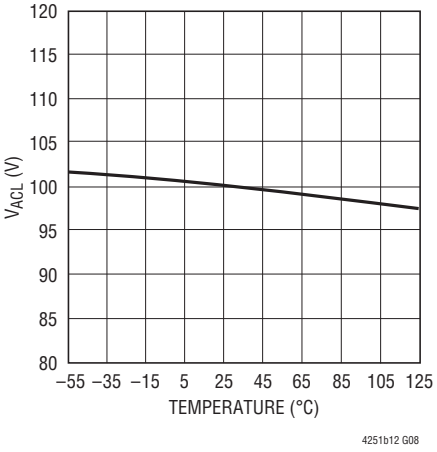
Undervoltage Lockout Hysteresis V_{LKH} vs Temperature



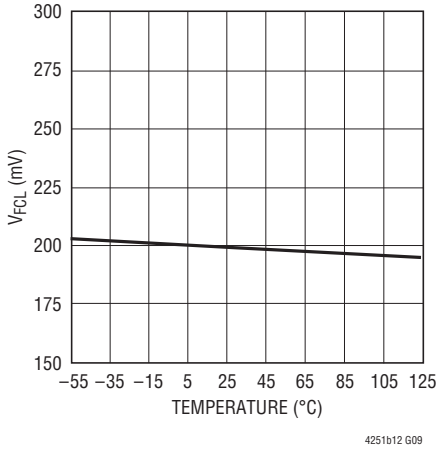
Circuit Breaker Current Limit Voltage V_{CB} vs Temperature



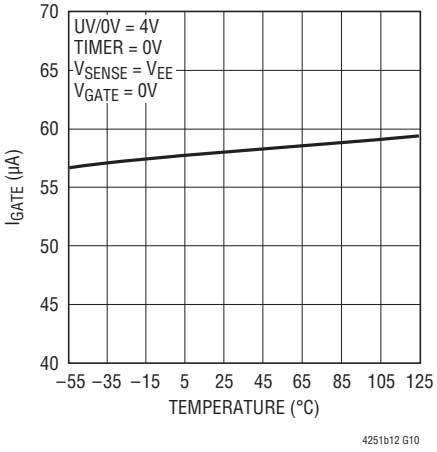
Analog Current Limit Voltage V_{ACL} vs Temperature



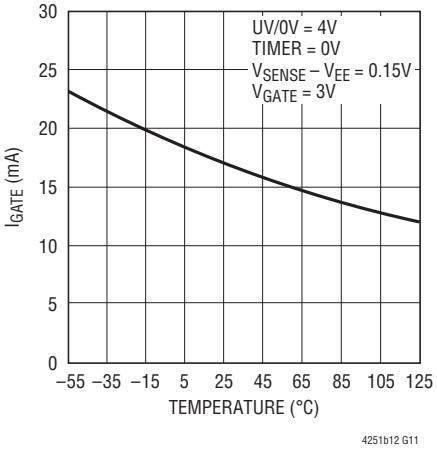
Fast Current Limit Voltage V_{FCL} vs Temperature



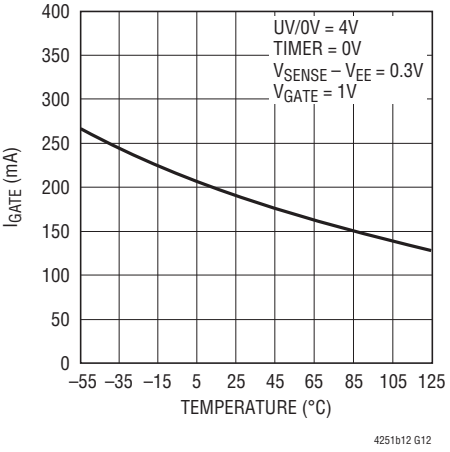
I_{GATE} (Source) vs Temperature



I_{GATE} (ACL, Sink) vs Temperature



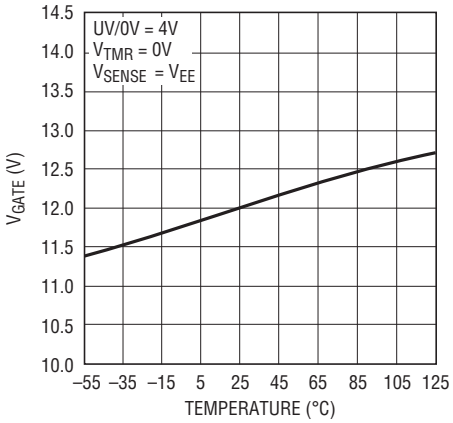
I_{GATE} (FCL, Sink) vs Temperature



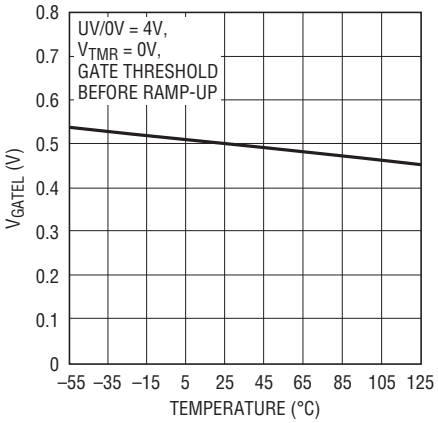
TYPICAL PERFORMANCE CHARACTERISTICS

UV/OV = 4V refers to UV = 4V for the LTC4251B-2.

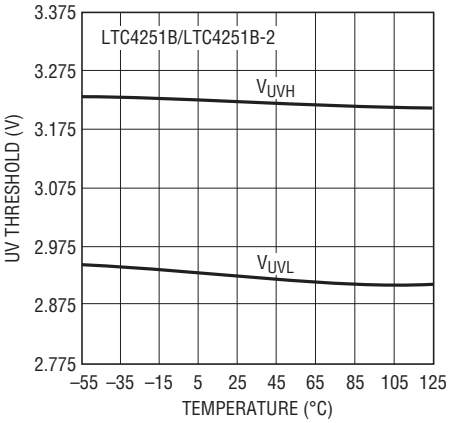
V_{GATE} vs Temperature



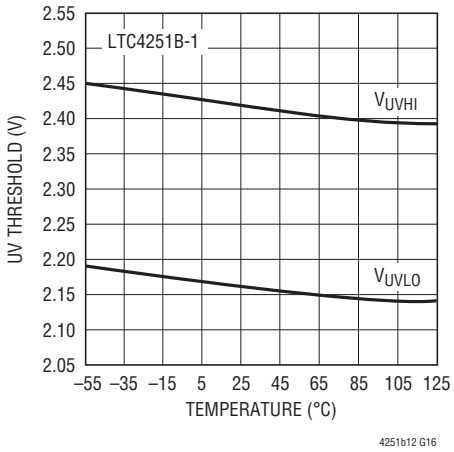
V_{GATEL} vs Temperature



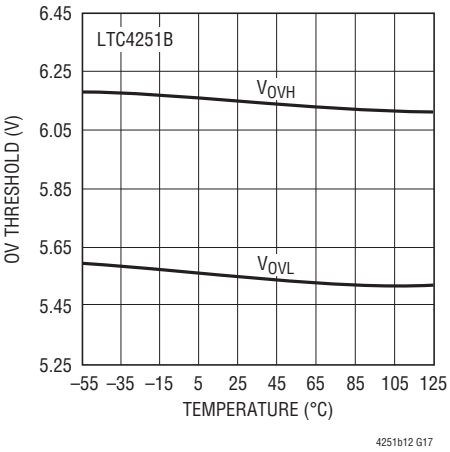
UV Threshold vs Temperature



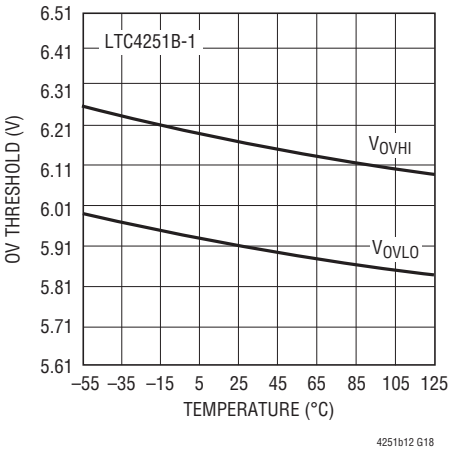
UV Threshold vs Temperature



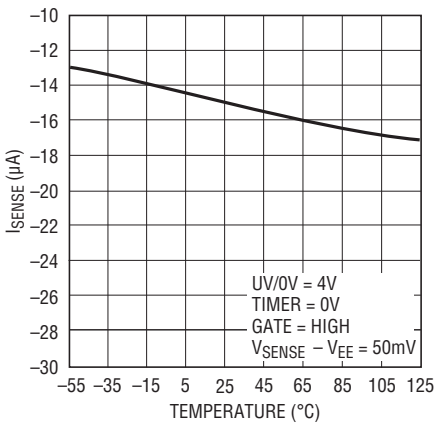
OV Threshold vs Temperature



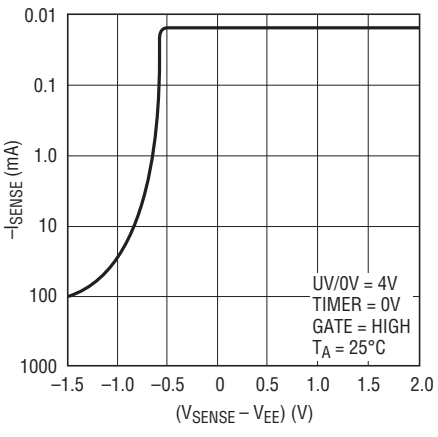
OV Threshold vs Temperature



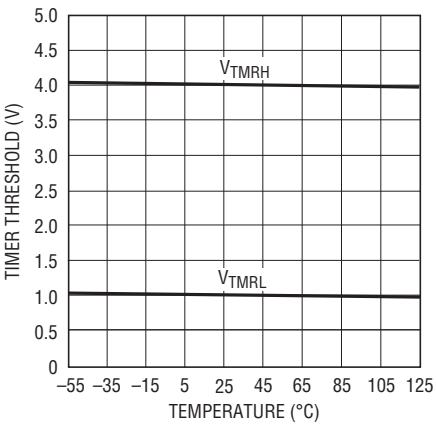
I_{SENSE} vs Temperature



I_{SENSE} vs ($V_{SENSE} - V_{EE}$)



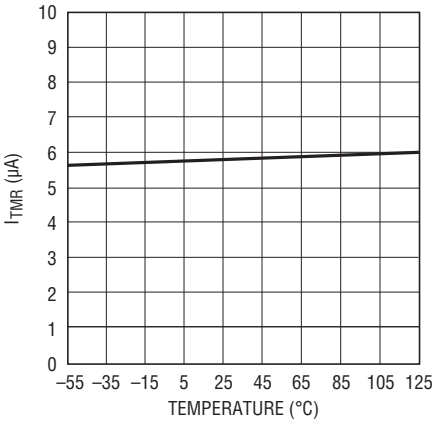
TIMER Threshold vs Temperature



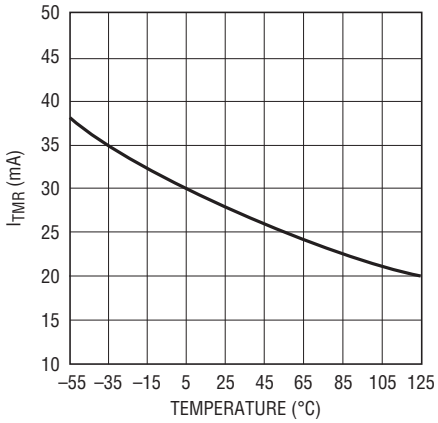
TYPICAL PERFORMANCE CHARACTERISTICS

UV/OV = 4V refers to UV = 4V for the LTC4251B-2.

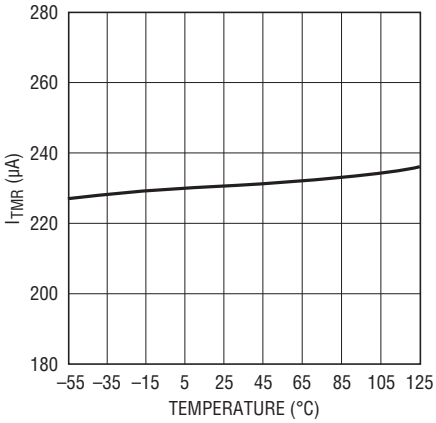
I_{TMR} (Initial Cycle, Sourcing) vs Temperature



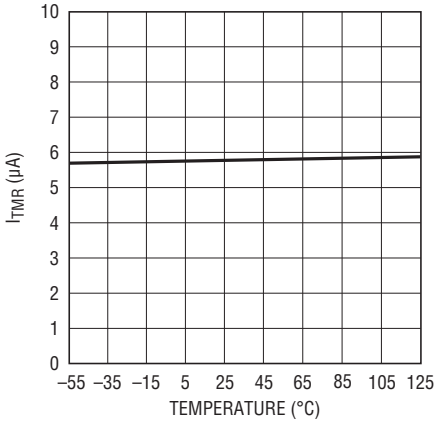
I_{TMR} (Initial Cycle, Sinking) vs Temperature



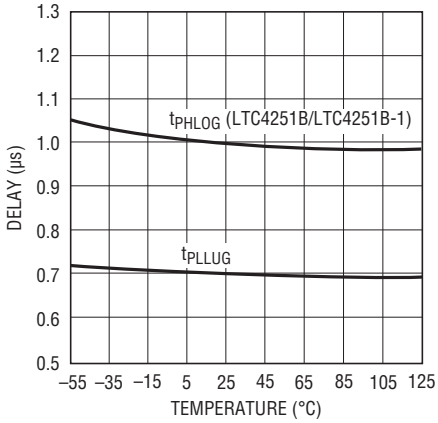
I_{TMR} (Circuit Breaking, Sourcing) vs Temperature



I_{TMR} (Cooling Cycle, Sinking) vs Temperature



t_{PLLUG} and t_{PHLOG} vs Temperature



PIN FUNCTIONS

UV/OV refers to the UV pin for the LTC4251B-2. The OV comparator in the LTC4251B-2 is disabled. All references in the text to overvoltage, OV, V_{OVHI} and V_{OVLO} do not apply to the LTC4251B-2.

SENSE (Pin 1): Circuit Breaker/Current Limit SENSE Pin. Load current is monitored by sense resistor R_S connected between SENSE and V_{EE}, and controlled in three steps. If SENSE exceeds V_{CB} (50mV), the circuit breaker comparator activates a 230µA TIMER pin pull-up current. The LTC4251B/LTC4251B-1/LTC4251B-2 latch off when C_T charges to 4V. If SENSE exceeds V_{ACL} (100mV), the analog current limit amplifier pulls GATE down and regulates the MOSFET current at V_{ACL}/R_S. In the event of a catastrophic short-circuit, SENSE may overshoot 100mV. If SENSE reaches V_{FCL} (200mV), the fast current limit comparator pulls GATE low with a strong pull-down. To disable the circuit breaker and current limit functions, connect SENSE to V_{EE}.

Kelvin-sense connections between the sense resistor and the V_{EE} and SENSE pins are strongly recommended, see Figure 6.

V_{EE} (Pin 2): Negative Supply Voltage Input. Connect this pin to the negative side of the power supply.

V_{IN} (Pin 3): Positive Supply Input. Connect this pin to the positive side of the supply through a dropping resistor. A shunt regulator typically clamps V_{IN} at 13V. An internal undervoltage lockout (UVLO) circuit holds GATE low until the V_{IN} pin is greater than V_{LKO} (9.2V), overriding UV/OV. If UV is high, OV is low and V_{IN} comes out of UVLO, TIMER starts an initial timing cycle before initiating a GATE ramp up. If V_{IN} drops below approximately 8.2V, GATE pulls low immediately.

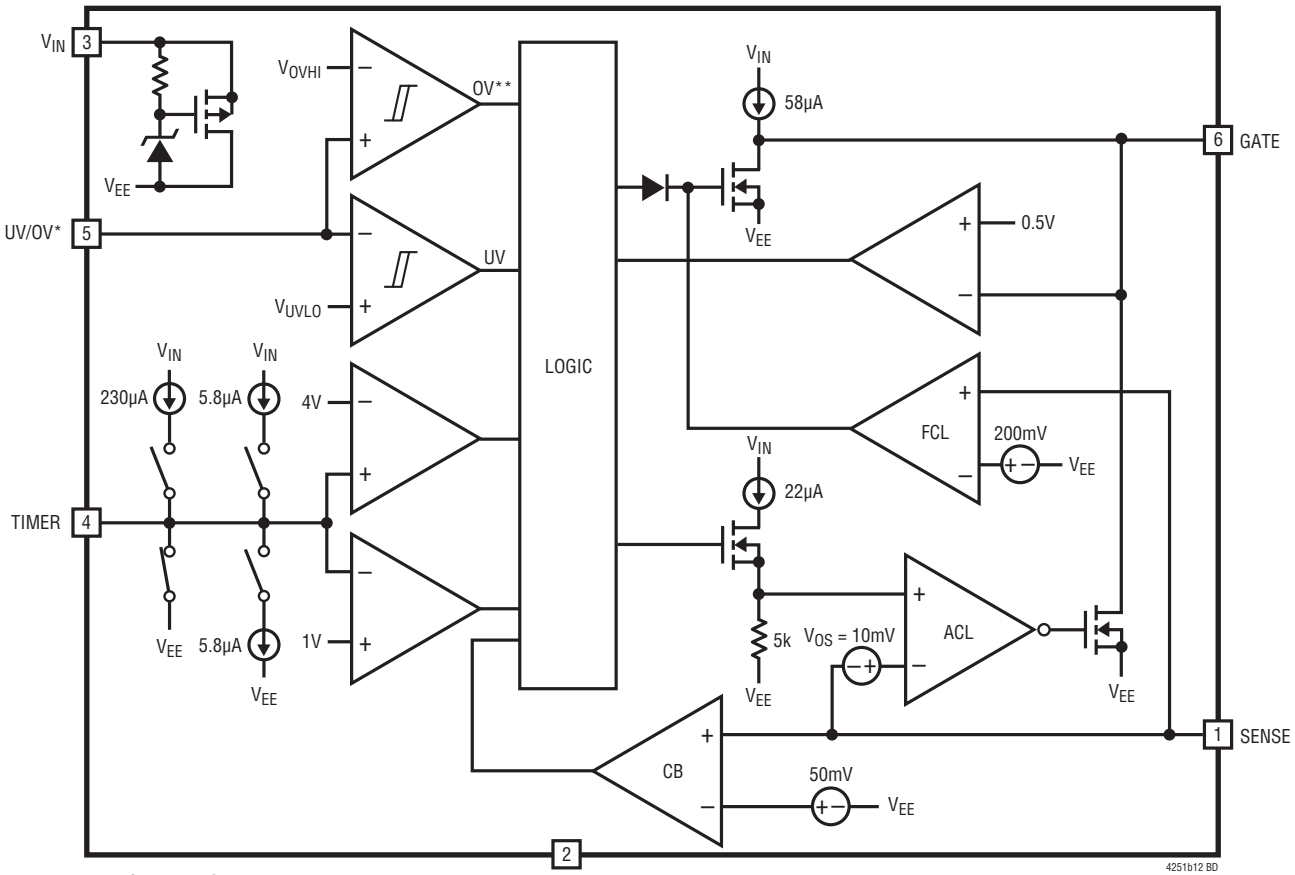
TIMER (Pin 4): Timer Input. TIMER is used to generate a delay at start-up, and to delay shutdown in the event of an output overload. TIMER starts an initial timing cycle when the following conditions are met: UV is high, OV is low, V_{IN} clears UVLO, TIMER pin is low, GATE is lower than V_{GATEL} and $V_{SENSE} – V_{EE} < V_{CB}$. A pull-up current of 5.8µA then charges C_T, generating a time delay. If C_T charges to V_{TMRH} (4V) the timing cycle terminates, TIMER quickly pulls low and GATE is activated.

If SENSE exceeds 50mV while GATE is high, a 230µA pull-up current charges C_T. If SENSE drops below 50mV before TIMER reaches 4V, a 5.8µA pull-down current slowly discharges C_T. In the event that C_T eventually integrates up to the 4V V_{TMRH} threshold, TIMER latches high with a 5.8µA pull-up source and GATE quickly pulls low. The LTC4251B/LTC4251B-1/LTC4251B-2 fault latches may be cleared by either pulling TIMER low with an external device, or by pulling UV/OV below V_{UVLO}.

UV/OV (Pin 5): Undervoltage/Overvoltage Input. This dual function pin detects undervoltage as well as overvoltage. The high threshold at the UV comparator is set at V_{UVHI} with V_{UVHST} hysteresis. The high threshold at the OV comparator is set at V_{OVHI} with V_{OVHST} hysteresis. If UV/OV < V_{UVLO} or UV/OV > V_{OVHI}, GATE pulls low. If UV/OV > V_{UVHI} and UV/OV < V_{OVLO}, the LTC4251B/LTC4251B-1/LTC4251B-2 attempt to start-up. The internal UVLO at V_{IN} always overrides UV/OV. A low at UV resets an internal fault latch. A high at OV pulls GATE low but does not reset the fault latch. A 1nF to 10nF capacitor at UV/OV eliminates transients and switching noise from affecting the UV/OV thresholds and prevents glitches at the GATE pin.

GATE (Pin 6): N-Channel MOSFET Gate Drive Output. This pin is pulled high by a 58µA current source. GATE is pulled low by invalid conditions at V_{IN} (UVLO), UV/OV, or the fault latch. GATE is actively servoed to control fault current as measured at SENSE. A compensation capacitor at GATE stabilizes this loop. A comparator monitors GATE to ensure that it is low before allowing an initial timing cycle, GATE ramp up after an overvoltage event, or restart after a current limit fault.

BLOCK DIAGRAM



*UV FOR THE LTC4251B-2
** THE OV COMPARATOR IS DISABLED FOR LTC4251B-2

OPERATION

Note that for simplicity, the following assumptions are made in the text. Firstly, UV/OV also means the UV pin of the LTC4251B-2. Secondly, all overvoltage conditions and references to OV, V_{OVHI} and V_{OVLO} do not apply to the LTC4251B-2 as the OV comparator in this part is disabled.

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors can draw huge transient currents from the power bus as they charge. The flow of current damages the connector pins and glitches the power bus, causing other boards in the system to reset. The LTC4251B/LTC4251B-1/LTC4251B-2 are designed to turn on a circuit board supply in a controlled manner, allowing insertion or removal without glitches or connector damage.

Initial Start-Up

The LTC4251B/LTC4251B-1/LTC4251B-2 reside on a removable circuit board and control the path between the connector and load or power conversion circuitry with an external MOSFET switch (see Figure 1). Both inrush control and short-circuit protection are provided by the MOSFET.

A detailed schematic is shown in Figure 2. –48V and –48RTN receive power through the longest connector pins, and are the first to connect when the board is inserted. The GATE pin holds the MOSFET off during this time. UV/OV determines whether or not the MOSFET should be turned on based upon internal, high accuracy thresholds and an external divider. UV/OV does double duty by also monitoring whether or not the connector is seated. The top of the divider detects –48RTN by way of a short connector pin that is the last to mate during the insertion sequence.

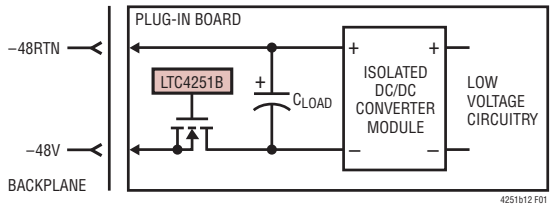


Figure 1. Basic LTC4251B Hot Swap Topology

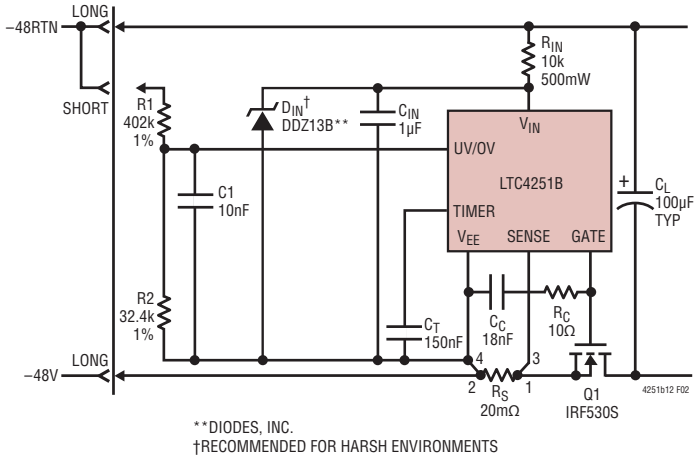


Figure 2. –48V, 2.5A Hot Swap Controller

Interlock Conditions

A start-up sequence commences once five initial "interlock" conditions are met:

1. The input voltage V_{IN} exceeds 9.2V (V_{LKO})
2. The voltage at UV/OV falls within the range of V_{UVHI} to V_{OVLO} (UV > V_{UVHI}, LTC4251B-2)
3. The (SENSE – V_{EE}) voltage is <50mV (V_{CB})
4. The voltage on the timer capacitor (C_T) is less than 1V (V_{TMRL})
5. GATE is less than 0.5V (V_{GATEL})

The first two conditions are continuously monitored and the latter three are checked prior to initial timing or GATE ramp-up. Upon exiting an OV condition, the TIMER pin voltage requirement is inhibited. Details are described in the Applications Information, Timing Waveforms section.

TIMER begins the start-up sequence by sourcing 5.8µA into C_T. If V_{IN} or UV/OV falls out of range, the start-up cycle stops and TIMER discharges C_T to less than 1V, then waits until the aforementioned conditions are once again met. If C_T successfully charges to 4V, TIMER pulls low and GATE is released. GATE sources 58µA (I_{GATE}), charging the MOSFET gate and associated capacitance.

OPERATION

Two modes of operation are possible during the time the MOSFET is first turning on, depending on the values of external components, MOSFET characteristics and nominal design current. One possibility is that the MOSFET will turn on gradually so that the inrush into the load capacitance remains a low value. The output will simply ramp to –48V and the MOSFET will be fully enhanced. A second possibility is that the load current exceeds the current limit threshold of 100mV/R_S. In this case, the LTC4251B/LTC4251B-1/LTC4251B-2 will ramp the output by sourcing 100mV/R_S current into the load capacitance. It is important to set the timer delay so that, regardless of which start-up mode is used, the start-up time is less than the TIMER delay time. If this condition is not met, the LTC4251B/LTC4251B-1/LTC4251B-2 may shutdown after one TIMER delay.

Board Removal

If the board is withdrawn from the card cage, the UV/OV divider is the first to lose connection. This shuts off the MOSFET and commutates the flow of current in the connector. When the power pins subsequently separate, there is no arcing.

Current Control

Three levels of protection handle short-circuit and overload conditions. Load current is monitored by SENSE and resistor R_S. There are three distinct thresholds at SENSE: 50mV for a timed circuit breaker function; 100mV for an analog current limit loop; and 200mV for a fast, feedforward comparator which limits peak current in the event of a catastrophic short-circuit.

If, owing to an output overload, the voltage drop across R_S exceeds 50mV, TIMER sources 230µA into C_T. C_T eventually charges to a 4V threshold and the LTC4251B/LTC4251B-1/LTC4251B-2 latchoff. If the overload goes away and SENSE measures less than 50mV, C_T slowly discharges (5.8µA). In this way the circuit breaker function will also respond to low duty cycle overloads, and accounts for fast heating and slow cooling characteristic of the MOSFET.

Higher overloads are handled by an analog current limit loop. If the drop across R_S reaches 100mV, the current limiting loop servos the MOSFET gate and maintains a constant output current of 100mV/R_S. Note that because SENSE > 50mV, TIMER charges C_T during this time and the LTC4251B/LTC4251B-1/LTC4251B-2 will eventually shut down.

Low impedance failures on the load side of the LTC4251B/LTC4251B-1/LTC4251B-2 coupled with 48V or more driving potential can produce current slew rates well in excess of 50A/µs. Under these conditions, overshoot is inevitable. A fast SENSE comparator with a threshold of 200mV detects overshoot and pulls GATE low much harder and hence much faster than can the weaker current limit loop. The 100mV/R_S current limit loop then takes over, and servos the current as previously described. As before, TIMER runs and latches the LTC4251B/LTC4251B-1/LTC4251B-2 off when C_T reaches 4V.

The LTC4251B/LTC4251B-1/LTC4251B-2 circuit breaker latch is reset by either pulling UV/OV momentarily low, or dropping the input voltage V_{IN} below the internal UVLO threshold of 8.2V.

Although short-circuits are the most obvious fault type, several operating conditions may invoke overcurrent protection. Noise spikes from the backplane or load, input steps caused by the connection of a second, higher voltage supply, transient currents caused by faults on adjacent circuit boards sharing the same power bus, or the insertion of non-hot swappable products could cause higher than anticipated input current and temporary detection of an overcurrent condition. The action of TIMER and C_T rejects these events allowing the LTC4251B/LTC4251B-1/LTC4251B-2 to “ride out” temporary overloads and disturbances that would trip a simple current comparator and in some cases, blow a fuse.

APPLICATIONS INFORMATION

SHUNT REGULATOR

A fast responding shunt regulator clamps the V_{IN} pin to 13V (V_Z). Power is derived from –48RTN by an external current limiting resistor, R_{IN}. A 1µF decoupling capacitor, C_{IN} filters supply transients and contributes a short delay at start-up.

To meet creepage requirements R_{IN} may be split into two or more series connected units, such as two 5.1k or three 3.3k resistors. This introduces a wider total spacing than is possible with a single component while at the same time ballasting the potential across the gap under each resistor. The LTC4251B is fundamentally a low voltage device that operates with –48V as its reference ground. To further protect against arc discharge into its pins, the area in and around the LTC4251B and all associated components should be free of any other planes such as chassis ground, return, or secondary-side power and ground planes.

V_{IN} is rated handle 30mA within the thermal limits of the package, and is tested to survive a 100µs, 100mA pulse. To protect V_{IN} against damage from higher amplitude spikes, clamp V_{IN} to V_{EE} with a 13V Zener diode. Star connect V_{EE} and all V_{EE} referred components to the sense resistor Kelvin terminal as illustrated in Figure 2, keeping trace lengths between V_{IN}, C_{IN}, D_{IN} and V_{EE} as short as possible.

INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

Internal circuitry monitors V_{IN} for undervoltage. The exact thresholds are defined by V_{LKO} and its hysteresis, V_{LKH}. When V_{IN} rises above 9.2V (V_{LKO}) the chip is enabled; below 8.2V (V_{LKO}-V_{LKH}) it is disabled and GATE is pulled low. The UVLO function at V_{IN} should not be confused with the UV/OV pin. These are completely separate functions.

UV/OV COMPARATORS

Two hysteretic comparators for detecting under- and overvoltage conditions, with the following thresholds, monitor the dual function UV/OV pin:

UV turning on at V_{UVHI}

UV turning off at V_{UVLO}

OV turning off at V_{OVHI}

OV turning on at V_{OVLO}

The UV and OV trip point ratio for LTC4251B is designed to match the standard telecom operating range of 43V to 75V. The LTC4251B-2 implements a UV threshold of 43V only.

A divider (R1, R2) is used to scale the supply voltage. Using R1 = 402k and R2 = 32.4k gives a typical operating range of 43.2V to 74.4V. The under- and overvoltage shutdown thresholds are then 39.2V and 82.5V. 1% divider resistors are recommended to preserve threshold accuracy. The same resistor values can be used for the LTC4251B-2.

The R1-R2 divider values shown in the Typical Application set a standing current of slightly more than 100µA, and define an impedance at UV/OV of 30k. In most applications, 30k impedance coupled with 300mV UV hysteresis makes the LTC4251B/LTC4251B-1/LTC4251B-2 insensitive to noise. If more noise immunity is desired, add a 1nF to 10nF filter capacitor from UV/OV to V_{EE}.

The UV and OV trip point thresholds for the LTC4251B-1 are designed to encompass the standard telecom operating range of –36V to –72V.

A divider (R1, R2) is used to scale the supply voltage. Using R1 = 442k and R2 = 34.8k gives a typical operating range of 33.2V to 81V. The typical under- and overvoltage shutdown thresholds are then 29.6V and 84.5V. 1% divider resistors are recommended to preserve threshold accuracy.

The R1-R2 divider values shown in the Typical Application set a standing current of slightly more than 100µA, and define an impedance at UV/OV of 32k. In most applications, 32k impedance coupled with 260mV UV hysteresis makes the LTC4251B-1 insensitive to noise. If more noise immunity is desired, add a 1nF to 10nF filter capacitor from UV/OV to V_{EE}.

UV/OV OPERATION

A low input to the UV comparator will reset the chip and pull the GATE and TIMER pins low. A low-to-high UV transition will initiate an initial timing sequence if the three remaining interlock conditions are met.

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Overvoltage conditions detected by the OV comparator will also pull GATE low, thereby shutting down the load, but it will not reset the circuit breaker latch. Returning the supply voltage to an acceptable range restarts the GATE pin provided all interlock conditions except TIMER are met.

TIMER

The operation of the TIMER pin is somewhat complex as it handles several key functions. A capacitor, C_T, is used at TIMER to provide timing for the LTC4251B/LTC4251B-1/LTC4251B-2. Four different charging and discharging modes are available at TIMER:

1. 5.8µA slow charge; initial timing delay
2. 230µA fast charge; circuit breaker delay
3. 5.8µA slow discharge; circuit breaker "cool-off"
4. Low impedance switch; resets capacitor after initial timing delay, in undervoltage lockout, and in overvoltage

For initial startup, the 5.8µA pull-up is used. The low impedance switch is turned off and the 5.8µA current source is enabled when the four interlock conditions are met. C_T charges to 4V in a time period given by:

$$t = \frac{4V \bullet C_T}{5.8\mu A} \quad (1)$$

When C_T reaches 4V (V_{TMRH}), the low impedance switch turns on and discharges C_T. The GATE output is enabled and the load turns on.

CIRCUIT BREAKER TIMER OPERATION

If the SENSE pin detects more than 50mV across R_S, the TIMER pin charges C_T with 230µA. If C_T charges to 4V, the GATE pin pulls low and the LTC4251B/LTC4251B-1/LTC4251B-2 latch off. The part remains latched off until either the UV/OV pin is momentarily pulsed low, or V_{IN} dips into UVLO and is then restored. The circuit breaker timeout period is given by

$$t = \frac{4V \bullet C_T}{230\mu A} \quad (2)$$

Intermittent overloads may exceed the 50mV threshold at SENSE, but if their duration is sufficiently short TIMER will not reach 4V and the LTC4251B/LTC4251B-1/LTC4251B-2 will not latch off. To handle this situation, the TIMER discharges C_T slowly with a 5.8µA pull-down whenever the SENSE voltage is less than 50mV. Therefore any intermittent overload with an aggregate duty cycle of 2.5% or more will eventually trip the circuit breaker and latch off the LTC4251B/LTC4251B-1/LTC4251B-2. Figure 3 shows the circuit breaker response time in seconds normalized to 1µF. The asymmetric charging and discharging of C_T is a fair gauge of MOSFET heating.

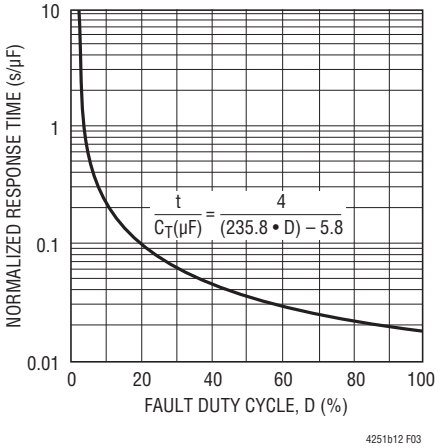

Figure 3. Circuit Breaker Response Time

GATE

GATE is pulled low to V_{EE} under any of the following conditions: in UVLO, during the initial timing cycle, in an overvoltage condition, or when the LTC4251B/LTC4251B-1/LTC4251B-2 are latched off after a short-circuit. When GATE turns on, a 58µA current source charges the MOSFET gate and any associated external capacitance. V_{IN} limits gate drive to no more than 14.5V.

Gate-drain capacitance (C_{GD}) feed through at the first abrupt application of power can cause a gate-source voltage sufficient to turn on the MOSFET. A unique circuit pulls GATE low with practically no usable voltage at V_{IN}, and eliminates current spikes at insertion. A large external gate-source capacitor is thus unnecessary for the purpose of compensating C_{GD}. Instead, a smaller value (≥10nF) capacitor C_C is adequate. C_C also provides compensation for the analog current limit loop.

APPLICATIONS INFORMATION

SENSE

The SENSE pin is monitored by the circuit breaker (CB) comparator, the analog current limit (ACL) amplifier, and the fast current limit (FCL) comparator. Each of these three measures the potential of SENSE relative to V_{EE}. If SENSE exceeds 50mV, the CB comparator activates the 230µA TIMER pull-up. At 100mV, the ACL amplifier servos the MOSFET current, and at 200mV the FCL comparator abruptly pulls GATE low in an attempt to bring the MOSFET current under control. If any of these conditions persists long enough for TIMER to charge C_T to 4V (see Equation (2)), the LTC4251B/LTC4251B-1/LTC4251B-2 latch off and pull GATE low.

If the SENSE pin encounters a voltage greater than 100mV, the ACL amplifier will servo GATE downwards in an attempt to control the MOSFET current. Since GATE overdrives the MOSFET in normal operation, the ACL amplifier needs time to discharge GATE to the threshold of the MOSFET. For a mild overload, the ACL amplifier can control the MOSFET current, but in the event of a severe overload the current may overshoot. At SENSE = 200mV, the FCL comparator takes over, quickly discharging the GATE pin to near V_{EE} potential. FCL then releases, and the ACL amplifier takes over. All the while TIMER is running. The effect of FCL is to add a nonlinear response to the control loop in favor of reducing MOSFET current.

Owing to inductive effects in the system, FCL typically overcorrects the current limit loop, and GATE undershoots. A zero in the loop (resistor R_C in series with the gate capacitor) helps the ACL amplifier recover.

SHORT-CIRCUIT OPERATION

Circuit behavior arising from a load-side low impedance short is shown in Figure 4. Initially, the current overshoots the analog current limit level of V_{SENSE} = 100mV (Trace 2) as the GATE pin works to bring V_{GS} under control (Trace 3). The overshoot glitches the backplane in the negative direction, and when the current is reduced to 100mV/R_S the backplane responds by glitching in the positive direction.

TIMER commences charging C_T (Trace 4) while the analog current limit loop maintains the fault current at 100mV/R_S, which in this case is 5A (Trace 2). Note that the backplane voltage (Trace 1) sags under load. When C_T reaches 4V, GATE turns off, the load current drops to zero and the backplane rings up to over 100V. The positive peak is usually limited by avalanche breakdown in the MOSFET, and can be further limited by adding a transient voltage suppressor across the input from –48V to –48RTN, such as Diodes Inc. SMAT70A.

A low impedance short on one card may influence the behavior of others sharing the same backplane. The initial glitch and backplane sag as seen in Figure 4, Trace 1, can rob charge from output capacitors on adjacent cards. When the faulty card shuts down, current flows in to refresh the capacitors. If LTC4251B, LTC4251B-1 or LTC4251B-2s are used throughout, they respond by limiting the inrush current to a value of 100mV/R_S. If C_T is sized correctly, the capacitors will recharge long before C_T times out.

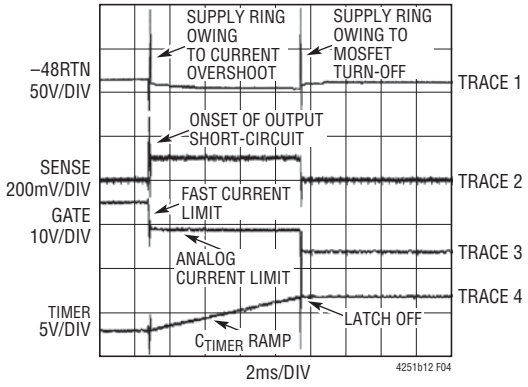

Figure 4. Output Short-Circuit Behavior (All Waveforms are Referenced to V_{EE})

MOSFET SELECTION

The external MOSFET switch must have adequate safe operating area (SOA) to charge the load capacitance on start-up and handle short-circuit conditions until TIMER latchoff. These considerations take precedence over DC current ratings. A MOSFET with adequate SOA for a given application can always handle the required current, but the opposite cannot be said. Consult the manufacturer's MOSFET data sheet for safe operating area and effective transient thermal impedance curves.

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MOSFET selection is a three-step process. First, R_S is calculated, and then the time required to charge the load capacitance is determined. This timing, along with the maximum short-circuit current and maximum input voltage defines an operating point that is checked against the MOSFET's SOA curve.

To begin a design, first specify the required load current and load capacitance, I_L and C_L. The circuit breaker current trip point (50mV/R_S) should be set to accommodate the maximum load current. Note that maximum input current to a DC/DC converter is expected at $V_{SUPPLY\ (MIN)}$. R_S is given by:

$$R_S = \frac{40mV}{I_{L(MAX)}} \quad (3)$$

where 40mV represents the guaranteed minimum circuit breaker threshold.

During the initial charging process, the LTC4251B/LTC4251B-1/LTC4251B-2 may operate the MOSFET in current limit, forcing 80mV to 120mV across R_S. The minimum inrush current is given by:

$$I_{INRUSH(MIN)} = \frac{80mV}{R_S} \quad (4)$$

Maximum short-circuit current limit is calculated using maximum V_{SENSE}, or:

$$I_{SHORT\text{-}CIRCUIT(MAX)} = \frac{120mV}{R_S} \quad (5)$$

The TIMER capacitor C_T must be selected based on the slowest expected charging rate; otherwise TIMER might time out before the load capacitor is fully charged. A value for C_T is calculated based on the maximum time it takes the load capacitor to charge. That time is given by:

$$t_{CL\ CHARGE} = \frac{C \bullet V}{I} = \frac{C_L \bullet V_{SUPPLY(MAX)}}{I_{INRUSH(MIN)}} \quad (6)$$

Substituting Equation (4) for $I_{INRUSH(MIN)}$ and equating (6) with (2) gives:

$$C_T = \frac{C_L \bullet V_{SUPPLY\ (MAX)} \bullet R_S \bullet 230\mu A}{(4V \bullet 80mV)} \quad (7)$$

Returning to Equation (2), the TIMER period is calculated and used in conjunction with $V_{SUPPLY(MAX)}$ and $I_{SHORT\text{-}CIRCUIT(MAX)}$ to check the SOA curves of a prospective MOSFET.

As a numerical design example, consider a 30W load, which requires 1A input current at 36V. If $V_{SUPPLY(MAX)}$ = 72V and C_L = 100µF, Equation (3) gives R_{SENSE} = 40mΩ; Equation (7) gives C_T = 207nF. To account for errors in R_{SENSE}, C_T, TIMER current (230µA) and TIMER threshold (4V), the calculated value should be multiplied by 1.5, giving a nearest standard value of C_T = 330nF.

If a short-circuit occurs, a current of up to 120mV/40mΩ = 3A will flow in the MOSFET for 5.7ms as dictated by C_T = 330nF in Equation (2). The MOSFET must be selected based on this criterion. The IRF530S can handle 100V and 3A for 10ms, and is safe to use in this application.

SUMMARY OF DESIGN FLOW

To summarize the design flow, consider the application shown in Figure 2, which was designed for 50W:

Calculate maximum load current: 50W/36V = 1.4A; allowing 83% converter efficiency, $I_{IN\ (MAX)}$ = 1.7A.

Calculate R_S: from Equation (3) R_S = 20mΩ.

Calculate C_T: from Equation (7) C_T = 150nF (including 1.5X correction factor).

Calculate TIMER period: from Equation (2) the short-circuit time-out period is t = 2.6ms.

Calculate maximum short-circuit current: from Equation (5) maximum short-circuit current could be as high as 120mV/20mΩ = 6A.

Consult MOSFET SOA curves: the IRF530S can handle 6A at 72V for 5ms, so it is safe to use in this application.

APPLICATIONS INFORMATION

FREQUENCY COMPENSATION

The LTC4251B/LTC4251B-1/LTC4251B-2 typical frequency compensation network for the analog current limit loop is a series R_C (10Ω) and C_C connected to V_{EE}. Figure 5 depicts the relationship between the compensation capacitor C_C and the MOSFET's C_{ISS}. The line in Figure 5 is used to select a starting value for C_C based upon the MOSFET's C_{ISS} specification. Optimized values for C_C are shown for several popular MOSFETs. Differences in the optimized value of C_C versus the starting value are small. Nevertheless, compensation values should be verified by board level short-circuit testing.

As seen in Figure 4 previously, at the onset of a short-circuit event, the input supply voltage can ring dramatically owing to series inductance. If this voltage avalanches the MOSFET, current continues to flow through the MOSFET to the output. The analog current limit loop cannot control this current flow and therefore the loop undershoots. This effect cannot be eliminated by frequency compensation. A zener diode is required to clamp the input supply voltage and prevent MOSFET avalanche.

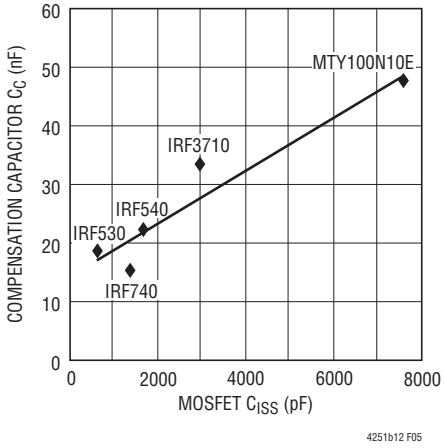

Figure 5. Recommended Compensation Capacitor C_C vs MOSFET C_{ISS}

SENSE RESISTOR CONSIDERATIONS

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the V_{EE} and SENSE pins are strongly recommended. The drawing in Figure 6 illustrates the correct way of making connections between the LTC4251B/LTC4251B-1/LTC4251B-2 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

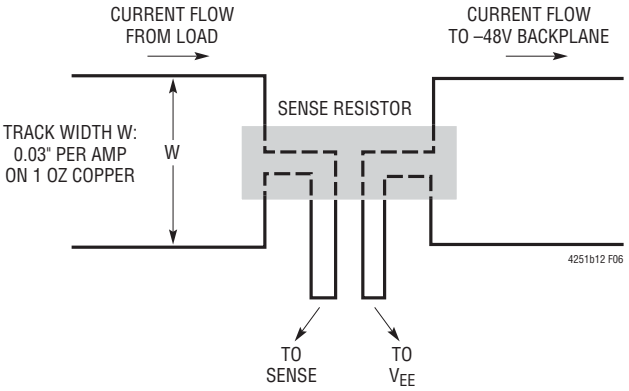

Figure 6. Making PCB Connections to the Sense Resistor

TIMING WAVEFORMS

System Power-Up

Figure 7 details the timing waveforms for a typical power-up sequence in the case where a board is already installed in the backplane and system power is applied abruptly. At time point 1, the supply ramps up, together with UV/OV and V_{OUT}. V_{IN} follows at a slower rate as set by the V_{IN} bypass capacitor. At time point 2, V_{IN} exceeds V_{LKO} and the internal logic checks for V_{UVHI} < UV/OV < V_{OVLO}, TIMER < V_{TMRL}, GATE < V_{GATEL} and SENSE < V_{CB}. When all conditions are met, an initial timing cycle starts and the TIMER capacitor is charged by a 5.8µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is then quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL} and SENSE < V_{CB} must be satisfied before a start-up cycle is allowed to begin. GATE sources 58µA into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor. At time point 5, the SENSE voltage ($V_{SENSE} – V_{EE}$) reaches the V_{CB} threshold and activates the TIMER. The TIMER capacitor

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is charged by a 230µA current-source pull-up. At time point 6, the analog current limit loop activates. Between time point 6 and time point 7, the GATE voltage is held essentially constant and the sense voltage is regulated at V_{ACL}. As the load capacitor nears full charge, its current begins to decline. At point 7, the load current falls and the sense voltage drops below V_{ACL}. The analog current limit loop shuts off and the GATE pin ramps further. At time point 8, the sense voltage drops below V_{CB} and TIMER now discharges through a 5.8µA current source pull-down. At time point 9, GATE reaches its maximum voltage as determined by V_{IN}.

Live Insertion with Short Pin Control of UV/OV

In this example as shown in Figure 8, power is delivered through long connector pins whereas the UV/OV divider makes contact through a short pin. This ensures the power connections are firmly established before the LTC4251B/LTC4251B-1/LTC4251B-2 are activated. At time point 1, the power pins make contact and V_{IN} ramps through V_{LKO}. At time point 2, the UV/OV divider makes contact and its voltage exceeds V_{UVHI}. In addition, the internal logic checks for V_{UVHI} < UV/OV < V_{OVHI}, TIMER < V_{TMRL}, GATE < V_{GATEL} and SENSE < V_{CB}. When all conditions are met, an initial timing cycle starts and the TIMER capacitor is charged by a 5.8µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is then quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL} and SENSE < V_{CB} must be satisfied before a start-up cycle is allowed to begin. GATE sources 58µA into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor. At time point 5, the SENSE voltage ($V_{SENSE} – V_{EE}$) reaches the V_{CB} threshold and activates the TIMER. The TIMER capacitor is charged by a 230µA current source pull-up. At time point 6, the analog current limit loop activates. Between time point 6 and time point 7, the GATE voltage is held essentially constant and the sense voltage is regulated at V_{ACL}. As the load capacitor nears full charge, its current begins to decline. At time point 7, the load current falls and the sense voltage drops below V_{ACL}. The analog current limit loop shuts off and the GATE pin ramps further. At time point 8, the sense voltage drops below V_{CB} and TIMER now discharges through a 5.8µA current source pull-down. At time point 9, GATE reaches its maximum voltage as determined by V_{IN}.

Undervoltage Lockout Timing

In Figure 9, when UV/OV drops below V_{UVLO} (time point 1), TIMER and GATE pull low. If current has been flowing, the SENSE pin voltage decreases to zero as GATE collapses. When UV/OV recovers and clears V_{UVHI} (time point 2), an initial time cycle begins followed by a start-up cycle.

Undervoltage Timing with Overvoltage Glitch

In Figure 10, when UV/OV clears V_{UVHI} (time point 1), an initial timing cycle starts. If the system bus voltage overshoots V_{OVHI} as shown at time point 2, TIMER discharges. At time point 3, the supply voltage recovers and drops below the V_{OVLO} threshold. The initial timing cycle restarts followed by a start-up cycle.

Overvoltage Timing

During normal operation, if UV/OV exceeds V_{OVHI} as shown at time point 1 of Figure 11, the TIMER status is unaffected. Nevertheless, GATE pulls down and disconnects the load. At time point 2, UV/OV recovers and drops below the V_{OVLO} threshold. A gate ramp up cycle ensues. If the overvoltage glitch is long enough to deplete the load capacitor, a full start-up cycle may occur as shown between time points 3 through 6.

Timer Behavior

In Figure 12a, the TIMER capacitor charges at 230µA if the SENSE pin exceeds V_{CB}. It is discharged with 5.8µA if the SENSE pin is less than V_{CB}. In Figure 12b, when TIMER exceeds V_{TMRH}, TIMER is latched high by the 5.8µA pull-up and GATE pulls down immediately. In Figure 12c, multiple momentary faults cause the TIMER capacitor to integrate until it latches.

APPLICATIONS INFORMATION

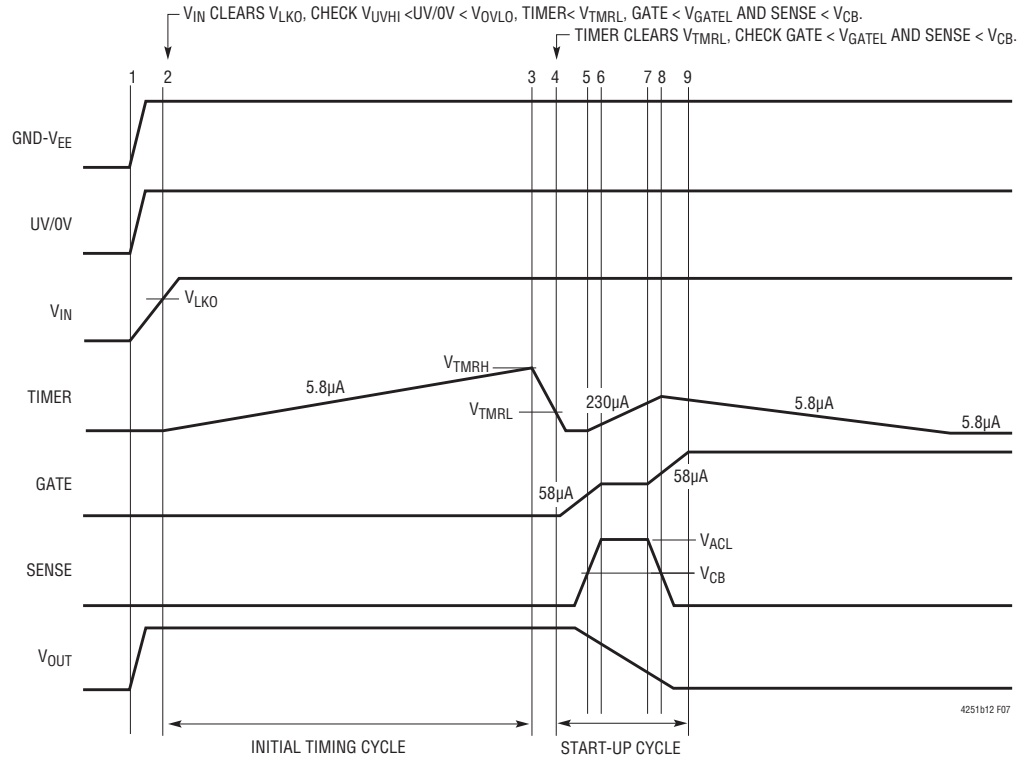


Figure 7. System Power-Up Timing (All Waveforms are Referenced to V_{EE})

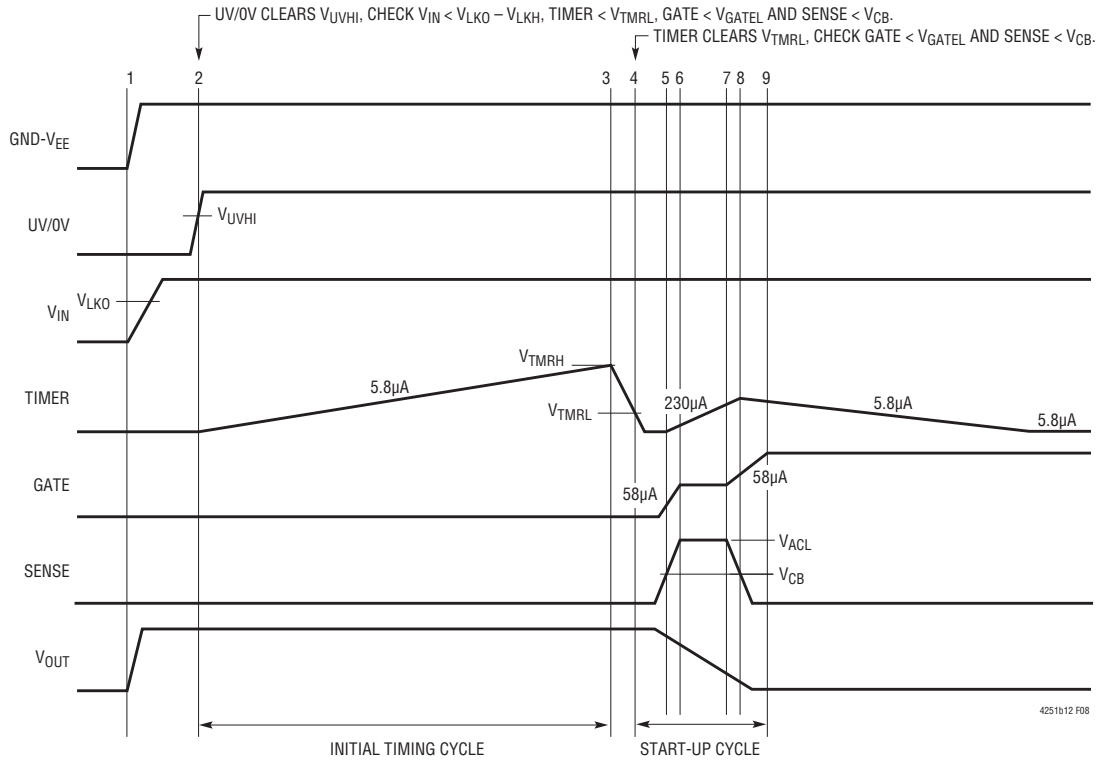


Figure 8. Power-Up Timing with a Short-Pin (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

Analog Current Limit and Fast Current Limit

In Figure 13a, when SENSE exceeds V_{ACL}, GATE is regulated by the analog current limit amplifier loop. When SENSE drops below V_{ACL}, GATE is allowed to pull up. In Figure 13b, when a severe fault occurs, SENSE exceeds V_{FCL} and GATE immediately pulls down until the analog current amplifier can establish control. If TIMER reaches V_{TMRH}, GATE pulls low and latches off.

Resetting a Fault Latch

As shown in Figure 14, a latched fault is reset by either pulling UV/OV below V_{UVLO} or pulling TIMER below V_{TMRL}. An initial timing cycle is initiated if UV/OV is used for reset. If TIMER is used for reset, the initial timing cycle is skipped.

Internal Soft-Start

An internal soft-start feature ramps the positive input of the analog current limit amplifier during initial start-up. The ramp duration is approximately 200µs. This feature reduces load current dI/dt at start-up. As illustrated in Figure 15, soft-start is initiated by a TIMER transition from V_{TMRH} to V_{TMRL} or when UV/OV falls below the V_{OVLO} threshold after an OV fault. After soft-start duration, load current is limited by V_{ACL}/R_S.

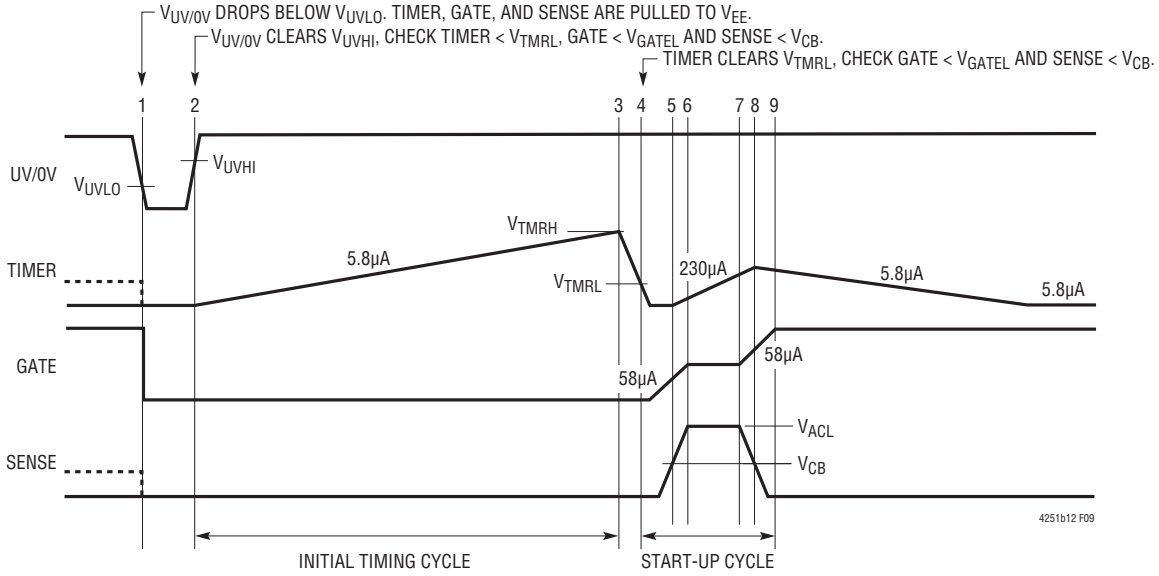


Figure 9. Undervoltage Lockout Timing (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

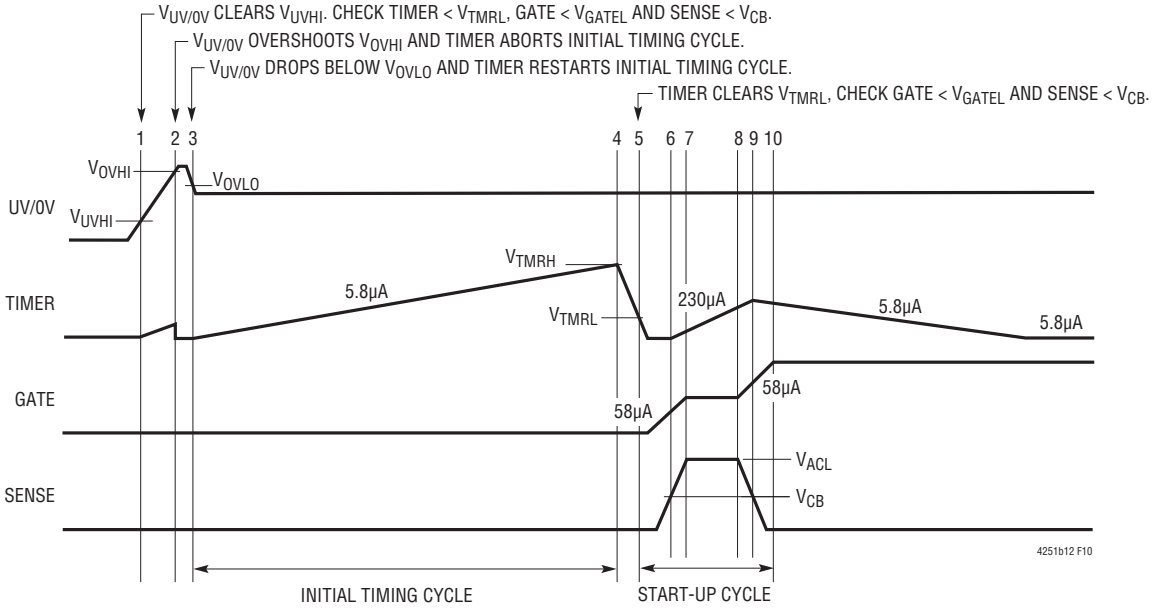


Figure 10. Undervoltage Timing with an Overvoltage Glitch (All Waveforms are Referenced to V_{EE})

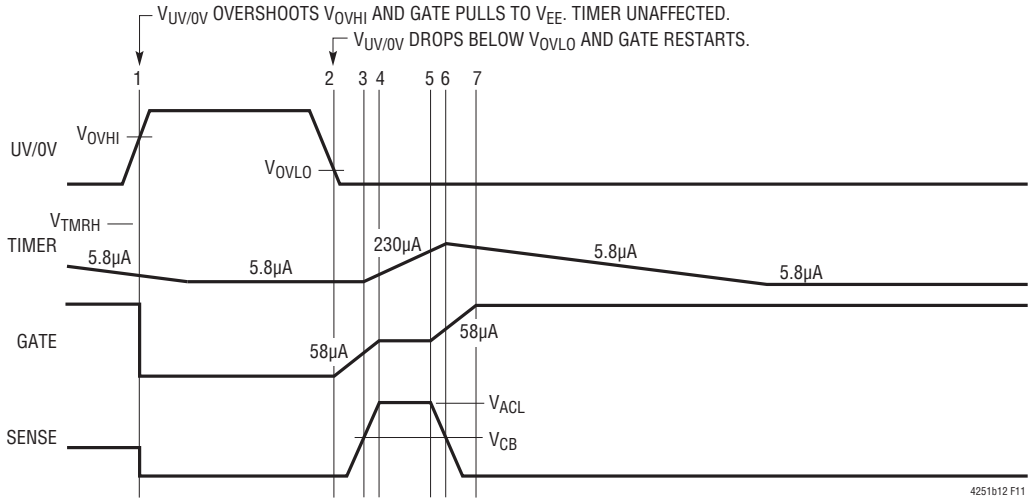
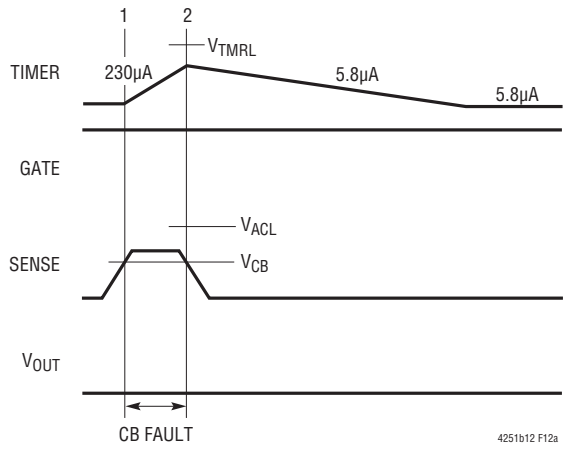
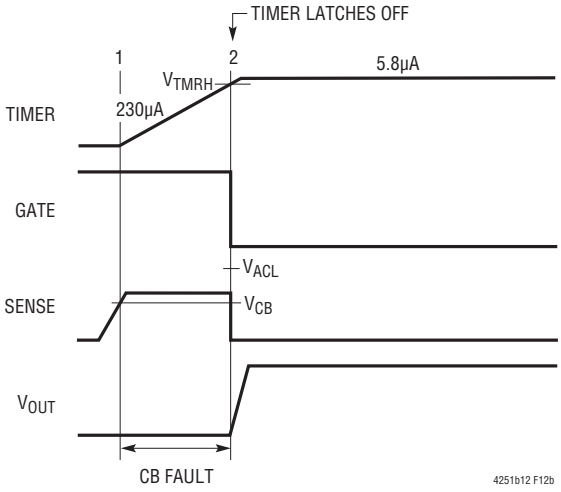


Figure 11. Overvoltage Timing (All Waveforms are Referenced to V_{EE})

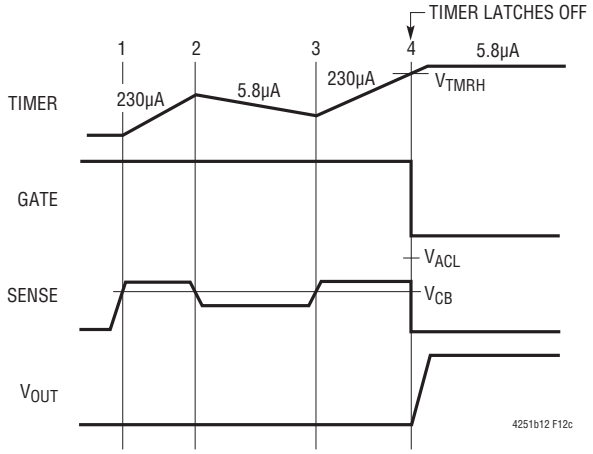
APPLICATIONS INFORMATION



(12a) Momentary Circuit-Breaker Fault



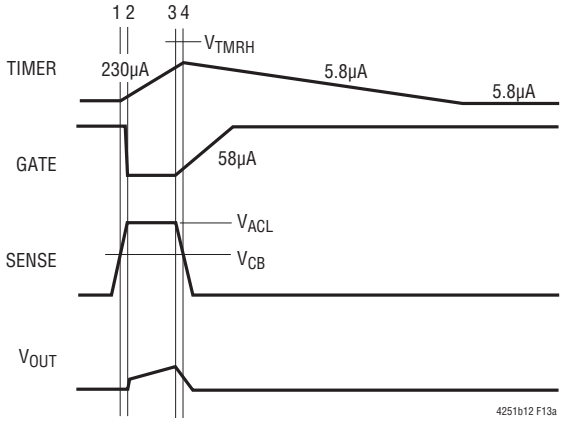
(12b) Circuit-Breaker Time-Out



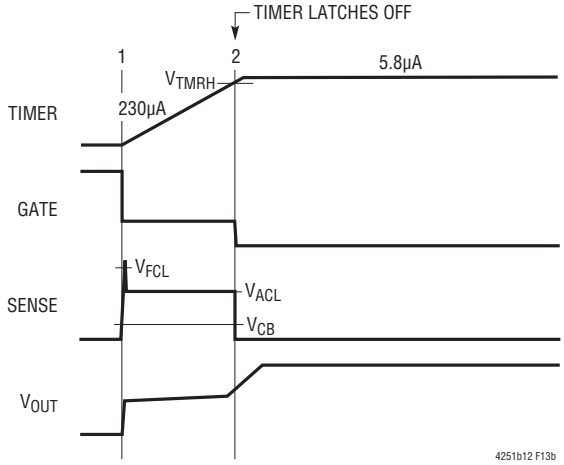
(12c) Multiple Circuit-Breaker Faults

Figure 12. Timer Behavior (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION



(13a) Analog Current Limit Fault



(13b) Fast Current Limit Fault

Figure 13. Current Limit Behavior (All Waveforms are Referenced to V_{EE})

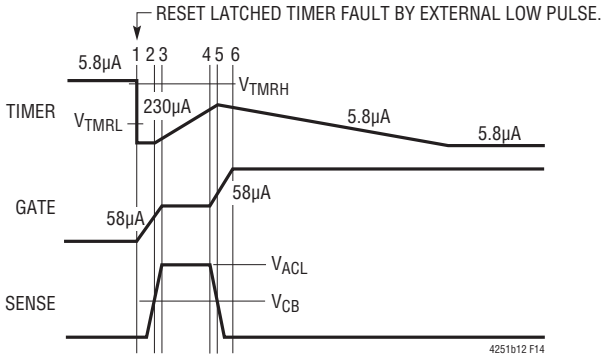


Figure 14. Latched Fault Reset Timing (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

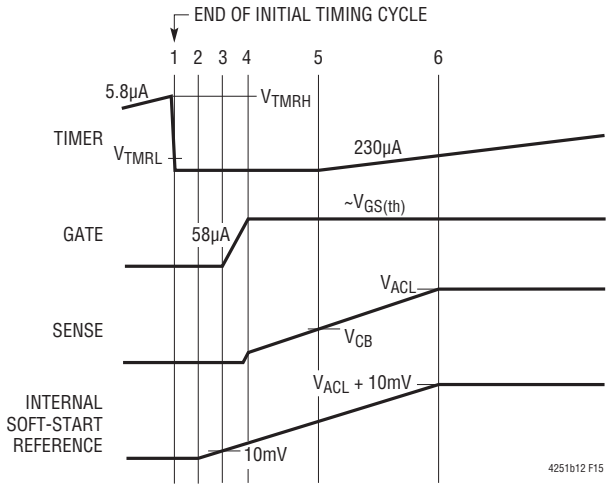
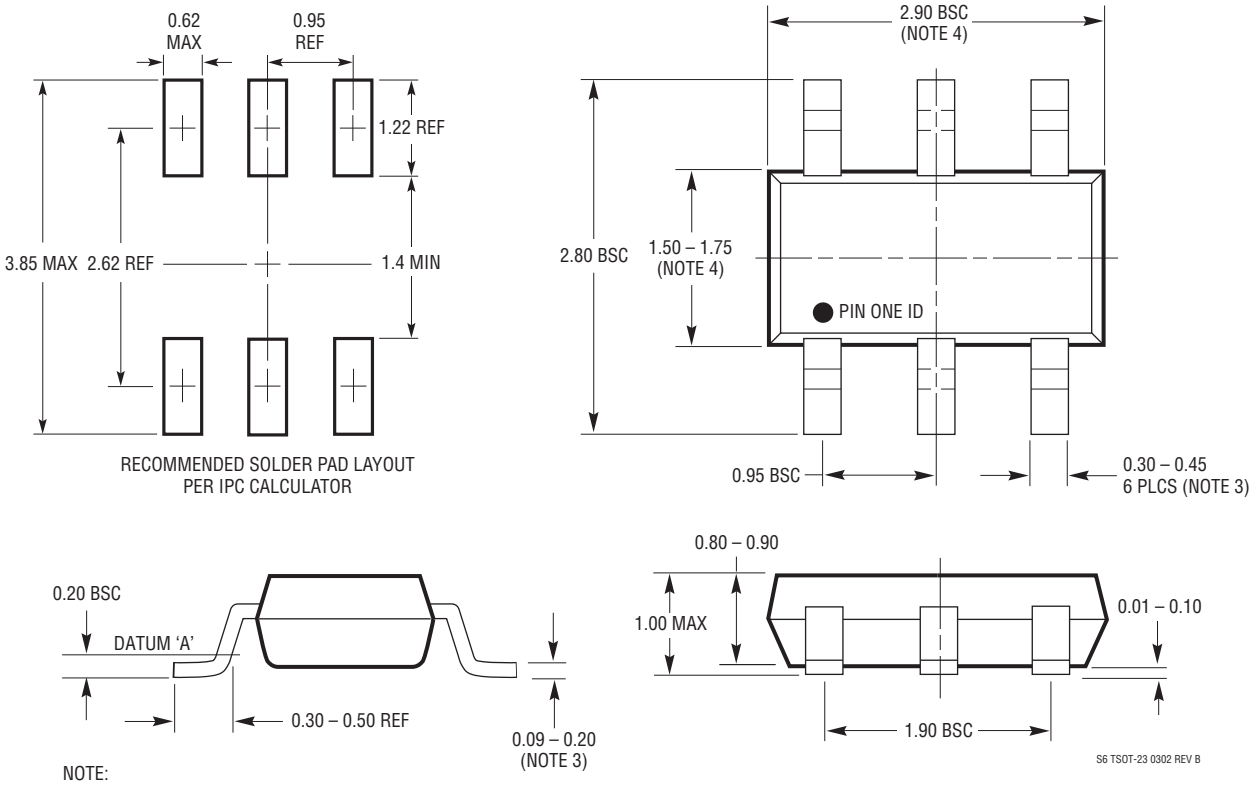


Figure 15. Internal Soft-Start Timing (All Waveforms are Referenced to V_{EE})

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193