Quad Network Power Controller with I²C Compatible Interface

FEATURES

- **Controls Four Independent –48V Power Channels**
- **Each Channel has Separate Relay Drivers, ON/OFF Control, Short-Circuit Protection with Current Foldback, Open-Circuit Detection, and Power Good Indication**
- Programmed via I²C™ Compatible Interface
- Five Bit Programmable Digital Address Allows Control of up to 32 LTC4255s (128 Channels)
- Interrupt on $\overline{\text{FAULT}}$ Output can be used to Eliminate Software Polling
- Programmable Current Limit and Open-Circuit Duration Periods
- Programmable Latchoff or Autoretry after Short-Circuit Faults
- Programmable Autoretry Duty Cycle

APPLICATIONS

- IP Phone Systems
- DTE Power Distribution

DESCRIPTION

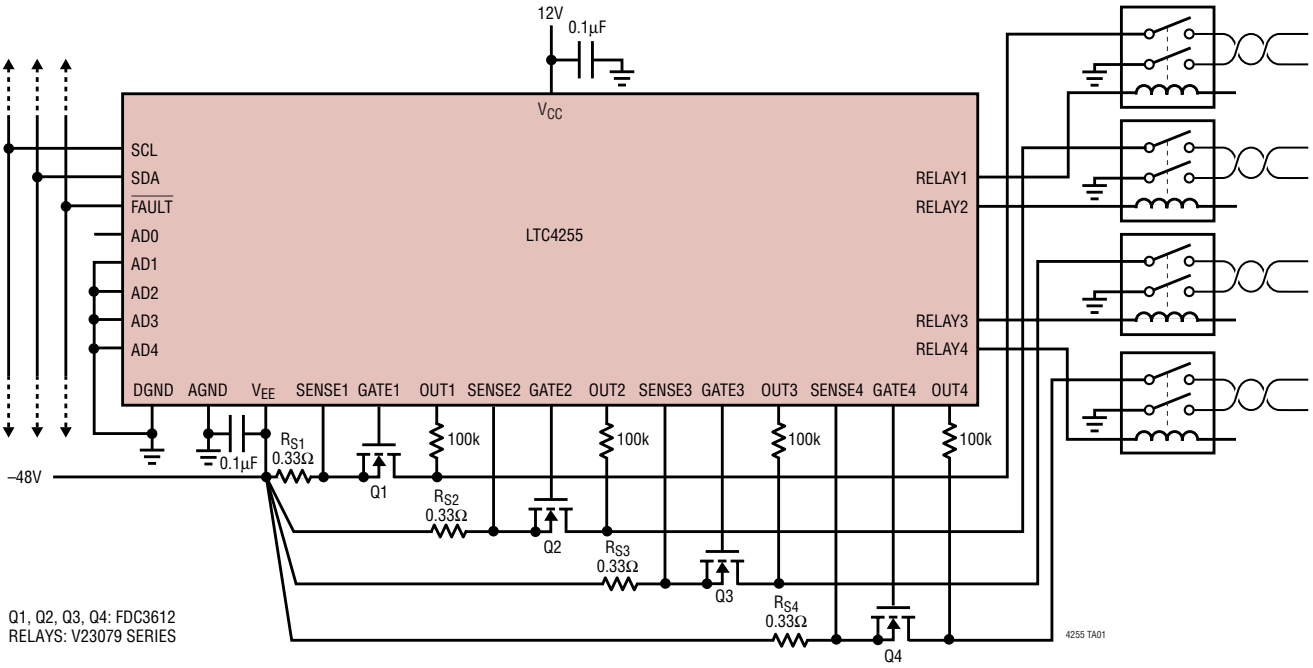
The LTC®4255 is a quad –48V network power controller with independent relay drivers and I²C compatible interface. Each channel can be turned on and off via software control, while providing short-circuit protection, open-circuit detection, and power good indication. The short-circuit protection includes a current foldback feature to reduce power dissipation in the switch during shorts and start-up.

The serial interface allows up to 128 channels to be controlled with only two digital lines. A $\overline{\text{FAULT}}$ output can be used as an interrupt line to eliminate fault detection by software polling.

External switches and current sense resistors allow easy scaling of current and power dissipation levels and provide the maximum protection against voltage and current spikes.

The LTC4255 is available in the 28-pin SSOP package.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- V_{CC} to DGND 18V
- V_{EE} to AGND ..... –80V
- DGND to AGND ..... ±5V

Digital Pin Voltages
- SCL, SDA, $\overline{FAULT}$ ..... DGND – 0.3V to 6V
- AD0-4 ..... DGND – 0.3V to 5.5V

Relay Driver Output Voltage
- RELAY1-4 (Note 5) ..... DGND –0.3V to DGND + 15V

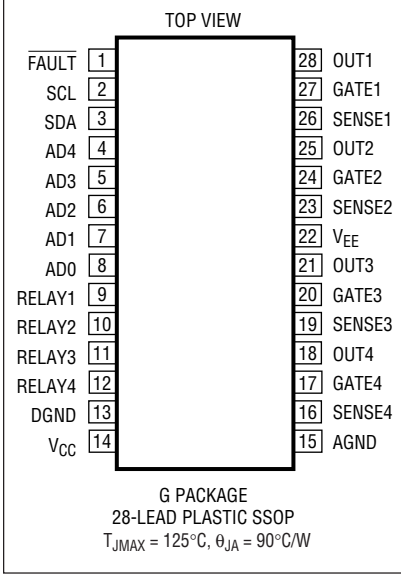
Analog Voltages
- SENSE1-4 ..... V_{EE} – 0.3V to V_{EE} + 1V
- OUT1-4 ..... V_{EE} – 80V to V_{EE} + 80V

Operating Temperature Range
- LTC4255C ..... 0°C to 70°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LTC4255CG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, V_{EE} = –48V, AGND = DGND = 0V (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
V_{CC}	Positive Supply Voltage	V_{CC} Referenced to DGND		10.8	12	13.2	V
I_{CC}	Positive Supply Current	Relays Off All Relays On			2.1 10	3 15	mA mA
V_{EE}	Negative Supply Voltage	V_{EE} Referenced to AGND			–48	–72	V
I_{EE}	Negative Supply Current				–1.9	–3	mA
ΔV_{GND}	DC Ground Difference	AGND – DGND (Note 3)		–5		5	V
V_{LKO}	V_{EE} Undervoltage Lockout				–27		V
ΔV_{GATE}	External Gate Voltage (V_{GATE} – V_{EE})	I_{GATE} = –1µA		10	13	15	V
I_{GATE}	GATE Pin Output Current	GATE On, V_{GATE} = V_{EE} GATE Off, V_{GATE} = V_{EE} + 5V		–30 30	–50 50	–70 80	µA µA
V_{SC}	Short-Circuit Sense Voltage	(V_{SENSE} – V_{EE}), V_{OUT} – V_{EE} = 0V	●	125	150	170	mV
V_{OC}	Open-Circuit Sense Voltage	(V_{SENSE} – V_{EE})	●	1	3	4.5	mV
V_{PG}	Power_OK Threshold Voltage	(V_{OUT} – V_{EE})	●	1	2	3	V
I_{OUT}	OUT Pin Current	V_{OUT} = V_{EE}			–1.4		µA
V_{OLR}	Relay Driver Output Low Voltage	(V_{RELAY} – DGND), I_{RELAY} = 50mA, RELAY On				0.3	V
V_{CLAMPR}	Relay Driver Clamp Voltage	(V_{RELAY} – DGND), I_{RELAY} = 50mA, RELAY Off (Note 5)			18	24	V
V_{OLD}	Digital Output Low Voltage	SDA, $\overline{FAULT}$, I = 3mA	●			0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, V_{EE} = –48V, AGND = DGND = 0V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{ILD}	Digital Input Low Voltage	SCL, SDA	●			0.8	V
V_{IHD}	Digital Input High Voltage	SCL, SDA	●	2.4			V
R_{PU}	AD0 to AD4 Pullup Resistors to 5V			30	50	90	kΩ
AC Characteristics							
t_{CL}	Current Limit Filter Time	B5 = 0, B4 = 0, Figure 2	●	4.8	6	7.2	ms
		B5 = 0, B4 = 1	●	9.6	12	14.4	ms
		B5 = 1, B4 = 0	●	19.2	24	28.8	ms
		B5 = 1, B4 = 1	●	76.8	96	115.2	ms
t_{OCD}	Open-Circuit Enable Delay After Power_OK	B7 = 0, B6 = 0	●	50	62	74	ms
		B7 = 0, B6 = 1	●	104	130	156	ms
		B7 = 1, B6 = 0	●	213	267	320	ms
		B7 = 1, B6 = 1	●	433	541	649	ms
t_{OCF}	Open-Circuit Filter Time	Figure 3	●	9.6	18	28.8	ms
t_{OD}	Turn-On Delay Time	Figure 4	●	9.6	18	28.8	ms
DC_R	Retry Duty Cycle	B3 = 0	●	0.78	0.83	0.89	%
		B3 = 1	●	5.5	6	6.7	%
t_{SCLK}	Clock Frequency	(Note 3)	●			400	kHz
t_1	Bus Free Time	Figure 1 (Notes 3, 4)	●	1.3			µs
t_2	Start Hold Time	Figure 1 (Notes 3, 4)	●	600			ns
t_3	SCL Low Time	Figure 1 (Notes 3, 4)	●	1.3			µs
t_4	SCL High Time	Figure 1 (Notes 3, 4)	●	600			ns
t_5	Data Hold Time	Figure 1 (Notes 3, 4)	●	150			ns
t_6	Data Setup Time	Figure 1 (Notes 3, 4)	●	200			ns
t_7	Start Setup Time	Figure 1 (Notes 3, 4)	●	600			ns
t_8	Stop Setup Time	Figure 1 (Notes 3, 4)	●	600			ns
t_9	Stop to Fault Clear	Figure 1 (Notes 3, 4)	●			300	ns
t_r	SCL, SDA Rise Time	Figure 1 (Notes 3, 4)	●	20		300	ns
t_f	SCL, SDA Fall Time	Figure 1 (Notes 3, 4)	●	20		150	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

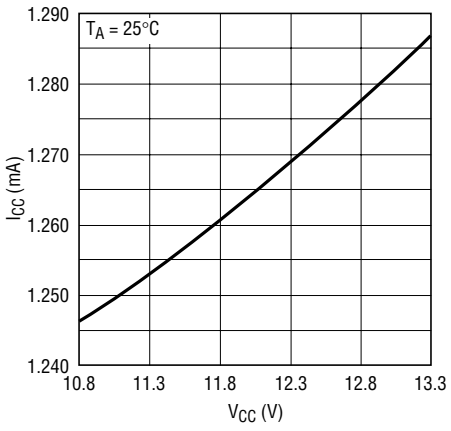
Note 3: Guaranteed by design, not subject to test.

Note 4: Values referred to V_{ILD} and V_{IHD}.

Note 5: A Zener diode clamps the relay drivers at 18V (RELAY 1-4).

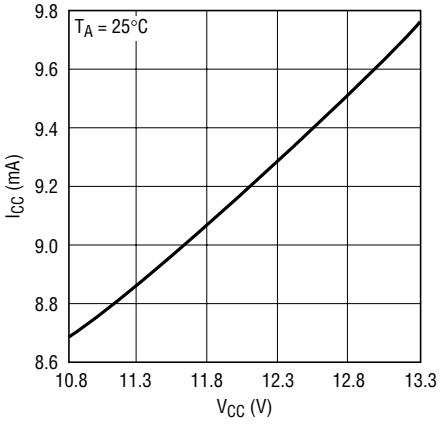
TYPICAL PERFORMANCE CHARACTERISTICS

I_{CC} vs V_{CC} (Relays Off)



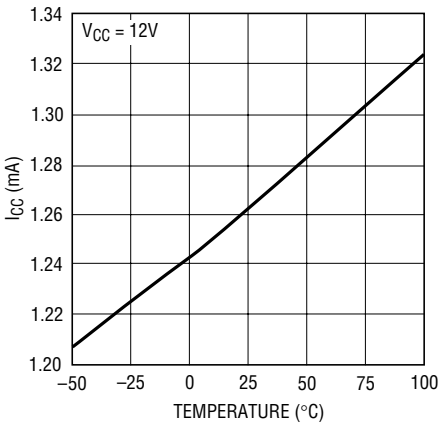
4255 G01

I_{CC} vs V_{CC} (Relays On)



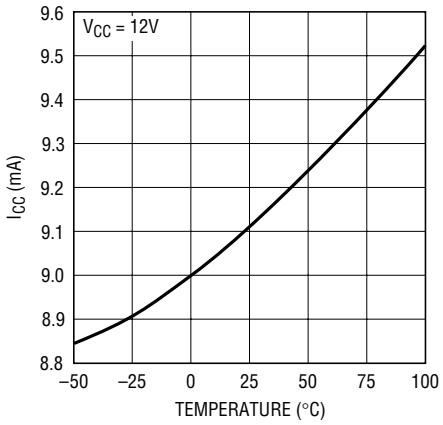
4255 G02

I_{CC} vs Temperature (Relays Off)



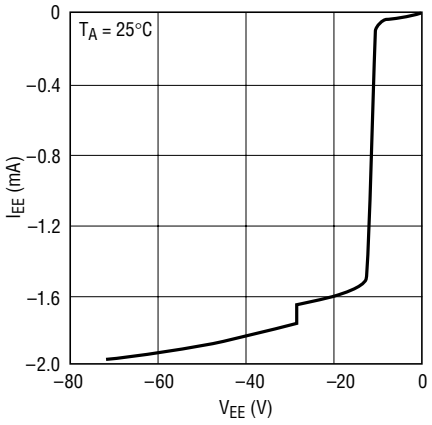
4255 G03

I_{CC} vs Temperature (Relays On)



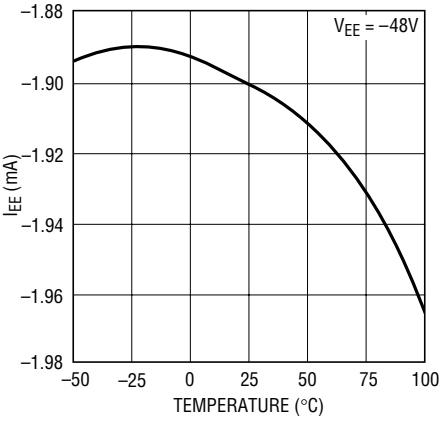
4255 G04

I_{EE} vs V_{EE}



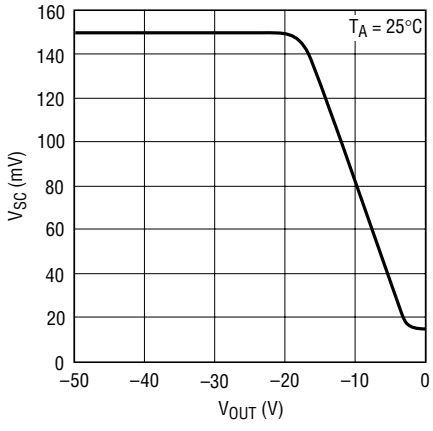
4255 G05

I_{EE} vs Temperature



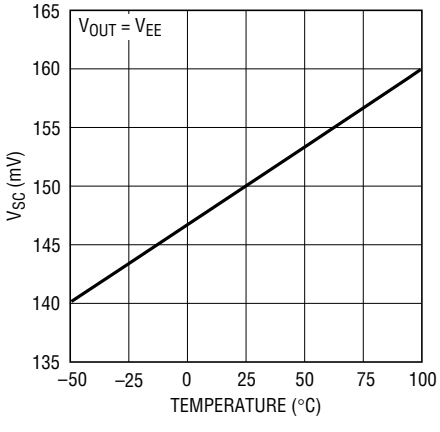
4255 G06

V_{SC} vs V_{OUT}



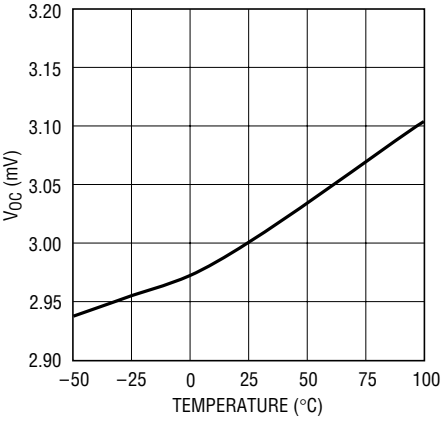
4255 G07

V_{SC} vs Temperature



4255 G08

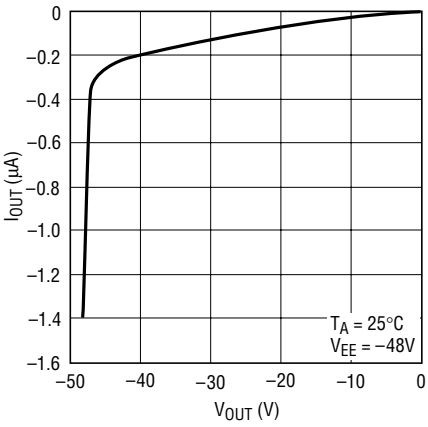
V_{OC} vs Temperature



4255 G09

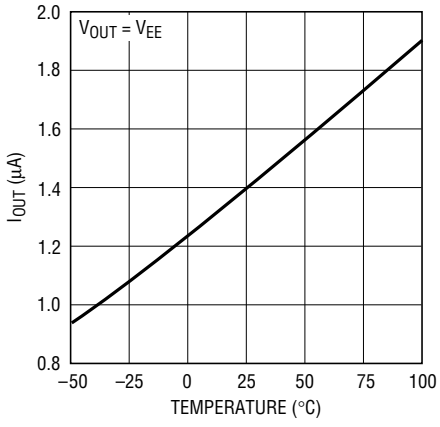
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUT} vs V_{OUT}



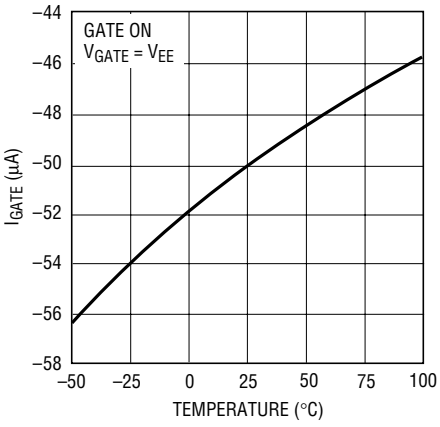
4255 G10

I_{OUT} vs Temperature



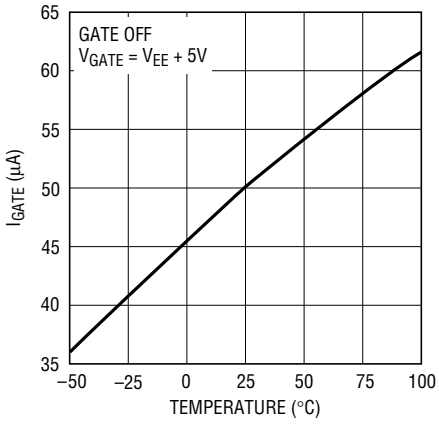
4255 G11

I_{GATE} vs Temperature



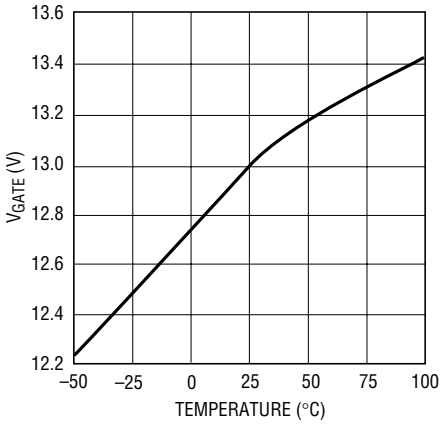
4255 G12

I_{GATE} vs Temperature



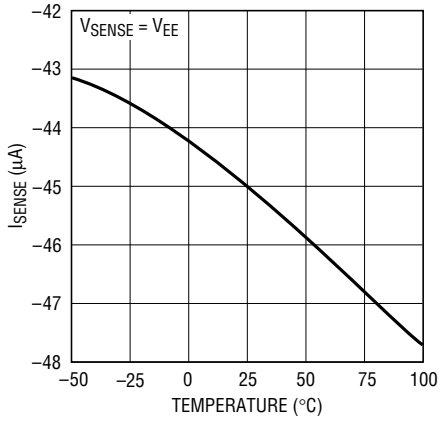
4255 G13

V_{GATE} vs Temperature



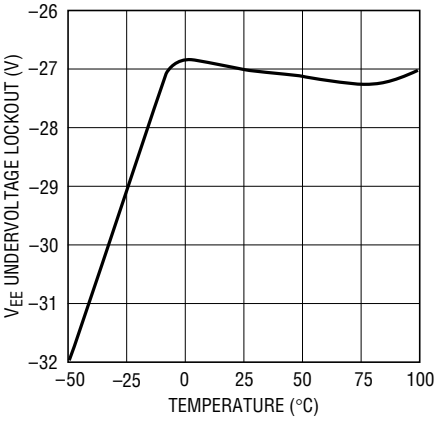
4255 G14

I_{SENSE} vs Temperature



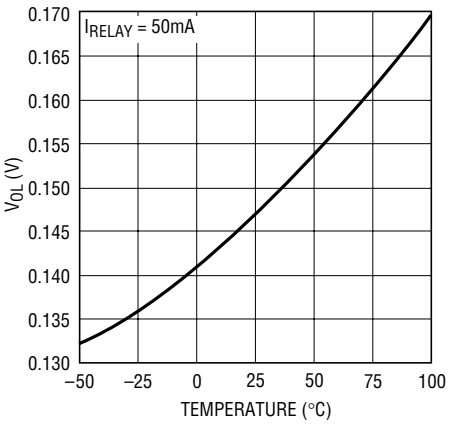
4255 G15

V_{EE} Undervoltage Lockout vs Temperature



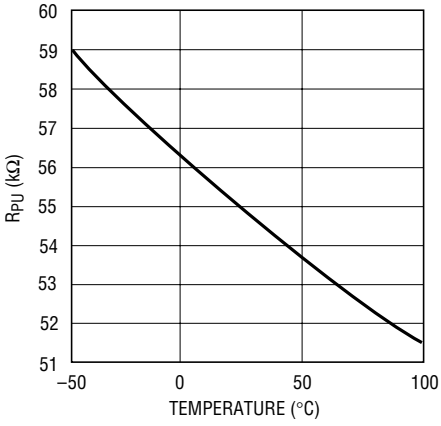
4255 G16

Relay Driver Output Low Voltage (V_{OLR}) vs Temperature



4255 G17

ADO-4 Pullup Resistors to 5V (R_{PU}) vs Temperature



4255 G18

PIN FUNCTIONS

$\overline{\text{FAULT}}$ (Pin 1): Open-Drain $\overline{\text{FAULT}}$ Output. Pulls low when a short-circuit or open circuit fault occurs. The signal can be used to generate a fault condition interrupt to the host controller eliminating the need for continuous software polling.

SCL (Pin 2): Serial Interface Clock Input. It requires a resistor or current source that pulls up to a supply that is less than 6V.

SDA (Pin 3): Serial Interface Data Input and Output. It requires a resistor or current source that pulls up to a supply that is less than 6V.

AD0-4 (Pins 4,5,6,7,8): Serial Interface Address Inputs. Connect to DGND for a low, float or connect to 3.3V or 5V supply for a high.

RELAY1-4 (Pins 9,10,11,12): Relay Driver Outputs. Open collector capable of sinking 50mA to within 0.3V of DGND. An internal 18V clamp to DGND will protect the part when the relay is turned off.

DGND (Pin 13): Digital Ground. Return for digital logic and relay drivers. Must be within ±5V of AGND.

V_{CC} (Pin 14): 12V Supply Input. Powers the digital section and relay drivers. Bypass with a 0.1µF capacitor to DGND.

AGND (Pin 15): Analog Ground.

SENSE1-4 (Pins 16,19,23,26): Current Sense Inputs. Monitors the FET current with a sense resistor placed between SENSE and V_{EE}. When the voltage across the sense resistor reaches the short-circuit sense voltage, the GATE pin voltage will be lowered to maintain a constant current in the FET. At the same time, the current limit timer will be started. If the short-circuit condition persists for the duration of the current limit timer period, the FET will be turned off. The short-circuit sense voltage is lowered to reduce the FET power dissipation when the voltage at the associated OUT pin is within 18V of AGND.

If the open-circuit enable bit is set and the voltage across the sense resister remains below the open-circuit sense voltage for longer than t_{OCF}, the open-circuit filter time, then the FET will be turned off.

GATE1-4 (Pins 17,20,24,27): Gate Drive Outputs. When the FET is turned on, a 50µA pull-up current source is connected to the pin. The gate voltage is clamped to 13V(typ) above V_{EE}. During a short-circuit condition, the GATE pin voltage will be driven to a lower voltage to maintain a constant current in the FET.

OUT1-4 (Pins 18,21,25,28): Output Voltage Monitor Inputs. A current limit foldback feature limits the power dissipation in the FET by reducing the short-circuit current when the voltage at the OUT pin is between AGND and AGND – 18V. The Power_OK bit is set when the voltage from OUT to V_{EE} is less than about 2V.

V_{EE} (Pin 22): –48V Supply Input.

REGISTER DEFINITIONS

Register 1: Control Register (Write Only)

A0: Switch 1 Enable. Logic high turns on Port 1 switch, logic low turns off the Port 1 switch.

A1: Switch 2 Enable. Logic high turns on Port 2 switch, logic low turns off Port 2 switch.

A2: Switch 3 Enable. Logic high turns on Port 3 switch, logic low turns off Port 3 switch.

A3: Switch 4 Enable. Logic high turns on Port 4 switch, logic low turns off Port 4 switch.

A4: Relay 1 Enable. Logic high turns on Port 1 relay, logic low turns off Port 1 relay.

A5: Relay 2 Enable. Logic high turns on Port 2 relay, logic low turns off Port 2 relay.

A6: Relay 3 Enable. Logic high turns on Port 3 relay, logic low turns off Port 3 relay.

A7: Relay 4 Enable. Logic high turns on Port 4 relay, logic low turns off Port 4 relay.

The default setting is all bits set low.

Register 2: Setup Register (Write Only)

B0: Fault Clear Bit. Logic high clears any fault bits that are set.

B1: Autoretry Enable Bit. Logic high enables autoretry following short-circuit faults. Logic low disables autoretry.

B2: Open-Circuit Detect Enable Bit. Logic high enables and logic low disables open-circuit fault detection.

B3: Retry Duty Cycle Select Bit. Logic high sets the autoretry duty cycle to 6%. Logic low sets the autoretry duty cycle to 0.83%. When autoretry is not enabled (B1 = low), the switch turn-on after A0 to A3 are set to high will be delayed to enforce the selected retry duty cycle.

B4: Current Limit Timer Select Bit 0. The current limit timer select bits configure t_{CL}, the time a current limit must be sustained before a short-circuit fault occurs. (See t_{CL} in AC Characteristics.)

B5: Current Limit Timer Select Bit 1. The current limit timer select bits configure t_{CL}, the time a current limit must be sustained before a short-circuit fault occurs. (See t_{CL} in AC Characteristics.)

B6: Open-Circuit Enable Delay Timer Select Bit 0. The open-circuit enable delay timer select bits configure t_{OCD}, the time following a Power_OK condition when no open-circuit faults will be generated. (See t_{OCD}, in AC Characteristics.)

B7: Open-Circuit Enable Delay Timer Select Bit 1. The open-circuit enable delay timer select bits configure t_{OCD}, the time following a Power_OK condition when no open-circuit faults will be generated. (See t_{OCD}, in AC Characteristics.)

The default setting is all bits set low.

Register 3: Status Register 1 (Read Only)

C0: Power_OK for Port 1. Logic high indicates switch 1 is on.

C1: Power_OK for Port 2. Logic high indicates switch 2 is on.

C2: Power_OK for Port 3. Logic high indicates switch 3 is on.

C3: Power_OK for Port 4. Logic high indicates switch 4 is on.

C4: Reserved. Logic high.

C5: Reserved. Logic low.

C6: Reserved. Logic low.

C7: Reserved. Logic low.

REGISTER DEFINITIONS

Register 4: Status Register 2 (Read Only)

D0: Current Limit Fault Status for Port 1. Logic high indicates a short-circuit has been detected on Port 1.

D1: Current Limit Fault Status for Port 2. Logic high indicates a short-circuit has been detected on Port 2.

D2: Current Limit Fault Status for Port 3. Logic high indicates a short-circuit has been detected on Port 3.

D3: Current Limit Fault Status for Port 4. Logic high indicates a short-circuit has been detected on Port 4.

D4: Open-Circuit Fault Status for Port 1. Logic high indicates an open-circuit has been detected on Port 1.

D5: Open-Circuit Fault Status for Port 2. Logic high indicates an open-circuit has been detected on Port 2.

D6: Open-Circuit Fault Status for Port 3. Logic high indicates an open-circuit has been detected on Port 3.

D7: Open-Circuit Fault Status for Port 4. Logic high indicates an open-circuit has been detected on Port 4.

TEST TIMING

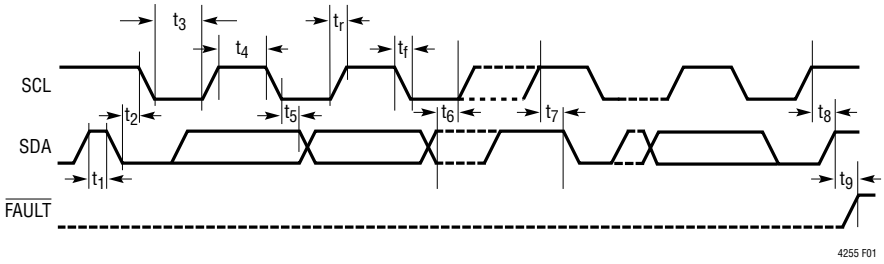


Figure 1. 2-Wire Interface Timing

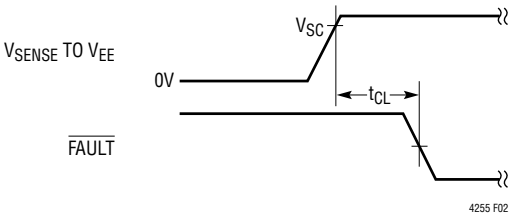


Figure 2. Current Limit Timing

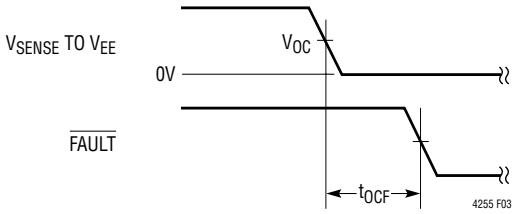


Figure 3. Open-Circuit Filter Timing

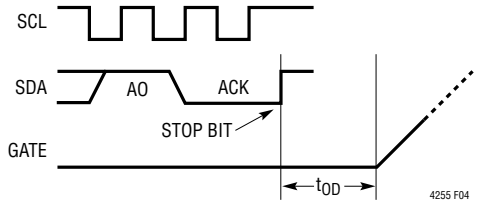


Figure 4. Turn-On Delay

TIMING DIAGRAMS

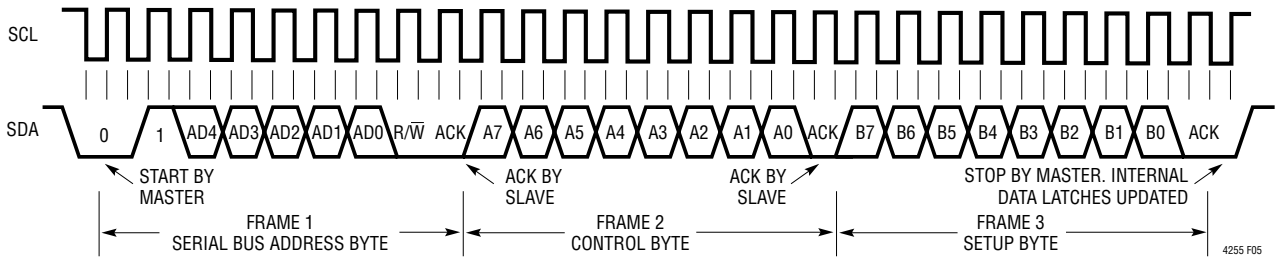


Figure 5. Writing to the Control and Setup Registers

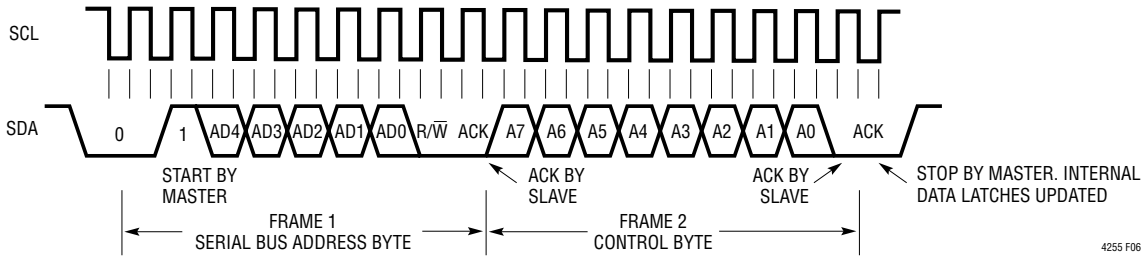


Figure 6. Writing to the Control Register Only

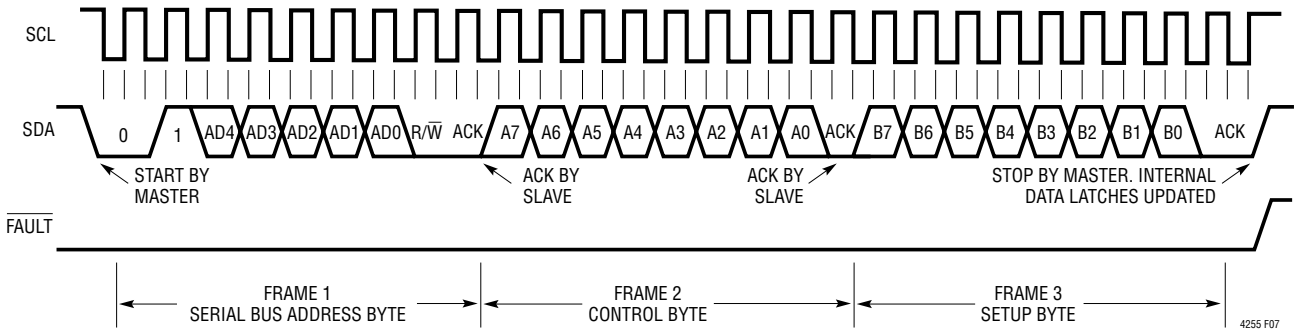


Figure 7. Clearing the $\overline{\text{FAULT}}$ Signal

TIMING DIAGRAMS

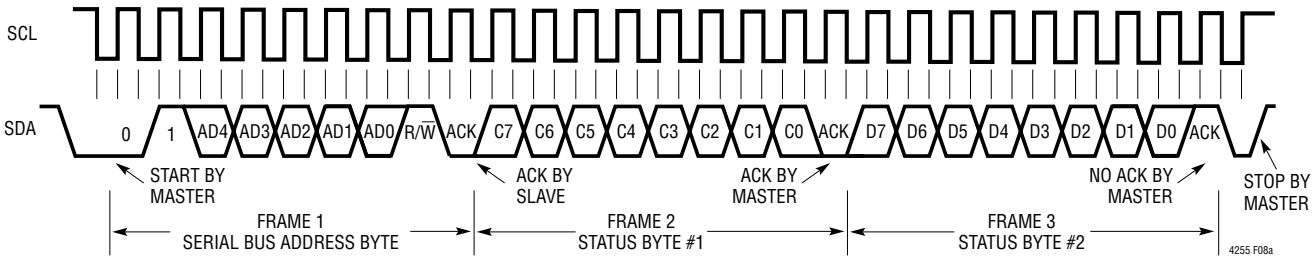


Figure 8a. Reading Both Status Registers

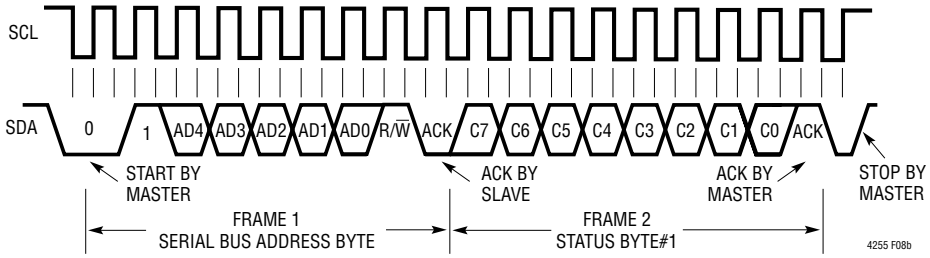


Figure 8b. Reading Status Register #1 Only

APPLICATIONS INFORMATION

Normal Power-Up

Using channel 1 as an example, a normal power-up cycle begins when the switch 1 enable bit (A0) and relay 1 enable bit (A4) are set high and then latched into the chip by a STOP bit on the serial interface (point A, Figure 9).

The RELAY1 output turns on immediately and energizes an optional relay connecting the AGND and OUT1 pins to the cable. After a fixed delay of approximately 18ms (t_{OD}), the GATE1 pin will start to pull high (point B). When the threshold voltage of the FET is reached, current will begin flowing in the external FET (point C). The voltage at the OUT1 pin will then fall at a rate determined by the current limit and the output load capacitance. Because the current limit is lower when the OUT1 pin is near AGND due to the foldback circuit, the voltage will fall slowly at first, then get faster. At the same time, the current limit timer will start. The OUT1 voltage must reach its final value and the analog current limit circuit must turn off before the current limit timer expires, or a current limit fault will be detected and the $\overline{FAULT}$ pin will be pulled low.

When the voltage at OUT1 is within 2V of V_{EE}, the Power_OK (C0) bit will be set (point D) and the open-circuit enable delay timer started. As long as the load current turns on before the open-circuit enable delay timer expires, the $\overline{FAULT}$ pin will remain in a high impedance state and the current limit fault status bit (D0) and open-circuit fault status bit (D4) bits will remain low, thus completing a normal power-up sequence. The Power_OK bit will remain high until the switch is turned off by setting the switch enable bit (A0) low or a short-circuit or open-circuit condition turns off the switch.

A normal power-down sequence begins when the switch enable bit (A0) and relay enable bit (A4) are cleared and then latched into the chip by a STOP bit on the serial interface (point E). The RELAY1 pin will go into a high impedance state and the inductive voltage spike from the primary coil will be clamped at about 18V. The relay will typically disengage several milliseconds later. At the same time, the GATE1 pin will be pulled low by a 50µA current source, the FET will turn off, and the Power_OK bit will be cleared.

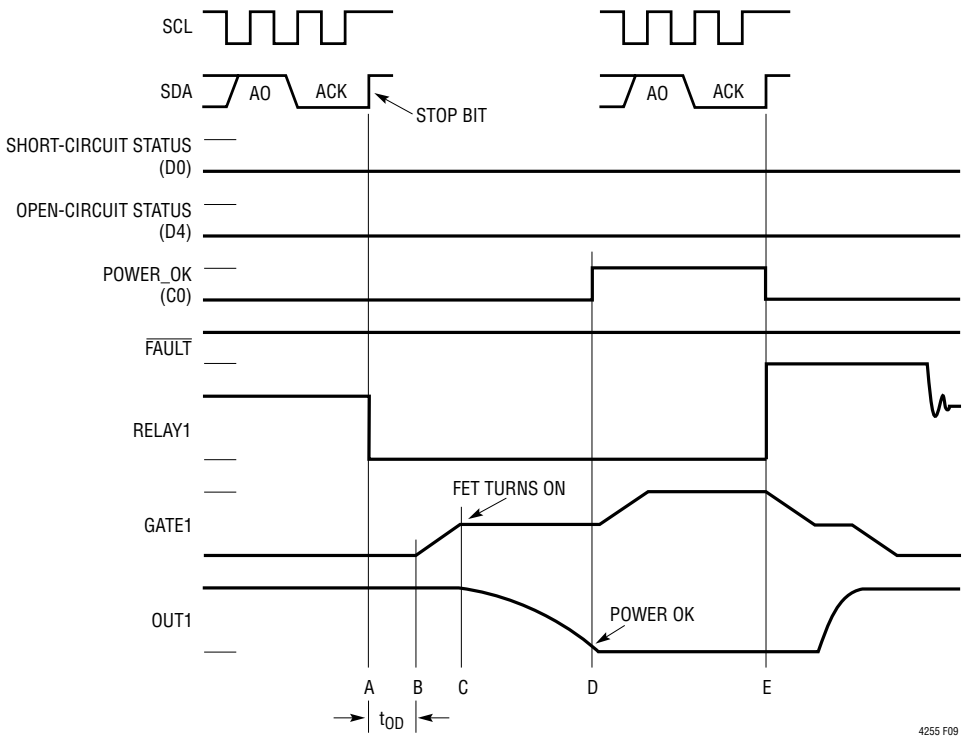


Figure 9. Normal Power-Up and Power-Down Sequence on Channel 1

APPLICATIONS INFORMATION

Power-Up with No Load

When a channel powers-up with no load, the initial sequence is the same as the normal case. When the V_{OUT1} voltage is within the power good threshold, the Power_OK bit is set (point D, Figure 10) and the open-circuit enable delay timer started. The duration of the timer can be programmed via bits B6-B7.

When the open-circuit enable timer expires (t_{OCD}, point E), the open-circuit detector is enabled if the global open-circuit detect enable bit (B2) has been set. When the voltage across the sense resistor is less than 3mV(typ) for at least 18ms (t_{OCF}), the FET will be turned off, and the open-circuit fault status bit (D4) will be set (point E). The $\overline{FAULT}$ pin will pull low to generate an interrupt to the processor which can then read the status register to determine which channel faulted.

When the fault clear bit (B0) is set during a write cycle via the 2-wire interface (point F), the $\overline{FAULT}$ pin goes into a high impendance state, the open-circuit fault status bit (D4) is cleared, and the channel is allowed to turn back on if the relay 1 enable (A4) and switch 1 (AO) enable bits are set (point G.)

The channel is always turned off after an open-circuit fault detection and not allowed to automatically restart.

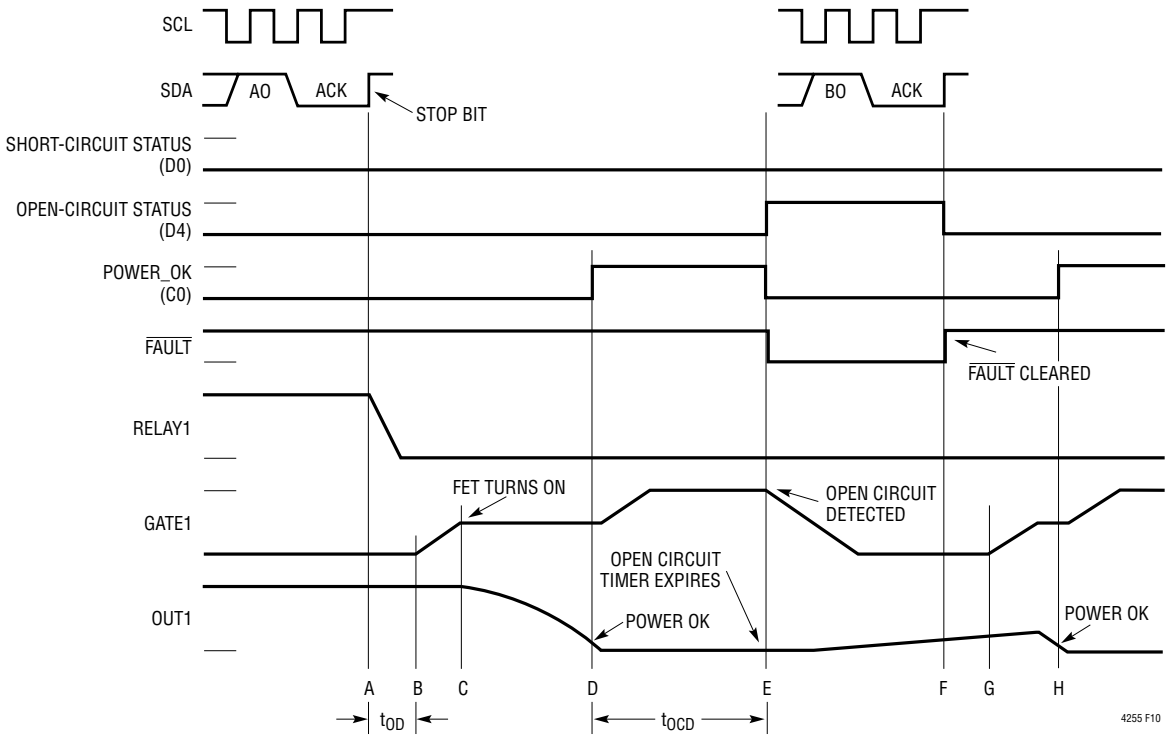


Figure 10. Power-Up Sequence with No Load on Channel 1

APPLICATIONS INFORMATION

Power-Up into a Short-Circuit

When a channel powers-up with a shorted load, the RELAY1 pin will pull low immediately and the GATE1 pin will start to pull high (point B Figure 11) after a turn-on delay (t_{OD}). When the FET turns on at point C, the current will reach a constant value and the programmable current limit timer (t_{CL}) will start. The current limit timer is programmed via bits B4 to B5. When the current limit timer expires, the GATE1 and $\overline{FAULT}$ pins will pull low, the current limit fault status bit (D0) will be set, and the retry timer (t_R) started (point D).

If the autoretry enable bit (B1) is not set, the channel will remain off until the fault is cleared by setting the fault clear bit (B0) and the channel is turned back on by setting the switch enable bit (A0) and the relay enable bit (A4) (point F). If the fault clear bit (B0) is set before the retry timer expires (point E) the channel turn-on will be delayed until the timer expires to enforce the maximum retry duty cycle (DC_R). This duty cycle is programmable via bit B3 and sets the maximum ratio of the FET on-time to off-time under a short-circuit condition.

$$DC_R = \frac{t_{CL}}{t_{CL} + t_R}$$

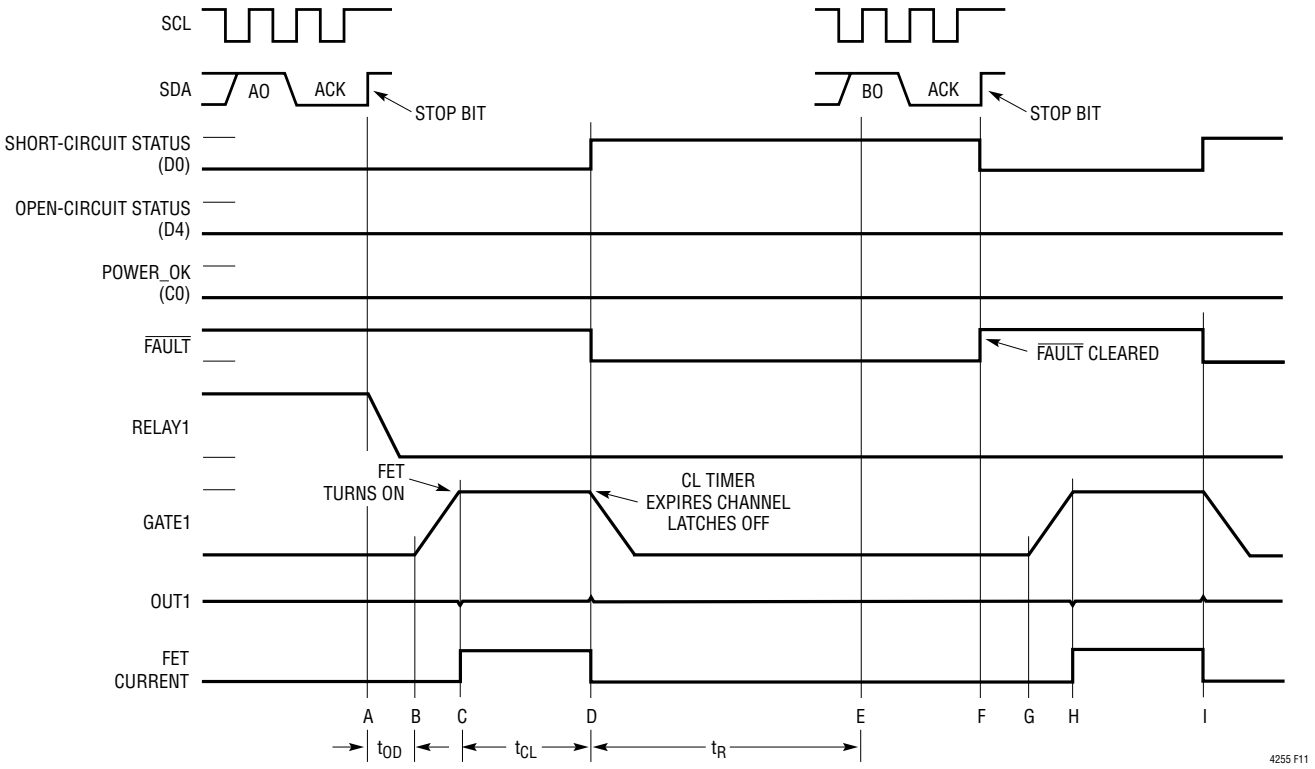


Figure 11. Power-Up Sequence with Shorted Load on Channel 1 with Autoretry Disabled

APPLICATIONS INFORMATION

If the autoretry enable bit (B1) is set, then the channel will automatically restart after the retry delay timer expires (Figure 12, point E). If the channel successfully powers up after an autoretry, the Power_OK bit (CO) will be set. However, $\overline{\text{FAULT}}$ will continue to pull down and the short-circuit bit (DO) will remain high until the fault is cleared by setting the $\overline{\text{FAULT}}$ clear bit (BO).

In the case of a short-circuit occuring after a normal power-up, high rates of change of current (high di/dt) through the inductance of the cable or even the traces on the PCB can cause the voltages at OUT1-4 to overshoot. A 100kΩ resistor should be placed between the drains of the FETs and the OUT1-4 pins to limit the energy absorbed by the LTC4255 if the drains of the FETs exceed OUT1-4's absolute maximum voltage rating. Also, if the FETs are not capable of safely absorbing this energy, high-speed Schottky diodes should be added between the drains of the FETs and AGND using a layout that minimizes the trace lengths between the parts.

Address Selection

The lower 5 bits of the serial interface address can be set by the address selection pins AD0 to AD4 with AD0 being the least significant bit. The upper two bits are preset to AD5 = high and AD6 = low. To force an address bit to low, the address selection pin should be connected to DGND. To force an address bit to high, the address selection pin can be left floating and an internal pull-up resistor will pull the pin up to the internal digital supply voltage (typically 5V). If more noise immunity is needed, the pin can be connected directly to a 5V or 3.3V external supply.

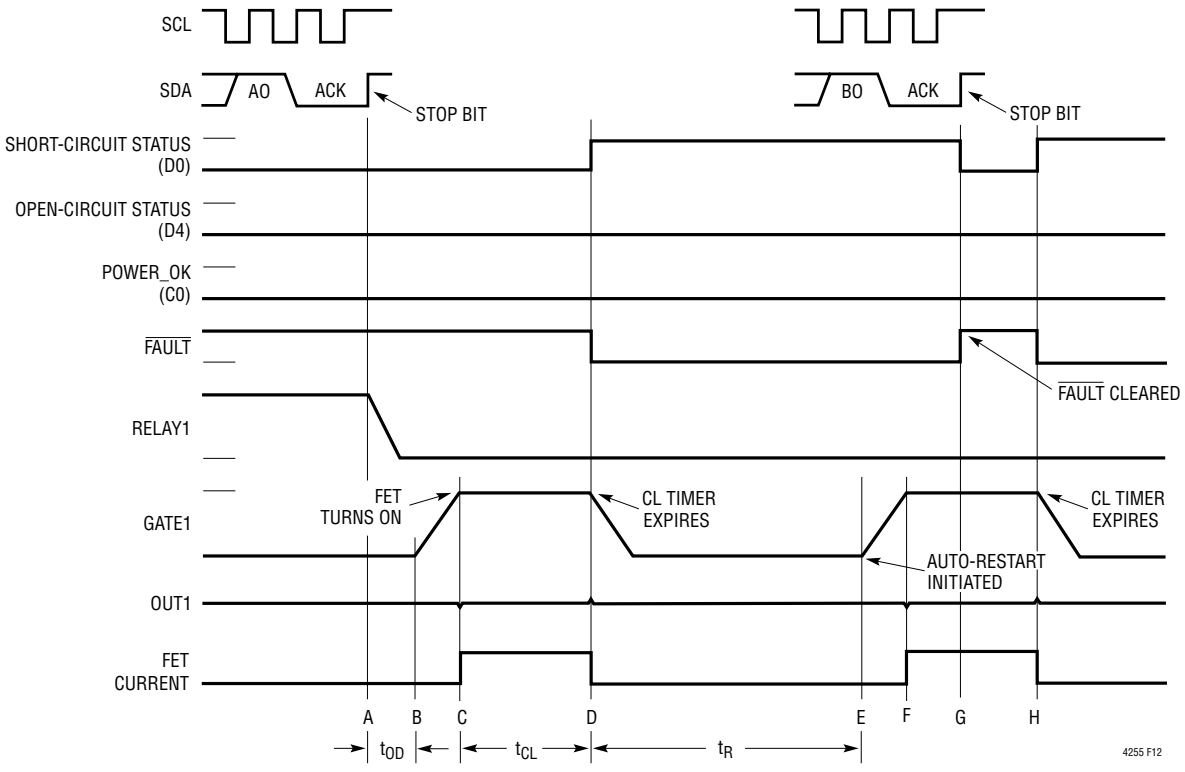


Figure 12. Power-Up Sequence with Shorted Load on Channel 1 with Autoretry Enabled

APPLICATIONS INFORMATION

Relay Drivers

The four relay drivers have an open collector NPN transistor with the ability to sink 50mA to within 0.3V of DGND (Figure 13).

An 18V Zener diode connected to DGND is provided to protect against the inductive kickback of the coil when the NPN transistor is turned off.

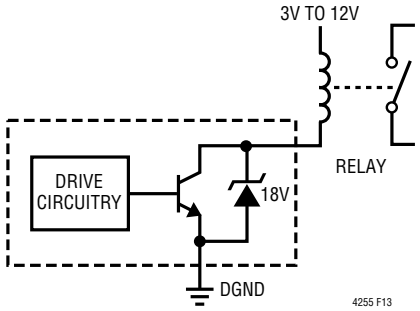
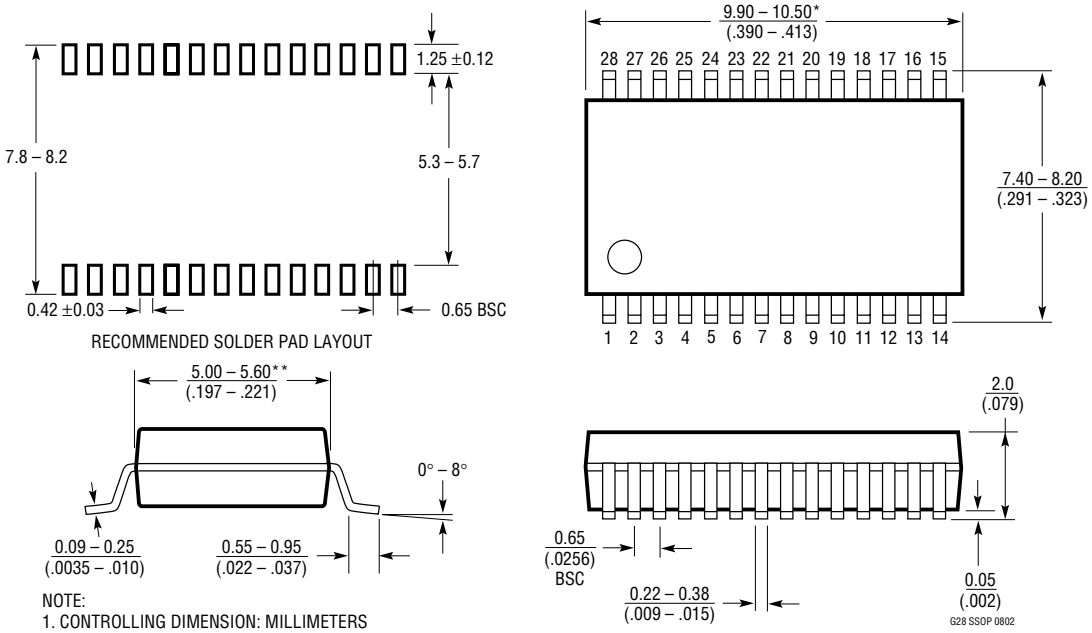


Figure 13. Relay Driver Output

PACKAGE DESCRIPTION

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE