High Power Single PSE Controller with Internal Switch

FEATURES

- **30W PSE Output Power**
- **IEEE 802®.3af Compatible**
- **Operation from a Single 56V Supply**
- **Fully Autonomous Operation Without a Microcontroller**
- **Internal MOSFET with Thermal Protection**
- Precision Inrush Control with Internal Sense Resistor
- Forced Current PD Detection for Noise Immunity
- AC and DC Disconnect Sensing
- Legacy PD Detection
- Robust Short-Circuit Protection
- Pin-Selectable Detection Backoff for Midspan PSEs
- LED Driver Indicates Port On and Blinks Status Codes
- Available in a Miniature14-Pin 4mm × 3mm DFN Package

APPLICATIONS

- High Power Endpoint/Midspan PSEs
- Single-Port or Multi-Port Power Injectors
- Low Port Count PSEs
- Environment B PSEs
- Standalone PSEs

DESCRIPTION

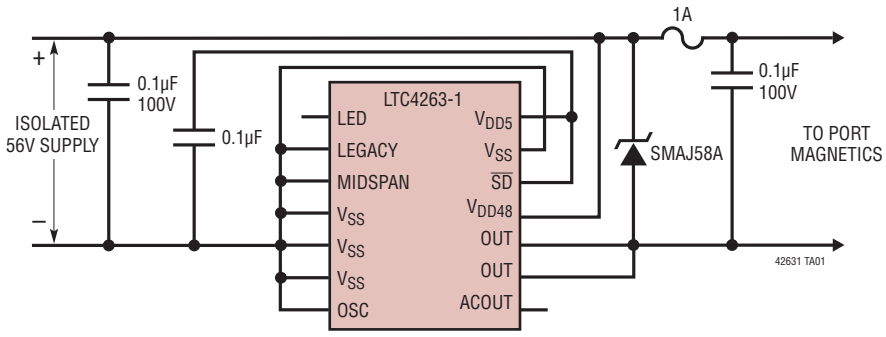
The LTC®4263-1 is a high power, single PSE controller for use in Power over Ethernet systems. The internal current limit and short-circuit protection are designed to provide up to 30W of PSE output power for power hungry PoE applications such as WAPs, security cameras and RFID readers.

The LTC4263-1 includes IEEE 802.3af compliant PD detection circuitry along with selectable AC and DC disconnect sensing, allowing seamless operation in conventional IEEE 802.3af systems as well as propriety, high power applications. The LTC4263-1 simplifies PSE implementation, needing only a single supply and a small number of passive support components. Onboard control algorithms provide complete PSE functionality without the need of a microcontroller and built-in foldback and thermal shutdown provide comprehensive fault protection. An LED pin indicates the state of the port and detection backoff timing is configurable for either endpoint or midspan operation.

The LTC4263-1 is available in a miniature 14-pin 4mm × 3mm DFN package.

TYPICAL APPLICATION

Single-Port Fully Autonomous High Power PSE



ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2)

Supply Voltages

V_{SS} – V_{DD48} ..... 0.3V to –80V

V_{DD5} ..... V_{SS} – 0.3V to V_{SS} + 6V

Pin Voltages and Currents

LEGACY, MIDSPAN, $\overline{SD}$, OSC .. V_{SS} – 0.3V to V_{SS} +6V

LED ..... V_{SS} – 0.3V to V_{SS} + 80V

OUT, ACOUT ..... (See Note 3)

Operating Ambient Temperature Range

LTC4263CDE-1 ..... 0°C to 70°C

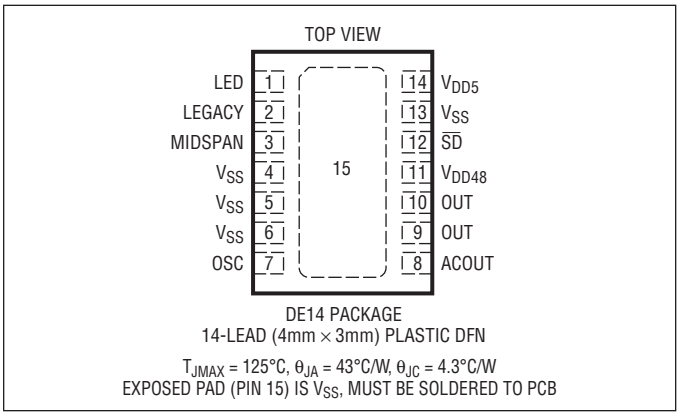
LTC4263IDE-1 ..... –40°C to 85°C

Junction Temperature (Note 4) ..... 125°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



DE14 PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 15) IS V_{SS}, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4263CDE-1#PBF	LTC4263CDE-1#TRPBF	42631	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4263IDE-1#PBF	LTC4263IDE-1#TRPBF	42631	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD48} – V_{SS} = 48V and V_{DD5} not driven externally. All voltages are relative to V_{SS} unless otherwise noted. (Note 2, Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
V_{SUPPLY}	Supply Voltage	V_{DD48} – V_{SS} 30W Output Power	● 	33	48 56	66	V V
V_{UVLO_OFF}	UVLO Turn-Off Voltage	V_{DD48} – V_{SS} Decreasing	●	29	31	33	V
V_{UVLO_HYS}	UVLO Hysteresis		●	0.1		1	V
V_{OVLO_OFF}	OVLO Turn-Off Voltage	V_{DD48} – V_{SS} Increasing	●	66	70	74	V
V_{OVLO_HYS}	OVLO Hysteresis		●	0.2		2	V
V_{DD5}	V_{DD5} Supply Voltage	Driven Externally	●	4.5	5	5.5	V
	V_{DD5} Internal Supply	Driven Internally	●	4.3	4.4	4.5	V
I_{DD48}	V_{DD48} Supply Current	V_{DD5} – V_{SS} = 5V Internal V_{DD5}	● ●		1 2	2 4	mA mA
I_{DD5}	V_{DD5} Supply Current	V_{DD5} – V_{SS} = 5V	●		1	2	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{DD48} – V_{SS}$ = 48V and V_{DD5} not driven externally. All voltages are relative to V_{SS} unless otherwise noted. (Note 2, Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power MOSFET							
R_{ON}	On-Resistance	I = 350mA, Measured From OUT to V_{SS}	 ●		1.5	2.4 3.0	Ω Ω
I_{OUT_LEAK}	OUT Pin Leakage	$V_{OUT} – V_{SS} = V_{DD48} – V_{SS}$ = 57V	●		1	10	µA
R_{PU}	OUT Pin Pull-Up Resistance to V_{DD48}	0V ≤ ($V_{DD48} – V_{OUT}$) ≤ 5V	●	360	500	640	kΩ
Current Control							
I_{CUT}	Overload Current Threshold		●	540	570	600	mA
I_{LIM}	Short-Circuit Current Limit	$V_{OUT} – V_{SS}$ = 5V $V_{DD48} – V_{OUT}$ = 30V	● ●	615 615	645 645	675 675	mA mA
I_{FB}	Foldback Current Limit	$V_{DD48} – V_{OUT}$ = 0V (Note 6) $V_{DD48} – V_{OUT}$ = 10V	● ●	45 165	90 220	180 275	mA mA
I_{MIN}	DC Disconnect Current Threshold		●	5.2	7.5	9.8	mA
I_{FAULT}	High Speed Fault Current Limit	(Note 7)	●	750	1000	1200	mA
Detection							
I_{DET}	Detection Current	First Point, $V_{DD48} – V_{OUT}$ = 10V Second Point, $V_{DD48} – V_{OUT}$ = 3.5V	● ●	235 160	255 180	275 200	µA µA
V_{DET}	Detection Voltage Compliance	$V_{DD48} – V_{OUT}$, Open Port $V_{DD48} – V_{SS}$ = 57V	●			21	V
R_{DETMIN}	Minimum Valid Signature Resistance		●	15.5	17	18.5	kΩ
R_{DETMAX}	Maximum Valid Signature Resistance		●	27.5	29.7	32	kΩ
R_{OPEN}	Open-Circuit Threshold		●	500		2000	kΩ
AC Disconnect							
R_{OSC}	OSC Pin Input Impedance	2V ≤ ($V_{OSC} – V_{SS}$) ≤ 3V	●	175	250	325	kΩ
I_{OSC}	OSC Pin Output Current	$V_{OSC} – V_{SS}$ = 2V	●	–140		140	µA
f_{OSC}	OSC Pin Frequency	$V_{OSC} – V_{SS}$ = 2V	●	103	110	115	Hz
A_{VACD}	Voltage Gain OSC to ACOUT	2V ≤ ($V_{OSC} – V_{SS}$) ≤ 3V	●	0.95	1.0	1.05	V/V
I_{ACDMAX}	AC Disconnect Output Current	$V_{OSC} – V_{SS}$ = 2V, 0V ≤ ($V_{ACOUT} – V_{SS}$) ≤ 4V	●	–1		1	mA
I_{ACDMIN}	Remain Connected AC Pin Current	$V_{OSC} – V_{SS}$ = 2V	●	130	160	190	µA
V_{ACDEN}	AC Disconnect Enable Signal	$V_{OSC} – V_{SS}$, Port On	●	1.5			V
Digital Interface (Note 8)							
V_{OLED}	LED Output Low Voltage	I_{LED} = 10mA	●		1.1	2.2	V
V_{ILD}	Digital Input Low Voltage	MIDSPAN, $\overline{SD}$ LEGACY	● ●			0.8 0.4	V V
V_{IHD}	Digital Input High Voltage	MIDSPAN, $\overline{SD}$ LEGACY	● ●	2.2 2.2			V V
V_{OZ}	Voltage of Legacy Pin if Left Floating		●	1.1	1.25	1.4	V
I_{OLEG}	Current In/Out of Legacy Pin	0V ≤ ($V_{LEGACY} – V_{SS}$) ≤ 5V	●	–60		60	µA
I_{FLT}	Maximum Allowed Leakage at Legacy Pin When Floating		●	–10		10	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{DD48} – V_{SS}$ = 48V and V_{DD5} not driven externally. All voltages are relative to V_{SS} unless otherwise noted. (Note 2, Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing Characteristics							
t_{DET}	Detection Time	Beginning to End of Detection	●	270	290	310	ms
t_{DETDLY}	Detection Delay	PD Insertion to Detection Complete	●	300		620	ms
t_{PON}	Power Turn-On Delay	End of Valid Detect to Application of Power	●	135	145	155	ms
t_{RISE}	Turn-On Rise Time	$V_{DD48} – V_{OUT}$: 10% to 90% C_{PSE} = 0.1µF	●	40	170		µs
t_{OVLD}	Overload/Short-Circuit Time Limit		●	52	62	72	ms
t_{ED}	Error Delay	I_{CUT} Fault to Next Detect	●	3.8	4.0	4.2	s
t_{MPDO}	Maintain Power Signature (MPS) Disconnect Delay	PD Removal to Power Removal	●	320	350	380	ms
t_{MPS}	MPS Minimum Pulse Width	PD Minimum Current Pulse Width Required to Stay Connected (Note 9)	●			20	ms
t_{DBO}	Midspan Mode Detection Backoff	R_{PORT} = 15.5kΩ	●	3.0	3.2	3.4	s
t_{DISDLY}	Power Removal Detection Delay		●	0.8	0.95	1.1	s

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{SS} unless otherwise specified.

Note 3: 80mA of current may be pulled from the OUT or ACOUT pin without damage whether the LTC4263-1 is powered or not. These pins will also withstand a positive voltage of V_{SS} + 80V.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: The LTC4263-1 operates with a negative supply voltage. To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 6: In order to reduce power dissipated in the switch while charging the PD, the LTC4263-1 reduces the current limit when $V_{OUT} – V_{SS}$ is large. Refer to the Typical Performance Characteristics for more information.

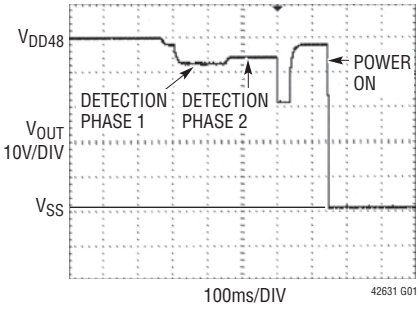
Note 7: The LTC4263-1 includes a high-speed current limit circuit intended to protect against faults. The fault protection is activated for port current in excess of I_{FAULT}. After the high-speed current limit activates, the short-circuit current limit (I_{LIM}) engages and restricts current to IEEE 802.3af levels.

Note 8: The LTC4263-1 digital interface operates with respect to V_{SS}. All logic levels are measured with respect to V_{SS}.

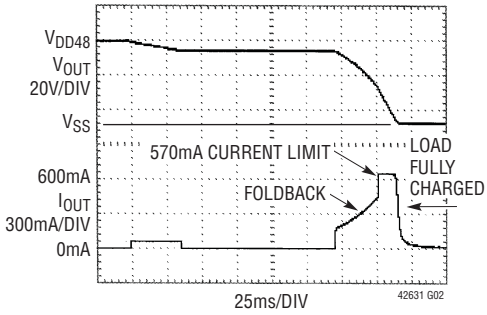
Note 9: The IEEE 802.3af specification allows a PD to present its Maintain Power Signature (MPS) on an intermittent basis without being disconnected. In order to stay powered, the PD must present the MPS for t_{MPS} within any t_{MPDO} time window.

TYPICAL PERFORMANCE CHARACTERISTICS

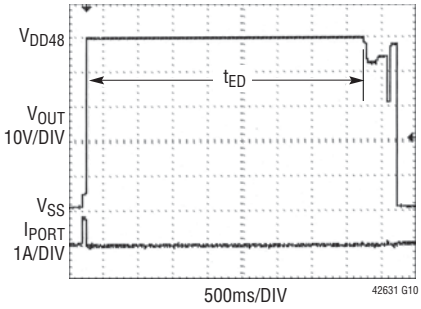
Powering an IEEE 802.3af PD



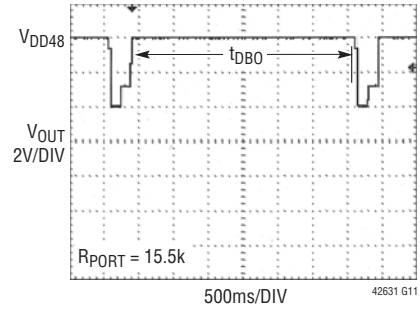
Powering a Legacy PD with 470µF Bypass Capacitor



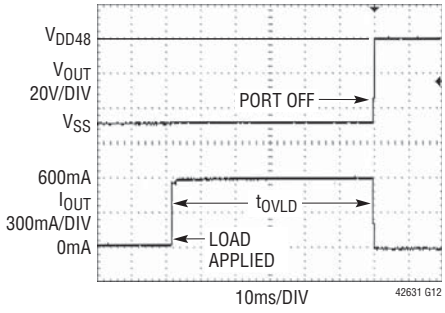
Overload Restart Delay



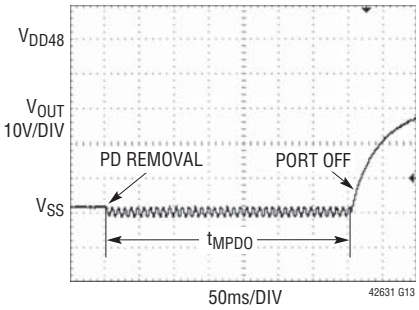
Midspan Backoff with Invalid PD



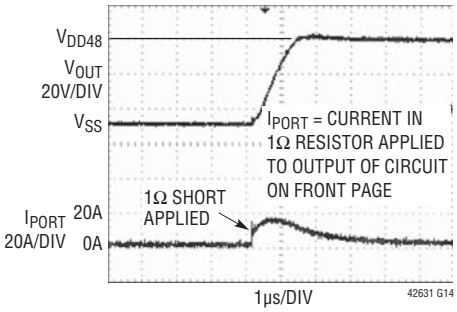
Overcurrent Response Time



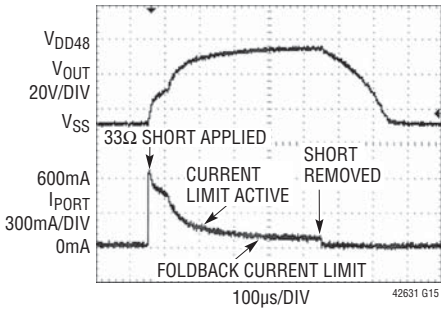
Response to PD Removal with AC Disconnect Enabled



Rapid Response to 1Ω Short



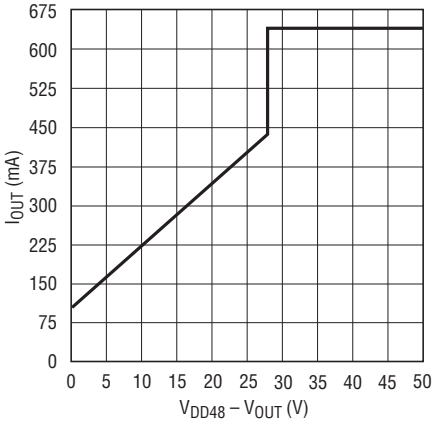
Rapid Response to Momentary 33Ω Short



IPORT = CURRENT IN 33Ω RESISTOR APPLIED TO OUTPUT OF CIRCUIT ON FRONT PAGE

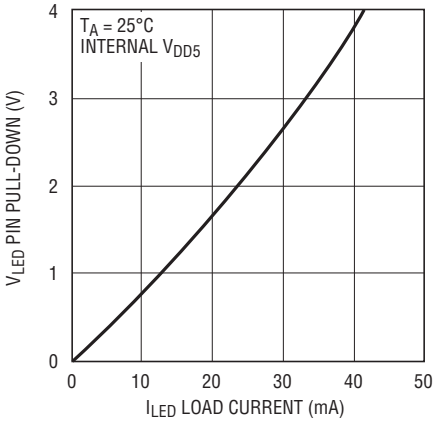
TYPICAL PERFORMANCE CHARACTERISTICS

Current Limit and Foldback



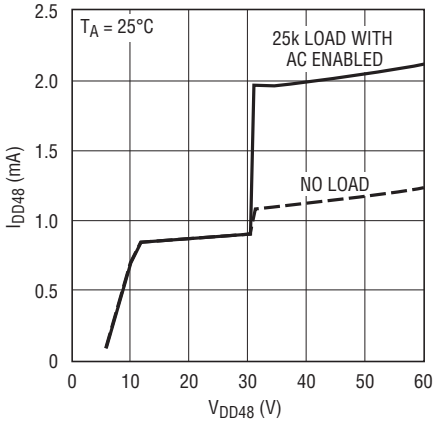
42631 G03

LED Pin Pull-Down vs Load Current



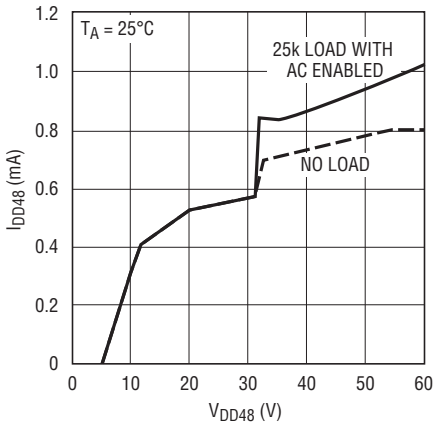
42631 G04

I_{DD48} DC Supply Current vs Supply Voltage with Internal V_{DD5}



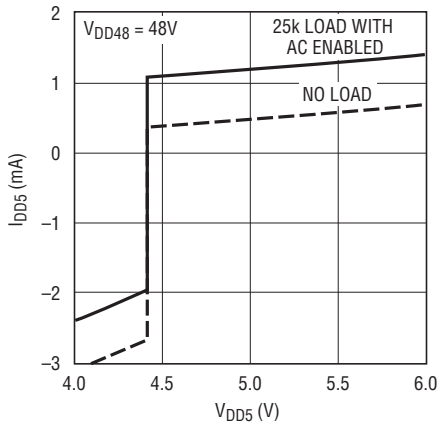
42631 G07

I_{DD48} DC Supply Current vs Supply Voltage with V_{DD5} = 5V



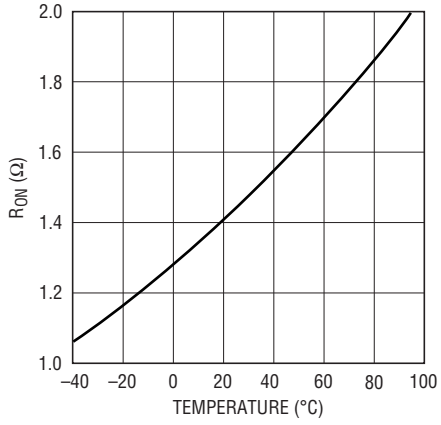
42631 G08

I_{DD5} DC Supply Current vs Supply Voltage



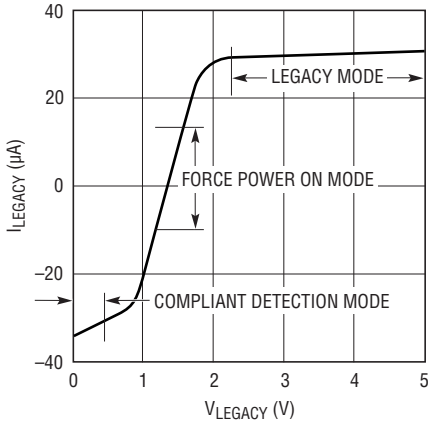
42631 G09

R_{ON} vs Temperature



42631 G16

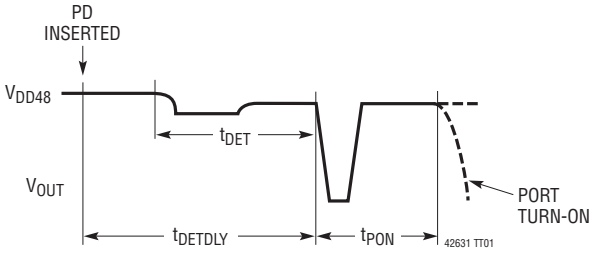
Legacy Pin Current vs Voltage



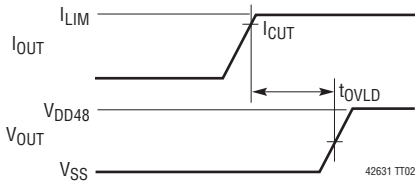
42631 G17

TEST TIMING

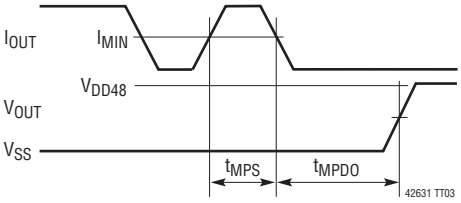
Detect and Turn-On Timing



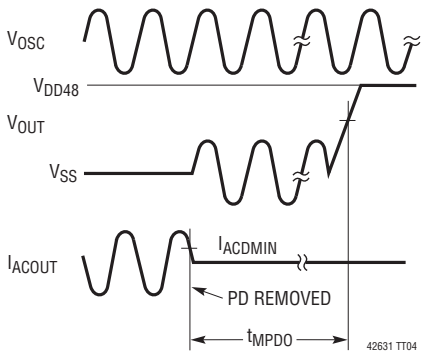
Current Limit Timing



DC Disconnect Timing



AC Disconnect Timing



PIN FUNCTIONS

LED (Pin 1): Port State LED Drive. This pin is an open-drain output that pulls down when the port is powered. Under port fault conditions, the LED will flash in patterns to indicate the nature of the port fault. See the Applications Information section for a description of these patterns. When the LTC4263-1 is operated from a single 48V supply, this pin is pulsed low with a 6% duty cycle during the periods when the LED should be on. This allows use of a simple inductor, diode, and resistor circuit to avoid excess heating due to the large voltage drop from V_{DD48}. See the Applications Information section for details on this circuit.

LEGACY (Pin 2): Legacy Detect. This pin controls whether legacy detect is enabled. If held at V_{DD5}, legacy detect is enabled and testing for a large capacitor is performed to detect the presence of a legacy PD on the port. See the Applications Information section for descriptions of legacy PDs that can be detected. If held at V_{SS}, only IEEE 802.3af compliant PDs are detected. If left floating, the LTC4263-1 enters force-power-on mode and any PD that generates between 1V and 10V when biased with 270µA of detection current will be powered as a legacy device. This mode is useful if the system uses a differential detection scheme to detect legacy devices.

MIDSPAN (Pin 3): Midspan Enable. If this pin is connected to V_{DD5}, Midspan backoff is enabled and a 3.2 second delay occurs after every failed detect cycle unless the result is open circuit. If held at V_{SS}, no delay occurs after failed detect cycles.

V_{SS} (Pins 4, 5, 6, 13): Negative Power Supply. Pins 4, 5, 6 and 13 should be tied together on the PCB. For optimum power delivery, supply voltage should be maximized. See Applications Information section for more information.

OSC (Pin 7) Oscillator for AC Disconnect. If AC disconnect is used, connect a 0.1µF X7R capacitor from OSC to V_{SS}. Tie OSC to V_{SS} to disable AC disconnect and enable DC disconnect.

ACOUT (Pin 8): AC Disconnect Sense. Senses the port to determine whether a PD is still connected when in AC disconnect mode. If port capacitance drops below about 0.15µF for longer than T_{MPDO} the port is turned off. If AC disconnect is used, connect this pin to the port with a series combination of a 1k resistor and a 0.47µF 100V X7R capacitor. See the Applications Information section for more information.

OUT (Pins 9, 10): Port Output. If DC disconnect is used, these pins are connected to the port. If AC disconnect is used, these pins are connected to the port through a parallel combination of a 1A diode and a 500k resistor. Pins 9 and 10 should be tied together on the PCB. See the Applications Information section for more information.

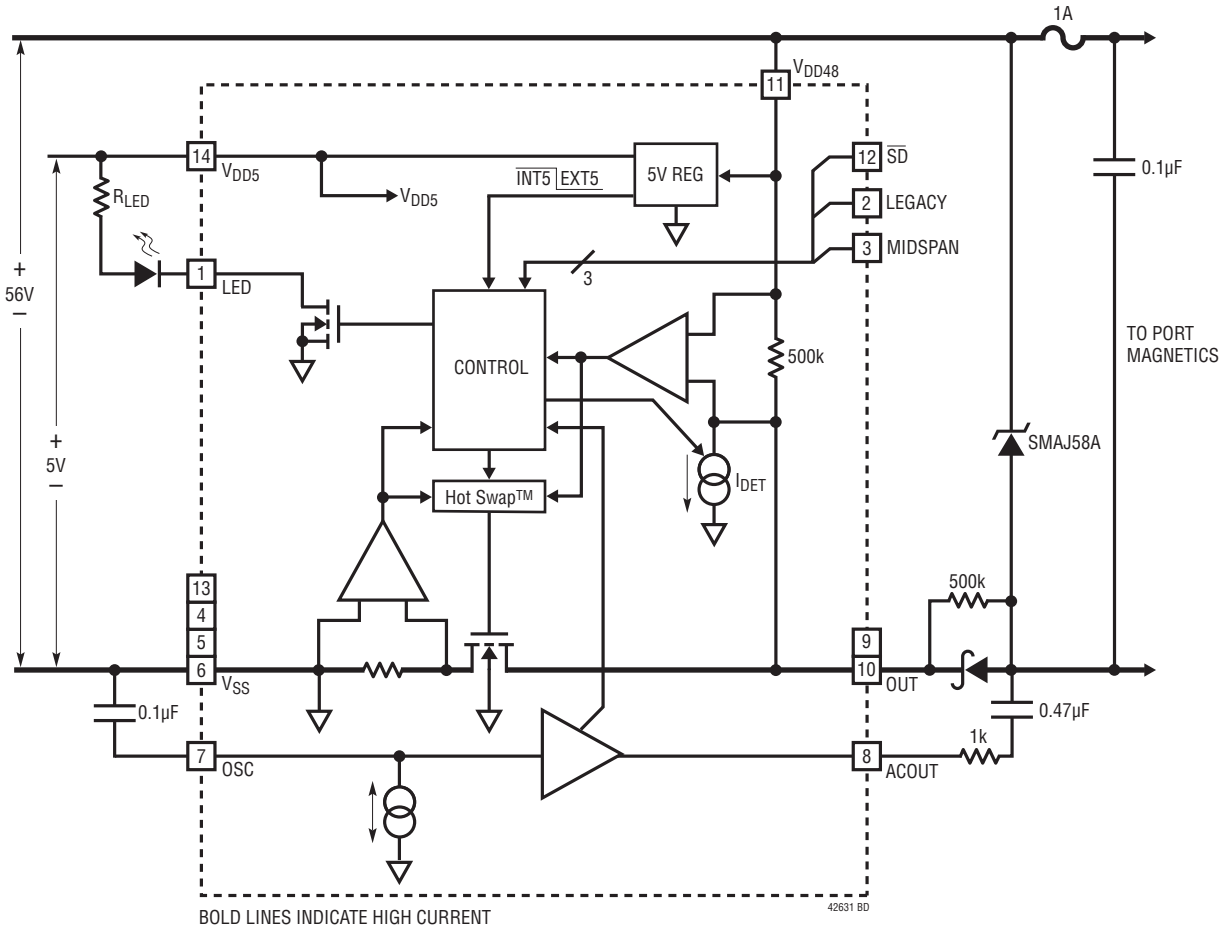
V_{DD48} (Pin 11): Power Return for V_{SS}. Must be bypassed with a 0.1µF capacitor to V_{SS}. For optimum power delivery, supply voltage should be maximized. See Applications Information section for more information.

$\overline{SD}$ (Pin 12): Shutdown. If held low, the LTC4263-1 is prevented from performing detection or powering the port. Pulling $\overline{SD}$ low will turn off the port if it is powered. When released, a 4-second delay will occur before detection is attempted. If not used, tie to V_{DD5}.

V_{DD5} (Pin 14): Logic Power Supply. Apply 5V referenced to V_{SS}, if such a supply is available, or place a 0.1µF bypass capacitor to V_{SS} to enable the internal regulator. When the internal regulator is used, this pin should only be connected to the bypass capacitor and to any logic pins of the LTC4263-1 that are being held at V_{DD5}.

Exposed Pad (Pin 15): V_{SS}. Must be connected to V_{SS} on the PCB. The Exposed Pad acts as a heat sink for the internal MOSFET.

BLOCK DIAGRAM



BOLD LINES INDICATE HIGH CURRENT
Hot Swap IS A TRADEMARK OF LINEAR TECHNOLOGY CORPORATION

APPLICATIONS INFORMATION

POE OVERVIEW

Over the years, twisted-pair Ethernet has become the most commonly used method for local area networking. The IEEE 802.3 group, the originator of the Ethernet standard, has defined an extension to the standard, IEEE 802.3af, which allows DC power to be delivered simultaneously over the same cable used for data communication. This has enabled a whole new class of Ethernet devices, including IP telephones, wireless access points, and PDA charging stations which do not require additional AC wiring or external power transformers, a.k.a. "wall warts." These small data devices can now be powered directly from their Ethernet connection. Sophisticated detection and power monitoring techniques prevent damage to legacy data-only devices while still supplying power to newer, Ethernet-powered devices over the twisted-pair cable.

The device that supplies power is called the Power Sourcing Equipment (PSE). A device that draws power from the wire is called a Powered Device (PD). A PSE is typically an Ethernet switch, router, hub, or other network switching equipment that is commonly found in the wiring closets where cables converge. PDs can take many forms. Digital IP telephones, wireless network access points, PDA or notebook computer docking stations, cell phone chargers, and HVAC thermostats are examples of devices that can draw power from the network.

A PSE is required to provide 44V to 57V DC between either the signal pairs or the spare pairs as shown in Figure 1. The power is applied as a voltage between two of the pairs, typically by powering the center taps of the isolation transformers used to couple the differential data signals to the wire. Since Ethernet data is transformer coupled at both ends and is sent differentially, a voltage difference between the transmit pairs and the receive pairs does not affect the data. A 10Base-T/100Base-TX Ethernet connection only uses two of the four pairs in the cable. The unused or spare pairs can optionally be powered directly, as shown in Figure 1, without affecting the data. 1000Base-T uses all four pairs and power must be connected to the transformer center taps if compatibility with 1000Base-T is required.

The LTC4263-1 provides a complete high power PSE solution for powering newer power hungry PDs such as dual-radio wireless access points, security cameras and RFID readers. With proper system design, proprietary high power PoE solutions using the LTC4263-1 can deliver 25W (min) to a high power 2-pair PD at the end of a 100 meter CAT5 cable and 50W (min) using a 4-pair solution.

The LTC4263-1 provides a high power PSE solution while simultaneously being compatible with existing IEEE 802.3af systems. By maintaining a compliant detection protocol, the LTC4263-1 insures legacy data-only devices are not

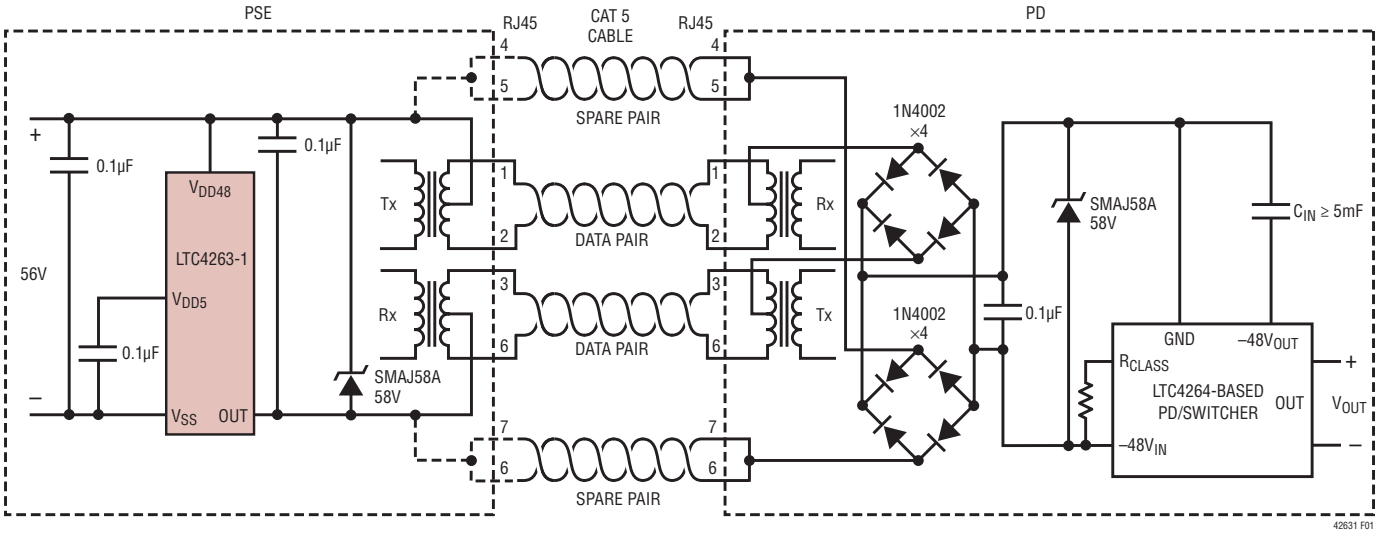


Figure 1. 2-Pair High Power PoE System Diagram

APPLICATIONS INFORMATION

accidentally powered. Disconnect with either AC or DC methods using the LTC4263-1 is fully compliant and insures safe power removal after PD disconnect. Command and control for the LTC4263-1 is handled internally without the need of a microcontroller, thereby simplifying system design.

LTC4263-1 OPERATION

Signature Detection

The IEEE 802.3af specification defines a specific pair-to-pair signature resistance used to identify a device that can accept power via its Ethernet connection. When the port voltage is below 10V, an IEEE 802.3af compliant PD will have an input resistance of approximately 25kΩ. Figure 2 illustrates the relationship between the PD signature resistance and the required resistance ranges the PSE must accept and reject. According to the IEEE 802.3af specification, the PSE must accept PDs with signatures between 19kΩ and 26.5kΩ and may or may not accept resistances in the two ranges of 15kΩ to 19kΩ and 26.5kΩ to 33kΩ. The black box in Figure 2 represents the typical 150Ω pair-to-pair termination used in Ethernet devices like a computer's network interface card (NIC) that cannot accept power.

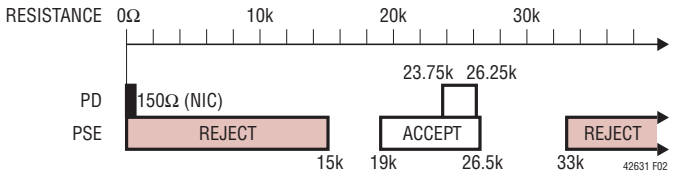


Figure 2. IEEE 802.3af Signature Resistance Ranges

The LTC4263-1 checks for the signature resistance by forcing two test currents on the port in sequence and measuring the resulting voltages. It then subtracts the two V-I points to determine the resistive slope while removing voltage offset caused by any series diodes or current offset caused by leakage at the port (see Figure 3). The LTC4263-1 will typically accept any PD resistance between 17kΩ and 29.7kΩ as a valid PD. Values outside this range (excluding open and short-circuits) are reported to the user by a code flashed via the LED pin.

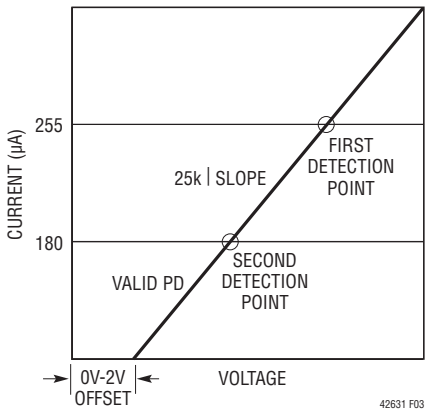


Figure 3. PD 2-Point Detection

The LTC4263-1 uses a force-current detection method in order to reduce noise sensitivity and provide a more robust detection algorithm. The first test point is taken by forcing a test current into the port, waiting a short time to allow the line to settle and measuring the resulting voltage. This result is stored and the second current is applied to the port, allowed to settle and the voltage measured.

The LTC4263-1 will not power the port if the PD has more than 5μF in parallel with its signature resistor unless legacy mode is enabled.

The LTC4263-1 autonomously tests for a valid PD connected to the port. It repeatedly queries the port every 580ms, or every 3.2s if midspan backoff mode is active (see below). If detection is successful, it then powers up the port.

Midspan Backoff

IEEE 802.3af requires the midspan PSE to wait two seconds after a failed detection before attempting to detect again unless the port resistance is greater than 500kΩ. This requirement is to prevent the condition of an endpoint PSE and a midspan PSE, connected to the same PD at the same time, from each corrupting the PD signature and preventing power-on. After the first corrupted detection cycle, the midspan PSE waits while the endpoint PSE completes detection and turns the port on. If the midspan mode of the LTC4263-1 is enabled by connecting the MIDSPAN pin to V_{DD5}, a 3.2 second delay occurs after every failed detect cycle unless the result is an open circuit.

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Power Control

The primary function of the LTC4263-1 is to control the delivery of power to the PSE port. In order to provide a robust solution, a variety of current limit and current monitoring functions are needed, as shown in Figure 4. All control circuitry is integrated and the LTC4263-1 requires no external MOSFET, sense resistor, or microcontroller.

The LTC4263-1 includes an internal MOSFET for driving the PSE port. The LTC4263-1 drives the gate of the internal MOSFET while monitoring the current and the output voltage at the OUT pin. This circuitry couples the 56V input supply to the port in a controlled manner that satisfies the PD's power needs while minimizing disturbances on the 56V backplane.

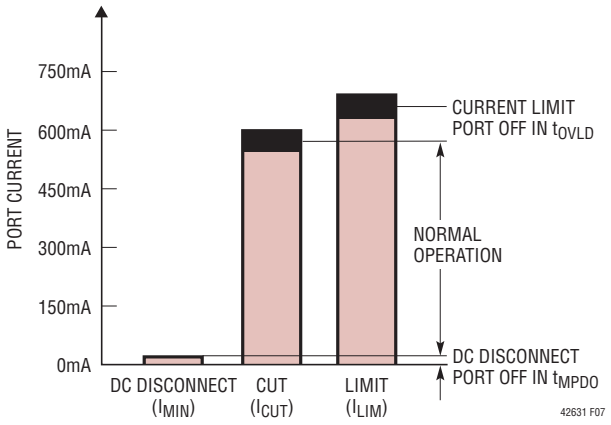

Figure 4. Current Thresholds and Current Limits

Port Overload

Based on the IEEE 802.3af standard, the LTC4263-1 detects port overload conditions by monitoring port current. This ensures the port stays within the designed continuous power budget while allowing for brief power surges. If the port current exceeds 570mA (typ) for greater than 62ms (typ), power is removed and the LTC4263-1 waits 4 seconds (typ) before returning to detection mode.

Port Inrush and Short-Circuit

When 56V power is applied to the port, the LTC4263-1 is designed to power-up the PD in a controlled manner without causing transients on the input supply. To accomplish this, the LTC4263-1 implements inrush current limit. At turn-on, current limit will allow the port voltage to quickly rise until the PD reaches its input turn-on threshold. At this point, the PD begins to draw current to charge its bypass capacitance, slowing the rate of port voltage increase.

If at any time the port is shorted or an excessive load is applied, the LTC4263-1 limits port current to avoid a hazardous condition. The current is limited to I_{LIM} for port voltages above 30V and is reduced for lower port voltages (see the Foldback section). Inrush and short-circuit current limit are allowed to be active for 62ms (typ) before the port is shut off.

Port Fault

If the port is suddenly shorted, the internal MOSFET power dissipation can rise to very high levels until the short-circuit current limit circuit can respond. A separate high-speed current limit circuit detects severe fault conditions (I_{OUT} > 1000mA (typ)) and quickly turns off the internal MOSFET if such an event occurs. The circuit then limits current to I_{LIM} while the t_{OVLD} timer increments. During a short-circuit, I_{LIM} will be reduced by the foldback circuitry.

t_{OVLD} Timing

For overload, inrush, and short-circuit conditions, the LTC4263-1 includes a 62ms (typ) t_{OVLD} timer to limit the duration of these events. The timer is incremented whenever current greater than I_{CUT} flows through the port. If the current is still above I_{CUT} when the t_{OVLD} timer expires, the LTC4263-1 will turn off power to the port and flash the LED. In this situation, the LTC4263-1 waits four seconds and then restarts detection. If the overload condition is removed before the t_{OVLD} timer expires, the port stays powered and the timer is reset.

Foldback

Foldback is designed to limit power dissipation in the LTC4263-1 during power-up and momentary short-circuit conditions. At low port output voltages, the voltage across the internal MOSFET is high, and power dissipation will be large if significant current is flowing. Foldback monitors the port output voltage and reduces the I_{LIM} current limit level for port voltages of less than 28V, as shown in Figure 5.

APPLICATIONS INFORMATION

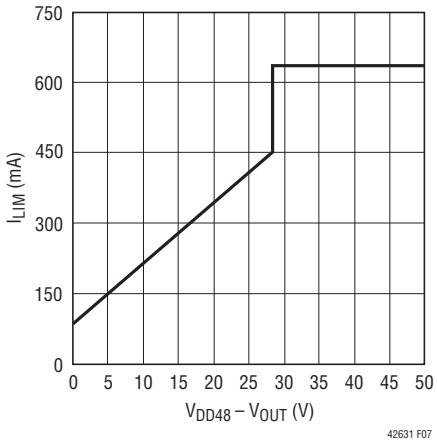

Figure 5. Current Limit Foldback

Thermal Protection

The LTC4263-1 includes thermal overload protection in order to provide full device functionality in a miniature package while maintaining safe operating temperatures. Several factors create the possibility for very large power dissipation within the LTC4263-1. At port turn-on, while I_{LIM} is active, the instantaneous power dissipated by the LTC4263-1 can be as high as 18W. This can cause 40°C or more of die heating in a single turn-on sequence. Similarly, excessive heating can occur if an attached PD repeatedly pushes the LTC4263-1 into I_{LIM} by drawing too much current. Excessive heating can also occur if the V_{DD5} pin is shorted or overloaded.

The LTC4263-1 protects itself from thermal damage by monitoring die temperature. If the die temperature exceeds the overtemperature trip point, the LTC4263-1 removes port power and shuts down all functions including the internal 5V regulator. Once the die cools, the LTC4263-1 waits four seconds, then restarts detection.

DC Disconnect

The DC disconnect circuit monitors port current whenever power is on to detect continued presence of the PD. IEEE 802.3af mandates a minimum current of 10mA that the PD must draw for periods of at least 75ms with optional dropouts of no more than 250ms. The t_{MPDO} disconnect timer increments whenever port current is below 7.5mA (typ). If the timer expires, the port is turned off and the LTC4263-1 waits 1.5 seconds before restarting detection. If the undercurrent condition goes away before t_{MPDO} (350ms (typ)), the timer is reset to zero. The DC disconnect circuit includes a glitch filter to prevent noise from falsely resetting the timer. The current must be present for a period of at least 20ms to guarantee reset of the timer. To enable DC disconnect, tie the OSC pin to V_{SS}.

AC Disconnect

AC disconnect is an alternate method of sensing the presence or absence of a PD by monitoring the port impedance. The LTC4263-1 forces an AC signal from an internal sine wave generator on to the port. The ACOUT pin current is then sampled once per cycle and compared to I_{ACDMIN}. Like DC disconnect, the AC disconnect sensing circuitry controls the t_{MPDO} disconnect timer. When the connection impedance rises due to the removal of the PD, AC peak current falls below I_{ACDMIN} and the disconnect timer increments. If the impedance remains high (AC peak current remains below I_{ACDMIN}), the disconnect timer counts to t_{MPDO} and the port is turned off. If the impedance falls, causing AC peak current to rise above I_{ACDMIN} for two consecutive samples before the maximum count of the disconnect timer, the timer resets and the port remains powered.

The AC disconnect circuitry senses the port via the ACOUT pin. Connect a 0.47µF 100V X7R capacitor (C_{DET}) and a 1k resistor (R_{DET}) from the DETECT pin to the port output as shown in Figure 6. This provides an AC path for sensing the port impedance. The 1k resistor, R_{DET}, limits current flowing through this path during port power-on and power-off. An AC blocking diode (D_{AC}) is inserted between the OUT pin and the port to prevent the AC signal from being shorted by the LTC4263-1's power control MOSFET. The 500k resistor across D_{AC} allows the port voltage to decay after disconnect occurs.

Sizing of capacitors is critical to ensure proper function of AC disconnect. C_{PSE} (Figure 6) controls the connection impedance on the PSE side. Its capacitance must be kept low enough for AC disconnect to be able to sense the PD. On the other hand, C_{DET} has to be large enough to pass the signal at 110Hz. The recommended values are 0.1µF for C_{PSE} and 0.47µF for C_{DET}. The sizes of C_{PSE}, C_{DET}, and R_{DET} are chosen to create an economical, physically

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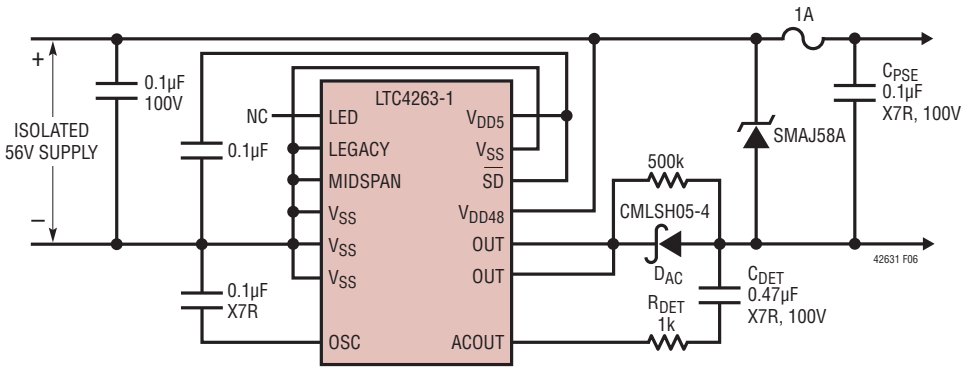

Figure 6. LTC4263-1 Using AC Disconnect

compact and functionally robust system. Moreover, the complete Power over Ethernet AC disconnect system (PSE, transformers, cabling, PD, etc.) is complex; deviating from the recommended values of C_{DET}, R_{DET} and C_{PSE} is strongly discouraged. Contact the Linear Technology Applications department for additional support.

Internal 110Hz AC Oscillator

The LTC4263-1 includes onboard circuitry to generate a 110Hz (typ), $2V_{P-P}$ sine wave on its OSC pin when a 0.1µF capacitor is connected between the OSC pin and V_{SS}. This sine wave is synchronized to the controller inside the LTC4263-1 and should not be externally driven. Tying the OSC pin to V_{SS} shuts down the oscillator and enables DC disconnect.

Power-On Reset and Reset/Backoff Timing

Upon startup, the LTC4263-1 waits four seconds before starting its first detection cycle. Depending on the results of this detection it will either power the port, repeat detection, or wait 3.2 seconds before attempting detection again if in midspan mode.

The LTC4263-1 may be reset by pulling the $\overline{SD}$ pin low. The port is turned off immediately and the LTC4263-1 sits idle. After $\overline{SD}$ is released there will be a 4-second delay before the next detection cycle begins.

V_{DD5} Logic-Level Supply

The V_{DD5} supply for the LTC4263-1 can either be supplied externally or generated internally from the V_{DD48} supply. If supplied externally, a voltage between 4.5V and 5.5V should be applied to the V_{DD5} pin to cause the internal regulator to shut down. If V_{DD5} is to be generated internally, the voltage will be 4.4V (typ) and a 0.1µF capacitor should be connected between V_{DD5} and V_{SS}. Do not connect the internally generated V_{DD5} to anything other than a bypass capacitor and the logic control pins of the same LTC4263-1.

LED Flash Codes

The LTC4263-1 includes a multi-function LED driver to inform the user of the port status. The LED is turned on when the port is connected to a PD and power is applied. If the port is not connected or is connected to a non-powered device with a 150Ω or shorted termination, the port will not be powered and the LED will be off. For other port conditions, the LTC4263-1 blinks a code to communicate the status to the user as shown in Table 1. One flash indicates low signature resistance, two flashes indicates high resistance and five flashes indicates an overload fault.

When active, the LED flash codes are repeated every 1.2 seconds. The duration of each LED flash is 75ms. Multiple LED flashes occur at a 300ms interval.

The LTC4263-1 includes a feature for efficiently driving the LED from a 56V power supply without the wasted power caused by having to drop over 52V in a current limit resistor. When operating the V_{DD5} supply internally, the LTC4263-1 drives the LED pin with a 6% duty cycle PWM signal. This allows use of the simple LED drive circuit in Figure 7 to minimize power dissipation. The modulation frequency of the LED drive is 28kHz, making the on period

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Table 1. Port Status and LED Flash Codes

PORT STATUS	LED FLASH CODE	FLASH PATTERN
Non-Powered Device $0\Omega < R_{PORT} < 200\Omega$	Off	LED Off
Port Open $R_{PORT} > 1M\Omega$	Off	LED Off
Port On $25k\Omega$	On	LED On
Low Signature Resistance $300\Omega < R_{PORT} < 15k\Omega$	1 Flash	☼ ● ● ● ☼ ● ● ● ☼ ● ● ●
High Signature Resistance $33k\Omega < R_{PORT} < 500k\Omega$	2 Flashes	☼ ☼ ● ● ☼ ☼ ● ● ☼ ☼ ● ●
Port Overload Fault	5 Flashes	● ● ● ● ☼ ☼ ☼ ☼ ☼ ● ● ●

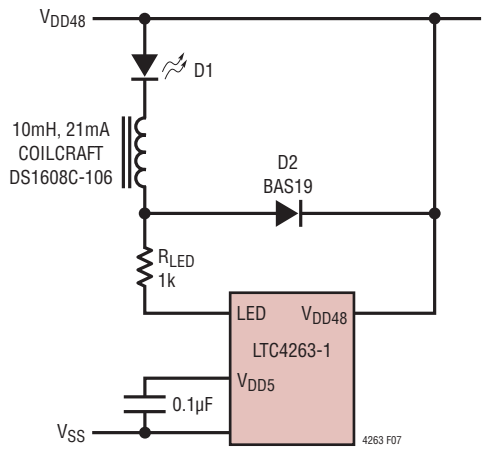

Figure 7. LED Drive Circuit with Single 48V Supply

2.2µs. During the 2.2µs that the LED pin is pulled low, current ramps up in the inductor, limited by R_{LED}. Diode D2 completes the circuit by allowing current to circulate while the LED pin is open circuit. Since current is only drawn from the power supply 6% of the time, power dissipation is substantially reduced.

When V_{DD5} is powered from an external supply, the PWM signal is disabled and the LED pin will pull down continuously when on. In this mode, the LED can be powered from the 5V supply with a simple series resistor.

EXTERNAL COMPONENT SELECTION

This section discusses the other elements needed to make a system including the LTC4263-1 function correctly. It is recommended to adhere closely to the example application circuits provided. For further assistance contact the Linear Technology Applications department.

PoE System Power Delivery

The LTC4263-1 can output over 30W(typ) and is designed to deliver 25W(min) to the PD over a 100 meter CAT5 cable for high power applications such as wireless access points, security cameras and RFID readers. There are several parameters external to the LTC4263-1 that limit the power available to the PD. Figure 8 provides a simple model used to calculate this power delivery.

The primary element affecting the delivery of power to the PD is the supply feeding the LTC4263-1. By maximizing this voltage, the highest and most efficient power delivery can be obtained. However, in order to adhere to common safety requirements, the supply is normally limited to 60V and the IEEE 802.3af committee has chosen 57V as a nominal maximum. In this example, a 56±1V power supply output sets the lower limit to 55V. The LTC4263-1 overload current limit monitors port current and removes

APPLICATIONS INFORMATION

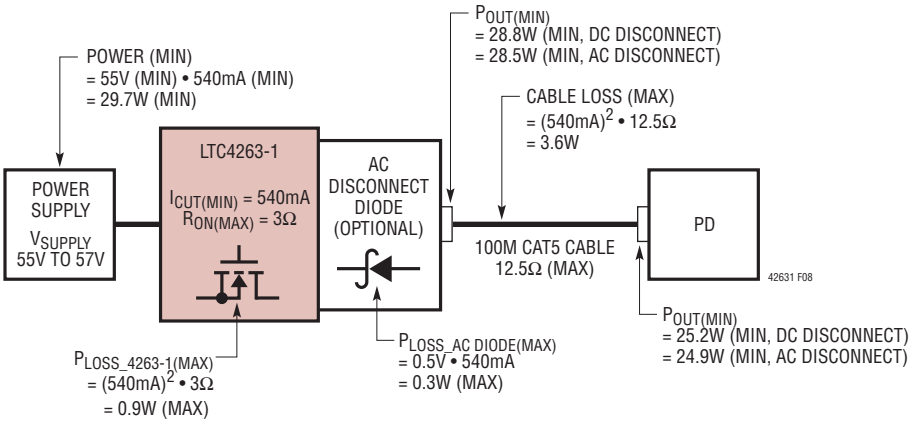

Figure 8. Example of Power Delivery Calculation Using the LTC4263-1

power if the port exceeds 540mA(min). This sets the maximum system operating current and along with the working voltage, limits the power available to the PD. The power at the PSE output is reduced by the resistance of the LTC4263-1 internal power MOSFET and the voltage drop of the AC blocking diode if used for AC disconnect as shown in Figure 8. The cabling can be responsible for the largest loss. In our example based on a worst-case 100 meter CAT5 cable and connectors, the power loss can be as much as 3.6W. Obviously for shorter cable runs the loss is less and lower resistance cables such as CAT6 will have correspondingly lower losses.

The total power available at the PD can be calculated taking in to account these losses using the formula:

$$P_{PD} = \left(V_{SUPPLY} \bullet I_{CUT}\right) - \left(I_{CUT}^{2} \bullet R_{ON}\right)$$
$$- \left(V_{DAC} \bullet I_{CUT}\right) - \left(I_{CUT}^{2} \bullet R_{CABLE}\right)$$

For many PoE systems, the only parameter affecting power delivery that is under the control of the PSE designer is the power supply. Optimum power delivery can be obtained by maximizing this power supply voltage. 4-pair systems can be treated as two independent 2-pair systems and therefore the power will be twice that of the 2-pair.

2-Pair vs 4-Pair

One of the basic architectural decisions associated with a high power PoE system is whether to deliver power using four conductors (2-pair) or all eight conductors (4-pair). Each method provides advantages and the system vendor needs to decide which method best suits their application.

2-pair power is used today in IEEE 802.3af systems (see Figure 1). One pair of conductors is used to deliver the current and a second pair is used for the return while two conductor pairs are not powered. This architecture offers the simplest implementation method but suffers from higher cable loss than an equivalent 4-pair system.

4-pair power delivers current to the PD via two conductor pairs in parallel (Figure 9). This lowers the cable resistance but raises the issue of current balance between each conductor pair. Differences in resistance of the transformer, cable and connectors along with differences in diode bridge forward voltage in the PD can cause an imbalance in the currents flowing through each pair. The 4-pair system in Figure 9 solves this problem by using two independent DC/DC converters in the PD. Using a 2-pair architecture with the LTC4263-1 allows delivery of 25W to the PD while using a 4-pair architecture allows delivery of 50W. Contact Linear Technology applications support for detailed information on implementing 2-pair and 4-pair PoE systems.

Common Mode Chokes

Both non-powered and powered Ethernet connections achieve best performance for data transfer and EMI when a common mode choke is used on each port. For cost reduction reasons, some designs share a common mode choke between two adjacent ports. This is not recommended.

APPLICATIONS INFORMATION

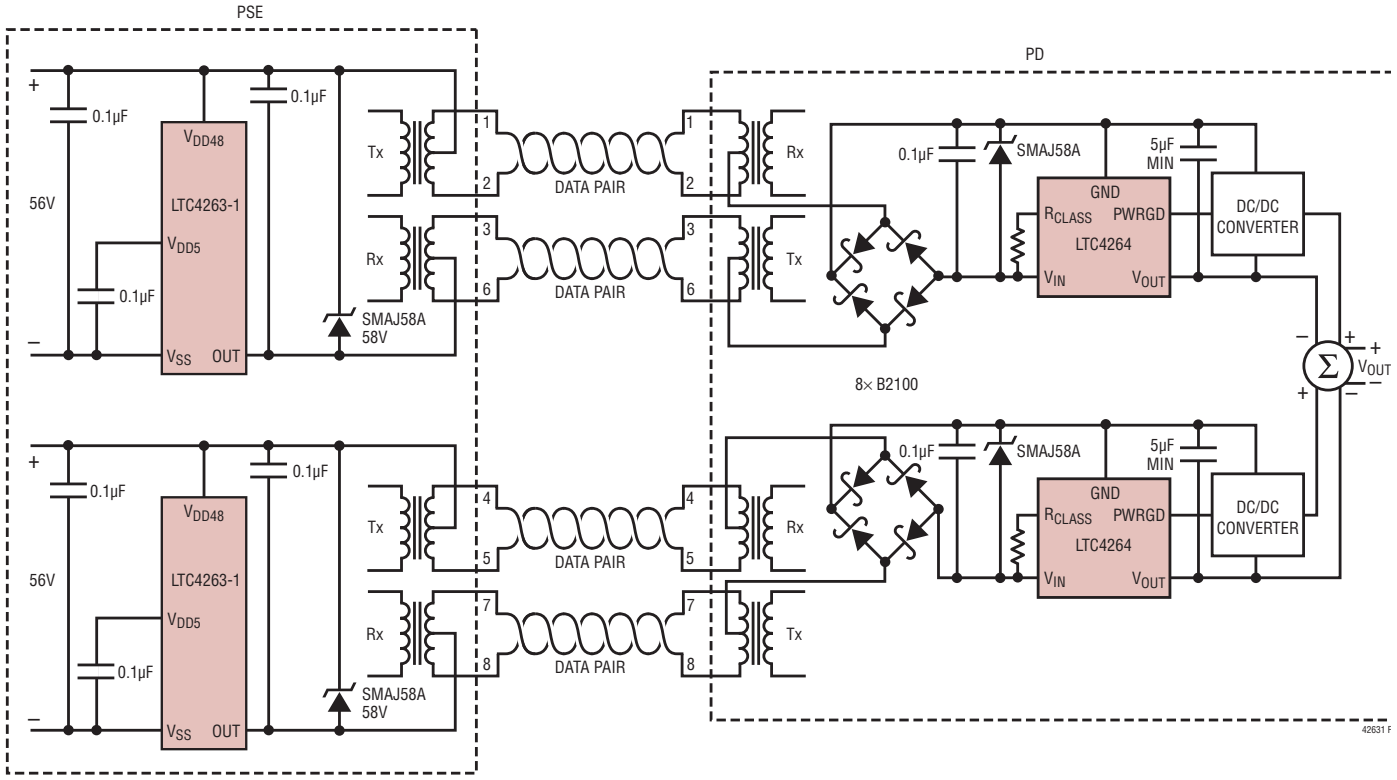

Figure 9. 4-Pair High Power PoE Gigabit Ethernet System Diagram

Sharing a common mode choke between two ports couples start-up, disconnect and fault transients from one port to the other. The end result can range from intermittent behavior to excessive voltages that may damage circuitry in both the PSE and PD connected to the port.

Transient Suppressor Diode

Power over Ethernet is a challenging Hot Swap application because it must survive unintentional abuse by repeated plugging in and out of devices at the port. Ethernet cables could potentially be cut or shorted together. Consequently, the PSE must be designed to handle these events without damage.

The most severe of these events is a sudden short on a powered port. What the PSE sees depends on how much CAT-5 cable is between it and the short. If the short occurs on the far end of a long cable, the cable inductance will prevent the current in the cable from increasing too quickly and the LTC4263-1 built-in short-circuit protection will control the current and turn off the port. However, the high current along with the cable inductance causes a large flyback voltage to appear across the port when the MOSFET is turned off. In the case of a short occurring with a minimum length cable, the instantaneous current can be extremely high due to the lower inductance. The LTC4263-1 has a high speed fault current limit circuit that shuts down the port in 20µs (typ). In this case, there is lower inductance but higher current so the event is still severe. A transient suppressor is required to clamp the port voltage and prevent damage to the LTC4263-1. An SMAJ58A or equivalent device works well to maintain port voltages within a safe range. A bidirectional transient suppressor should not be used.

Good layout practices place the transient voltage suppressor close to the LTC4263-1, before the common mode choke (if used) and data magnetics to enhance the protective function.

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If the port voltage reverses polarity and goes positive, the OUT pin can be overstressed because this voltage is stacked on top of the 56V supply. In this case, the transient suppresser is used to clamp the voltage to a small positive value to protect the LTC4263-1 and the PSE capacitor. For this reason, it is critical that only a **unidirectional** TVS be used.

Component leakages across the port can have an adverse affect on AC disconnect and even affect DC disconnect if the leakage becomes severe. The SMAJ58A is rated at less than 5µA leakage at 58V and works well in this application. There is a potential for stress induced leakage, so sufficient margins should be used when selecting transient suppressors for these applications.

Capacitors

Sizing of both the C_{DET} and C_{PSE} capacitors is critical for proper operation of the LTC4263-1 AC disconnect sensing. See the AC Disconnect section for more information. Note that many ceramic capacitors have dramatic DC voltage and temperature coefficients. Use 100V or higher rated X7R capacitors for C_{DET} and C_{PSE}, as these have reduced voltage dependence while also being relatively small and inexpensive. Bypass the 48V supply with a 0.1µF, 100V capacitor located close to the LTC4263-1. The V_{DD5} supply also requires a 0.1µF bypass capacitor.

Fuse

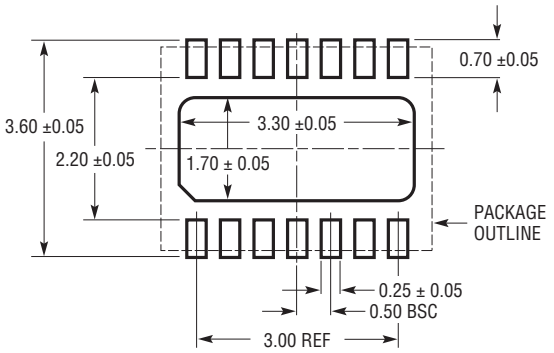
While the LTC4263-1 does not require a fuse for proper operation, some safety requirements state that the output current must be limited to less than 2A in less than 60 seconds if any one component fails or is shorted. Since the LTC4263-1 is the primary current limiter, its failure could result in excess current to the port. To meet these safety requirements, a fuse can be placed in the positive leg of the port. The fuse must be large enough that it will pass at least 675mA when derated for high temperature but small enough that it will fuse at less than 2A at cold temperature. This requirement can usually be satisfied with a 1A fuse or PTC. Placing the fuse between the RJ-45 connector and the LTC4263-1 and its associated circuitry provides additional protection for this circuitry. Consult a safety requirements expert for the application specific requirements.

Isolation

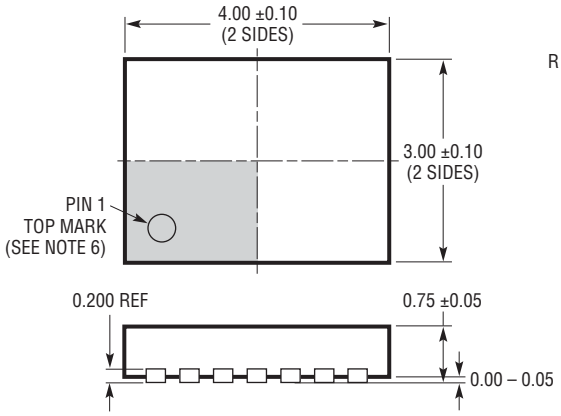
The IEEE 802.3af standard requires Ethernet ports to be electrically isolated from all other conductors that are user accessible. This includes the metal chassis, other connectors, and the AC power line. Environment A isolation is the most common and applies to wiring within a single building serviced by a single AC power system. For this type of application, the PSE isolation requirement can be met with the use of a single, isolated 56V supply powering several LTC4263-1 ports. Environment B, the stricter isolation requirement, is for networks that cross an AC power distribution boundary. In this case, electrical isolation must be maintained between each port in the PSE. The LTC4263-1 can be used to build a multi-port Environment B PSE by powering each LTC4263-1 from a separate, isolated 56V supply. In all PSE applications, there should be no user accessible connections to the LTC4263-1 other than the RJ-45 port.

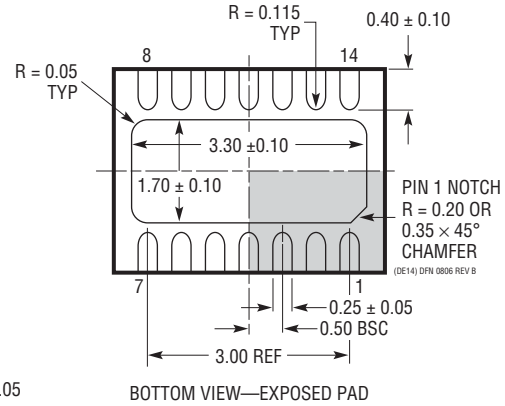
PACKAGE DESCRIPTION

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE