Quad IEEE 802.3at Power over Ethernet Controller

FEATURES

- **Four Independent PSE Channels**
- **Compliant with IEEE 802.3at Type 1 and 2**
- **0.34Ω Total Channel Resistance**
  - **130mW/Port at 600mA**
- **Advanced Power Management**
  - **8-Bit Programmable Current Limit (I_{LIM})**
  - **7-Bit Programmable Overload Currents (I_{CUT})**
  - **Fast Shutdown of Preselected Ports**
  - **14.5-Bit Port Current/Voltage Monitoring**
  - **2-Event Classification**
- **Very High Reliability 4-Point PD Detection**
  - **2-Point Forced Voltage**
  - **2-Point Forced Current**
- **High Capacitance Legacy Device Detection**
- LTC4259A-1 and LTC4258 Pin and SW Compatible
- 1MHz I^2C Compatible Serial Control Interface
- Midspan Backoff Timer
- Supports Proprietary Power Levels Above 25W
- Available in 38-Pin 5mm × 7mm QFN and 36-Pin SSOP Packages

APPLICATIONS

- High Power PSE Switches/Routers
- High Power PSE Midspans

DESCRIPTION

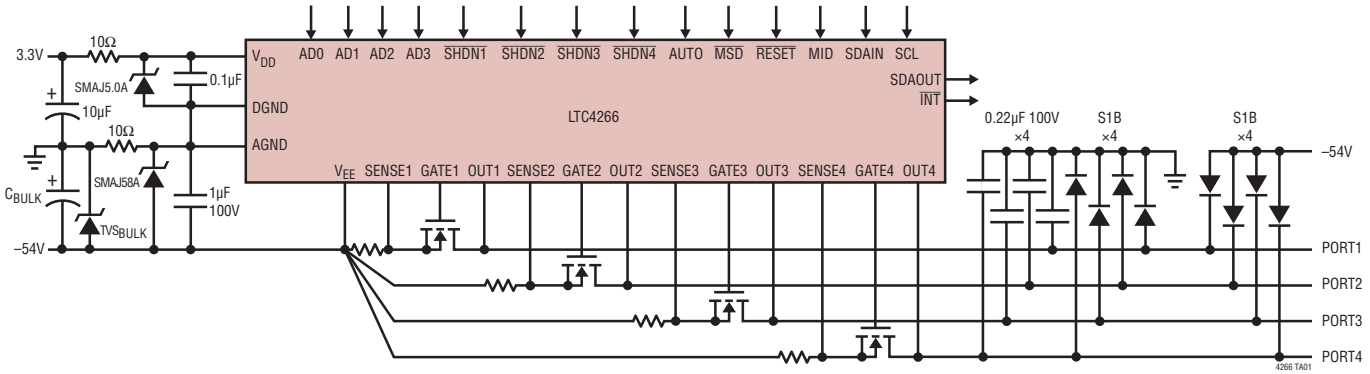
The LTC®4266 is a quad PSE controller designed for use in IEEE 802.3 Type 1 and Type 2 (high power) compliant Power over Ethernet systems. External power MOSFETs enhance system reliability and minimize channel resistance, cutting power dissipation and eliminating the need for heatsinks even at Type 2 power levels. External power components also allow use at very high power levels while remaining otherwise compatible with the IEEE standard. 80V-rated port pins provide robust protection against external faults.

The LTC4266 includes advanced power management features, including current and voltage readback and programmable I_{CUT} and I_{LIM} thresholds. Available C libraries simplify power-management software development; an optional AUTO pin mode provides fully IEEE-compliant standalone operation with no software required. Proprietary 4-point PD detection circuitry minimizes false PD detection while supporting legacy phone operation. Midspan operation is supported with built-in 2-event classification and backoff timing. Host communication is via a 1MHz I^2C serial interface.

The LTC4266 is available in a 5mm × 7mm QFN package that significantly reduces board space compared with competing solutions. A legacy-compatible 36-pin SSOP package is also available.

TYPICAL APPLICATION

Complete 4-Port Ethernet High Power Source



ABSOLUTE MAXIMUM RATINGS

Supply Voltages (Note 1)
- AGND – V_{EE} ..... –0.3V to 80V
- DGND – V_{EE} ..... –0.3V to 80V
- V_{DD} – DGND ..... –0.3V to 5.5V

Digital Pins
- SCL, SDAIN, SDAOUT, $\overline{INT}$, $\overline{SHDN}$n, $\overline{MSD}$, ADn, $\overline{RESET}$, AUTO, MID..... DGND –0.3V to V_{DD} + 0.3V

Analog Pins
- GATEn, SENSEn, OUTn ..... V_{EE} –0.3V to V_{EE} + 80V

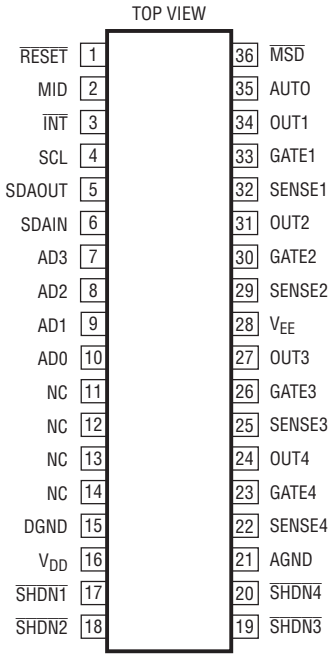
Operating Temperature Range
- LTC4266C ..... 0°C to 70°C
- LTC4266I ..... –40°C to 85°C

Junction Temperature (Note 2) ..... 125°C

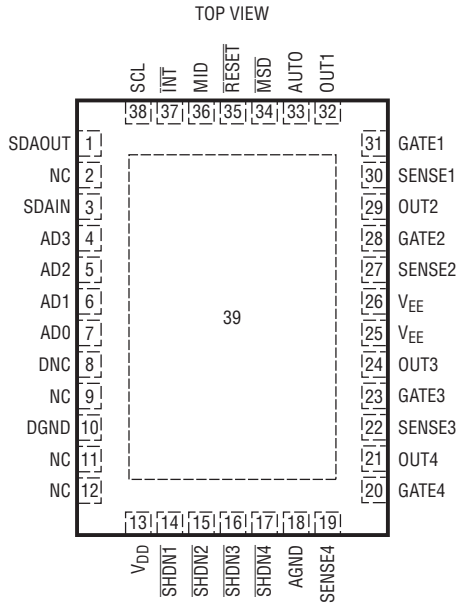
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



GW36 PACKAGE
36-LEAD PLASTIC WIDE SSOP
T_{JMAX} = 125°C, θ_{JA} = 80°C/W



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
EXPOSED PAD IS V_{EE} (PIN 39) MUST BE SOLDERED TO PCB
T_{JMAX} = 125°C, θ_{JA} = 34°C/W

ORDER INFORMATION

http://www.linear.com/product/LTC4266#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4266CGW#PBF	LTC4266CGW#TRPBF	LTC4266CGW	36-Lead Plastic Wide SSOP	0°C to 70°C
LTC4266IGW#PBF	LTC4266IGW#TRPBF	LTC4266IGW	36-Lead Plastic Wide SSOP	–40°C to 85°C
LTC4266CUHF#PBF	LTC4266CUHF#TRPBF	4266	38-Lead (5mm × 7mm) Plastic QFN	0°C to 70°C
LTC4266IUHF#PBF	LTC4266IUHF#TRPBF	4266	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 54V, AGND = DGND, and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3, 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Main PoE Supply Voltage	AGND – V_{EE}					
		For IEEE Type 1 Complaint Output	●	45		57	V
		For IEEE Type 2 Complaint Output	●	51		57	V
	Undervoltage Lock-out Level		●	20	25	30	V
V_{DD}	V_{DD} Supply Voltage	V_{DD} – DGND	●	3.0	3.3	4.3	V
	Undervoltage Lock-out		●		2.2		V
	Allowable Digital Ground Offset	DGND – V_{EE}	●	25		57	V
I_{EE}	V_{EE} Supply Current	(AGND – V_{EE}) = 55V	●		–2.4	–5	mA
I_{DD}	V_{DD} Supply Current	(V_{DD} – DGND) = 3.3V	●		1.1	3	mA
Detection							
	Detection Current – Force Current	First Point, AGND – V_{OUTn} = 9V	●	220	240	260	µA
		Second Point, AGND – V_{OUTn} = 3.5V	●	140	160	180	µA
	Detection Voltage – Force Voltage	AGND – V_{OUTn}, 5µA ≤ I_{OUTn} ≤ 500µA					
		First Point	●	7	8	9	V
		Second Point	●	3	4	5	V
	Detection Current Compliance	AGND – V_{OUTn} = 0V	●		0.8	0.9	mA
V_{OC}	Detection Voltage Compliance	AGND – V_{OUTn}, Open Port	●		10.4	12	V
	Detection Voltage Slew Rate	AGND – V_{OUTn}, C_{PORT} = 0.15µF	●			0.01	V/µs
	Min. Valid Signature Resistance		●	15.5	17	18.5	kΩ
	Max. Valid Signature Resistance		●	27.5	29.7	32	kΩ
Classification							
V_{CLASS}	Classification Voltage	AGND – V_{OUTn}, 0mA ≤ I_{CLASS} ≤ 50mA	●	16.0		20.5	V
	Classification Current Compliance	V_{OUTn} = AGND	●	53	61	67	mA
	Classification Threshold Current	Class 0 – 1	●	5.5	6.5	7.5	mA
		Class 1 – 2	●	13.5	14.5	15.5	mA
		Class 2 – 3	●	21.5	23	24.5	mA
		Class 3 – 4	●	31.5	33	34.9	mA
		Class 4 – Overcurrent	●	45.2	48	50.8	mA
V_{MARK}	Classification Mark State Voltage	AGND – V_{OUTn}, 0.1mA ≤ I_{CLASS} ≤ 10mA	●	7.5	9	10	V
	Mark State Current Compliance	V_{OUTn} = AGND	●	53	61	67	mA
Gate Driver							
	GATE Pin Pull-Down Current	Port Off, V_{GATEn} = V_{EE} + 5V	●	0.4			mA
		Port Off, V_{GATEn} = V_{EE} + 1V	●	0.08	0.12		mA
	GATE Pin Fast Pull-Down Current	V_{GATEn} = V_{EE} + 5V			30		mA
	GATE Pin On Voltage	V_{GATEn} – V_{EE}, I_{GATEn} = 1µA	●	8	12	14	V
Output Voltage Sense							
V_{PG}	Power Good Threshold Voltage	V_{OUTn} – V_{EE}	●	2	2.4	2.8	V
	OUT Pin Pull-Up Resistance to AGND	0V ≤ (AGND – V_{OUTn}) ≤ 5V	●	300	500	700	kΩ

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense							
V_{CUT}	Overcurrent Sense Voltage	$V_{SENSEn} – V_{EE}$, icut12 = icut34 = hpen = 00h	●	180	188	196	mV
		hpen = 0Fh, cutn[5:0] ≥ 4 (Note 12)					
		cutrng = 0	●	9	9.38	9.75	mV/LSB
		cutrng = 1	●	4.5	4.69	4.88	mV/LSB
	Overcurrent Sense in AUTO pin mode	Class 0, Class 3	●	90	94	98	mV
		Class 1	●	26	28	30	mV
		Class 2	●	49	52	55	mV
		Class 4	●	152	159	166	mV
V_{LIM}	Active Current Limit in 802.3af Compliant Mode	$V_{SENSEn} – V_{EE}$, dblpwr = hpen = 00h					
		V_{EE} = 55V (Note 12)					
		$V_{EE} < V_{OUT} <$ AGND – 29V	●	204	212	220	mV
		AGND – V_{OUT} = 0V	●	40		100	mV
V_{LIM}	Active Current Limit in High Power Mode	hpen = 0Fh, limn = C0h, V_{EE} = 55V					
		$V_{OUT} – V_{EE}$ = 0V to 10V	●	204	212	221	mV
		V_{EE} + 23V < V_{OUT} < AGND – 29V	●	100	106	113	mV
		AGND – V_{OUT} = 0V	●	20		50	mV
V_{LIM}	Active Current Limit in AUTO pin mode	$V_{OUT} – V_{EE}$ = 0V to 10V, V_{EE} = 55V					
		Class 0 to Class 3	●	102	106	110	mV
		Class 4	●	204	212	221	mV
V_{MIN}	DC Disconnect Sense Voltage	$V_{SENSEn} – V_{EE}$, rdis = 0	●	2.6	3.8	4.8	mV
		$V_{SENSEn} – V_{EE}$, rdis = 1	●	1.3	1.9	2.41	mV
V_{SC}	Short-Circuit Sense	$V_{SENSEn} – V_{EE} – V_{LIM}$, rdis = 0	●	160	200	255	mV
		$V_{SENSEn} – V_{EE} – V_{LIM}$, rdis = 1	●	75	100	135	mV
Port Current ReadBack							
	Resolution	No missing codes, fast_iv = 0			14		bits
	LSB Weight	$V_{SENSEn} – V_{EE}$			30.5		µV/LSB
	50-60Hz Noise Rejection	(Note 7)			30		dB
Port Voltage ReadBack							
	Resolution	No missing codes, fast_iv = 0			14		bits
	LSB Weight	AGND – V_{OUTn}			5.835		mV/LSB
	50-60Hz noise rejection	(Note 7)			30		dB
Digital Interface							
V_{ILD}	Digital Input Low Voltage	ADn, $\overline{SHDN}$n, $\overline{RESET}$, $\overline{MSD}$, AUTO, MID (Note 6)	●			0.8	V
	I^2C Input Low Voltage	SCL, SDAIN (Note 6)	●			0.8	V
V_{IHD}	Digital Input High Voltage	(Note 6)	●	2.2			V
	Digital Output Low Voltage	I_{SDAOUT} = 3mA, $I_{\overline{INT}}$ = 3mA	●			0.4	V
		I_{SDAOUT} = 5mA, $I_{\overline{INT}}$ = 5mA	●			0.7	V
	Internal Pull-Up to V_{DD}	ADn, $\overline{SHDN}$n, $\overline{RESET}$, $\overline{MSD}$			50		kΩ
	Internal Pull-Down to DGND	AUTO, MID			50		kΩ

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing Characteristics							
t_{DET}	Detection Time	Beginning to End of Detection (Note 7)	●	270	290	310	ms
t_{DETDLY}	Detection Delay	From PD Connected to Port to Detection Complete (Note 7)	●	300		470	ms
t_{CLE1}	First Class Event Duration	(Note 7)	●	11	12	13	ms
t_{ME1}	First Mark Event Duration	(Notes 7, 11)	●	6.8	8.6	10.3	ms
t_{CLE2}	Second Class Event Duration	(Note 7)	●	11	12	13	ms
t_{ME2}	Second Mark Event Duration	(Note 7)	●	19	22		ms
t_{CLE3}	Third Class Event Duration	C_{PORT} = 0.6µF (Note 7)	●			0.1	ms
t_{PON}	Power On Delay in AUTO pin mode	From End of Valid Detect to Application of Power to Port (Note 7)	●			60	ms
	Turn On Rise Time	(AGND – V_{OUT}): 10% to 90% of (AGND – V_{EE}), C_{PORT} = 0.15µF (Note 7)	●	15	24		µs
	Turn On Ramp Rate	C_{PORT} = 0.15µF (Note 7)	●			10	V/µs
	Fault Delay	From I_{CUT} Fault to Next Detect	●	1.0	1.1		s
	Midspan Mode Detection Backoff	Rport = 15.5kΩ (Note 7)	●	2.3	2.5	2.7	s
	Power Removal Detection Delay	From Power Removal After t_{DIS} to Next Detect (Note 7)	●	1.0	1.3	2.5	s
t_{START}	Maximum Current Limit Duration During Port Start-Up	t_{START1} = 0, t_{START0} = 0 (Notes 7, 12)	●	52	62.5	66	ms
t_{LIM}	Maximum Current Limit Duration After Port Start-Up	t_{CUT1} = 0, t_{CUT0} = 0, t_{LIM} = 0h (Notes 7, 12)	●	52	62.5	66	ms
t_{CUT}	Maximum Overcurrent Duration After Port Start-Up	t_{CUT1} = 0, t_{CUT0} = 0 (Notes 7, 12)	●	52	62.5	66	ms
	Maximum Overcurrent Duty Cycle	(Note 7)	●	5.8	6.3	6.7	%
t_{MPS}	Maintain Power Signature (MPS) Pulse Width Sensitivity	Current Pulse Width to Reset Disconnect Timer (Notes 7, 8)	●	1.6		3.6	ms
t_{DIS}	Maintain Power Signature (MPS) Dropout Time	t_{conf} [1:0] = 00b (Notes 5, 7, 12)	●	320	350	380	ms
t_{MSD}	Masked Shut Down Delay	(Note 7)	●			6.5	µs
t_{SHDN}	Port Shut Down Delay	(Note 7)	●			6.5	µs
	I^2C Watchdog Timer Duration		●	1.5	2	3	s
	Minimum Pulse Width for Masked Shut Down	(Note 7)	●	3			µs
	Minimum Pulse Width for SHDN	(Note 7)	●	3			µs
	Minimum Pulse Width for RESET	(Note 7)	●	4.5			µs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Timing							
	Clock Frequency	(Note 7)	●			1	MHz
t_1	Bus Free Time	Figure 5 (Notes 7, 9)	●	480			ns
t_2	Start Hold Time	Figure 5 (Notes 7, 9)	●	240			ns
t_3	SCL Low Time	Figure 5 (Notes 7, 9)	●	480			ns
t_4	SCL High Time	Figure 5 (Notes 7, 9)	●	240			ns
t_5	Data Hold Time	Figure 5 (Notes 7, 9) Data into chip Data out of chip	● ●	60		 120	ns ns
t_6	Data Set-Up Time	Figure 5 (Notes 7, 9)	●	80			ns
t_7	Start Set-Up Time	Figure 5 (Notes 7, 9)	●	240			ns
t_8	Stop Set-Up Time	Figure 5 (Notes 7, 9)	●	240			ns
t_r	SCL, SDAIN Rise Time	Figure 5 (Notes 7, 9)	●			120	ns
t_f	SCL, SDAIN Fall Time	Figure 5 (Notes 7, 9)	●			60	ns
	Fault Present to $\overline{INT}$ Pin Low	(Notes 7, 9, 10)	●			150	ns
	Stop Condition to $\overline{INT}$ Pin Low	(Notes 7, 9, 10)	●			1.5	µs
	ARA to $\overline{INT}$ Pin High Time	(Notes 7, 9)	●			1.5	µs
	SCL Fall to ACK Low	(Notes 7, 9)	●			120	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 140°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: All currents into device pins are positive; all currents out of device pins are negative.

Note 4: The LTC4266 operates with a negative supply voltage (with respect to ground). To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 5: t_{DIS} is the same as t_{MPDO} defined by IEEE 802.3at.

Note 6: The LTC4266 digital interface operates with respect to DGND. All logic levels are measured with respect to DGND.

Note 7: Guaranteed by design, not subject to test.

Note 8: The IEEE 802.3af specification allows a PD to present its Maintain Power Signature (MPS) on an intermittent basis without being disconnected. In order to stay powered, the PD must present the MPS for t_{MPS} within any t_{MPDO} time window.

Note 9: Values measured at $V_{ILD(MAX)}$ and $V_{IHD(MIN)}$.

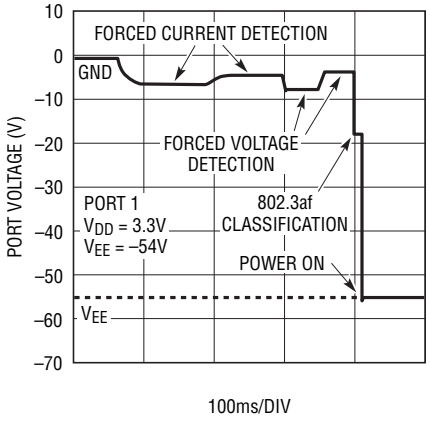
Note 10: If fault condition occurs during an I²C transaction, the $\overline{INT}$ pin will not be pulled down until a stop condition is present on the I²C bus.

Note 11: Load Characteristic of the LTC4266 during Mark:
7V < (AGND – V_{OUTn}) < 10V or I_{OUT} < 50µA

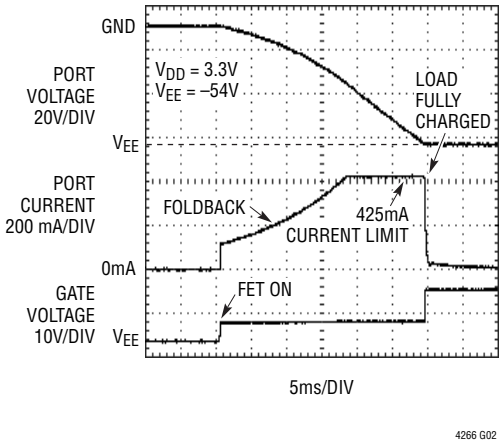
Note 12: See the LTC4266 Software Programming documentation for information on serial bus usage and device configuration and status registers.

TYPICAL PERFORMANCE CHARACTERISTICS

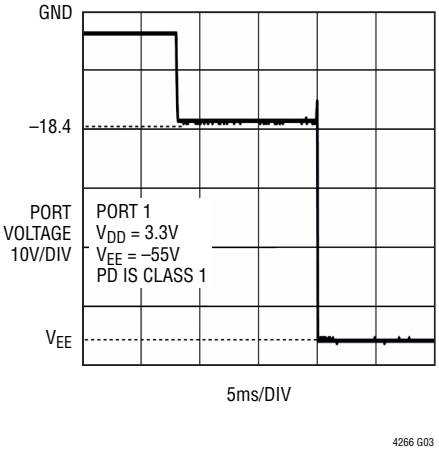
Power On Sequence in AUTO Pin Mode



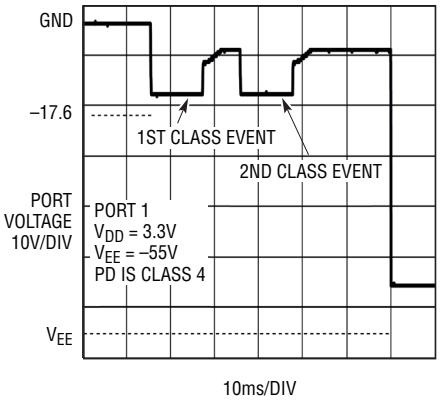
Powering Up into a 180µF Load



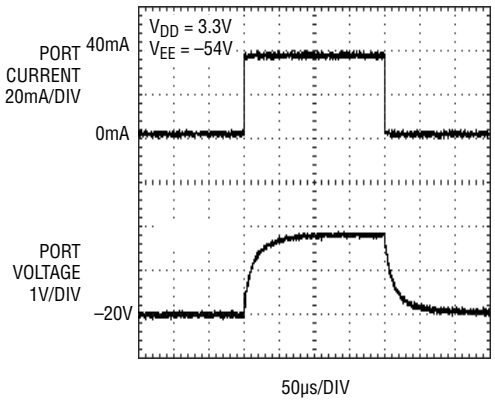
802.3af Classification in AUTO Pin Mode



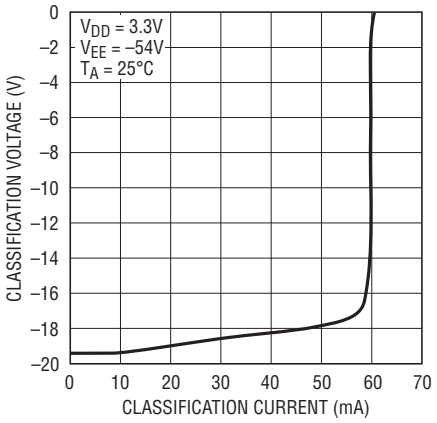
2-Event Classification in Auto Pin Mode



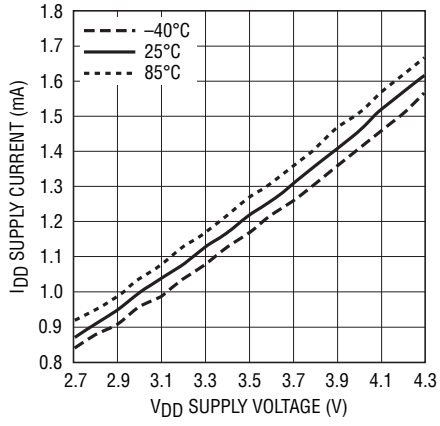
Classification Transient Response to 40mA Load Step



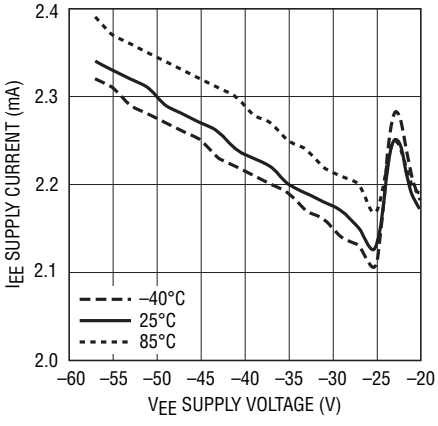
Classification Current Compliance



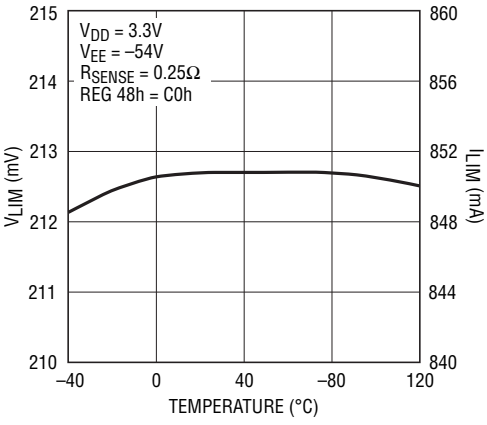
V_{DD} Supply Current vs Voltage



V_{EE} Supply Current vs Voltage

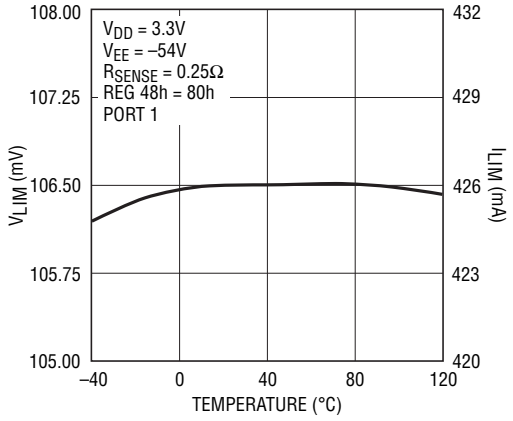


802.3at I_{LIM} Threshold vs Temperature



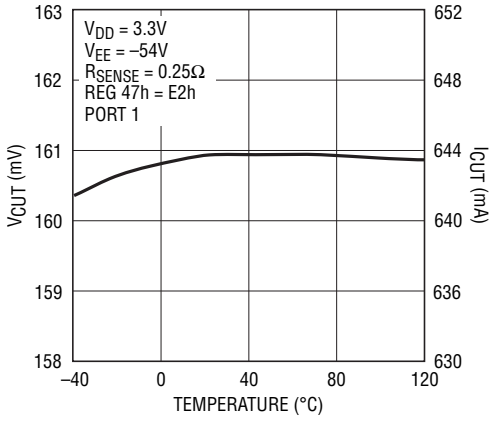
TYPICAL PERFORMANCE CHARACTERISTICS

802.3af I_{LIM} Threshold vs Temperature



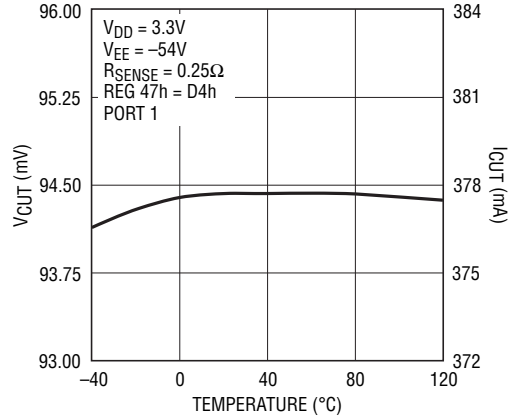
4266 G10

802.3at I_{CUT} Threshold vs Temperature



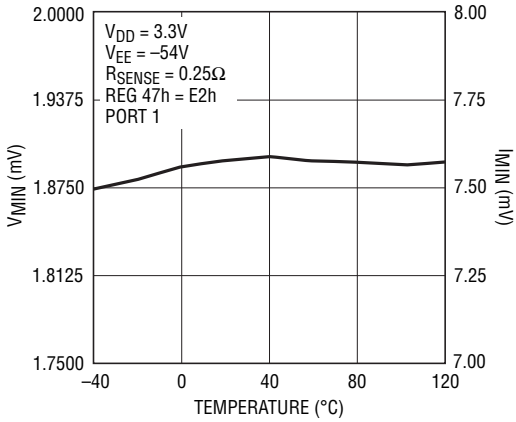
4266 G11

802.3af I_{CUT} Threshold vs Temperature



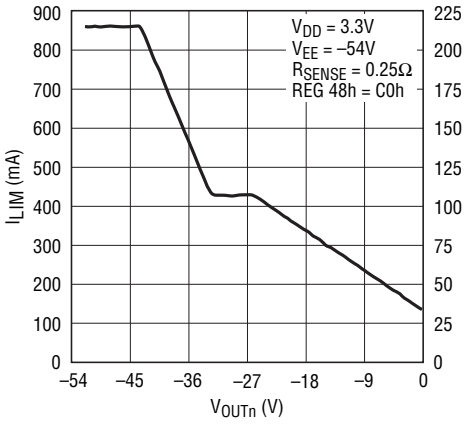
4266 G12

DC Disconnect Threshold vs Temperature



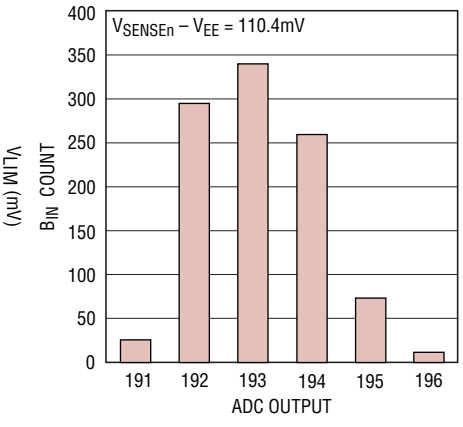
4266 G13

Current Limit Foldback



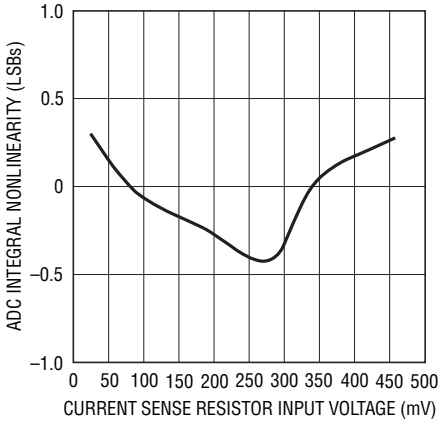
4266 G14

ADC Noise Histogram Current Readback in Fast Mode



4266 G15

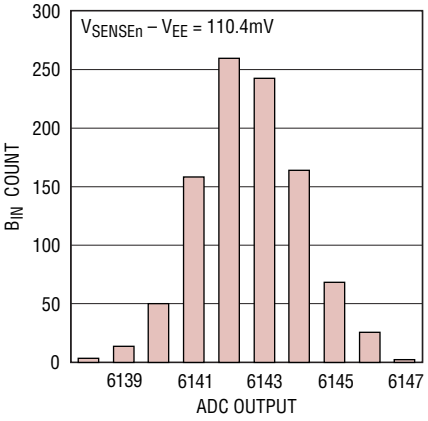
ADC Integral Nonlinearity Current Readback in Fast Mode



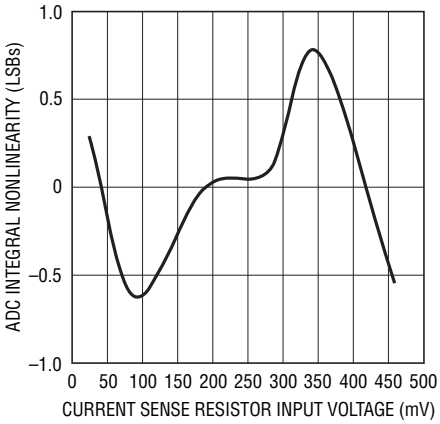
4266 G16

TYPICAL PERFORMANCE CHARACTERISTICS

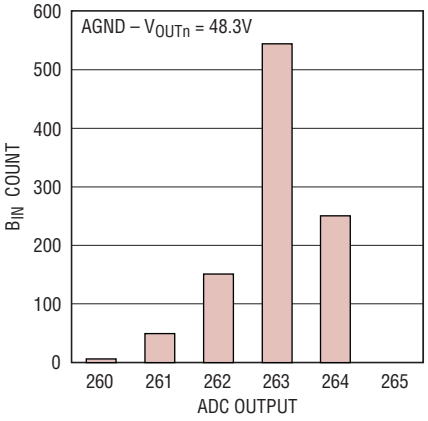
ADC Noise Histogram Current Readback in Slow Mode



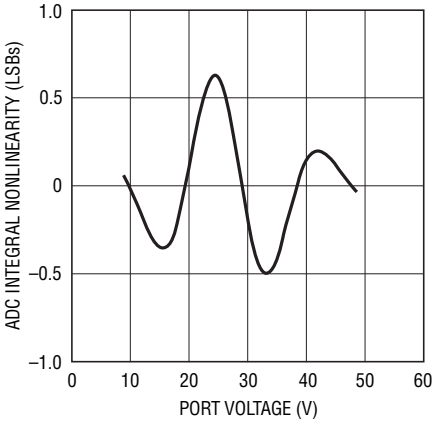
ADC Integral Nonlinearity Current Readback in Slow Mode



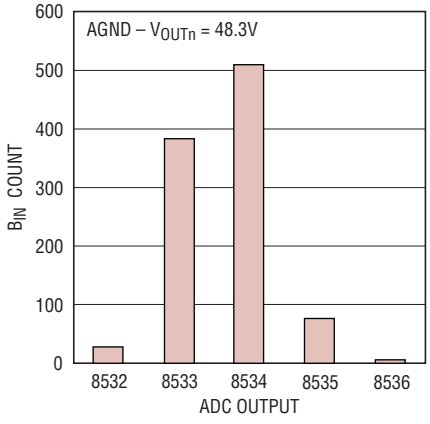
ADC Noise Histogram Port Voltage Readback in Fast Mode



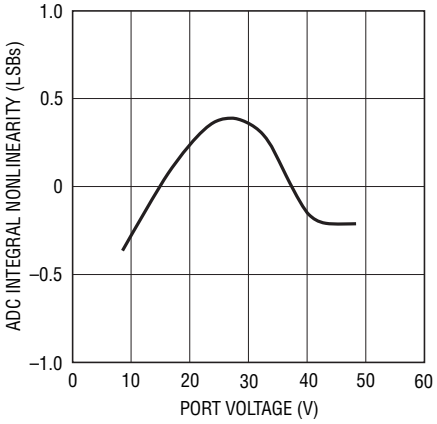
ADC Integral Nonlinearity Voltage Readback in Fast Mode



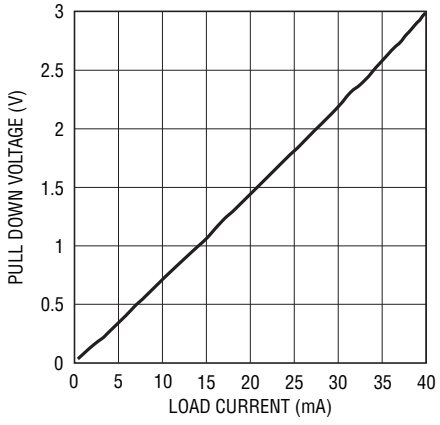
ADC Noise Histogram Port Voltage Readback in Slow Mode



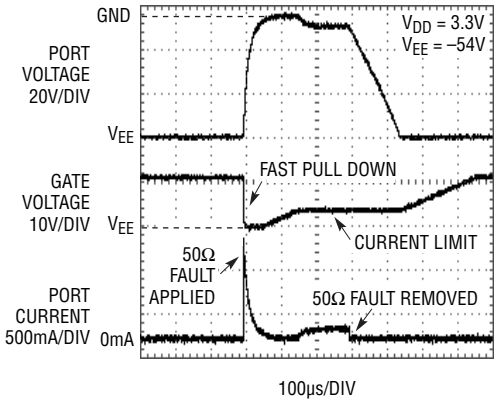
ADC Integral Nonlinearity Voltage Readback in Slow Mode



$\overline{INT}$ and SDAOUT Pull Down Voltage vs Load Current



MOSFET Gate Drive With Fast Pull Down



TEST TIMING DIAGRAMS

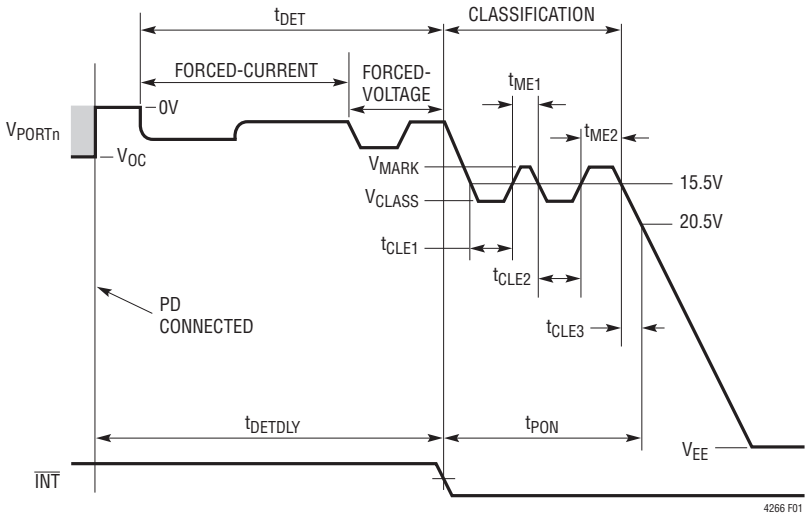


Figure 1. Detect, Class and Turn-On Timing in AUTO Pin or Semi-Auto Modes

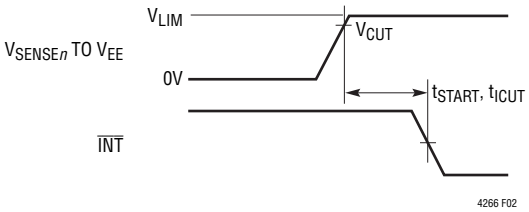


Figure 2. Current Limit Timing

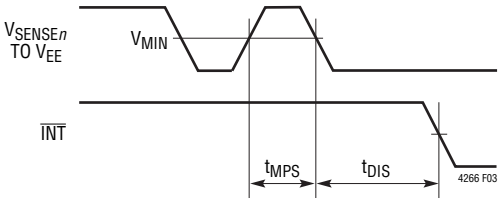


Figure 3. DC Disconnect Timing

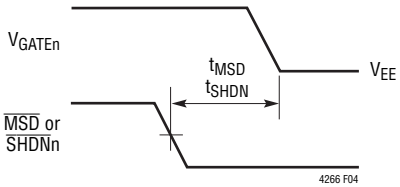


Figure 4. Shut Down Delay Timing

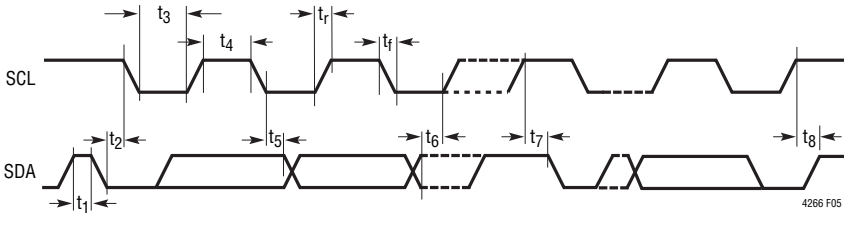


Figure 5. I²C Interface Timing

I²C TIMING DIAGRAMS

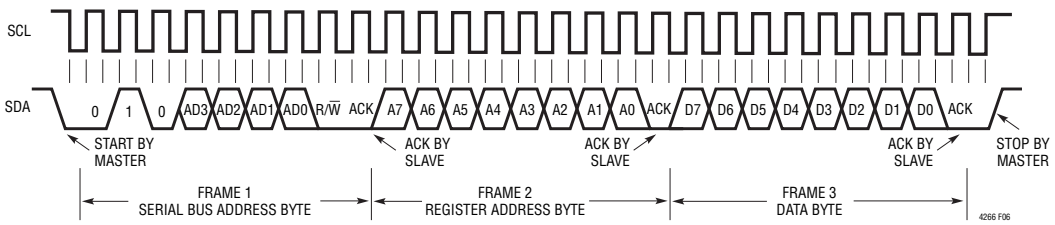


Figure 6. Writing to a Register

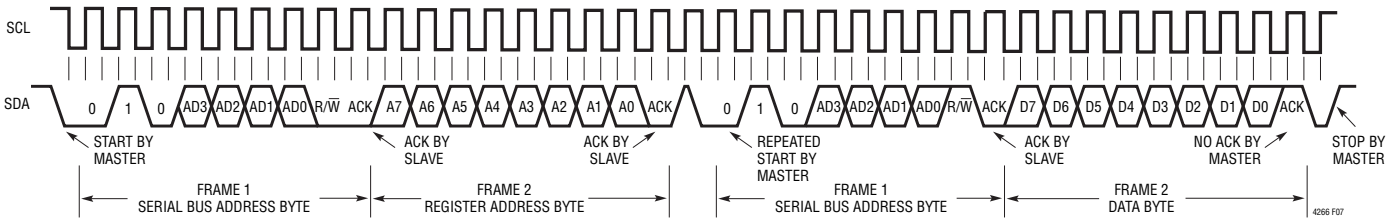


Figure 7. Reading from a Register

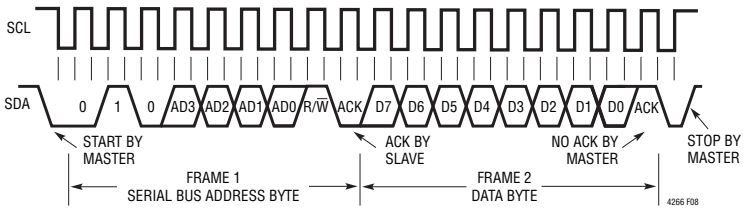


Figure 8. Reading the Interrupt Register (Short Form)

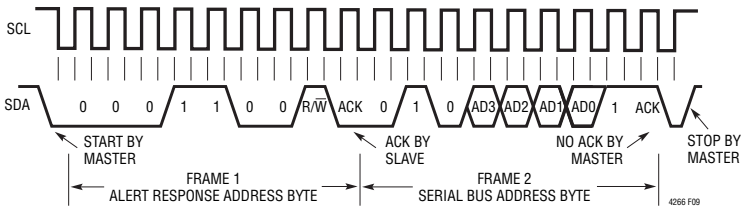


Figure 9. Reading from Alert Response Address

PIN FUNCTIONS

$\overline{\text{RESET}}$: Chip Reset, Active Low. When the $\overline{\text{RESET}}$ pin is low, the LTC4266 is held inactive with all ports off and all internal registers reset to their power-up states. When $\overline{\text{RESET}}$ is pulled high, the LTC4266 begins normal operation. $\overline{\text{RESET}}$ can be connected to an external capacitor or RC network to provide a power turn-on delay. Internal filtering of the $\overline{\text{RESET}}$ pin prevents glitches less than 1µs wide from resetting the LTC4266. Internally pulled up to V_{DD}.

MID: Midspan Mode Input. When high, the LTC4266 acts as a midspan device. Internally pulled down to DGND.

$\overline{\text{INT}}$: Interrupt Output, Open Drain. $\overline{\text{INT}}$ will pull low when any one of several events occur in the LTC4266. It will return to a high impedance state when bits 6 or 7 are set in the Reset PB register (1Ah). The $\overline{\text{INT}}$ signal can be used to generate an interrupt to the host processor, eliminating the need for continuous software polling. Individual $\overline{\text{INT}}$ events can be disabled using the Int Mask register (01h). See LTC4266 Software Programming documentation for more information. The $\overline{\text{INT}}$ pin is only updated between I^2C transactions.

SCL: Serial Clock Input. High impedance clock input for the I^2C serial interface bus. SCL must be tied high if not used.

SDAOUT: Serial Data Output, Open Drain Data Output for the I^2C Serial Interface Bus. The LTC4266 uses two pins to implement the bidirectional SDA function to simplify opto-isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. SDAOUT should be grounded or left floating if not used. See Applications Information for more information.

SDAIN: Serial Data Input. High impedance data input for the I^2C serial interface bus. The LTC4266 uses two pins to implement the bidirectional SDA function to simplify opto-isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. SDAIN must be tied high if not used. See Applications Information for more information.

AD3: Address Bit 3. Tie the address pins high or low to set the I^2C serial address to which the LTC4266 responds. This address will be $010A_3A_2A_1A_0b$. Internally pulled up to V_{DD}.

AD2: Address Bit 2. See AD3.

AD1: Address Bit 1. See AD3.

AD0: Address Bit 0. See AD3.

NC, DNC: All pins identified with "NC" or "DNC" must be left unconnected.

DGND: Digital Ground. DGND is the return for the V_{DD} supply.

V_{DD}: Logic Power Supply. Connect to a 3.3V power supply relative to DGND. V_{DD} must be bypassed to DGND near the LTC4266 with at least a 0.1µF capacitor.

$\overline{\text{SHDN1}}$: Shutdown Port 1, Active Low. When pulled low, $\overline{\text{SHDN1}}$ shuts down port 1, regardless of the state of the internal registers. Pulling $\overline{\text{SHDN1}}$ low is equivalent to setting the Reset Port 1 bit in the Reset Pushbutton register (1Ah). Internal filtering of the $\overline{\text{SHDN1}}$ pin prevents glitches less than 1µs wide from resetting the port. Internally pulled up to V_{DD}.

$\overline{\text{SHDN2}}$: Shutdown Port 2, Active Low. See $\overline{\text{SHDN1}}$.

$\overline{\text{SHDN3}}$: Shutdown Port 3, Active Low. See $\overline{\text{SHDN1}}$.

$\overline{\text{SHDN4}}$: Shutdown Port 4, Active Low. See $\overline{\text{SHDN1}}$.

AGND: Analog Ground. AGND is the return for the V_{EE} supply.

SENSE4: Port 4 Current Sense Input. SENSE4 monitors the external MOSFET current via a 0.5Ω or 0.25Ω sense resistor between SENSE4 and V_{EE}. Whenever the voltage across the sense resistor exceeds the overcurrent detection threshold V_{CUT}, the current limit fault timer counts up. If the voltage across the sense resistor reaches the current limit threshold V_{LIM}, the GATE4 pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. If the port is unused, the SENSE4 pin must be tied to V_{EE}.

PIN FUNCTIONS

GATE4: Port 4 Gate Drive. GATE4 should be connected to the gate of the external MOSFET for port 4. When the MOSFET is turned on, the gate voltage is driven to 12V (typ) above V_{EE}. During a current limit condition, the voltage at GATE4 will be reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATE4 is pulled down, turning the MOSFET off and recording a t_{CUT} or t_{START} event. If the port is unused, float the GATE4 pin.

OUT4: Port 4 Output Voltage Monitor. OUT4 should be connected to the output port. A current limit foldback circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the drain-to-source voltage exceeds 10V. The port 4 Power Good bit is set when the voltage from OUT4 to V_{EE} drops below 2.4V (typ). A 500k resistor is connected internally from OUT4 to AGND when the port is idle. If the port is unused, OUT4 pin must be floated.

SENSE3: Port 3 Current Sense Input. See SENSE4.

GATE3: Port 3 Gate Drive. See GATE4.

OUT3: Port 3 Output Voltage Monitor. See OUT4.

V_{EE}: Main Supply Input. Connect to a –45V to –57V supply, relative to AGND.

SENSE2: Port 2 Current Sense Input. See SENSE4.

GATE2: Port 2 Gate Drive. See GATE4.

OUT2: Port 2 Output Voltage Monitor. See OUT4.

SENSE1: Port 1 Current Sense Input. See SENSE4.

GATE1: Port 1 Gate Drive. See GATE 4.

OUT1: Port 1 Output Voltage Monitor. See OUT4.

AUTO: AUTO Pin Mode Input. AUTO pin mode allows the LTC4266 to detect and power up a PD even if there is no host controller present on the I^2C bus. The voltage of the AUTO pin determines the state of the internal registers when the LTC4266 is reset or comes out of V_{DD} UVLO (see the Register map). The states of these register bits can subsequently be changed via the I^2C interface. The real-time state of the AUTO pin is read at bit 0 in the Pin Status register (11h). Internally pulled down to DGND. Must be tied locally to either V_{DD} or DGND.

$\overline{\text{MSD}}$: Maskable Shutdown Input. Active low. When pulled low, all ports that have their corresponding mask bit set in the Misc Config register (17h) will be reset, equivalent to pulling the $\overline{\text{SHDN}}$ pin low. Internal filtering of the $\overline{\text{MSD}}$ pin prevents glitches less than 1µs wide from resetting ports. Internally pulled up to V_{DD}.

OPERATION

Overview

Power over Ethernet, or PoE, is a standard protocol for sending DC power over copper Ethernet data wiring. The IEEE group that administers the 802.3 Ethernet data standards added PoE powering capability in 2003. This original PoE spec, known as 802.3af, allowed for 48V DC power at up to 13W. This initial spec was widely popular, but 13W was not adequate for some requirements. In 2009, the IEEE released a new standard, known as 802.3at or PoE+, increasing the voltage and current requirements to provide 25W of power.

The IEEE standard also defines PoE terminology. A device that provides power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: Endpoints (typically network switches or routers), which provide data and power; and Midspans, which provide power but pass through data. Midspans are typically used to add PoE capability to existing non-PoE networks. PDs are typically IP phones, wireless access points, security cameras, and similar devices, but could be nearly anything that runs from 25W or less and includes an RJ45-style network connector.

The LTC4266 is a third-generation quad PSE controller that implements four PSE ports in either an endpoint or midspan design. Virtually all necessary circuitry is included to implement a IEEE 802.3at compliant PSE design, requiring only an external power MOSFET and sense resistor per channel; these minimize power loss compared to alternative designs with on-board MOSFETs and increase system reliability in the event a single channel is damaged.

PoE Basics

Common Ethernet data connections consist of two or four twisted pairs of copper wire (commonly known as CAT-5 cable), transformer-coupled at each end to avoid ground loops. PoE systems take advantage of this coupling arrangement by applying voltage between the center-taps of the data transformers to transmit power from the PSE to the PD without affecting data transmission. Figure 10 shows a high-level PoE system schematic.

To avoid damaging legacy data equipment that does not expect to see DC voltage, the PoE spec defines a protocol that determines when the PSE may apply and remove power. Valid PDs are required to have a specific 25k common-mode resistance at their input. When such a PD is connected to the cable, the PSE detects this signature resistance and turns on the power. When the PD is later

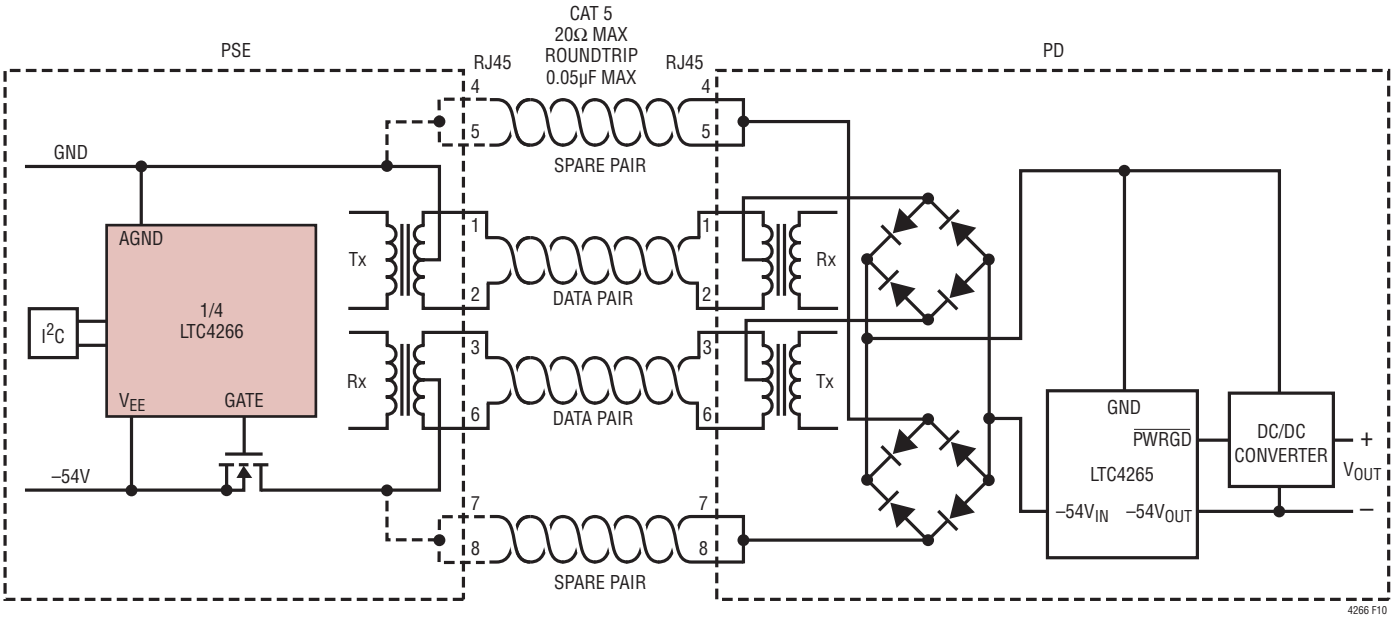


Figure 10. Power Over Ethernet System Diagram

OPERATION

disconnected, the PSE senses the open circuit and turns power off. The PSE also turns off power in the event of a current fault or short circuit.

When a PD is detected, the PSE optionally looks for a classification signature that tells the PSE the maximum power the PD will draw. The PSE can use this information to allocate power among several ports, police the current consumption of the PD, or to reject a PD that will draw more power that the PSE has available. The classification step is optional; if a PSE chooses not to classify a PD, it must assume that the PD is a 13W (full 802.3af power) device.

New in 802.3at

The newer 802.3at standard supersedes 802.3af and brings several new features:

- A PD may draw as much as 25.5W. Such PDs (and the PSEs that support them) are known as Type 2. Older 13W 802.3af equipment is classified as Type 1. Type 1 PDs will work with all PSEs; Type 2 PDs may require Type 2 PSEs to work properly. The LTC4266 is designed to work in both Type 1 and Type 2 PSE designs, and also supports non-standard configurations at higher power levels.
- The Classification protocol is expanded to allow Type 2 PSEs to detect Type 2 PDs, and to allow Type 2 PDs to determine if they are connected to a Type 2 PSE. Two versions of the new Classification protocol are available: an expanded version of the 802.3af Class Pulse protocol, and an alternate method integrated with the existing LLDP protocol (using the Ethernet data path). The LTC4266 fully supports the new Class Pulse protocol and is also compatible with the LLDP protocol (which is implemented in the data communications layer, not in the PoE circuitry).
- Fault protection current levels and timing are adjusted to reduce peak power in the MOSFET during a fault; this allows the new 25.5W power levels to be reached using the same MOSFETs as older 13W designs.

BACKWARDS COMPATIBILITY

The LTC4266 is designed to be backward compatible with earlier PSE chips in both software and pin functions. Existing systems using either the LTC4258 or LTC4259A (or compatible) devices can be substituted with the LTC4266 without software or PCB layout changes; only minor BOM changes are required to implement a fully compliant 802.3at design.

Because of the backwards compatibility features, some of the internal registers are redundant or unused when the LTC4266 is operated as recommended. For more details on usage in compatibility mode, refer to the LTC4258/ LTC4259A device data sheets.

Special Compatibility Mode Notes

- The LTC4266 can use either 0.5Ω or 0.25Ω sense resistors, while the LTC425x chips always used 0.5Ω. To maintain compatibility, if the AUTO pin is low when the LTC4266 powers up it assumes the sense resistor is 0.5Ω; if it is high at power up, the LTC4266 assumes 0.25Ω. The resistor value setting can be reconfigured at any time after power up. In particular, systems that use 0.25Ω sense resistors and have AUTO tied low must reconfigure the resistor settings after power up.
- The LTC4259A included both AC and DC disconnect sensing circuitry, but the LTC4266 has only DC disconnect sensing. For the sake of compatibility, register bits used to enable AC disconnect in the LTC4259A are implemented in the LTC4266, but they simply mirror the bits used for DC disconnect.
- The LTC4258 and LTC4259A required 10k resistors between the OUTn pins and the drains of the external MOSFETs. These resistors must be shorted or replaced with zero ohm jumpers when using the LTC4266.
- The LTC4258 and LTC4259A included a BYP pin, decoupled to AGND with 0.1µF. This pin changes to the MID pin on the LTC4266. The capacitor should be removed for Endspan applications, or replaced with a zero ohm jumper for Midspan applications.

APPLICATIONS INFORMATION

Operating Modes

The LTC4266 includes four independent ports, each of which can operate in one of four modes: manual, semi-auto, AUTO pin or shutdown.

Table 1. Operating Modes

MODE	AUTO PIN	OPMD	DETECT/ CLASS	POWER-UP	AUTOMATIC I_{CUT}/I_{LIM} ASSIGNMENT
AUTO Pin	1	11b	Enabled at Reset	Automatically	Yes
Reserved	0	11b	N/A	N/A	N/A
Semi-auto	0	10b	Host Enabled	Upon Request	No
Manual	0	01b	Once Upon Request	Upon Request	No
Shutdown	0	00b	Disabled	Disabled	No

- In manual mode, the port waits for instructions from the host system before taking any action. It runs a single detection or classification cycle when commanded to by the host, and reports the result in its Port Status register. The host system can command the port to turn on or off the power at any time. This mode should only be used for diagnostic and test purposes.
- In semi-auto mode, the port repeatedly attempts to detect and classify any PD attached to it. It reports the status of these attempts back to the host, and waits for a command from the host before turning on power to the port. The host must enable detection (and optionally classification) for the port before detection will start.
- AUTO pin mode operates the same as semi-auto mode except that it will automatically turn on the power to the port if detection is successful. In AUTO pin mode, I_{CUT} and I_{LIM} values are set automatically by the LTC4266. This operational mode is only valid if the AUTO pin is high at reset or power-up and remains high during operation.
- In shutdown mode, the port is disabled and will not detect or power a PD.

Regardless of which mode it is in, the LTC4266 will remove power automatically from any port that generates a current limit fault. It will also automatically remove power from any port that generates a disconnect event if disconnect detection is enabled. The host controller may also command the port to remove power at any time.

Reset and the AUTO/MID Pins

The initial LTC4266 configuration depends on the state of the AUTO and MID pins during reset. Reset occurs at power-up, or whenever the $\overline{\text{RESET}}$ pin is pulled low or the global Reset All bit is set. Changing the state of AUTO or MID after power-up will not properly change the port behavior of the LTC4266 until a reset occurs.

Although typically used with a host controller, the LTC4266 can also be used in a standalone mode with no connection to the serial interface. If there is no host present, the AUTO pin must be tied high so that, at reset, all ports will be configured to operate automatically. Each port will detect and classify repeatedly until a PD is discovered, set I_{CUT} and I_{LIM} according to the classification results, apply power after successful detection, and remove power when a PD is disconnected. Similarly, if the standalone application is a midspan, the MID pin must be tied high to enable correct midspan detection timing.

Table 2 shows the I_{CUT} and I_{LIM} values that will be automatically set in AUTO pin mode, based on the discovered class.

Table 2. I_{CUT} and I_{LIM} Values in AUTO pin mode

CLASS	I_{CUT}	I_{LIM}
Class 1	112mA	425mA
Class 2	206mA	425mA
Class 3 or Class 0	375mA	425mA
Class 4	638mA	850mA

The automatic setting of the I_{CUT} and I_{LIM} values only occurs if the LTC4266 is reset with the AUTO pin high.

APPLICATIONS INFORMATION

DETECTION

Detection Overview

To avoid damaging network devices that were not designed to tolerate DC voltage, a PSE must determine whether the connected device is a real PD before applying power. The IEEE specification requires that a valid PD have a common-mode resistance of 25k ±5% at any port voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k (shaded regions in Figure 11). The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer network ports, many of which have 150Ω common-mode termination resistors that will be damaged if power is applied to them (the black region at the left of Figure 11).

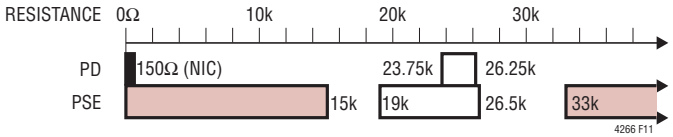


Figure 11. IEEE 802.3af Signature Resistance Ranges

4-Point Detection

The LTC4266 uses a 4-point detection method to discover PDs. False-positive detections are minimized by checking for signature resistance with both forced-current and forced-voltage measurements. Initially, two test currents are forced onto the port (via the OUTn pin) and the resulting voltages are measured. The detection circuitry subtracts the two V-I points to determine the resistive slope while removing offset caused by series diodes or leakage at the port (see Figure 12). If the forced-current detection yields a valid signature resistance, two test voltages are then forced onto the port and the resulting currents are measured and subtracted. Both methods must report valid resistances for the port to report a valid detection. PD signature resistances between 17k and 29k (typically) are detected as valid and reported as Detect Good in the corresponding Port Status register. Values outside this range, including open and short circuits, are also reported. If the port measures less than 1V at the first forced-current test, the detection cycle will abort and Short Circuit will be reported. Table 3 shows the possible detection results.

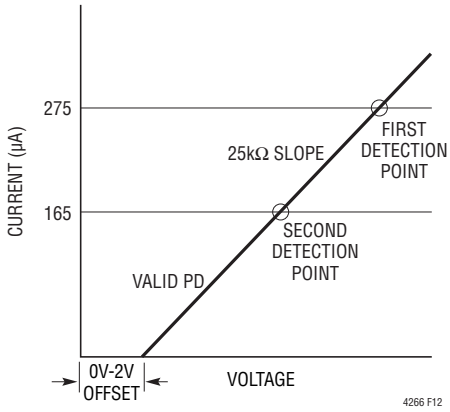


Figure 12. PD Detection

Table 3. Detection Status

MEASURED PD SIGNATURE	DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
<2.4k	Short Circuit
Capacitance > 2.7μF	C_{PD} too High
2.4k < R_{PD} < 17k	R_{SIG} too Low
17k < R_{PD} < 29k	Detect Good
>29k	R_{SIG} too High
>50k	Open Circuit
Voltage > 10V	Port Voltage Outside Detect Range

Operating Modes

The port's operating mode determines when the LTC4266 runs a detection cycle. In manual mode, the port will idle until the host orders a detect cycle. It will then run detection, report the results, and return to idle to wait for another command.

In semi-auto mode, the LTC4266 autonomously polls a port for PDs, but it will not apply power until commanded to do so by the host. The Port Status register is updated at the end of each detection cycle. If a valid signature resistance is detected and classification is enabled, the port will classify the PD and report that result as well. The port will then wait for at least 100ms (or 2 seconds if midspan mode is enabled), and will repeat the detection cycle to ensure that the data in the port status register is up-to-date.

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If the port is in semi-auto mode and high power operation is enabled, the port will not turn on in response to a power-on command unless the current detect result is Detect Good. Any other detect result will generate a t_{START} fault if a power-on command is received. If the port is not in high power mode, it will ignore the detection result and apply power when commanded, maintaining backwards compatibility with the LTC4259A.

Behavior in AUTO pin mode is similar to semi-auto; however, after Detect Good is reported and the port is classified (if classification is enabled), it is automatically powered on without further intervention. In AUTO pin mode, the I_{CUT} and I_{LIM} thresholds are automatically set; see the Reset and the AUTO/MID Pins section for more information.

The signature detection circuitry is disabled when the port is initially powered up with the AUTO pin low, in shutdown mode, or when the corresponding detect enable bit is cleared.

Detection of Legacy PDs

Proprietary PDs that predate the original IEEE 802.3af standard are commonly referred to today as legacy devices. One type of legacy PD uses a large common-mode capacitance (>10µF) as the detection signature. Note that PDs in this range of capacitance are defined as invalid, so a PSE that detects legacy PDs is technically noncompliant with the IEEE spec.

The LTC4266 can be configured to detect this type of legacy PD. Legacy detection is disabled by default, but can be manually enabled on a per-port basis. When enabled, the port will report detect good when it sees either a valid IEEE PD or a high-capacitance legacy PD. With legacy mode disabled, only valid IEEE PDs will be recognized.

CLASSIFICATION

802.3af Classification

A PD can optionally present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage

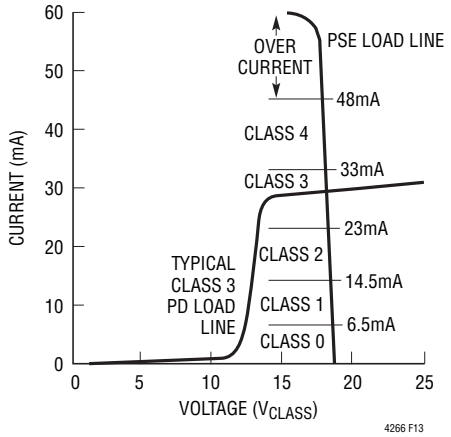

Figure 13. PD Classification

is in the V_{CLASS} range (between 15.5V and 20.5V), with the current level indicating one of 5 possible PD classes. Figure 13 shows a typical PD load line, starting with the slope of the 25kΩ signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the V_{CLASS} range. Table 4 shows the possible classification values.

Table 4. Classification Values

CLASS	RESULT
Class 0	No Class Signature Present; Treat Like Class 3
Class 1	3W
Class 2	7W
Class 3	13W
Class 4	25.5W (Type 2)

If classification is enabled, the port will classify the PD immediately after a successful detection cycle in semi-auto or AUTO pin modes, or when commanded to in manual mode. It measures the PD classification signature by applying 18V for 12ms (both values typical) to the port via the OUT*n* pin and measuring the resulting current; it then reports the discovered class in the port status register. If the LTC4266 is in AUTO pin mode, it will additionally use the classification result to set the I_{CUT} and I_{LIM} thresholds. See the Reset and the AUTO/MID Pins section for more information.

The classification circuitry is disabled when the port is initially powered up with the AUTO pin low, in shutdown mode, or when the corresponding class enable bit is cleared.

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802.3at 2-Event Classification

The 802.3at spec defines two methods of classifying a Type 2 PD.

One method adds extra fields to the Ethernet LLDP data protocol; although the LTC4266 is compatible with this classification method, it cannot perform classification directly since it doesn't have access to the data path. LLDP classification requires the PSE to power the PD as a standard 802.3af (Type 1) device. It then waits for the host to perform LLDP communication with the PD and update the PSE port data. The LTC4266 supports changing the I_{LIM} and I_{CUT} levels on the fly, allowing the host to complete LLDP classification.

The second 802.3at classification method, known as 2-event classification or ping-pong, is fully supported by the LTC4266. A Type 2 PD that is requesting more than 13W will indicate Class 4 during normal 802.3af classification. If the LTC4266 sees Class 4, it forces the port to a specified lower voltage (called the mark voltage, typically 9V), pauses briefly, and then re-runs classification to verify the Class 4 reading (Figure 1). It also sets a bit in the High Power Status register to indicate that it ran the second classification cycle. The second cycle alerts the PD that it is connected to a Type 2 PSE which can supply Type 2 power levels.

2-event ping-pong classification is enabled by setting a bit in the port's High Power Mode register. Note that a ping-pong enabled port only runs the second classification cycle when it detects a Class 4 device; if the first cycle returns Class 0 to 3, the port assumes it is connected to a Type 1 PD and does not run the second classification cycle.

Invalid Type 2 Class Combinations

The 802.3at spec defines a Type 2 PD class signature as two consecutive Class 4 results; a Class 4 followed by a Class 0-3 is not a valid signature. In AUTO pin mode, the LTC4266 will power a detected PD regardless of the classification results, with one exception: if the PD presents an invalid Type 2 signature (Class 4 followed by Class 0 to 3), the LTC4266 will not provide power and will restart the detection process. To aid in diagnosis, the Port Status register will always report the results of the last class pulse, so an invalid Class 4–Class 2 combination would report a second class pulse was run in the High Power Status register (which implies that the first cycle found Class 4), and Class 2 in the Port Status register.

POWER CONTROL

External MOSFET, Sense R Summary

The primary function of the LTC4266 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage of an external power MOSFET while monitoring the current via an external sense resistor and the output voltage at the OUT pin. This circuitry serves to couple the raw V_{EE} input supply to the port in a controlled manner that satisfies the PD's power needs while minimizing power dissipation in the MOSFET and disturbances on the V_{EE} backplane.

The LTC4266 is designed to use 0.25Ω sense resistors to minimize power dissipation. It also supports 0.5Ω sense resistors, which are the default when LTC4258/LTC4259A compatibility is desired.

Inrush Control

Once the command has been given to turn on a port, the LTC4266 ramps up the GATE pin of that port's external MOSFET in a controlled manner. Under normal power-up circumstances, the MOSFET gate will rise until the port current reaches the inrush current limit level (typically 450mA), at which point the GATE pin will be servoed to maintain the specified I_{INRUSH} current. During this inrush period, a timer (t_{START}) runs. When output charging is complete, the port current will fall and the GATE pin will be allowed to continue rising to fully enhance the MOSFET and minimize its on-resistance. The final V_{GS} is nominally 12V. If the t_{START} timer expires before the inrush period completes, the port will be turned back off and a t_{START} fault reported.

Current Limit

Each LTC4266 port includes two current limiting thresholds (I_{CUT} and I_{LIM}), each with a corresponding timer (t_{CUT} and t_{LIM}). Setting the I_{CUT} and I_{LIM} thresholds depends

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on several factors: the class of the PD, the voltage of the main supply (V_{EE}), the type of PSE (1 or 2), the sense resistor (0.5Ω or 0.25Ω), the SOA of the MOSFET, and whether or not the system is required to implement class enforcement.

Per the IEEE spec, the LTC4266 will allow the port current to exceed I_{CUT} for a limited period of time before removing power from the port, whereas it will actively control the MOSFET gate drive to keep the port current below I_{LIM}. The port does not take any action to limit the current when only the I_{CUT} threshold is exceeded, but does start the t_{CUT} timer. The t_{LIM} timer starts when the I_{LIM} threshold is exceeded and current limit is active. If the current drops below the I_{CUT} current threshold before its timer expires, the t_{CUT} timer counts back down, but at 1/16 the rate that it counts up. This allows the current limit circuitry to tolerate intermittent overload signals with duty cycles below about 6%; longer duty cycle overloads will turn the port off.

I_{CUT} is typically set to a lower value than I_{LIM} to allow the port to tolerate minor faults without current limiting.

Per the IEEE specification, the LTC4266 will automatically set I_{LIM} to 425mA (shown in bold in Table 5) during inrush at port turn-on, and then switch to the programmed I_{LIM} setting once inrush has completed. To maintain IEEE compliance, I_{LIM} should kept at 425mA for all Type 1 PDs, and 850mA if a Type 2 PD is detected. I_{LIM} is automatically reset to 425mA when a port turns off.

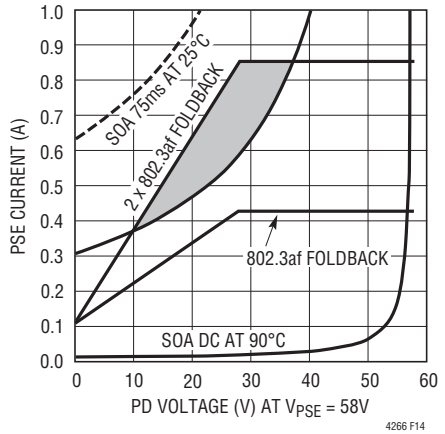

Figure 14. Turn On Currents vs FET Safe Operating Area at 90°C Ambient

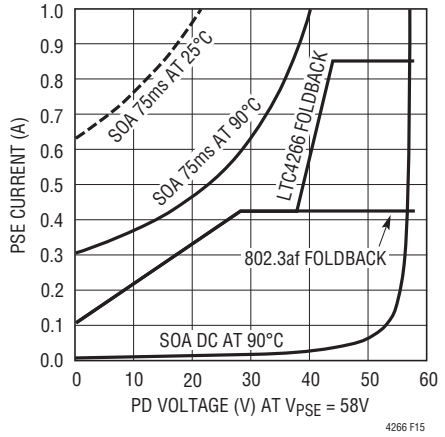

Figure 15. LTC4266 Foldback vs FET Safe Operating Area at 90°C Ambient

Table 5. Example Current Limit Settings

	INTERNAL REGISTER SETTING (hex)	
I_{LIM} (mA)	R_{SENSE} = 0.5Ω	R_{SENSE} = 0.25Ω
53	88	
106	08	88
159	89	
213	80	08
266	8A	
319	09	89
372	8B	
425	**00**	**80**
478	8E	
531	92	8A
584	CB	
638	10	90
744	D2	9A
850	**40**	**C0**
956	4A	CA
1063	50	D0
1169	5A	DA
1275	60	E0
1488	52	49
1700		40
1913		4A
2125		50
2338		5A
2550		60
2975		52

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I_{LIM} Foldback

The LTC4266 features a two-stage foldback circuit that reduces the port current if the port voltage falls below the normal operating voltage. This keeps MOSFET power dissipation at safe levels for typical 802.3af MOSFETs, even at extended 802.3at power levels. Current limit and foldback behavior are programmable on a per-port basis. Figure 14 shows MOSFET power dissipation with 802.3af-style foldback compared with a typical MOSFET SOA curve; Figure 15 demonstrates how two-stage foldback keeps the FET within its SOA under the same conditions. Table 5 gives examples of recommended I_{LIM} register settings.

The LTC4266 will support current levels well beyond the maximum values in the 802.3at specification. The shaded areas in Table 5 indicate settings that may require a larger external MOSFET, additional heat sinking, or a reduced t_{LIM} setting.

MOSFET Fault Detection

LTC4266 PSE ports are designed to tolerate significant levels of abuse, but in extreme cases it is possible for the external MOSFET to be damaged. A failed MOSFET may short source to drain, which will make the port appear to be on when it should be off; this condition may also cause the sense resistor to fuse open, turning off the port but causing the LTC4266 SENSE pin to rise to an abnormally high voltage. A failed MOSFET may also short from gate to drain, causing the LTC4266 GATE pin to rise to an abnormally high voltage. The LTC4266 SENSE and GATE pins are designed to tolerate up to 80V faults without damage.

If the LTC4266 sees any of these conditions for more than 180µs, it disables all port functionality, reduces the gate drive pull-down current for the port and reports a FET Bad fault. This is typically a permanent fault, but the host can attempt to recover by resetting the port, or by resetting the entire chip if a port reset fails to clear the fault. If the MOSFET is in fact bad, the fault will quickly return, and the port will disable itself again. The remaining ports of the LTC4266 are unaffected.

An open or missing MOSFET will not trigger a FET Bad fault, but will cause a t_{START} fault if the LTC4266 attempts to turn on the port.

Voltage and Current Readback

The LTC4266 measures the output voltage and current at each port with an internal A/D converter. Port data is only valid when the port power is on. The converter has two modes:

- Slow mode: 14 samples per second, 14.5 bits resolution
- Fast mode: 440 samples per second, 9.5 bits resolution

In fast mode, the least significant 5 bits of the lower byte are zeroes so that bit scaling is the same in both modes.

Disconnect

The LTC4266 monitors the port to make sure that the PD continues to draw the minimum specified current. A disconnect timer counts up whenever port current is below 7.5mA (typ), indicating that the PD has been disconnected. If the t_{DIS} timer expires, the port will be turned off and the disconnect bit in the fault event register will be set. If the current returns before the t_{DIS} timer runs out, the timer resets and will start counting from the beginning if the undercurrent condition returns. As long as the PD exceeds the minimum current level more often than t_{DIS}, it will stay powered.

Although not recommended, the DC disconnect feature can be disabled by clearing the corresponding DC Disconnect Enable bits. Note that this defeats the protection mechanisms built into the IEEE spec, since a powered port will stay powered after the PD is removed. If the still-powered port is subsequently connected to a non-PoE data device, the device may be damaged.

The LTC4266 does not include AC disconnect circuitry, but includes AC disconnect enable bits to maintain compatibility with the LTC4259A. If the AC Disconnect Enable bits are set, DC disconnect will be used.

Shutdown Pins

The LTC4266 includes a hardware $\overline{SHDN}$ pin for each port. When a $\overline{SHDN}$ pin is pulled to DGND, the corresponding port will be shut off immediately. The port remains shut down until re-enabled via I^2C or a device reset in AUTO pin mode.

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Masked Shutdown

The LTC4266 provides a low latency port shedding feature to quickly reduce the system load when required. By allowing a pre-determined set of ports to be turned off, the current on an overloaded main power supply can be reduced rapidly while keeping high priority devices powered. Each port can be configured to high or low priority; all low-priority ports will shut down within 6.5µs after the MSD pin is pulled low. If multiple ports in a LTC4266 device are shut down via MSD, they are staggered by at least 0.55µs to help reduce voltage transients on the main supply. If a port is turned off via MSD, the corresponding detection and classification enable bits are cleared, so the port will remain off until the host explicitly re-enables detection.

SERIAL DIGITAL INTERFACE

Overview

The LTC4266 communicates with the host using a standard SMBus/I^2C 2-wire interface. The LTC4266 is a slave-only device, and communicates with the host master using the standard SMBus protocols. Interrupts are signaled to the host via the $\overline{INT}$ pin. The timing diagrams (Figures 5 through 9) show typical communication waveforms and their timing relationships. More information about the SMBus data protocols can be found at www.smbus.org.

The LTC4266 requires both the V_{DD} and V_{EE} supply rails to be present for the serial interface to function.

Bus Addressing

The LTC4266's primary serial bus address is 010xxxxb, with the lower four bits set by the AD3-AD0 pins; this allows up to 16 LTC4266s on a single bus. All LTC4266s also respond to the address 0110000b, allowing the host to write the same command (typically configuration commands) to multiple LTC4266s in a single transaction. If the LTC4266 is asserting the $\overline{INT}$ pin, it will also respond to the alert response address (0001100b) per the SMBus spec.

Interrupts and SMBALERT

Most LTC4266 port events can be configured to trigger an interrupt, asserting the $\overline{INT}$ pin and alerting the host to the event. This removes the need for the host to poll the LTC4266, minimizing serial bus traffic and conserving host CPU cycles. Multiple LTC4266s can share a common $\overline{INT}$ line, with the host using the SMBALERT protocol (ARA) to determine which LTC4266 caused an interrupt.

Register Description

For information on serial bus usage and device configuration and status, refer to the LTC4266 Software Programming documentation.

EXTERNAL COMPONENT SELECTION

Power Supplies and Bypassing

The LTC4266 requires two supply voltages to operate. V_{DD} requires 3.3V (nominally) relative to DGND. V_{EE} requires a negative voltage of between –45V and –57V for Type 1 PSEs, or –51V to –57V for Type 2 PSEs, relative to AGND. The relationship between the two grounds is not fixed; AGND can be referenced to any level from V_{DD} to DGND, although it should typically be tied to either V_{DD} or DGND.

V_{DD} provides power for most of the internal LTC4266 circuitry, and draws a maximum of 3mA. A ceramic decoupling cap of at least 0.1µF should be placed from V_{DD} to DGND, as close as practical to each LTC4266 chip.

Figure 16 shows a three component low dropout regulator for a negative supply to DGND generated from the negative V_{EE} supply. V_{DD} is tied to AGND and DGND is

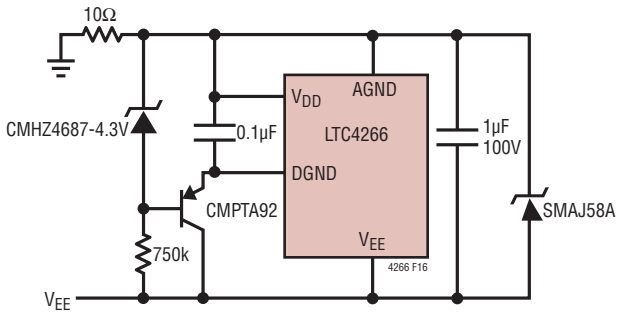

Figure 16. Negative LDO to DGND

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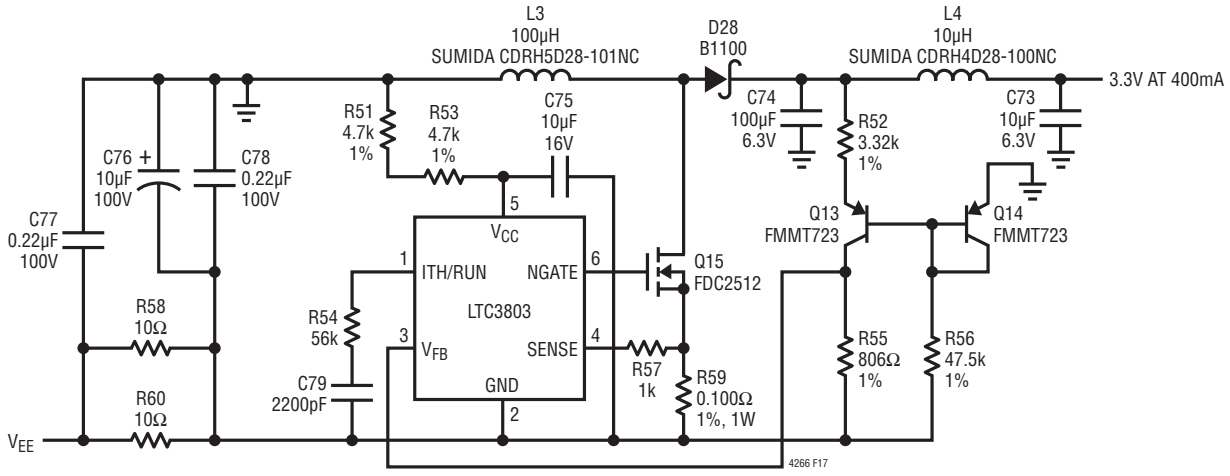

Figure 17. Positive V_{DD} Boost Converter

negative referenced to AGND. This regulator drives a single LTC4266 device. In Figure 17, DGND is tied to AGND in this boost converter circuit for a positive V_{DD} supply of 3.3V above AGND. This circuit can drive multiple LTC4266 devices and opto couplers.

V_{EE} is the main supply that provides power to the PDs. Because it supplies a relatively large amount of power and is subject to significant current transients, it requires more design care than a simple logic supply. For minimum IR loss and best system efficiency, set V_{EE} near maximum amplitude (57V), leaving enough margin to account for transient over- or undershoot, temperature drift, and the line regulation specs of the particular power supply used.

Bypass capacitance between AGND and V_{EE} is very important for reliable operation. If a short circuit occurs at one of the output ports it can take as long as 1µs for the LTC4266 to begin regulating the current. During this time the current is limited only by the small impedances in the circuit and a high current spike typically occurs, causing a voltage transient on the V_{EE} supply and possibly causing the LTC4266 to reset due to a UVLO fault. A 1µF, 100V X7R capacitor placed near the V_{EE} pin is recommended to minimize spurious resets.

Isolating the Serial Bus

The LTC4266 includes a split SDA pin (SDAIN and SDAOUT) to ease opto-isolation of the bidirectional SDA line.

IEEE 802.3 Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, network segments are not required to be isolated from each other, provided that the segments are connected to devices residing within a single building on a single power distribution system.

For simple devices such as small PoE switches, the isolation requirement can be met by using an isolated main power supply for the entire device. This strategy can be used if the device has no electrically conducting ports other than twisted-pair Ethernet. In this case, the SDAIN and SDAOUT pins can be tied together and will act as a standard I^2C/SMBus SDA pin.

If the device is part of a larger system, contains additional external non-Ethernet ports, or must be referenced to protective ground for some other reason, the Power over Ethernet subsystem (including all LTC4266s) must be

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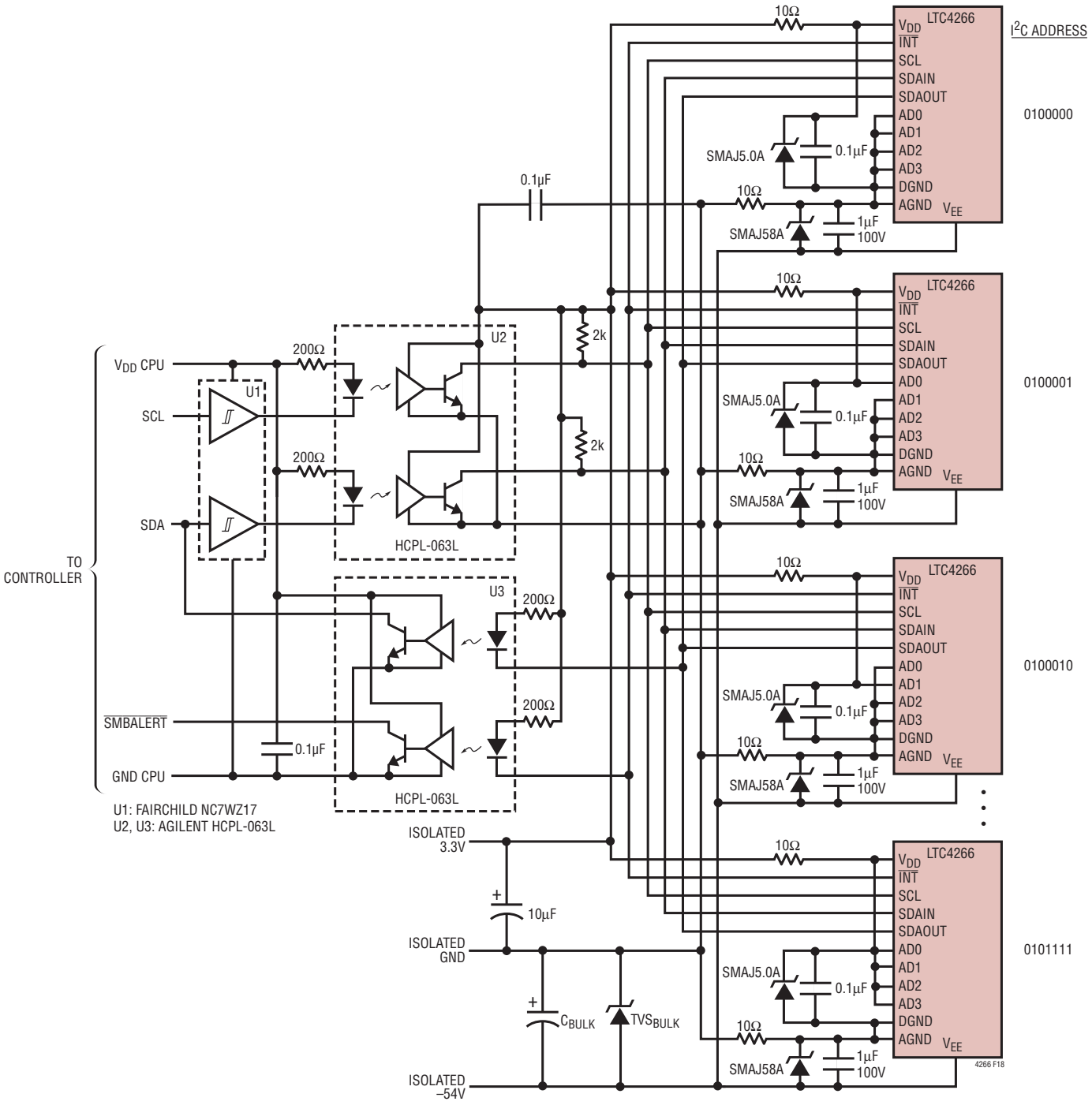

Figure 18. Opto-Isolating the I²C Bus

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electrically isolated from the rest of the system. Figure 18 shows a typical isolated serial interface. The SDAOUT pin of the LTC4266 is designed to drive the inputs of an opto-coupler directly. Standard I^2C/SMBus devices typically cannot drive opto-couplers, so U1 is used to buffer the signals from the host controller side.

External MOSFET

Careful selection of the power MOSFET is critical to system reliability. LTC recommends either Fairchild IRFM120A, FDT3612, FDMC3612 or Philips PHT6NQ10T for their proven reliability in Type 1 and Type 2 PSE applications. Non-standard applications that provide more current than the 850mA IEEE maximum may require heat sinking and other MOSFET design considerations. Contact LTC Applications before using a MOSFET other than one of these recommended parts.

Sense Resistor

The LTC4266 is designed to use either 0.5Ω or 0.25Ω current sense resistors. For new designs 0.25Ω is recommended to reduce power dissipation; the 0.5Ω option is intended for existing systems where the LTC4266 is used as a drop-in replacement for the LTC4258 or LTC4259A. The lower sense resistor values reduce heat dissipation. Four commonly available 1Ω resistors (0402 or larger package size) can be used in parallel in place of a single 0.25Ω resistor. In order to meet the I_{CUT} and I_{LIM} accuracy required by the IEEE specification, the sense resistors should have ±1% tolerance or better, and no more than ±200ppm/°C temperature coefficient.

Output Cap

Each port requires a 0.22µF cap across its outputs to keep the LTC4266 stable while in current limit during startup or overload. Common ceramic capacitors often have significant voltage coefficients; this means the capacitance is reduced as the applied voltage increases. To minimize this problem, X7R ceramic capacitors rated for at least 100V are recommended.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 19, are required at the main supply, at the LTC4266 pins, and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply and should be sized to accommodate system level surge requirements. A large capacitance of 10µF or greater (C3) is required across the +3.3V supply if V_{DD} is above AGND.

Each LTC4266 requires a 10Ω, 0805 resistor (R1) in series from supply AGND to the LTC4266 AGND pin. Across the LTC4266 AGND pin and V_{EE} pin are an SMAJ58A, 58V TVS (D1) and a 1µF, 100V bypass capacitor (C1). These components must be placed close to the LTC4266 pins.

If the V_{DD} supply is above AGND, each LTC4266 requires a 10Ω, 0805 resistor (R2) in series from the +3.3V supply positive rail to the LTC4266 V_{DD} pin. Across the LTC4266

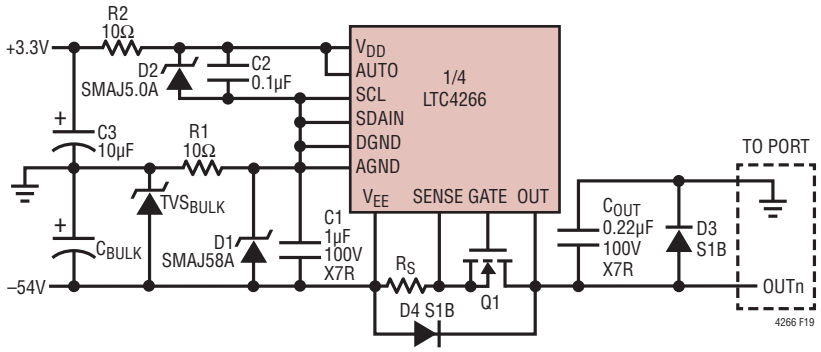

Figure 19. LTC4266 Surge Protection

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V_{DD} pin and DGND pin are an SMAJ5.0A, 5.0V TVS (D2) and a 0.1µF capacitor (C2). These components must be placed close to the LTC4266 pins. DGND is tied directly to the protected AGND pin. Pull-ups at the logic pins should be to the protected side of the 10Ω resistors at the V_{DD} pin. Pull-downs at the logic pins should be to the protected side of the 10Ω resistors at the tied AGND and DGND pins.

Finally, each port requires a pair of S1B clamp diodes, one from OUTn to supply AGND (D3) and one from OUTn to supply V_{EE} (D4). The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance.

Further considerations include LTC4266 applications with off-board connections, such as a daughter card to a mother board or headers to an external supply or host control board. Additional protection may be required at the LTC4266 pins to these off-board connections.

LAYOUT GUIDELINES

Standard power layout guidelines apply to the LTC4266: place the decoupling caps for the V_{DD} and V_{EE} supplies near their respective supply pins, use ground planes, and use wide traces wherever there are significant currents.

The main layout challenge involves the arrangement of the current sense resistors, and their connections to the LTC4266. Because the sense resistor values are very low, layout parasitics can cause significant errors. Care is required to achieve specified accuracy, particularly with disconnect currents.

Figure 20 illustrates the problem. In the example on the left, two ports have load currents I_1 and I_2 that return to the V_{EE} power supply through a mutual resistance R_M. R_M represents the combined resistances of any traces, planes, and vias in the PCB that I_1 and I_2 share as they return to the V_{EE} supply. The LTC4266 measures the voltage difference between its SENSE and V_{EE} pins to sense the voltage drop across R_{S1}, but as the example shows, R_M introduces errors.

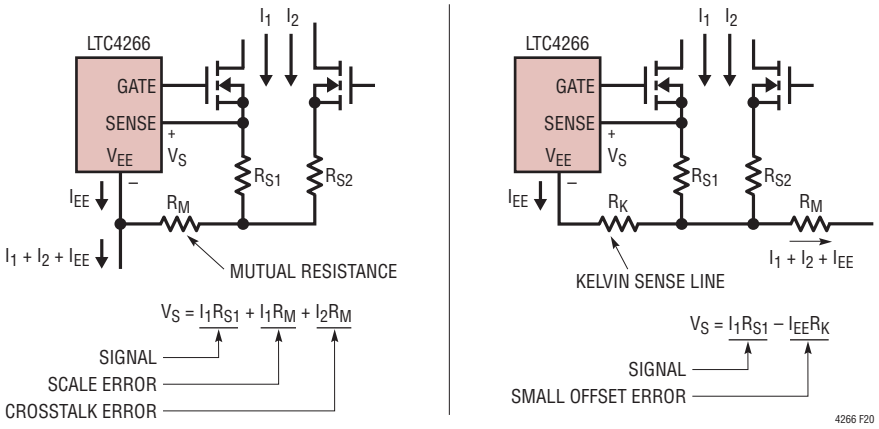

Figure 20. Layout Affects Current Readback Accuracy

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The example on the right shows how errors can be minimized with a good layout. The circuit is rearranged so that R_M no longer affects V_S, and the V_{EE} connection to the LTC4266 is used as a Kelvin sense trace. V_{EE} is not a perfect Kelvin connection because all four ports controlled by the LTC4266 share the same sense trace, and because the current through the trace (I_{EE}) is not zero. However, as the equation shows, the remaining error is a small offset term.

Figure 21 shows two LTC4266 chips controlling eight ports (A though H). The ports are separated into two groups of four; each has its own trace on the top PCB layer that connects to the V_{EE} plane with a via. Currents from the U1 sub-circuit are effectively isolated from the U2 sub-circuit, reducing the layout problem down to 4-port chunks; this arrangement can be expanded for any number of ports.

Figure 22 shows an example of good 4-port layout. Each 0.25Ω sense resistor consists of four 1Ω resistors in parallel. The four groups of resistors are arranged to minimize the overlap in their current flows, which minimizes mutual resistance. The horizontal slits cut in the copper help to keep the currents separate. Wide copper paths connect each group of resistors to the vias at the center, so the resistance is very low.

Proper connection of the sense line is also important. In Figure 22, U1 is not connected directly to the V_{EE} plane but is connected instead to a Kelvin sense trace that leads to the sense resistor array. Similarly, the via at the center of the sense resistor array has a matching hole in the V_{EE} plane. This arrangement prevents the mutual resistance of the four large vias from influencing the current measurements.

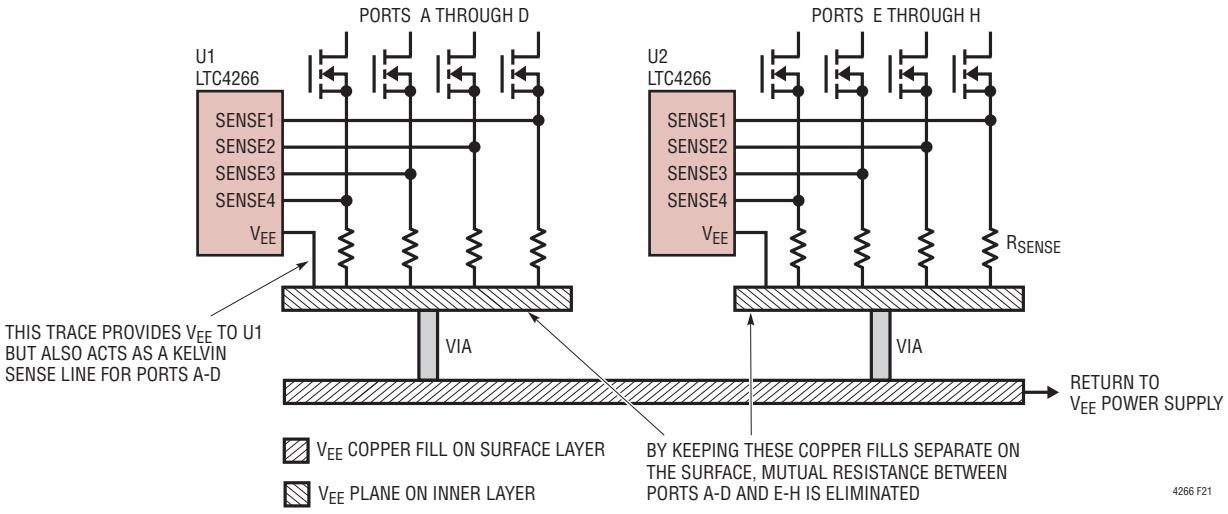


Figure 21. Layout Strategy to Reduce Mutual Resistance

APPLICATIONS INFORMATION

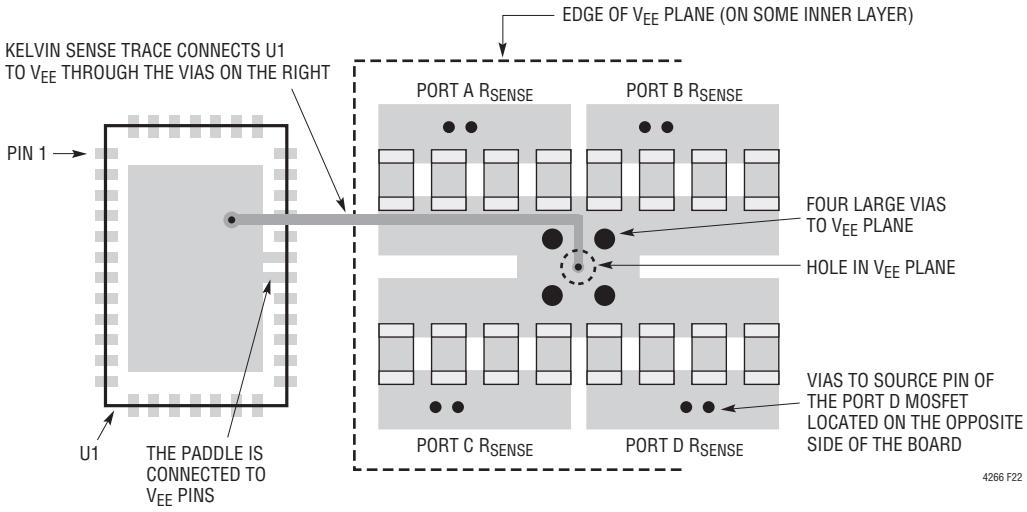
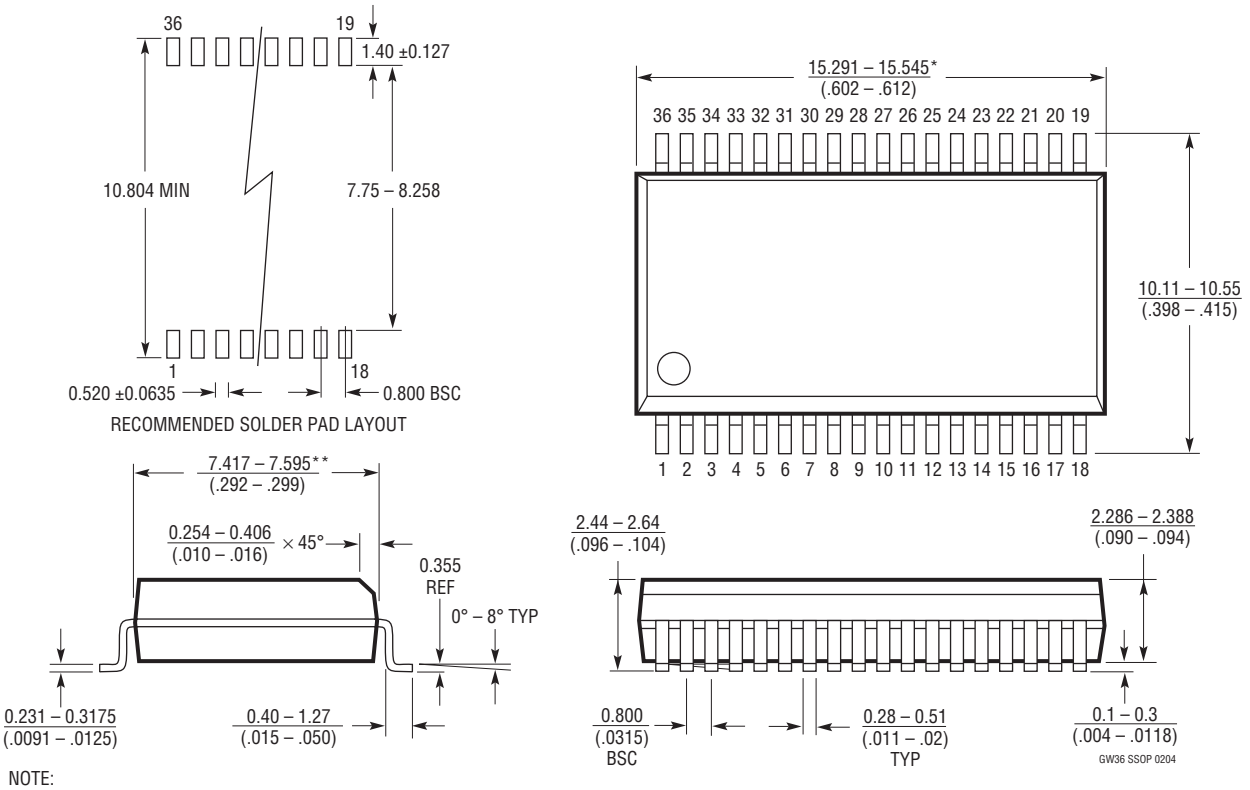


Figure 22. Good PCB Layout Example

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4266#packaging for the most recent package drawings.

GW Package
36-Lead Plastic SSOP (Wide .300 Inch)
(Reference LTC DWG # 05-08-1642)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$

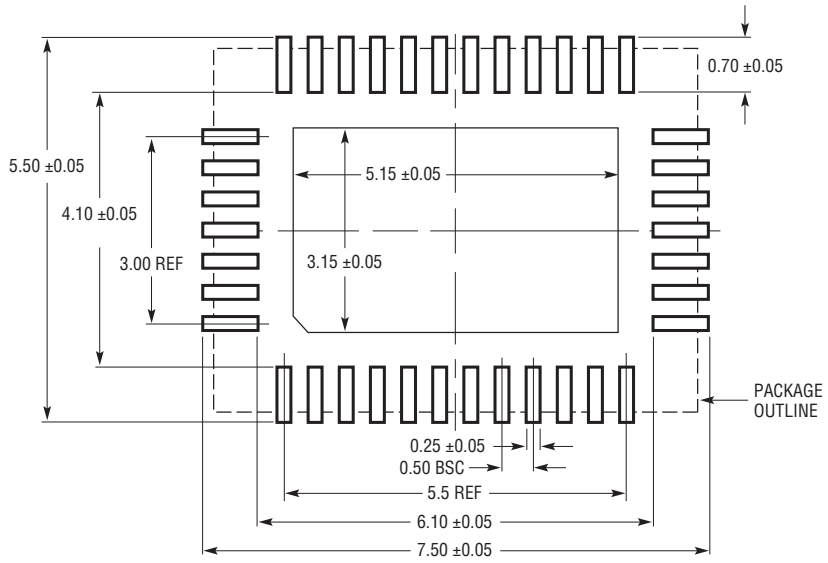
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

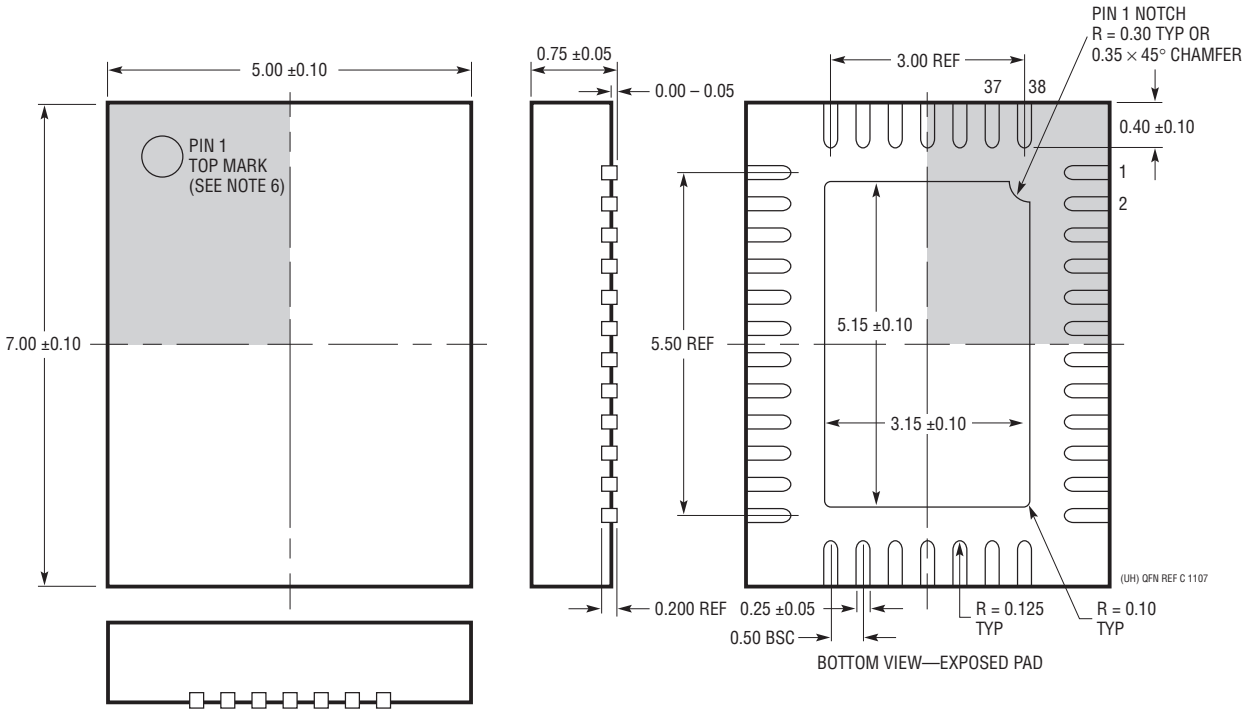
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4266#packaging for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	3/11	Revised AGND and DGND pin references throughout data sheet.	1 to 6, 9, 13
		Revised auto mode to AUTO pin mode throughout data sheet.	1 to 26
		Added text to Operating Modes and made minor text edits throughout Applications Information section.	19 to 26
C	8/11	Changed –48 Supply Voltage to Main PoE Supply Voltage.	3
		Changed Gate Typical voltage to 12V.	3, 13, 19
		Changed SCL, SDAIN V_{IL} to 1.0V (I^2C compliance).	4
		Fix t_{CUT} to differentiate from t_{LIM}, Electrical Characteristics.	5
		Added (mA) to Classification Current Compliance, x-axis title.	7
		802.3af Classification section, changed Figure 14 reference to Figure 13.	18
		Power Supplies and Bypassing section changed to –45 for Type 1 minimum and –51 for Type 2 minimum.	22
D	1/12	Revised MAX value for V_{ILD} I^2C Input Low Voltage	4
		Clarified AUTO pin mode relationship to reset pin	16
E	5/14	Fixed part marking for GW package.	2
F	06/15	Updated surge protection recommendations	1, 22, 24, 25, 30
		Simplified Power over Ethernet system diagram	14
		Updated Figure numbers	25 to 27
		Added component value (Figure 17)	23
G	06/17	Updated Figures 16 and 19	22, 25