Hot Swappable 2-Wire Bus Buffers

FEATURES

- **Bidirectional Buffer for SDA and SCL Lines Increases Fanout**
- **Prevents SDA and SCL Corruption During Live Board Insertion and Removal From Backplane**
- Isolates Input SDA and SCL Lines From Output
- Compatible with I^2C, I^2C Fast Mode and SMBus Standards (Up to 400kHz Operation)
- Low I_{CC} Chip Disable: <1µA (LTC4300-1)
- READY Open-Drain Output (LTC4300-1)
- 1V Precharge on All SDA and SCL Lines
- Supports Clock Stretching, Arbitration and Synchronization
- 5V to 3.3V Level Translation (LTC4300-2)
- High Impedance SDA, SCL Pins for V_{CC} = 0V
- Small MSOP 8-Lead Package

APPLICATIONS

- Hot Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- Desktop Computer

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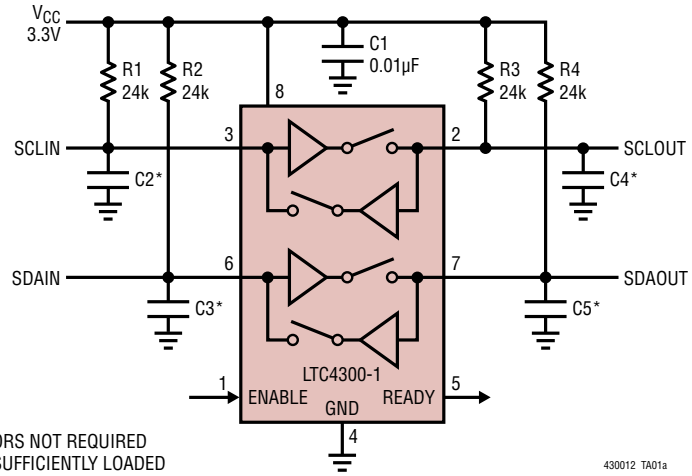
DESCRIPTION

The LTC®4300 series hot swappable 2-wire bus buffers allow I/O card insertion into a live backplane without corruption of the data and clock busses. When the connection is made, the LTC4300-1/LTC4300-2 provide bidirectional buffering, keeping the backplane and card capacitances isolated. Rise time accelerator circuitry* allows the use of weaker DC pull-up currents while still meeting rise time requirements. During insertion, the SDA and SCL lines are precharged to 1V to minimize bus disturbances.

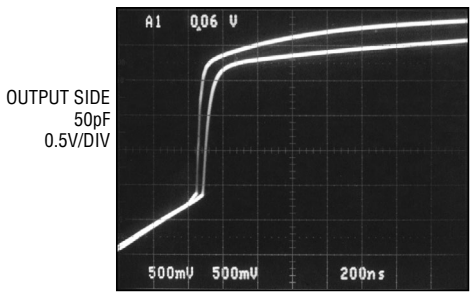
The LTC4300-1 incorporates a CMOS threshold digital ENABLE input pin, which forces the part into a low current mode when driven to ground and sets normal operation when driven to V_{CC}. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. The LTC4300-2 replaces the ENABLE pin with a dedicated supply voltage pin, V_{CC2}, for the card side, providing level shifting between 3.3V and 5V systems. Both the backplane and card may be powered with supply voltages ranging from 2.7V to 5.5V, with no constraints on which supply voltage is higher. The LTC4300-2 also replaces the READY pin with a digital CMOS input pin, ACC, which enables and disables the rise time accelerator currents.

The LTC4300 is available in a small 8-lead MSOP package.

TYPICAL APPLICATION



Input–Output Connection t_{PLH}

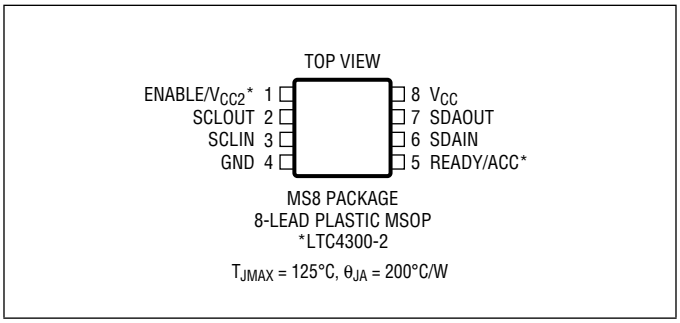


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND .....–0.5V to 7V
V_{CC2} to GND (LTC4300-2).....–0.5V to 7V
SDAIN, SCLIN, SDAOUT, SCLOUT.....–0.5V to 7V
READY, ENABLE (LTC4300-1).....–0.5V to 7V
ACC (LTC4300-2).....–0.5V to 7V
Operating Temperature Range
LTC4300-1C/LTC4300-2C .....0°C to 70°C
LTC4300-1I/LTC4300-2I .....–40°C to 85°C
Storage Temperature Range .....–65°C to 125°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4300-1CMS8#PBF	LTC4300-1CMS8#TRPBF	LTUB	8-Lead Plastic MSOP	0°C to 70°C
LTC4300-1IMS8#PBF	LTC4300-1IMS8#TRPBF	LTUC	8-Lead Plastic MSOP	–40°C to 85°C
LTC4300-2CMS8#PBF	LTC4300-2CMS8#TRPBF	LTVJ	8-Lead Plastic MSOP	0°C to 70°C
LTC4300-2IMS8#PBF	LTC4300-2IMS8#TRPBF	LTVK	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part markings, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V, LTC4300-1	●		2.8	6	mA
I_{SD}	Supply Current in Shutdown Mode	V_{ENABLE} = 0V, LTC4300-1			0.1		µA
V_{CC2}	Card Side Supply Voltage	LTC4300-2	●	2.7		5.5	V
I_{VCC1}	V_{CC} Supply Current	V_{SDAIN} = V_{SCLIN} = 0V, V_{CC1} = V_{CC2} = 5.5V, LTC4300-2			1.8	3.6	mA
I_{VCC2}	V_{CC2} Supply Current	V_{SDAOUT} = V_{SCLOUT} = 0V, V_{CC1} = V_{CC2} = 5.5V, LTC4300-2			1.2	2.4	mA
Start-Up Circuitry							
V_{PRE}	Precharge Voltage	SDA, SCL Floating	●	0.8	1.0	1.2	V
t_{IDLE}	Bus Idle Time		●	50	95	150	µs
V_{EN}	ENABLE Threshold Voltage	LTC4300-1			0.5 • V_{CC}	0.9 • V_{CC}	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{CC2} = 2.7V to 5.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DIS}	Disable Threshold Voltage	LTC4300-1, ENABLE Pin		0.1 • V_{CC}	0.5 • V_{CC}		V
I_{EN}	ENABLE Input Current	ENABLE from 0V to V_{CC}, LTC4300-1			±0.1	±1	µA
t_{PHL}	ENABLE Delay, On-Off	LTC4300-1			100		ns
	READY Delay, Off-On	LTC4300-1			10		ns
t_{PLH}	ENABLE Delay, Off-On	LTC4300-1			80		µs
	READY Delay, On-Off	LTC4300-1			10		µs
I_{OFF}	READY OFF State Leakage Current	LTC4300-1			±0.1		µA
V_{OL}	READY Output Low Voltage	I_{PULLUP} = 3mA, LTC4300-1	●			0.4	V
Rise Time Accelerators							
$I_{PULLUPAC}$	Transient Boosted Pull-Up Current	Positive Transition on SDA, SCL, V_{CC} = 2.7V, Slew Rate = 1.25V/µs (Note 2), LTC4300-2, ACC = 0.7 • V_{CC2}, V_{CC2} = 2.7V		1	2		mA
V_{ACCDIS}	Accelerator Disable Threshold	LTC4300-2		0.3 • V_{CC2}	0.5 • V_{CC2}		V
V_{ACCEN}	Accelerator Enable Threshold	LTC4300-2			0.5 • V_{CC2}	0.7 • V_{CC2}	V
I_{VACC}	ACC Input Current	LTC4300-2			±0.1	±1	µA
t_{PDOFF}	ACC Delay, On/Off	LTC4300-2			5		ns
Input-Output Connection							
V_{OS}	Input-Output Offset Voltage	10k to V_{CC} on SDA, SCL, V_{CC} = 3.3V (Note 3), LTC4300-2, V_{CC2} = 3.3V, V_{IN} = 0.2V	●	0	75	150	mV
$f_{SCL, SDA}$	Operating Frequency	Guaranteed by Design, Not Subject to Test		0		400	kHz
C_{IN}	Digital Input Capacitance	Guaranteed by Design, Not Subject to Test				10	pF
V_{OL}	Output Low Voltage, Input = 0V	SDA, SCL Pins, I_{SINK} = 3mA, V_{CC} = 2.7V, V_{CC2} = 2.7V, LTC4300-2	●	0		0.4	V
I_{LEAK}	Input Leakage Current	SDA, SCL Pins = V_{CC} = 5.5V, LTC4300-2, V_{CC2} = 5.5V				±5	µA
Timing Characteristics							
f_{I2C}	I^2C Operating Frequency	(Note 4)		0		400	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	(Note 4)		1.3			µs
$t_{hD,STA}$	Hold Time After (Repeated) START Condition	(Note 4)		0.6			µs
$t_{su,STA}$	Repeated START Condition Setup Time	(Note 4)		0.6			µs
$t_{su,STO}$	STOP Condition Setup Time	(Note 4)		0.6			µs
$t_{hD, DAT}$	Data Hold Time	(Note 4)		300			ns
$t_{su, DAT}$	Data Setup Time	(Note 4)		100			ns
t_{LOW}	Clock LOW Period	(Note 4)		1.3			µs
t_{HIGH}	Clock HIGH Period	(Note 4)		0.6			µs
t_f	Clock, Data Fall Time	(Notes 4, 5)		20 + 0.1 • C_B		300	ns
t_r	Clock, Data Rise Time	(Notes 4, 5)		20 + 0.1 • C_B		300	ns
$t_{PHL,SKEW}$	High-to-Low Propagation Delay Skew, SCL-SDA	LTC4300-1: V_{CC} = 2.7V, V_{CC} = 5.5V (Note 6)	●		0	±75	ns
		LTC4300-2: V_{CC} = 2.7V, V_{CC2} = 5.5V; V_{CC} = 5.5V, V_{CC2} = 2.7V (Note 6)	●		0	±75	ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage, as shown in the Typical Performance Characteristics section.

Note 3: The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.

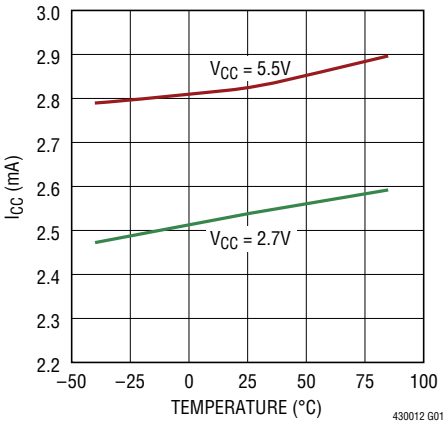
Note 4: Guaranteed by design, not subject to test.

Note 5: C_B = total capacitance of one bus line in pF.

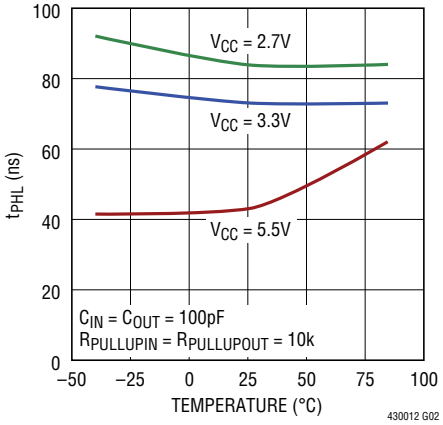
Note 6: These tests measure the difference in high-to-low propagation delay t_{PHL} between the clock and data channels. The delay on each channel is measured from the 50% point of the falling driven input signal to the 50% point of the output driven by the LTC4300-1/LTC4300-2. The skew is defined as ($t_{PHL(SCL)}$ - $t_{PHL(SDA)}$). Testing is performed in both directions—from input bus to output bus and vice versa. Tests are performed with approximately 500pF of distributed equivalent capacitance on each SDA and SCL pin.

TYPICAL PERFORMANCE CHARACTERISTICS

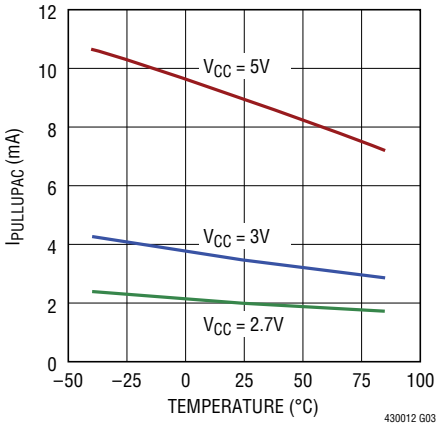
I_{CC} vs Temperature (LTC4300-1)



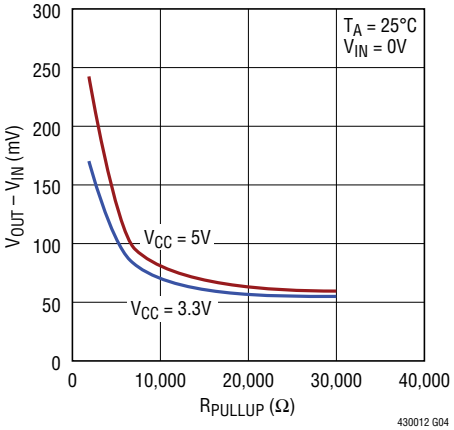
Input–Output t_{PHL} vs Temperature (LTC4300-1)



$I_{PULLUPAC}$ vs Temperature



Connection Circuitry $V_{OUT} - V_{IN}$



PIN FUNCTIONS

ENABLE/V_{CC2} (Pin 1): Chip Enable Pin/Card Supply Voltage. For the LTC4300-1, this is a digital CMOS threshold input pin. Grounding this pin puts the part in a low current (<1µA) mode. It also disables the rise time accelerators, disables the bus precharge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. Drive ENABLE all the way to V_{CC} for normal operation. Connect ENABLE to V_{CC} if this feature is not being used. For the LTC4300-2, this is the supply voltage for the devices on the card I^2C busses. Connect pull-up resistors from SDAOUT and SCLOUT to this pin. Place a bypass capacitor of at least 0.01µF close to this pin for best results.

SCLOUT (Pin 2): Serial Clock Output. Connect this pin to the SCL bus on the card. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

SCLIN (Pin 3): Serial Clock Input. Connect this pin to the SCL bus on the backplane. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

GND (Pin 4): Ground. Connect this pin to a ground plane for best results.

READY/ACC (Pin 5): Connection Flag/Rise time Accelerator Control. For the LTC4300-1, this is an open-drain NMOS output which pulls LOW when either ENABLE is LOW or the start-up sequence described in the Operation section has not been completed. READY goes HIGH when ENABLE is HIGH and start-up is complete. Connect a 10k resistor from this pin to V_{CC} to provide the pull up. For the LTC4300-2, this is a CMOS threshold digital input pin that enables and disables the rise time accelerators on all four SDA and SCL pins. Drive ACC all the way to the V_{CC2} supply voltage to enable all four accelerators; drive ACC to ground to turn them off.

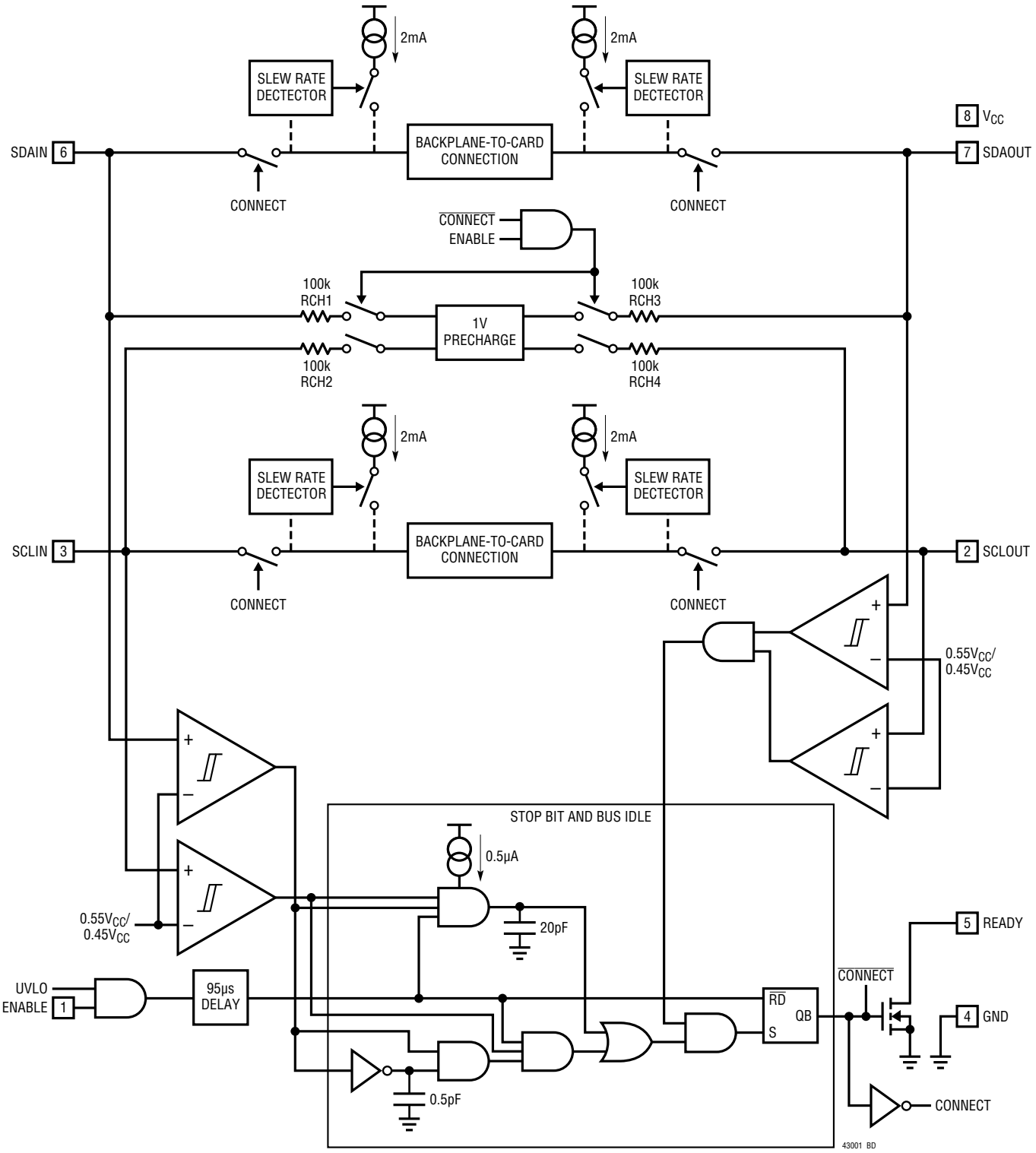
SDAIN (Pin 6): Serial Data Input. Connect this pin to the SDA bus on the backplane. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

SDAOUT (Pin 7): Serial Data Output. Connect this pin to the SDA bus on the card. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

V_{CC} (Pin 8): Main Input Power Supply From Backplane. This is the supply voltage for the devices on the backplane I^2C busses. Connect pull-up resistors from SDAIN and SCLIN to this pin. Place a bypass capacitor of at least 0.01µF close to this pin for best results.

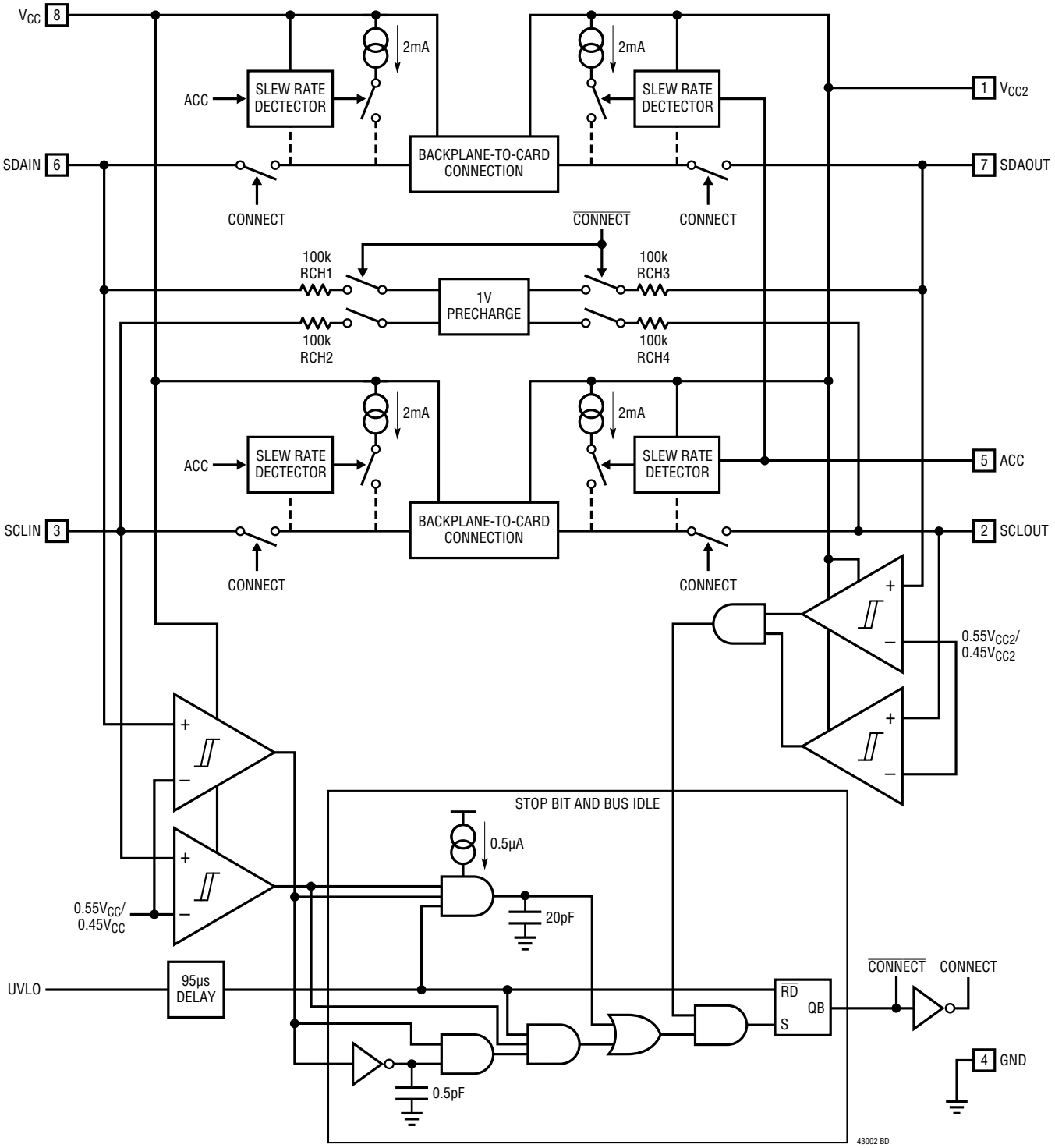
BLOCK DIAGRAM LTC4300-1

2-Wire Bus Buffer and Hot Swap™ Controller



BLOCK DIAGRAM LTC4300-2

2-Wire Bus Buffer and Hot Swap Controller



OPERATION

Start-Up

When the LTC4300 first receives power on its V_{CC} pin, either during power-up or during hot swapping, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above 2.5V. For the LTC4300-2, the part also waits for V_{CC2} to rise above 2V. This ensures that the part does not try to function until it has enough voltage to do so.

During this time, the 1V precharge circuitry is also active and forces 1V through 100k nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0V and V_{CC}. Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

Once the LTC4300 comes out of UVLO, it assumes that SDAIN and SCLIN have been hot swapped into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a STOP bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A LOW forced on either pin at any time results in both pin voltages being LOW. SDAIN and SDAOUT enter a logic HIGH state only when all devices on both SDAIN and SDAOUT force a HIGH. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4300.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms, as described here.

Input to Output Offset Voltage

When a logic LOW voltage, V_{LOW1}, is driven on any of the LTC4300's data or clock pins, the LTC4300 regulates the voltage on the other side of the chip (call it V_{LOW2}) to a slightly higher voltage, as directed by the following equation:

$$V_{LOW2} = V_{LOW1} + 50mV + (V_{CC}/R) \bullet 100$$

where R is the bus pull-up resistance in ohms. For example, if a device is forcing SDAOUT to 10mV and if V_{CC} = 3.3V and the pull-up resistor R on SDAIN is 10k, then the voltage on SDAIN = 10mV + 50mV + (3.3/10000) • 100 = 93mV. See the Typical Performance Characteristics section for curves showing the offset voltage as a function of V_{CC} and R.

Propagation Delays

During a rising edge, the rise time on each side is determined by the combined pull-up current of the LTC4300 boost current and the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 1 for V_{CC} = 3.3V and a 10k pull-up resistor on each side (50pF on one side and 150pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective t_{PLH} is negative.

There is a finite propagation delay, t_{PHL}, through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms for the same V_{CC}, pull-up resistors and equivalent capacitance conditions as used in Figure 1. An external NMOS device pulls down the voltage on the side with 150pF capacitance; the LTC4300 pulls down the voltage on the opposite side, with a delay of 55ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows t_{PHL} as a function of temperature and voltage for 10k pull-up

OPERATION

resistors and 100pF equivalent capacitance on both sides of the part. By comparison with Figure 2, the V_{CC} = 3.3V curve shows that increasing the capacitance from 50pF to 150pF results in a t_{PHL} increase from 55ns to 75ns. Larger output capacitances translate to longer delays (up to 150ns). Users must quantify the difference in propagation times for a rising edge vs a falling edge in their systems and adjust setup and hold times accordingly.

Rise Time Accelerators

Once connection has been established, rise time accelerator circuits on all four SDA and SCL pins are activated. These allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise time requirements. During positive bus transitions, the LTC4300 switches in 2mA of current to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6V. Using a general rule of 20pF of capacitance for every device on the bus (10pF for the device and 10pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 1.25V/µs to guarantee activation of the accelerators.

For example, assume an SMBus system with V_{CC} = 3V, a 10k pull-up resistor and equivalent bus capacitance of 200pF. The rise time of an SMBus system is calculated from ($V_{IL(MAX)}$ – 0.15V) to ($V_{IH(MIN)}$ + 0.15V), or 0.65V to 2.25V. It takes an RC circuit 0.92 time constants to traverse this voltage for a 3V supply; in this case, 0.92 • (10k • 200pF) = 1.85µs. Thus, the system exceeds the maximum allowed rise time of 1µs by 85%. However, using the rise time accelerators, which are activated at a DC threshold of below 0.65V, the worst-case rise time is: (2.25V – 0.65V) • 200pF/1mA = 320ns, which meets the 1µs rise time requirement.

READY Digital Output (LTC4300-1)

This pin provides a digital flag which is low when either ENABLE is low or the start-up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is high and start-up is complete. The pin is driven by an open drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor of 10k to V_{CC} to provide the pull-up. This feature is available for the LTC4300-1 only.

ENABLE Low Current Disable (LTC4300-1)

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise time accelerators, drives READY low, disables the bus precharge circuitry and puts the part in a near-zero current state. When the pin voltage is driven all the way to V_{CC}, the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides. This feature is available for the LTC4300-1 only.

ACC Boost Current Enable (LTC4300-2)

Users having lightly loaded systems may wish to disable the rise time accelerators. Driving this pin to ground turns off the rise time accelerators on all four SDA and SCL pins. Driving this pin to the V_{CC2} voltage enables normal operation of the rise time accelerators, as described in the Rise time Accelerators section above. This feature is available for the LTC4300-2 only.

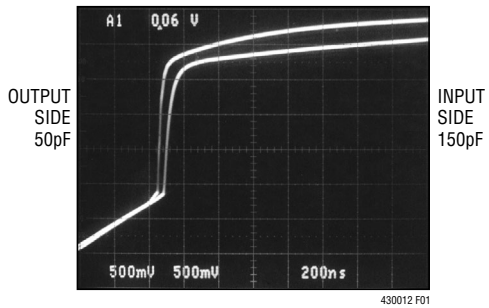


Figure 1. Input–Output Connection t_{PLH}

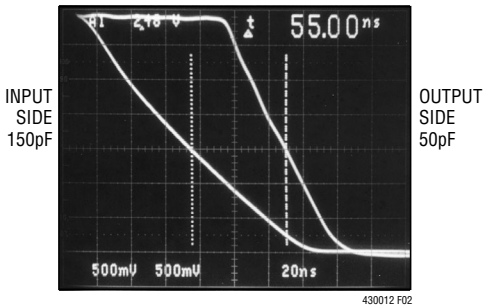


Figure 2. Input–Output Connection t_{PHL}

APPLICATIONS INFORMATION

Resistor Pull-Up Value Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value R using the formula:

$$R \leq (V_{CC(MIN)} - 0.6)\ (800{,}000) / C$$

where R is the pull-up resistor value in ohms, $V_{CC(MIN)}$ is the minimum V_{CC} voltage and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose R ≤ 16k for V_{CC} = 5.5V maximum, R ≤ 24k for V_{CC} = 3.6V maximum. The start-up circuitry requires logic high voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in Figures 3 and 4 for guidance in resistor pull-up selection.

Minimum SDA and SCL Capacitance Requirements

The LTC4300 I/O connection circuitry requires a minimum capacitance loading on the SDA and SCL pins in order to function properly. The value of this capacitance is a function of V_{CC} and the bus pull-up resistance. Estimate the bus capacitance on both the backplane and the card data and clock busses, and refer to Figures 3 and 4 to choose appropriate pull-up resistor values. Note from the figures that 5V systems must have at least 47pF capacitance on their busses and 3.3V systems must have at least 22pF capacitance for proper operation of the LTC4300. For applications with less capacitance, add a capacitor to ground to ensure these minimum capacitance conditions.

Hot Swapping and Capacitance Buffering Application

Figures 5 through 8 illustrate the usage of the LTC4300 in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise and fall time requirements difficult to meet. Placing a LTC4300 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4300 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4300, which is less than 10pF.

Figure 5 shows the LTC4300-1 in a CompactPCI configuration. Connect V_{CC} to the output of one of the CompactPCI power supply Hot Swap circuits and connect ENABLE to the short "board ENABLE" pin. V_{CC} is monitored by a filtered UVLO circuit. With the V_{CC} voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients

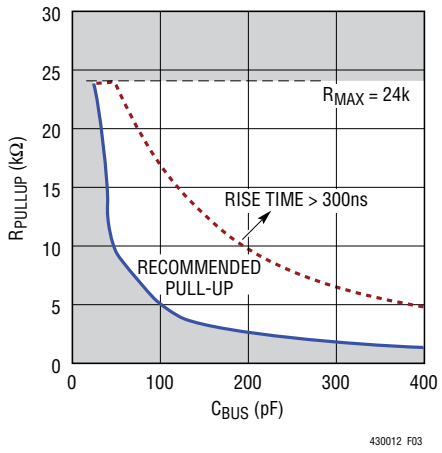


Figure 3. Bus Requirements for 3.3V Systems

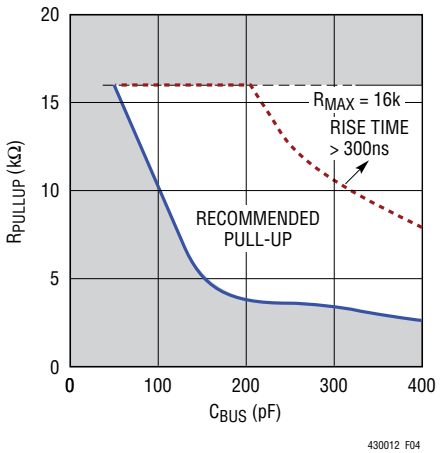


Figure 4. Bus Requirements for 5V Systems

APPLICATIONS INFORMATION

associated with hot swapping have settled. Owing to their small capacitance, the SDAIN and SCLIN pins cause minimal disturbance on the backplane busses when they make contact with the connector.

Figure 6 shows the LTC4300-2 in a CompactPCI configuration. The LTC4300-2 receives its V_{CC} voltage from one of the long "early power" pins. Because this power is not switched, add a 5Ω to 10Ω resistor between the V_{CC} pins of the connector and the LTC4300-2, as shown in the figure. In addition, make sure that the V_{CC} bypassing on the backplane is large compared to the 0.01µF bypass capacitor on the card. Establishing early power V_{CC} ensures that the 1V precharge voltage is present at the SDAIN and SCLIN pins before they make contact. Connect V_{CC2} to the output of one of the CompactPCI power supply Hot Swap circuits. V_{CC2} is monitored by a filtered UVLO circuit. With the V_{CC2} voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients associated with hot swapping have settled.

Figure 7 shows the LTC4300-1 in a PCI application, where all of the pins have the same length. In this case, connect an RC series circuit on the I/O card between V_{CC} and ENABLE. An RC product of 10ms provides a filter to prevent the LTC4300-1 from becoming activated until the transients associated with hot swapping have settled.

Figure 8 shows the LTC4300-2 in an application where the user has a custom connector with pins of three different lengths available. Making V_{CC2} the shortest pin ensures that all other pins are firmly connected before V_{CC2} receives any voltage. A filtered UVLO circuit on V_{CC2} ensures that the V_{CC2} pin is firmly connected before the LTC4300-2 connects the backplane to the card.

Repeater/Bus Extender Application

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two LTC4300-1s back-to-back, as shown in Figure 9. The I^2C specification allows for 400pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise and fall time specifications are to be met. The strong pull-up and pull-down impedances of the LTC4300-1 are capable of meeting rise and fall time specifications for one nanofarad of capacitance, thus allowing much more interconnect distance. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic LOW voltage with respect to the ground at one end of the system may violate the allowed V_{OL} specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back LTC4300-1s add together, directly contributing to the same problem.

Systems with Disparate Supply Voltages (LTC4300-1)

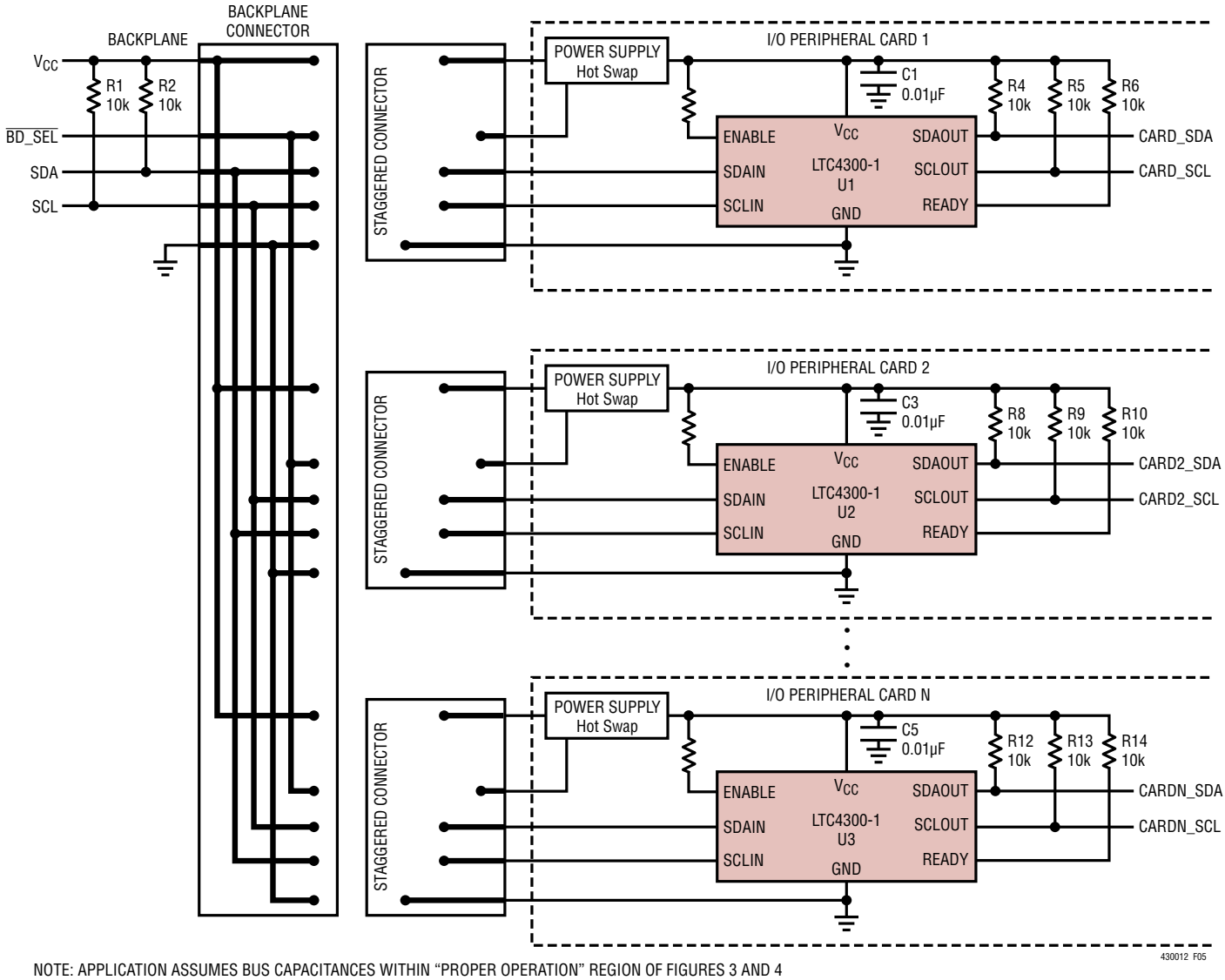
In large 2-wire systems, the V_{CC} voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is well modelled by a series resistor in the V_{CC} line, as shown in Figure 10. For proper operation of the LTC4300-1, make sure that $V_{CC(BUS)} \geq V_{CC(LTC4300)} - 0.5V$.

5V to 3.3V Level Translator and Power Supply Redundancy (LTC4300-2)

Systems requiring different supply voltages for the backplane side and the card side can use the LTC4300-2, as shown in Figure 11. The pull-up resistors on the card side connect from SDAOUT to SCLOUT to V_{CC2}, and those on the backplane side connect from SDAIN and SCLIN to V_{CC}. The LTC4300-2 functions for voltages ranging from 2.7V to 5.5V on both V_{CC} and V_{CC2}. There is no constraint on the voltage magnitudes of V_{CC} and V_{CC2} with respect to each other.

This application also provides power supply redundancy. If either the V_{CC} or V_{CC2} voltage falls below its UVLO threshold, the LTC4300-2 disconnects the backplane from the card, so that the side that is still powered can continue to function.

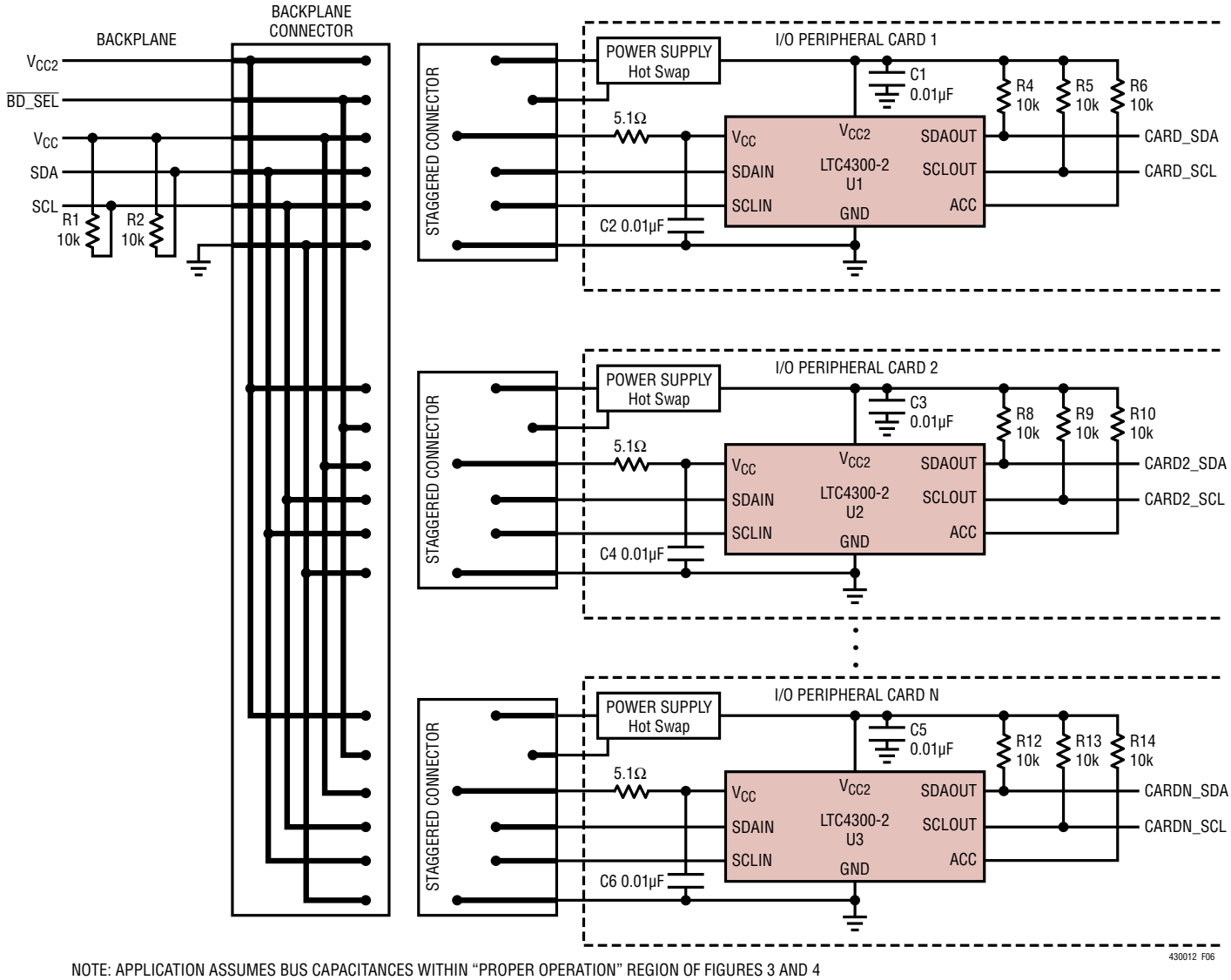
APPLICATIONS INFORMATION



NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN "PROPER OPERATION" REGION OF FIGURES 3 AND 4

Figure 5. Hot Swapping Multiple I/O Cards into a Backplane Using the LTC4300-1 in a CompactPCI System

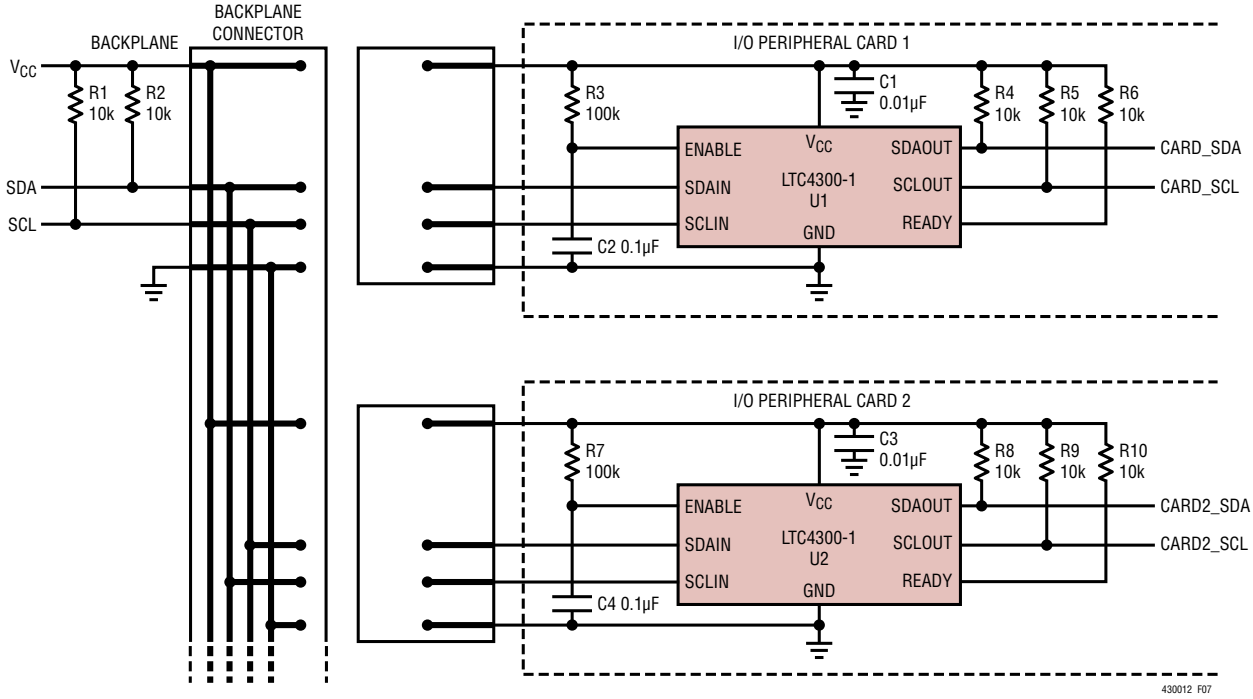
APPLICATIONS INFORMATION



NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN "PROPER OPERATION" REGION OF FIGURES 3 AND 4

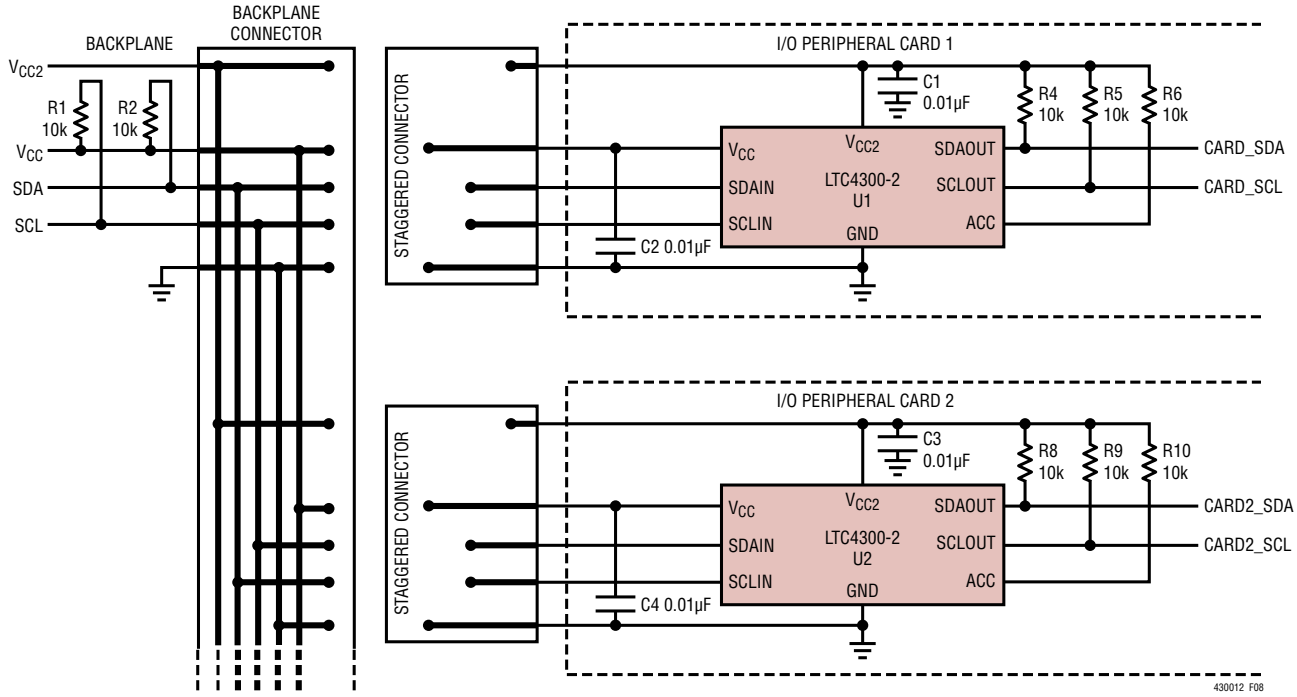
Figure 6. Hot Swapping Multiple I/O Cards into a Backplane Using the LTC4300-2 in a CompactPCI System

APPLICATIONS INFORMATION



NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN "PROPER OPERATION" REGION OF FIGURES 3 AND 4

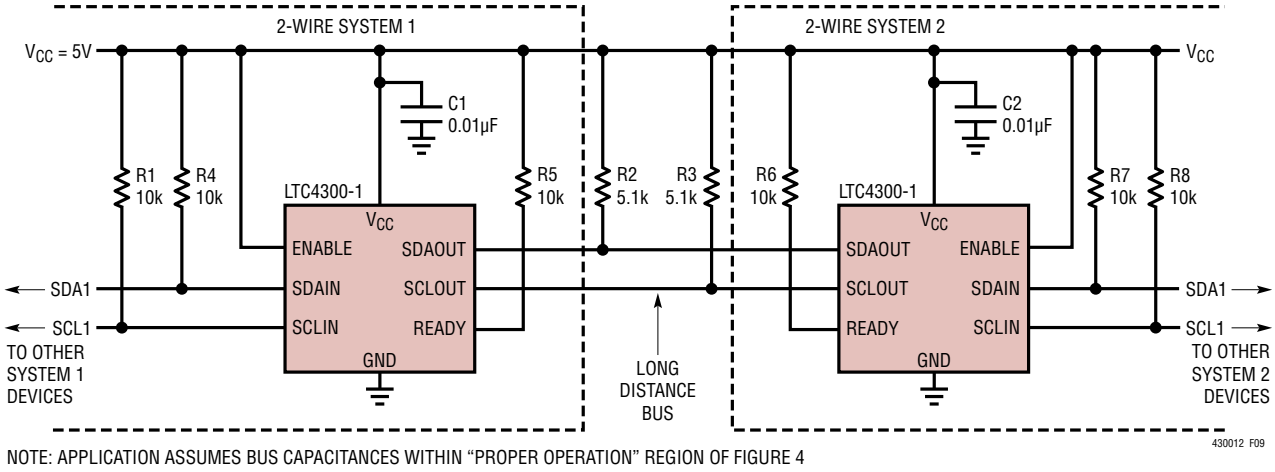
Figure 7. Hot Swapping Multiple I/O Cards into a Backplane Using the LTC4300-1 in a PCI System



NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN "PROPER OPERATION" REGION OF FIGURES 3 AND 4

Figure 8. Hot Swapping Multiple I/O Cards into a Backplane Using the LTC4300-2 with a Custom Connector

APPLICATIONS INFORMATION



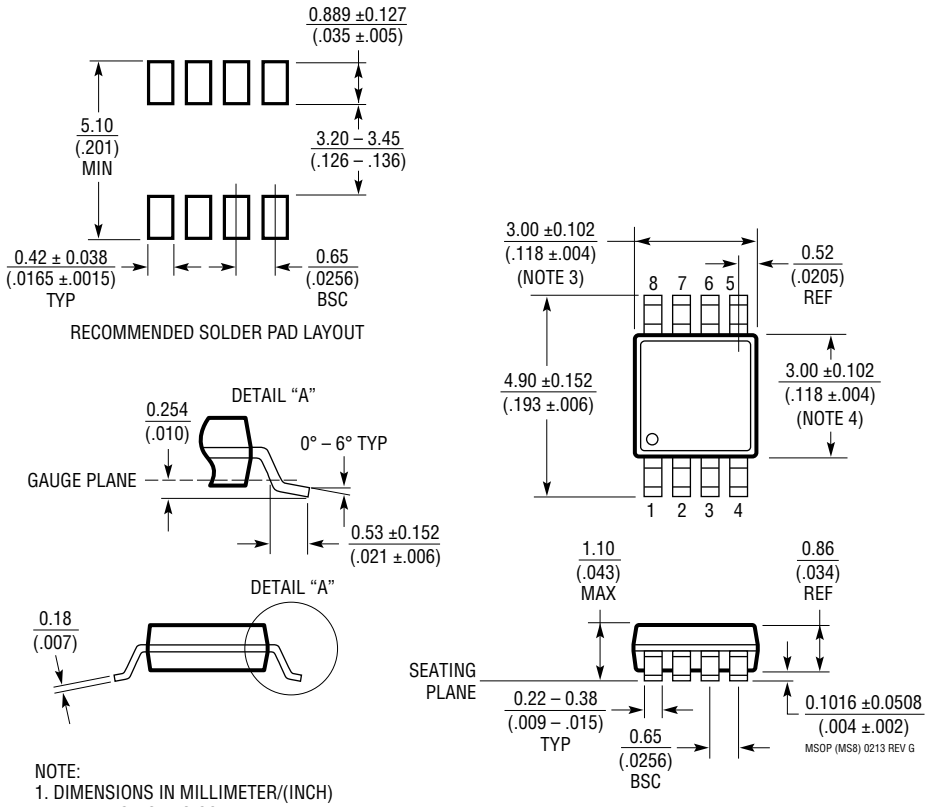
NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN "PROPER OPERATION" REGION OF FIGURE 4

Figure 9. Repeater/Bus Extender Application

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/12	Added $T_{PHL,SKEW}$ parameter to Electrical Characteristics	3
		Updated format	1-18
B	04/14	Updated MS8 Package Drawing	16

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