Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation

FEATURES

- **Level Translates 1V Signals to Standard 3.3V and 5V Logic Rails**
- **Allows Bus Pull-Up Voltages as Low as 1V on SDAIN and SCLIN**
- **Bidirectional Buffer* for SDA and SCL Lines Increases Fanout**
- **Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane**
- **Isolates Input SDA and SCL Line from Output**
- **10kV Human Body Model ESD Protection**
- Supports Clock Stretching, Arbitration and Synchronization
- High Impedance SDA, SCL Pins for V_{CC} = 0V
- $\overline{CS}$ Gates Connection from Input to Output
- Compatible with I²C™, I²C Fast Mode and SMBus Standards (Up to 400kHz Operation)
- Small 8-Pin MSOP and DFN (3mm × 3mm) Packages

APPLICATIONS

- Hot Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- Desktop Computers

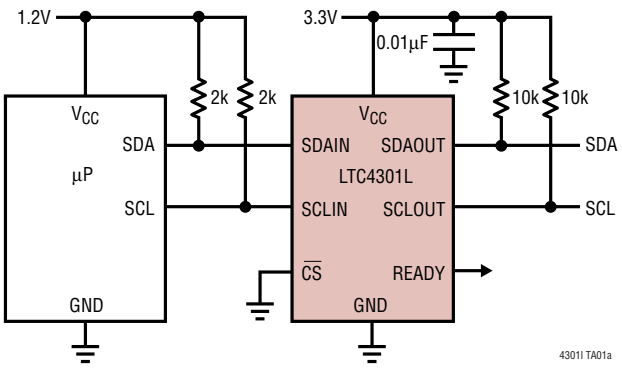
DESCRIPTION

The LTC®4301L hot swappable, 2-wire bus buffer allows I/O card insertion into a live backplane without corruption of the data and clock busses. In addition, the LTC4301L SDAIN and SCLIN pins are compatible with systems with pull-up voltages as low as 1V. Control circuitry prevents the backplane from being connected to the card until a stop bit or a bus idle is present. When the connection is made, the LTC4301L provides bidirectional buffering, keeping the backplane and card capacitances isolated.

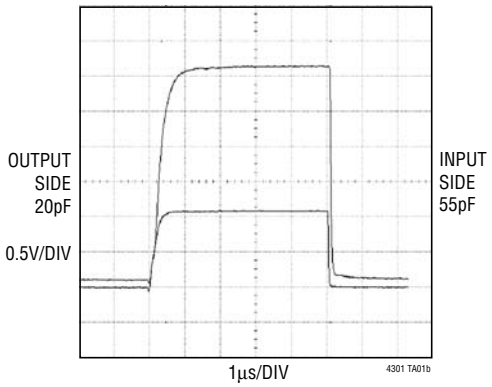
When driven low, the $\overline{CS}$ input pin allows the part to connect after a stop bit or bus idle occurs. Driving $\overline{CS}$ high breaks the connection between SCLIN and SCLOUT and between SDAIN and SDAOUT. A logic high on READY indicates that the backplane and card sides are connected together.

The LTC4301L is offered in 8-pin DFN (3mm × 3mm) and MSOP packages.

TYPICAL APPLICATION



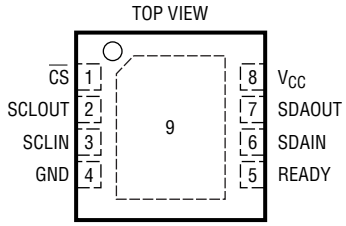
Input-Output Connection



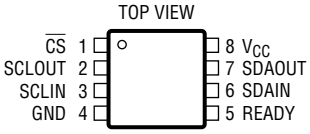
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to GND ..... –0.3V to 7V
SDAIN, SCLIN, SDAOUT, SCLOUT, $\overline{CS}$ ..... –0.3V to 7V
READY ..... –0.3V to 6V
Operating Temperature Range
LTC4301LC ..... 0°C to 70°C
LTC4301LI ..... –40°C to 85°C
Storage Temperature Range
MSOP ..... –65°C to 150°C
DFN ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND
PCB CONNECTION OPTIONAL



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER PART NUMBER	DD PART MARKING	ORDER PART NUMBER	MS8 PART MARKING
LTC4301LCDD LTC4301LIDD	LBHS	LTC4301LCMS8 LTC4301LIMS8	LTBHQ

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V V_{CC} = 5.5V, $\overline{CS}$ = 5.5V	●		4.5 300	6.2	mA µA
Start-Up Circuitry							
V_{PRE}	Precharge Voltage	SDAOUT, SCLOUT Floating	●	0.85	1.05	1.25	V
t_{IDLE}	Bus Idle Time		●	60	95	175	µs
RDY_{VOL}	READY Output Low Voltage	I_{PULLUP} = 3mA	●			0.4	V
$V_{THR\overline{CS}}$	Connection Sense Threshold			0.8	1.4	2	V
$I_{\overline{CS}}$	$\overline{CS}$ Input Current	$\overline{CS}$ from 0V to V_{CC}			±0.1	±1	µA

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{THR}	SDAIN, SCLIN Logic Input Threshold Voltage SDAOUT, SCLOUT Logic Input Threshold Voltage	Rising Edge Rising Edge		0.45 1.55	0.6 1.8	0.75 2.0	V V
V_{HYS}	SDAIN, SCLIN Logic Input Threshold Hysteresis SDAOUT, SCLOUT Logic Input Threshold Hysteresis	(Note 3) (Note 3)			85 50		mV mV
t_{PLH}	$\overline{CS}$ Delay On-Off READY Delay Off-On				10 10		ns ns
t_{PHL}	$\overline{CS}$ Delay Off-On READY Delay On-Off				95 10		µs ns
I_{OFF}	Ready Off Leakage Current				±0.1		µA
Input-Output Connection							
V_{OS}	Input-Output Offset Voltage	10k to V_{CC} on SDA, SCL, V_{CC} = 3.3V, SDA or SCL = 0.2V (Note 2)	●	0	100	175	mV
C_{IN}	Digital Input Capacitance SDAIN, SDAOUT, SCLIN, SCLOUT	(Note 3)				10	pF
I_{LEAK}	Input Leakage Current	SDA, SCL Pins				±5	µA
V_{OL}	Output Low Voltage, Input = 0V	SDA, SCL Pins, I_{SINK} = 3mA, V_{CC} = 2.7V SDA, SCL Pins, I_{SINK} = 1mA, V_{CC} = 2.7V	●	0 0		0.4 0.2	V V
Timing Characteristics							
$f_{I2C,MAX}$	I^2C Maximum Operating Frequency	(Note 3)		400	600		kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 3)				1.3	µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition	(Note 3)				100	ns
$t_{SU,STA}$	Repeated Start Condition Set-Up Time	(Note 3)				0	ns
$t_{SU,STO}$	Stop Condition Set-Up Time	(Note 3)				0	ns
$t_{HD,DATI}$	Data Hold Time Input	(Note 3)				0	ns
$t_{SU,DAT}$	Data Set-Up Time	(Note 3)				100	ns

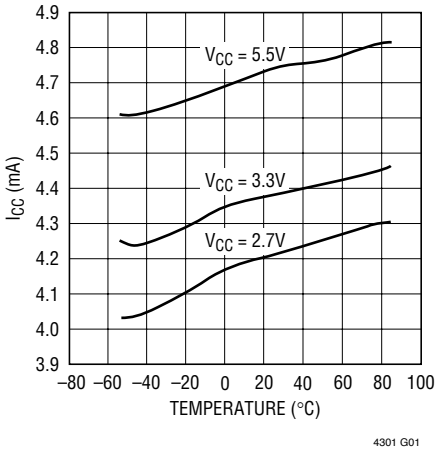
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.

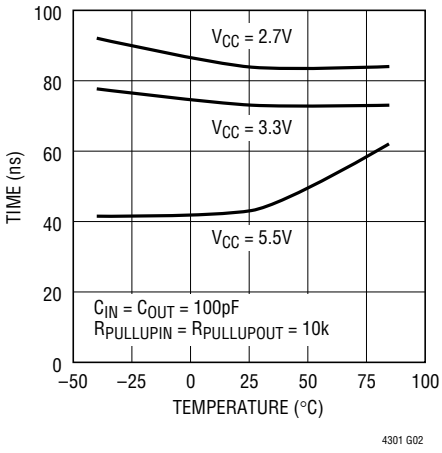
Note 3: Determined by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

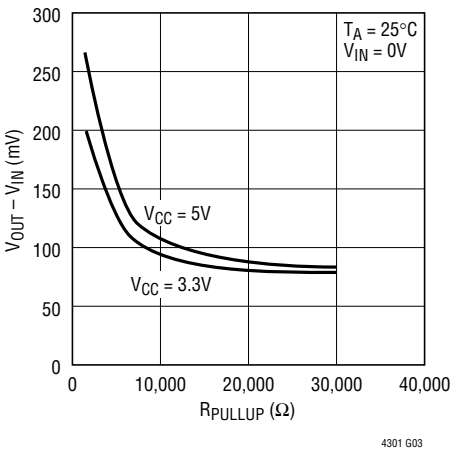
I_{CC} vs Temperature



Input – Output High to Low Propagation Delay vs Temperature



Connection Circuitry $V_{OUT} – V_{IN}$



PIN FUNCTIONS

$\overline{CS}$ (Pin 1): The connection sense pin is a 1.4V threshold digital input pin. For normal operation $\overline{CS}$ is grounded. Driving $\overline{CS}$ above the 1.4V threshold isolates SDAIN from SDAOUT and SCLIN from SCLOUT and asserts READY low.

SCLOUT (Pin 2): Serial Clock Output. Connect this pin to the SCL bus on the card.

SCLIN (Pin 3): Serial Clock Input. Connect this pin to SCL on the bus backplane.

GND (Pin 4, 9): Ground. Connect this pin to a ground plane for best results. Exposed pad (DFN package) is ground.

READY (Pin 5): The READY pin is an open drain N-channel MOSFET output which pulls down when $\overline{CS}$ is high or when the start-up sequence described in the Operation section has not been completed. READY goes high when $\overline{CS}$ is low and a start-up is complete.

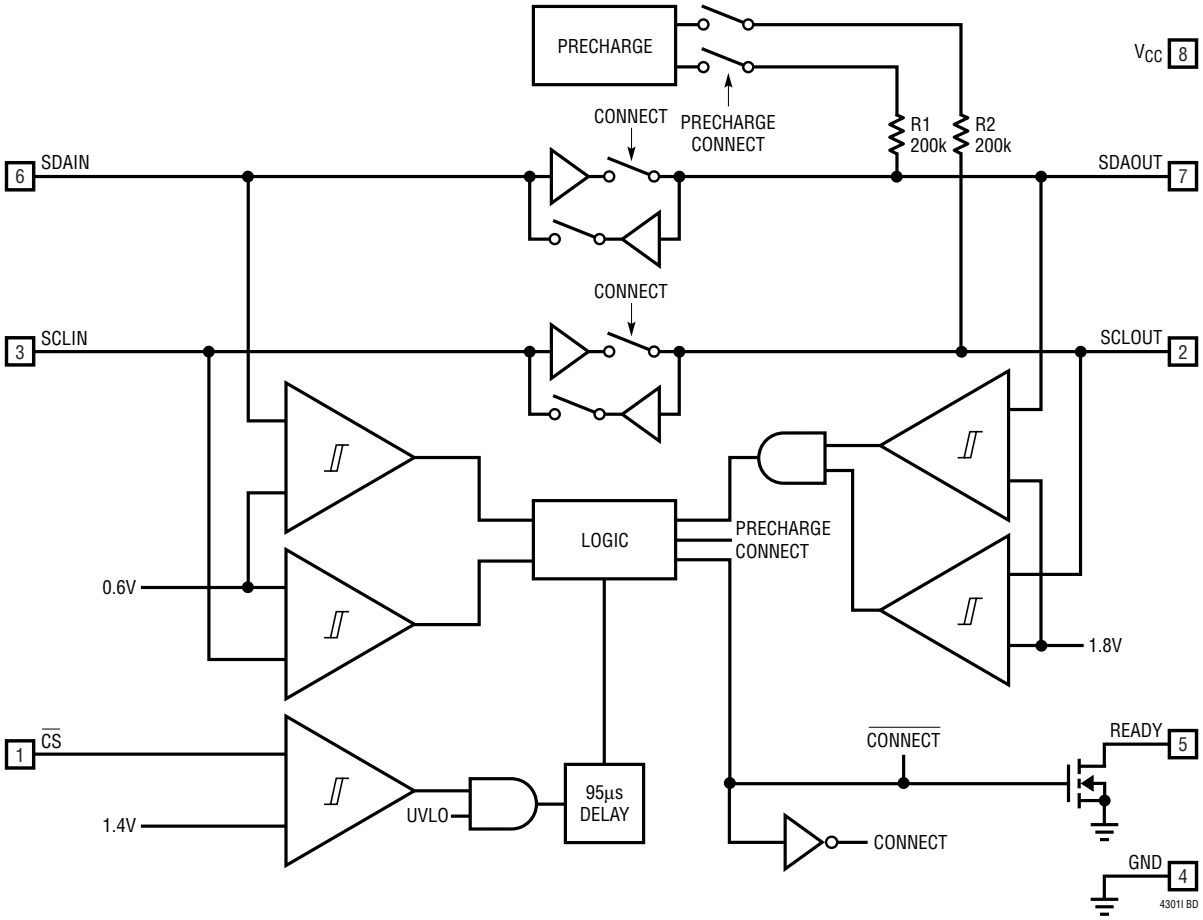
SDAIN (Pin 6): Serial Data Input. Connect this pin to the SDA bus on the backplane.

SDAOUT (Pin 7): Serial Data Output. Connect this pin to the SDA bus on the card.

V_{CC} (Pin 8): Main Input Supply. Place a bypass capacitor of at least 0.01µF close to V_{CC} for best results.

BLOCK DIAGRAM

LTC4301L Supply Independent 2-Wire Bus Buffer



OPERATION

Start-Up

When the LTC4301L first receives power on its V_{CC} pin, either during power-up or live insertion, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until V_{CC} rises above 2.5V. This is to ensure that the part does not try to function until it has enough voltage to do so.

During this time, the 1V precharge circuitry is active and forces 1V through 200k nominal resistors to the SDAOUT and SCLOUT pins. Precharging the SCLOUT and SDAOUT pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing bus disturbances.

Once the LTC4301L comes out of UVLO, it assumes that SDAIN and SCLIN have been inserted into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a stop bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. For proper operation, logic low input voltages should be no higher than 0.4V with respect to the ground pin voltage of the LTC4301L. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4301L.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms as described here.

Input-to-Output Offset Voltage

When a logic low voltage, V_{LOW1}, is driven on any of the LTC4301L's data or clock pins, the LTC4301L regulates the voltage on the other side of the device (call it V_{LOW2}) at a slightly higher voltage, as directed by the following equation:

$$V_{LOW2} = V_{LOW1} + 75mV + (V_{CC}/R) \bullet 70\Omega \text{ (typical)}$$

where R is the bus pull-up resistance in ohms. For example, if a device is forcing SDAOUT to 10mV where V_{CC} = 3.3V and the pull-up resistor R on SDAIN is 10k, then the voltage on SDAIN = 10mV + 75mV + (3.3/10000) • 70 = 108mV(typical). See the Typical Performance Characteristics section for curves showing the offset voltage as a function of V_{CC} and R.

Propagation Delays

During a rising edge, the rise time on each side is determined by the bus pull-up resistor and the equivalent capacitance on the line. In Figure 1, V_{CC} = 3.3V, SDAOUT and SCLOUT are pulled-up to 3.3V with 10k resistor (20pF on this side) and SDAIN and SCLIN are pulled-up to 1.2V with a 2k resistor (55pF on this side). Lower pull-up resistor values are used on the input side to allow the output side to be released sooner.

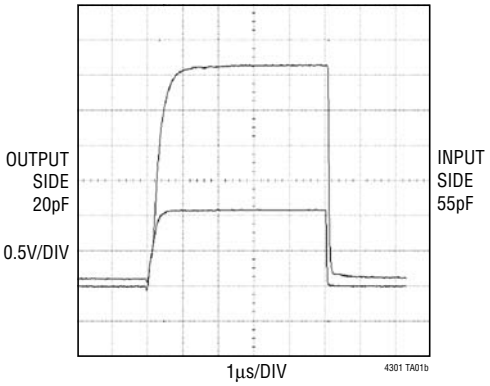


Figure 1. Input-Output Connection

There is a finite high to low propagation delay through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms for the same pull-up resistors and equivalent capacitance conditions as used in Figure 1. An external N-channel MOSFET device pulls down the voltage on the side with 55pF capacitance; LTC4301L pulls down the voltage on the opposite side with a delay of 60ns.

OPERATION

This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows the high to low propagation delay as a function of temperature and voltage for 10k pull-up resistors pulled-up to V_{CC} and 100pF equivalent capacitance on both sides of the part. Larger output capacitances translate to longer delays (up to 150ns). Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

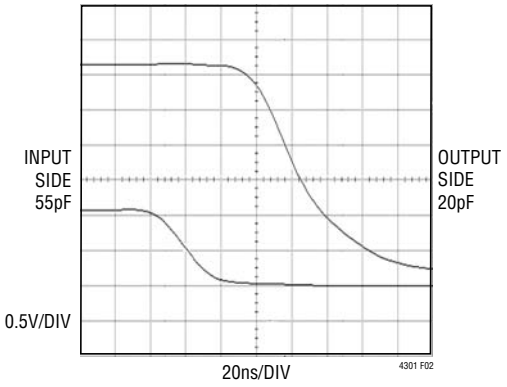


Figure 2. Input-Output Connection High to Low Propagation Delay

Ready Digital Output

This pin provides a digital flag which is low when either $\overline{CS}$ is high or the start-up sequence described earlier in this section has not been completed. READY goes high when $\overline{CS}$ is low and start-up is complete. The pin is driven by an open-drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor of 10k to V_{CC} to provide the pull-up.

Connection Sense

When the $\overline{CS}$ pin is driven above 1.4V with respect to the LTC4301L's ground, the backplane side is disconnected from the card side and the READY pin is internally pulled low. When the pin voltage is low, the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides. At this time the internal pulldown on READY releases.

APPLICATIONS INFORMATION

Live Insertion and Capacitance Buffering Application

Figure 3 illustrates applications of the LTC4301L with different bus pull-up and V_{CC} voltages, demonstrating its ability to recognize and buffer bus data levels that are above or below its V_{CC} supply. All of these applications take advantage of the LTC4301L's Hot Swap™ controlling, capacitance buffering and precharge features. If the I/O cards were plugged directly into the backplane without the LTC4301L buffer, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing an LTC4301L on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4301L drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4301L, which is less than 10pF.

In most applications the LTC4301L will be used with a staggered connector where V_{CC} and GND will be long pins. SDA and SCL are medium length pins to ensure that the V_{CC} and GND pins make contact first. This will allow the precharge circuitry to be activated on SDA and SCL before they make contact. $\overline{CS}$ is a short pin that is pulled up when not connected. This is to ensure that the connection between the backplane and the cards data and clock busses is not enabled until the transients associated with live insertion have settled.

Figure 4 shows the LTC4301L in an application where all of the pins have the same length. In this case, an RC filter circuit on the I/O card with a product of 10ms provides a filter to prevent the LTC4301L from becoming activated until the transients associated with live insertion have settled. Connect the capacitor between V_{CC} and $\overline{CS}$, and the resistor from $\overline{CS}$ to GND.

Hot Swap is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

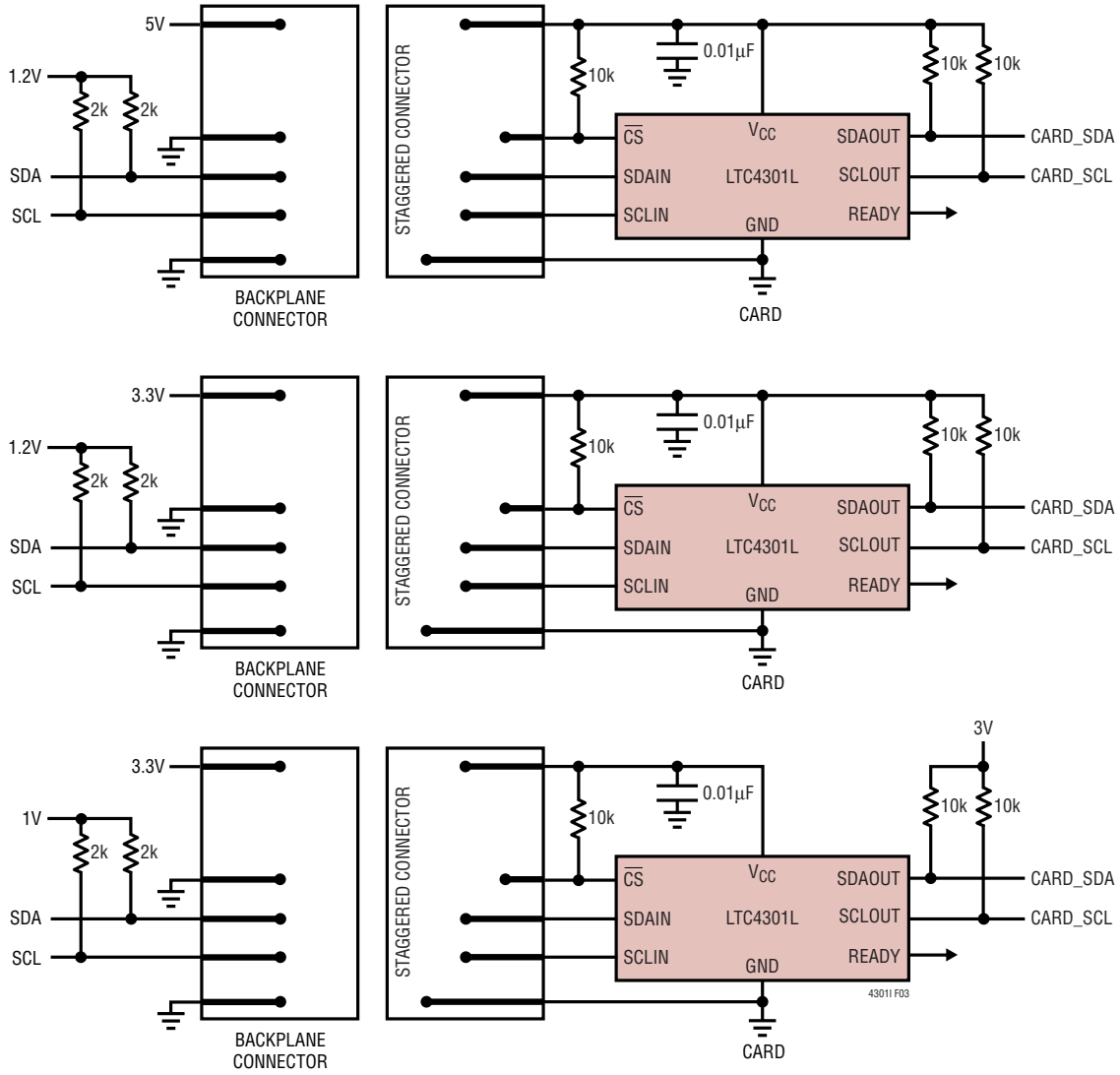


Figure 3. Typical Supply Independent Applications

APPLICATIONS INFORMATION

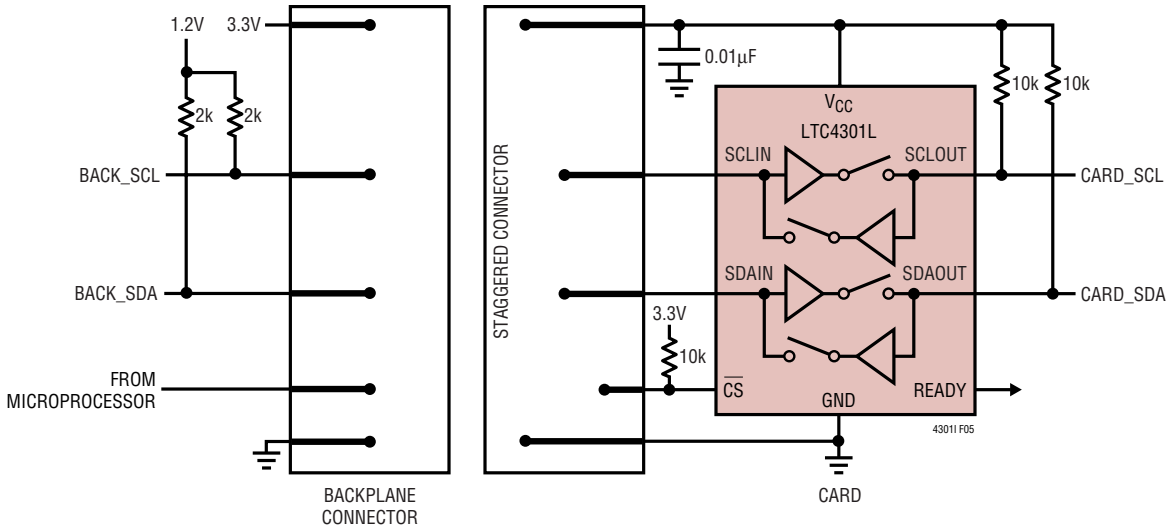
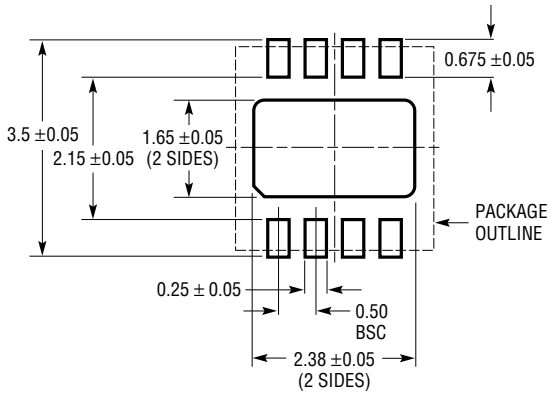


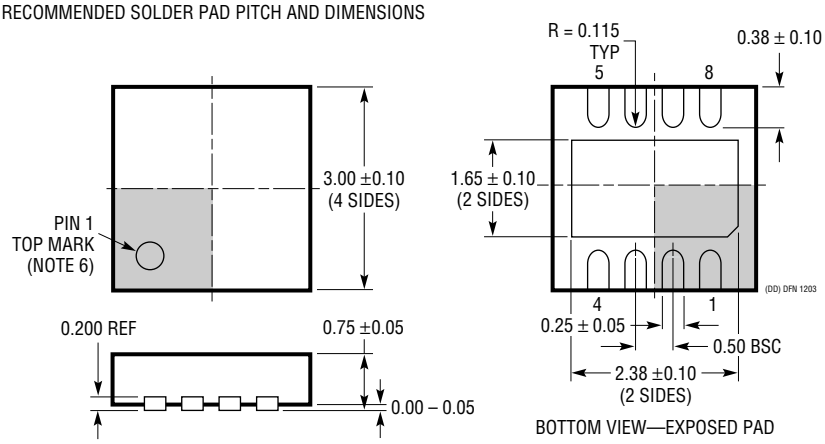
Figure 4. Inserting Multiple I/O Cards into a Live Backplane Using a Connector with All the Pins the Same Length

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

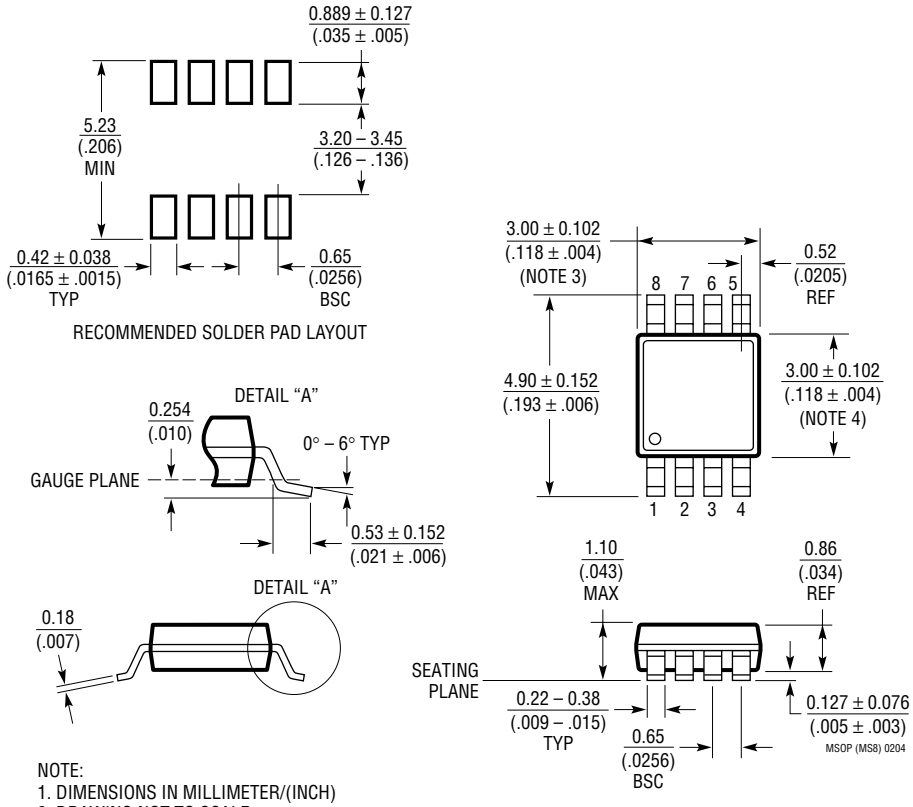


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX