Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery

FEATURES

- **Automatic Disconnect of SDA/SCL Lines when Bus is Stuck Low for ≥ 30ms**
- **Recovers Stuck Busses with Automatic Clocking***
- **Bidirectional Buffer* for SDA and SCL Lines Increases Fanout**
- **Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane**
- **Pin Compatible with LTC4300A-1**
- **±15kV Human Body Model ESD Protection**
- Isolates Input SDA and SCL Lines from Output
- Compatible with I²C™, I²C Fast-Mode and SMBus Standards (Up to 400kHz Operation)
- READY Open Drain Output
- 1V Precharge on All SDA and SCL Lines
- High Impedance SDA, SCL Pins for V_{CC} = 0V
- ENABLE Gates Connection from Input to Output
- MSOP 8-Pin and DFN (3mm × 3mm) Packages

APPLICATIONS

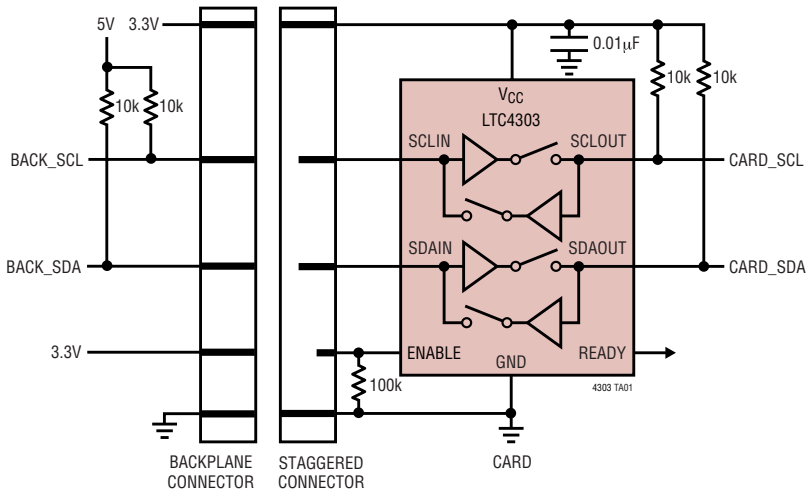
- Hot Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- RAID Systems

DESCRIPTION

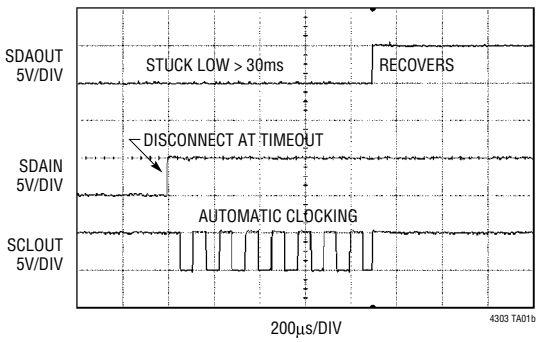
The LTC®4303 hot swappable 2-wire Bus Buffer allows I/O card insertion into a live backplane without corruption of the data and clock busses. When a connection is made, the LTC4303 provides bidirectional buffering, keeping the backplane and card capacitances isolated. If SDAOUT or SCLOUT is low for ≥ 30ms (typ), the LTC4303 automatically breaks the data and clock bus connection. At this time the LTC4303 automatically generates up to 16 clock pulses on SCLOUT in an attempt to free the bus. A connection will be enabled automatically when the bus becomes free.

Rise-time accelerator circuitry allows the use of larger pull-up resistance while still meeting rise-time requirements. During insertion, the SDA and SCL lines are precharged to 1V to minimize bus disturbances. When driven high, ENABLE allows the LTC4303 to connect after a stop bit or bus idle occurs. Driving ENABLE low breaks the connection between SDAIN and SDAOUT, SCLIN and SCLOUT. READY is an open drain output that indicates when the backplane and card sides are connected together.

TYPICAL APPLICATION



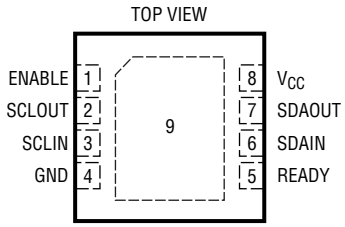
Stuck Bus Resolved with Automatic Clocking



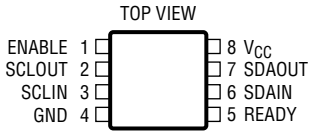
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

V_{CC} to GND .....–0.3V to 7V
SDAIN, SCLIN, SDAOUT, SCLOUT, READY, ENABLE.....–0.3V to 7V
Operating Temperature
LTC4303C ..... 0°C to 70°C
LTC4303I .....–40°C to 85°C
SDAIN, SCLIN, SDAOUT, SCLOUT, READY (Note 3).....30mA
Storage Temperature Range
MSOP .....–65°C to 150°C
DFN.....–65°C to 125°C
Lead Temperature (Soldering, 10sec)
MSOP ..... 300°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9)
PCB CONNECTION OPTIONAL



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER PART NUMBER	DD PART MARKING*	ORDER PART NUMBER	MS8 PART MARKING*
LTC4303CDD LTC4303IDD	LBPZ	LTC4303CMS8 LTC4303IMS8	LTBPY

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Supply Current, ENABLE = GND	V_{CC} = 5.5V, V_{SDAIN} = V_{SDAOUT} = 0V (Note 7) V_{CC} = 5.5V	●		6 1.5	8	mA mA
Startup Circuitry							
V_{PRE}	Precharge Voltage	SDA, SCL Floating, V_{CC} = 5.5V	●	0.8	1	1.2	V
T_{IDLE}	Bus Idle Time		●	60	95	175	µs
V_{OL_READY}	READY Output Low Voltage	I_{PULLUP} = 3mA I_{PULLUP} = 6mA, V_{CC} = 4.7V	● ●			0.4 0.4	V V
V_{THR_ENABLE}	ENABLE Threshold		●	0.8	1.4	2	V
I_{ENABLE}	ENABLE Input Current	ENABLE from 0 to V_{CC}	●		0.1	±1.5	µA
V_{THR}	SDA, SCL Logic Input Threshold Voltage	Rising Edge	●	1.6	1.8	2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{HYS}	SDA, SCL, Logic Input Threshold Voltage Hysteresis	(Note 6)			50		mV
t_{PHL_ENABLE}	Delay ENABLE High-Low to Disconnect	V_{CC} = 3.3V			300		ns
t_{PHL_READY}	Delay READY High-Low after Disconnect				10		ns
t_{PLH_ENABLE}	Delay ENABLE Low-High to Connect	V_{CC} = 3.3V	●	60	95	175	µs
t_{PLH_READY}	Delay READY Low-High after Connect				10		ns
I_{OFF_READY}	Ready Off Leakage Current		●			±10	µA
Rise-Time Accelerators							
$I_{PULLUPAC}$	Transient Boosted Pull-Up Current	Positive Transition on SDA, SCL, V_{CC} = 2.7V, Slew Rate = 0.8V/µs (Note 5)		2	3.5	5.5	mA
Bus Stuck Low Timeout							
$t_{TIMEOUT}$	Bus Stuck Low Timer	SDAOUT, SCLOUT = 0V	●	25	30	35	ms
Input-Output Connection							
V_{OS}	Input-Output Offset Voltage	10k to V_{CC} on SDA, SCL, 2.7k to V_{CC} on SDA, SCL V_{CC} = 3.3V, $V_{SDA/SCL}$ = 0.2V (Note 4)	● ●	40 50	80 100	120 150	mV mV
C_{IN}	Digital Input Capacitance SDAIN, SDAOUT, SCLIN, SCLOUT	(Note 6)				10	pF
$V_{IL, MAX}$	Input Logic Low Voltage		●			0.4	V
I_{LEAK}	Input Leakage Current	SDA, SCL, V_{CC} = 5.5V	●			±5	µA
V_{OL}	Output Low Voltage, Input = 0	SDA, SCL Pins, I_{SINK} = 4mA, V_{CC} = 2.7V	●	0	0.19	0.3	V
Timing Characteristics							
$f_{I2C, MAX}$	I^2C Maximum Operating Frequency	(Note 6)		400	600		kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 6)				1.3	µs
$t_{HD, STA}$	Hold Time After (Repeated) Start Condition	(Note 6)				100	ns
$t_{SU, STA}$	Repeated Start Condition Set-Up Time	(Note 6)				0	ns
$t_{SU, STO}$	Stop Condition Set-Up Time	(Note 6)				0	ns
$t_{HD, DATI}$	Data Hold Time Input	(Note 6)				0	ns
$t_{SU, DAT}$	Data Set-Up Time	(Note 6)				100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

Note 3: Pulsed less than 5µs.

Note 4: The connection circuitry always regulates the output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.

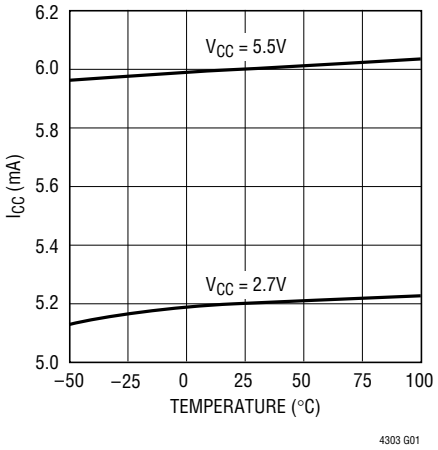
Note 5: $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage, as shown in the Typical Performance Characteristics section.

Note 6: Guaranteed by design, not tested in production.

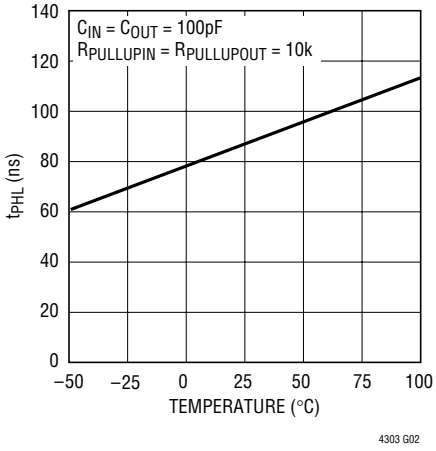
Note 7: I_{CC} test performed with connection circuitry active.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise indicated.

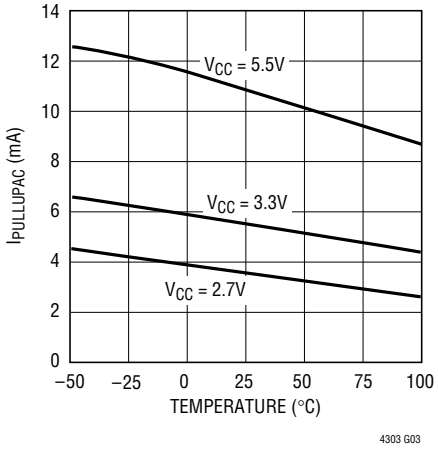
I_{CC} vs Temperature



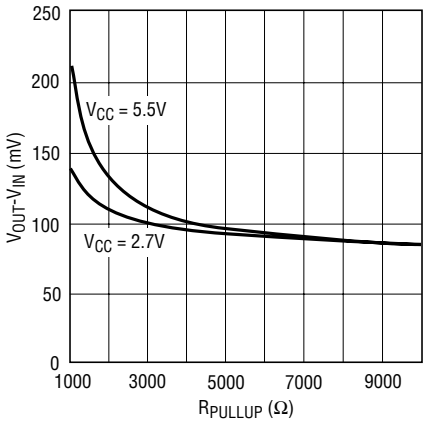
Input-Output t_{PHL} vs Temperature



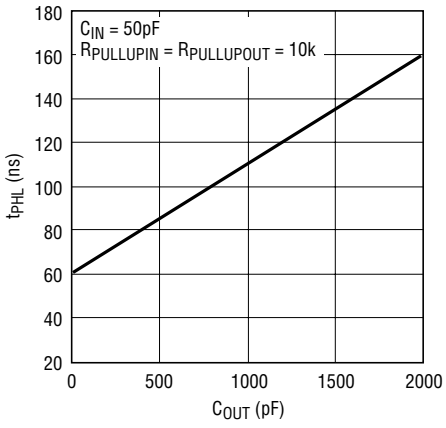
$I_{PULLUPAC}$ vs Temperature



Connection Circuitry V_{OUT} - V_{IN}



Input-Output t_{PHL} vs C_{OUT}



PIN FUNCTIONS

ENABLE (Pin 1): Connection Enable. This is a digital threshold input pin. For normal operation ENABLE is high. Driving ENABLE below 0.8V isolates SDAIN from SDAOUT, SCLIN from SCLOUT, asserts READY low and disables automatic clocking. A rising edge on ENABLE after a fault has occurred unconditionally forces a connection between SDAIN, SDAOUT and SCLIN, SCLOUT.

SCLOUT (Pin 2): Serial Clock Output. Connect this pin to the SCL bus on the card.

SCLIN (Pin 3): Serial Clock Input. Connect this pin to SCL on the bus backplane.

GND (Pin 4): Device Ground. Connect this pin to a ground plane for best results.

READY (Pin 5): Connection Status Flag. READY provides a digital flag which indicates the status of the connection circuitry described in the "Connection Circuitry" section. Connect a resistor of 10k to V_{CC} to provide the pull-up.

SDAIN (Pin 6): Serial Data Input. Connect this pin to the SDA bus on the backplane.

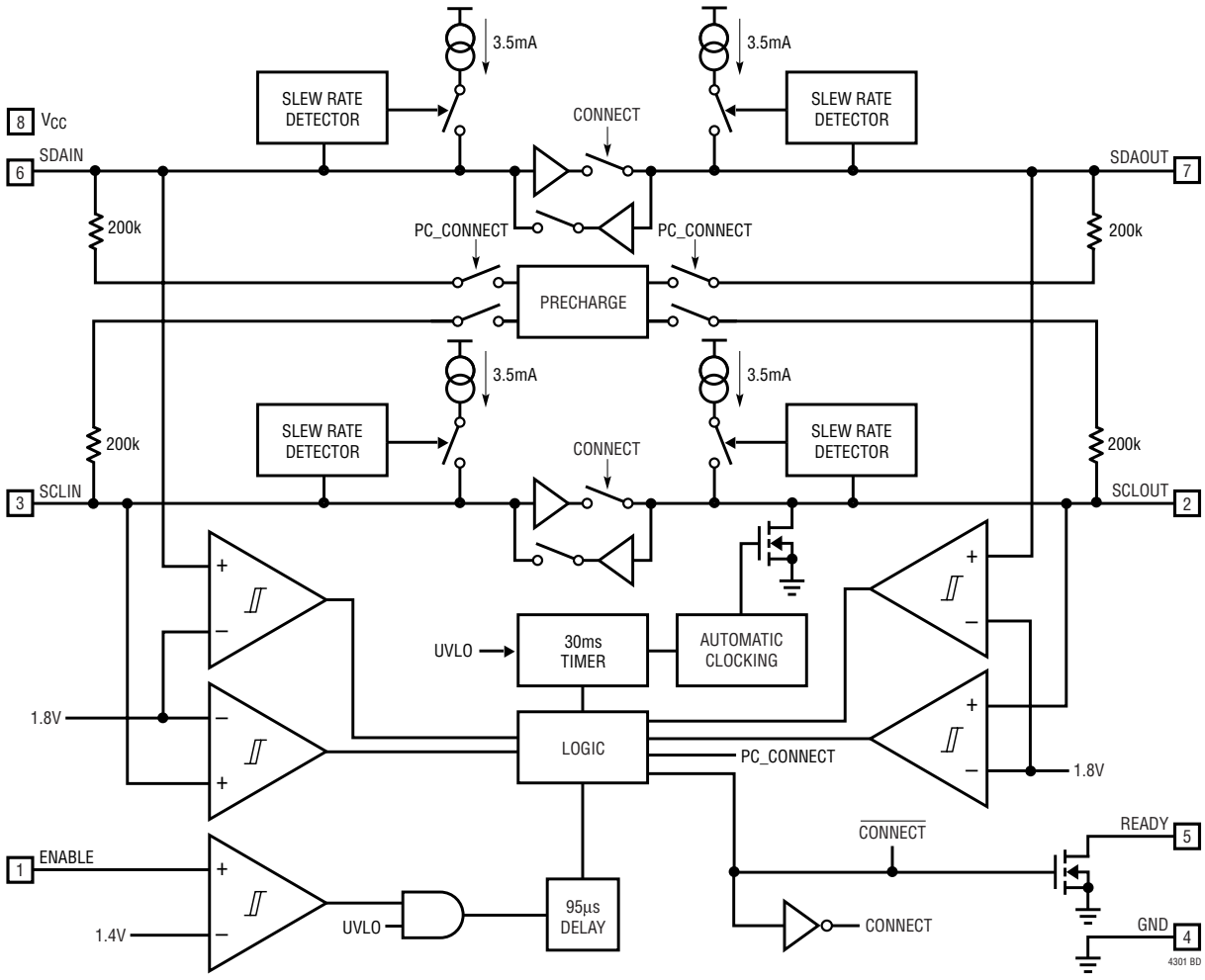
SDAOUT (Pin 7): Serial Data Output. Connect this pin to the SDA bus on the card.

V_{CC} (Pin 8): Supply Voltage Input. Place a bypass capacitor of at least 0.01µF close to V_{CC} for best results.

Exposed Pad (Pin 9, DFN Only): Exposed pad may be left open or connected to the ground plane.

BLOCK DIAGRAM

LTC4303 2-Wire Bus Buffer with Stuck Bus Protection



OPERATION

Start-Up

When the LTC4303 first receives power on its V_{CC} pin, either during power up or live insertion, it starts in an under voltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until V_{CC} rises above 2.5V (typical).

During this time, the precharge circuitry is active and forces 1V through 200k nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0V and V_{CC}. Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

Once the LTC4303 comes out of UVLO, it assumes that SDAIN and SCLIN have been inserted into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a stop bit or bus idle condition on the input side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane and READY goes high.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. **For proper operation, logic low input voltages should be no higher than 0.4V with respect to the ground pin voltage of the LTC4303.** SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4303.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms, as described here.

Input to Output Offset Voltage

When a logic low voltage, V_{LOW1}, is driven on any of the LTC4303's data or clock pins, the LTC4303 regulates the voltage on the opposite side of the part (call it V_{LOW2}) to a slightly higher voltage, as directed by the following equation:

$$V_{LOW2} = V_{LOW1} + 75mV + (V_{CC}/R) \bullet 20\Omega \text{ (typical)}$$

where R is the bus pull-up resistance in ohms. For example, if a device is forcing SDAOUT to 10mV where V_{CC} = 3.3V and the pull-up resistor R on SDAIN is 10k, then the voltage on SDAIN = 10mV + 75mV + (3.3/10000) • 20 = 91.6mV (typical). See the Typical Performance Characteristics section for curves showing the offset voltage as a function of V_{CC} and R.

Bus Stuck Low Time-Out

When SDAOUT or SCLOUT is low, an internal timer starts. The timer is only reset when SDAOUT and SCLOUT are both high. If they do not go high within 30ms (typical), the connection between SDAIN and SDAOUT, and SCLIN and SCLOUT is broken. After a delay of at least 40µs the LTC4303 automatically generates up to 16 clock pulses at 8.5kHz (typical) on SCLOUT in an attempt to unstick the bus. When SDAOUT and SCLOUT go high, reconnection occurs when the conditions described in the "Start-Up" section above are satisfied.

When powering up into a bus stuck low condition, the connection circuitry joining the SDA and SCL busses on the I/O card with those on the backplane is not activated. 30ms after UVLO, automatic clocking takes place as described above.

Propagation Delays

During a rising edge, the rise-time on each side is determined by the bus pull-up resistor and the equivalent capacitance on the line. If the pull-up resistors are the same, a difference in rise-time occurs which is directly proportional to the difference in capacitance between

OPERATION

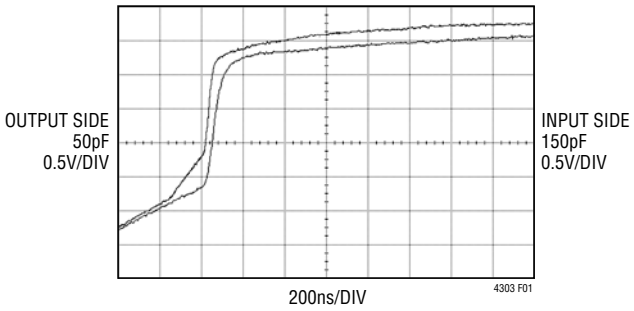


Figure 1. Input-Output Connection t_{PLH}

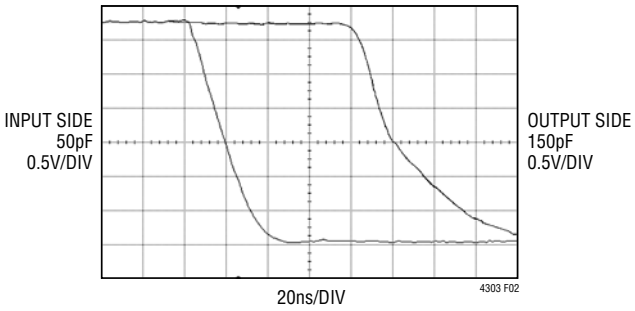


Figure 2. Input-Output Connection t_{PHL}

the two sides. This effect is displayed in Figure 1 for a V_{CC} = 3.3V and a 10k pull-up resistor on each side (50pF on one side and 150pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective t_{PLH} is negative.

There is a propagation delay, t_{PHL}, through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms. An external driver pulls down the voltage on the side with 50pF capacitance; LTC4303 pulls down the voltage on the opposite side with a delay of 80ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows t_{PHL} as a function of temperature and voltage for 10k pull-up resistors and 100pF equivalent capacitance on both sides of the part. Larger output capacitances translate to longer delays. Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

READY Digital Output

The READY pin provides a digital flag which indicates the status of the connection circuitry described previously in the "Connection Circuitry" section. READY is high when the connection circuitry is active, and pulls low when there is not a valid connection. The pin is driven by an open drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor of 10k to V_{CC} to provide the pull-up.

ENABLE

When the ENABLE pin is driven below 0.8V with respect to the LTC4303's ground, the backplane side is disconnected from the card side, and the READY pin is internally pulled low. When the pin is driven above 2V, the part waits for data transactions on the IN side to be complete and for the OUT side to be high (as described in the Start-Up section) before connecting the two sides. At this time the internal pull-down on READY releases. When ENABLE is low, automatic clocking is disabled.

A rising edge on ENABLE after a stuck bus condition has occurred forces a connection between SDAIN, SDAOUT and SCLIN, SCLOUT even if bus idle conditions are not met. At this time the internal 30ms timer is reset but not disabled.

Rise Time Accelerators

Once connection has been established, rise time accelerator circuits on all four SDA and SCL pins are activated. These allow the use of larger pull-up resistors, reducing power consumption, or bus capacitance beyond that specified in I^2C, while still meeting system rise time requirements. During positive bus transitions, the LTC4303 switches in 3.5mA (typical) of current to quickly slew the SDA and SCL lines once their DC voltages exceed 0.8V. Choose a pull-up resistor so that the bus will rise on its own at a rate of at least 0.8V/µs to guarantee activation of the accelerators. Rise time accelerators turn off when SDA and SCL lines are approximately 1V below V_{CC}.The rise time accelerators are automatically disabled during automatic clocking.

APPLICATIONS INFORMATION

Resistor Pull-Up Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 0.8V/µs on the SDA and SCL pins, in order to activate the rise time accelerators during rising edges. Choose maximum resistor value $R_{PULL\text{-}UP(MAX)}$ using the formula:

where V_{BUSMIN} is the minimum operating pull-up supply voltage, and C_{BUS} the total capacitance on respective bus line.

$$R_{PULLUP(MAX)}[k\Omega] = \frac{\left(V_{BUS(MIN)} - 0.8V\right) \bullet 1250[ns/V]}{C_{BUS}[pF]}$$

For example, assume $V_{BUS} = V_{CC} = 3.3V$, and assuming ±10% supply tolerance, $V_{BUSMIN} = 2.97V$. With C_{BUS} = 100pF, $R_{PULL\text{-}UP, MAX}$ = 27.1k. Therefore a smaller pull-up resistor than 27.1k must be used, so 10k works fine.

Live Insertion and Capacitance Buffering Application

Figures 3 through 6 illustrate applications of the LTC4303 that take advantage of both its Hot Swap™ controlling and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane without the LTC4303 buffer, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a LTC4303 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4303 drives the capacitance on the card side and the backplane must drive only the digital input capacitance of the LTC4303, which is less than 10pF.

In most applications the LTC4303 will be used with a staggered connector where V_{CC} and GND will be long pins. SDA and SCL are medium length pins to ensure that the V_{CC} and GND pins make contact first. This will allow the precharge circuitry to be activated on SDA and SCL before they make contact. ENABLE is a short pin that is pulled down when not connected. This is to ensure that the connection between the backplane and the cards data and clock busses is not enabled until the transients associated with live insertion have settled.

Figure 3 shows the LTC4303 in a CompactPCI™ configuration. Connect V_{CC} and ENABLE to the output of one of the CompactPCI power supply Hot Swap circuits. Use a pull-up resistor to ENABLE for a card side enable/disable. V_{CC} is monitored by a filtered UVLO circuit. With the V_{CC} voltage powering up after all the other pins have established connection, the UVLO circuit ensures that the backplane and the card data and clock busses are not connected until the transients associated with live insertion have settled. Owing to their small capacitance, the SDAIN and SCLIN pins cause minimal disturbance on the backplane busses when they make contact with the connector.

Figure 4 shows the LTC4303 in a PCI application where all of the pins have the same length. In this case, a RC filter circuit on the I/O card with a product of 10ms provides a filter to prevent the LTC4303 from becoming activated until the transients associated with live insertion have settled. Connect the capacitor between ENABLE and GND, and the resistor from V_{CC} to ENABLE.

Hot Swap is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

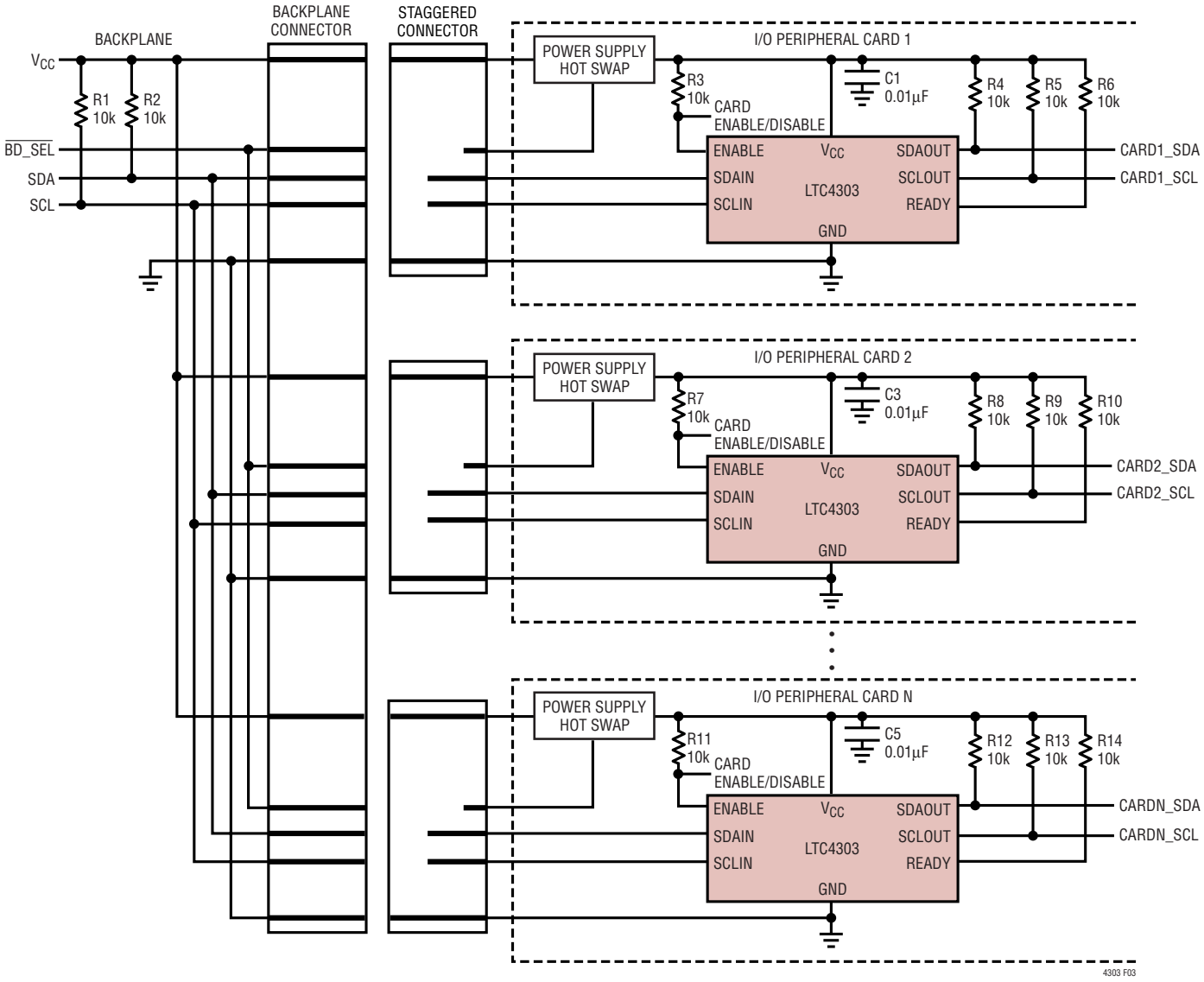


Figure 3. Inserting Multiple I/O Cards into a Live Backplane Using the LTC4303 in a CompactPCI System

APPLICATIONS INFORMATION

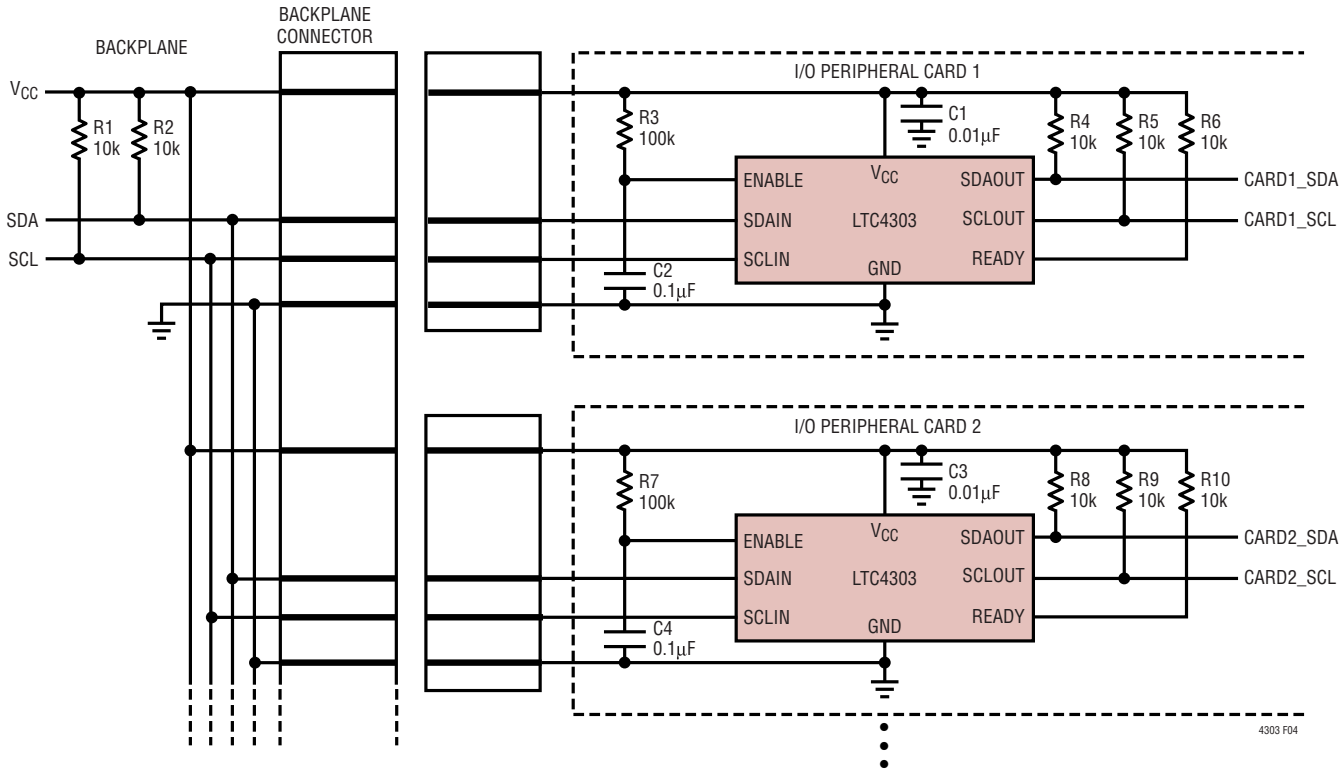


Figure 4. Inserting Multiple I/O Cards into a Live Backplane Using the LTC4303 in a PCI System

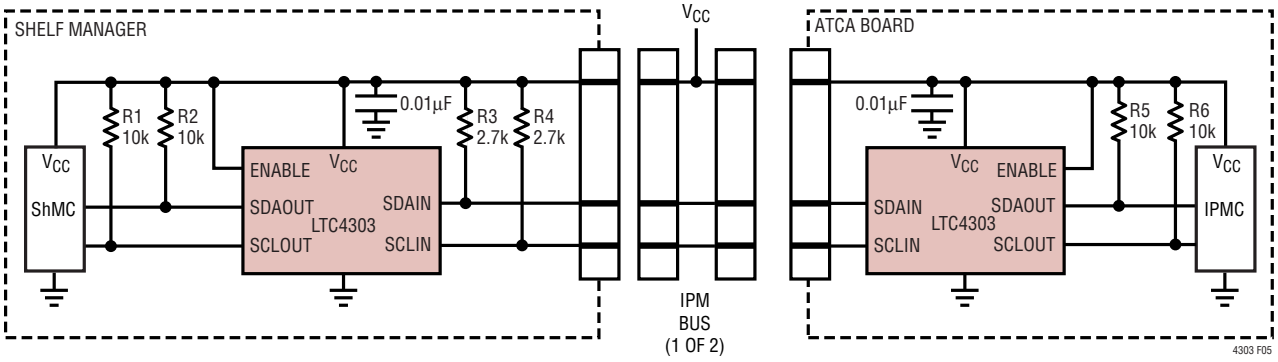
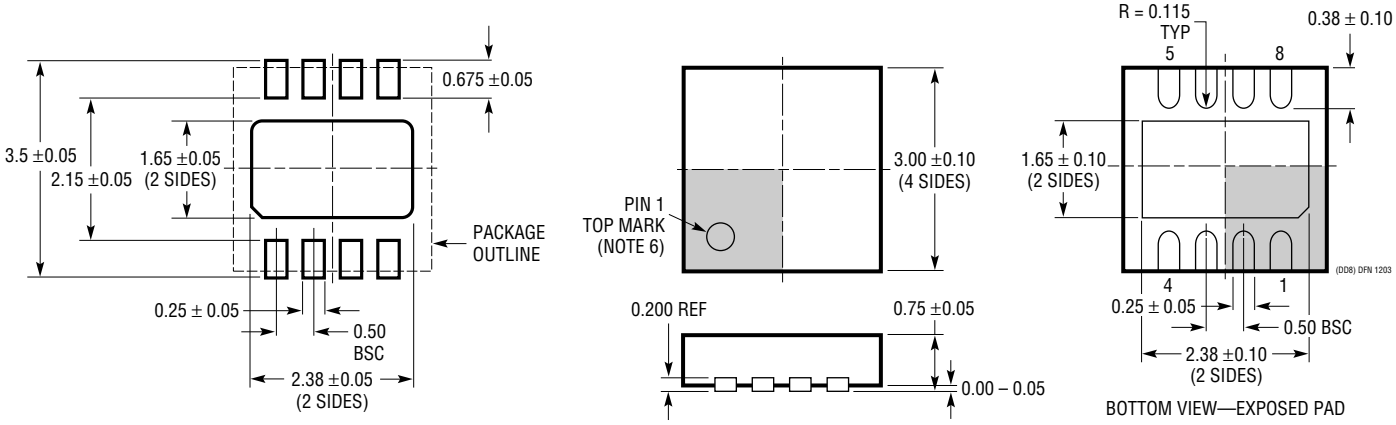


Figure 5. Simplified ATCA IPMB Application

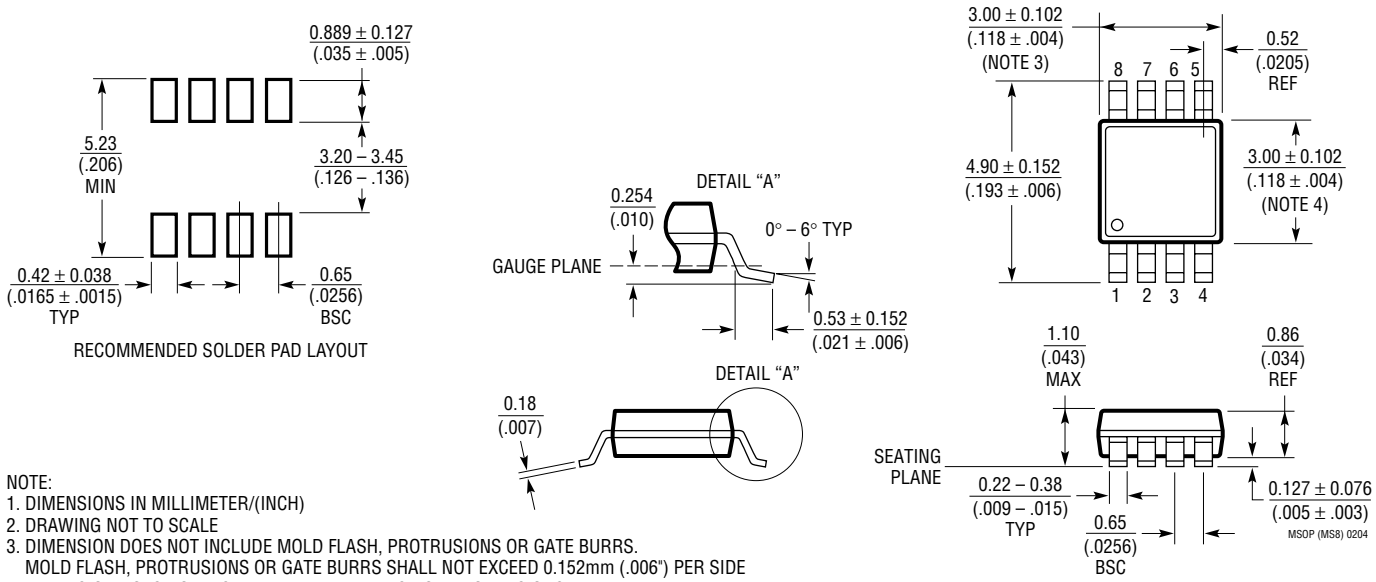
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX