High Definition Multimedia Interface (HDMI) Level-Shifting 2-Wire Bus Buffer

FEATURES

- **Bidirectional Buffer for Display Data Channel (DDC)**
- **Compliant with HDMI Specification Version 1.3 DDC Capacitance Requirement**
- **Level Translation Between 3.3V and 5V**
- **±5kV Human Body Model ESD Protection**
- **60mV Buffer Offset Independent of Load**
- **Compatible with Non-Compliant V_{OL} I^2C Devices**
- Isolates Input SDA and SCL Line from Output
- Compatible with I^2C™, I^2C Fast Mode and SMBus
- READY Open-Drain Output
- High Impedance SDA, SCL Pins for V_{CC} = 0V
- Small 8-Lead (3mm × 3mm) DFN and 8-Lead MSOP Packages

APPLICATIONS

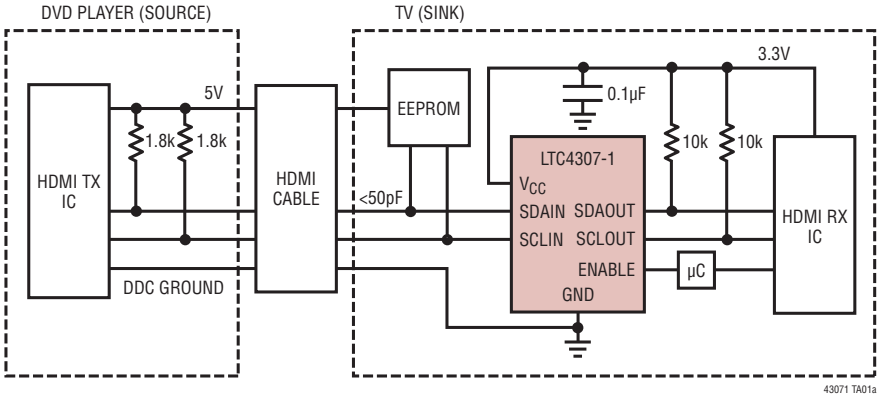
- HDMI
- 3.3V/5V Level Translation
- Capacitance Buffer/Bus Extender

DESCRIPTION

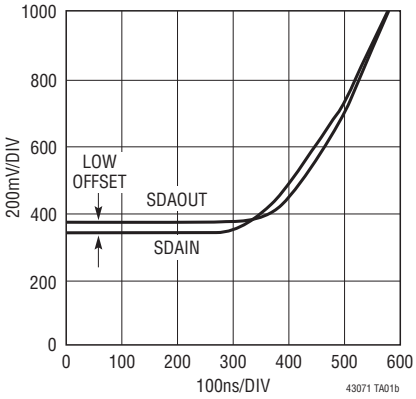
The LTC4307-1 is a 2-wire bus buffer that provides capacitance buffering between input and output. The HDMI specification requires that devices have less than 50pF of input capacitance on their DDC bus lines. The LTC4307-1's capacitance buffering feature, in conjunction with its sub-10pF data and clock input capacitance, allows HDMI components to easily meet the 50pF requirement and tolerate high capacitance on the internal bus.

The LTC4307-1 also provides level-shifting between 3.3V and 5V systems to allow lower voltage HDMI transmitters, receivers and EEPROM to interface to the 5V DDC bus. READY is an open-drain digital output flag that indicates whether or not the input and output busses are connected and can interface to the HDMI hot plug detect (HPD) signal. When driven high, the ENABLE digital input allows the LTC4307-1 to connect after a stop bit or bus idle. Driving ENABLE low breaks the connection between the input and output busses.

TYPICAL APPLICATION



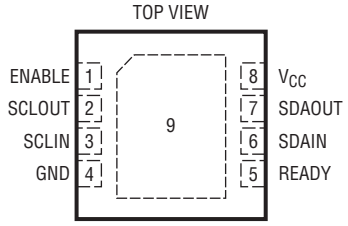
Rising Edge from Asserted Low



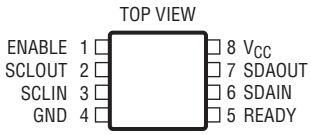
ABSOLUTE MAXIMUM RATINGS (Notes 1, 6)

V_{CC} to GND ..... –0.3V to 6V
SDAIN, SCLIN, SDAOUT, SCLOUT,
READY, ENABLE..... –0.3V to 6V
Maximum Sink Current (SDAIN, SCLIN, SDAOUT,
SCLOUT, READY)..... 50mA
Operating Temperature Range
LTC4307C ..... 0°C to 70°C
LTC4307I .....–40°C to 85°C
Storage Temperature Range
DFN.....–65°C to 125°C
MSOP .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4307CDD-1#PBF	LTC4307CDD-1#TRPBF	LDBP	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4307IDD-1#PBF	LTC4307IDD-1#TRPBF	LDBP	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4307CMS8-1#PBF	LTC4307CMS8-1#TRPBF	LTDBN	8-Lead Plastic MSOP	0°C to 70°C
LTC4307IMS8-1#PBF	LTC4307IMS8-1#TRPBF	LTDBN	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.3		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.5V, V_{SCLOUT} = V_{SDAOUT} = 0V (Note 5)	●		8	11	mA
I_{SD}	Shutdown Supply Current	V_{CC} = 5.5V, ENABLE = GND, SDA, SCL = 5.5V	●		900	1200	µA
t_{IDLE}	Bus Idle Time		●	55	95	175	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{THR_ENABLE}	ENABLE Threshold			0.8	1.4	2	V
I_{ENABLE}	ENABLE Input Current	ENABLE from 0V to V_{CC}	●		0.1	±5	µA
t_{PLH_EN}	ENABLE Delay Off-On	V_{CC} = 3.3V (Figure 1)			95		µs
t_{PHL_EN}	ENABLE Delay On-Off	V_{CC} = 3.3V (Note 3) (Figure 1)			10		ns
t_{PLH_READY}	READY Delay Off-On	V_{CC} = 3.3V (Note 3) (Figure 1)			10		ns
t_{PHL_READY}	READY Delay On-Off	V_{CC} = 3.3V (Note 3) (Figure 1)			10		ns
V_{OL_READY}	READY Output Low Voltage	I_{PULLUP} = 3mA, V_{CC} = 2.3V	●			0.4	V
I_{OFF_READY}	READY Off Leakage Current	V_{CC} = READY = 5.5V	●		0.1	±5	µA
Propagation Delay							
t_{PHL}	SDA/SCL Propagation Delay High to Low	C_{LOAD} = 50pF, 2.7k to V_{CC} on SDA, SCL, V_{CC} = 3.3V (Notes 2, 3) (Figure 1)			70		ns
t_{PLH}	SDA/SCL Propagation Delay Low to High	C_{LOAD} = 50pF, 2.7k to V_{CC} on SDA, SCL, V_{CC} = 3.3V (Notes 2, 3) (Figure 1)			10		ns
t_{FALL}	SDA/SCL Transition Time High to Low	C_{LOAD} = 100pF, 10k to V_{CC} on SDA, SCL, V_{CC} = 3.3V (Notes 3, 4) (Figure 1)			30	300	ns
Input-Output Connection							
V_{OS}	Input-Output Offset Voltage	2.7k to V_{CC} on SDA, SCL, V_{CC} = 3.3V, Driven SDA, SCL = 0.2V	●	20	60	100	mV
V_{THR}	SDA, SCL Logic Input Threshold Voltage	Rising Edge		0.45V_{CC}	0.55V_{CC}	0.65V_{CC}	V
V_{HYS}	SDA, SCL Logic Input Threshold Voltage Hysteresis	(Note 3)			50		mV
C_{IN}	Digital Input Capacitance SDAIN, SDAOUT, SCLIN, SCLOUT	(Note 3)				10	pF
I_{LEAK}	Input Leakage Current	SDA, SCL, Pins	●			±5	µA
V_{OL}	Output Low Voltage	SDA, SCL Pins, I_{SINK} = 4mA, SDAIN/SCLIN = 0.2V, V_{CC} = 2.7V	●	0		0.4	V
		2.7k to V_{CC} on SDA, SCL, V_{CC} = 3.3V, Driven SDA, SCL = 0.1V	●	120	160	205	mV
V_{ILMAX}	Buffer Input Logic Low Voltage	V_{CC} = 3.3V	●			1.2	V
Timing Characteristics							
$f_{I2C,MAX}$	I^2C Maximum Operating Frequency	(Note 3)		400	600		kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 3)				1.3	µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition	(Note 3)				100	ns
$t_{SU,STA}$	Repeated Start Condition Set-Up Time	(Note 3)				0	ns
$t_{SU,STO}$	Stop Condition Set-Up Time	(Note 3)				0	ns
$t_{HD,DATI}$	Data Hold Time Input	(Note 3)				0	ns
$t_{SU,DAT}$	Data Set-Up Time	(Note 3)				100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: See "Propagation Delays" in the Operations section for a discussion of t_{PHL} and t_{PLH} as a function of pull-up resistance and bus capacitance.

Note 3: Determined by design, not tested in production.

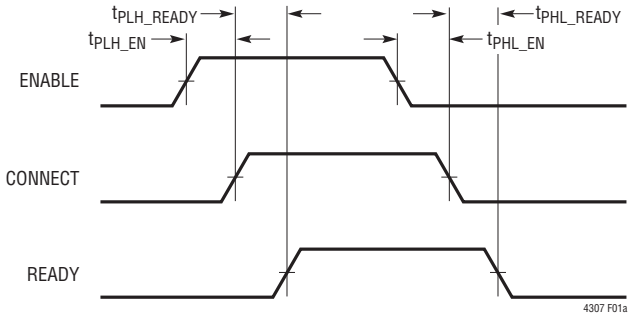
Note 4: Measure points are 0.3 • V_{CC} and 0.7 • V_{CC}.

Note 5: I_{CC} test performed with connection circuitry active.

Note 6: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

TIMING DIAGRAMS

ENABLE, CONNECT, READY Timing



Rising and Falling Propagation Delay and Rise and Fall Times for SDAIN, SDAOUT and SCLIN, SCLOUT

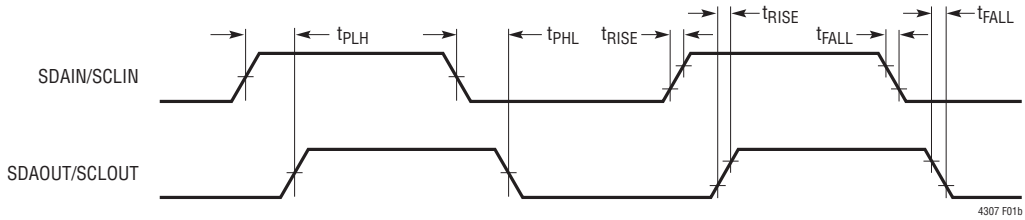
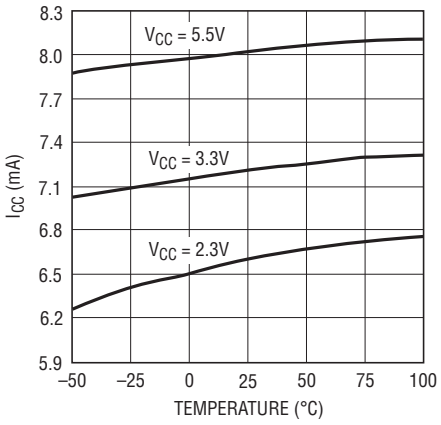


Figure 1. Timing Diagrams

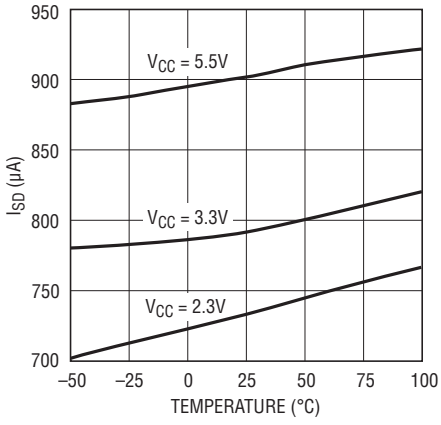
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{CC} = 3.3V, unless otherwise indicated.

I_{CC} vs Temperature



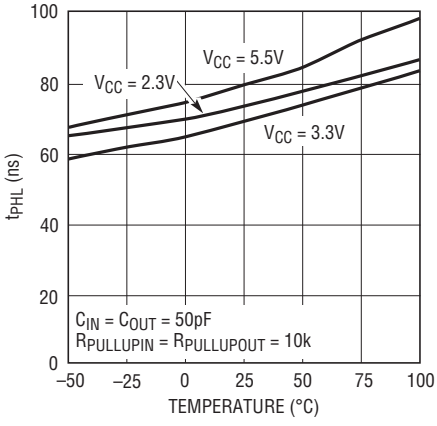
4307 G01

I_{SD} vs Temperature



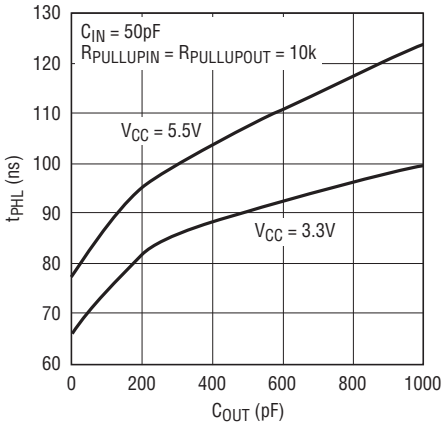
4307 G02

Input-Output High to Low Propagation Delay vs Temperature



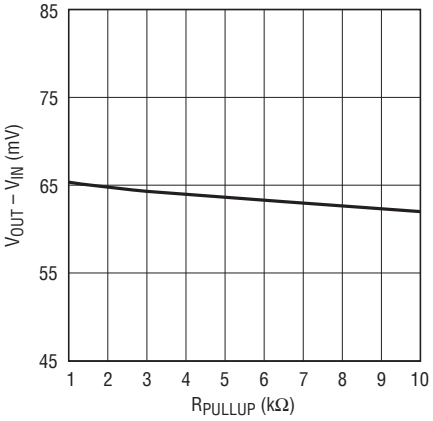
4307 G03

Input-Output High to Low Propagation Delay vs C_{OUT}



4307 G04

Connection Circuitry $V_{OUT} - V_{IN}$ (V_{OS})



4307 G05

PIN FUNCTIONS

ENABLE (Pin 1): Connection Enable Input. This is a 1.4V digital threshold input pin. For normal operation pull or tie ENABLE high. Driving ENABLE below 0.8V isolates SDAIN from SDAOUT, SCLIN from SCLOUT and asserts READY low. A rising edge on ENABLE after a fault has occurred forces a connection between SDAIN, SDAOUT and SCLIN, SCLOUT. Connect to V_{CC} if unused.

SCLOUT (Pin 2): Serial Clock Output. Connect this pin to the clock line of a DDC bus. A pull-up resistor should be connected between this pin and a supply voltage greater than or equal to the V_{CC} voltage.

SCLIN (Pin 3): Serial Clock Input. Connect this pin to the clock line of a DDC bus. A pull-up resistor should be connected between this pin and a supply voltage greater than or equal to the V_{CC} voltage.

GND (Pin 4): Device Ground. Connect this pin to a ground plane for best results.

READY (Pin 5): Connection READY Status Output. The READY pin is an open-drain N-channel MOSFET output that pulls low when ENABLE is low, or when the start-up and connection sequence described in the Operation section has not been completed. READY goes high when ENABLE is high and a connection is made. READY can be used to control the HDMI HPD signal. Connect a pull-up resistor, typically 10k, from this pin to V_{CC} to provide the pull-up. This pin can be floated if unused.

SDAIN (Pin 6): Serial Data Input. Connect this pin to the data line of a DDC bus. A pull-up resistor should be connected between this pin and a supply voltage greater than or equal to the V_{CC} voltage.

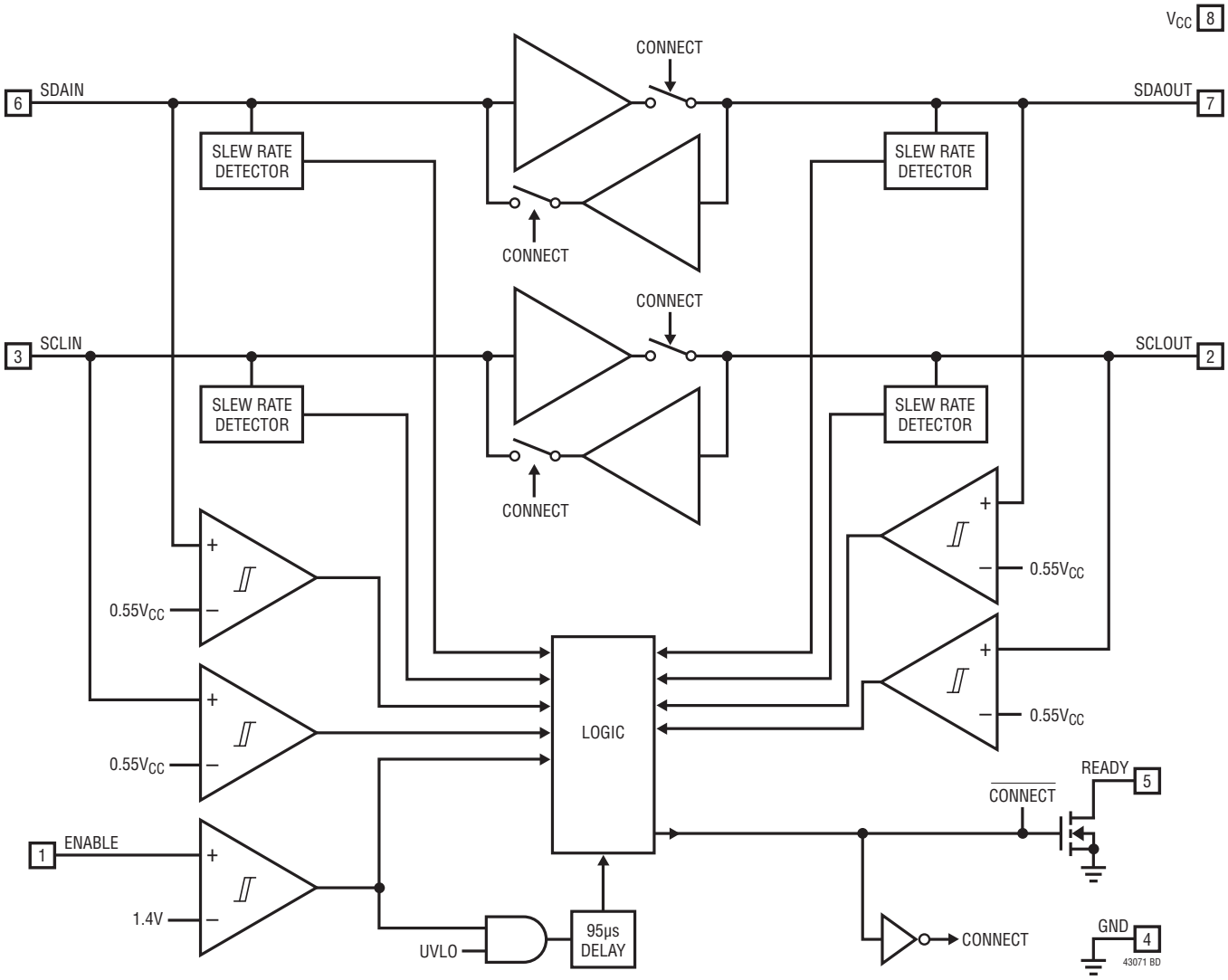
SDAOUT (Pin 7): Serial Data Output. Connect this pin to the data line of a DDC bus. A pull-up resistor should be connected between this pin and a supply voltage greater than or equal to the V_{CC} voltage.

V_{CC} (Pin 8): Supply Voltage Input. Place a bypass capacitor of at least 0.01µF close to V_{CC} for best results.

Exposed Pad (Pin 9, DFN Package Only): Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM

Low Offset Level-Shifting 2-Wire Bus Buffer



OPERATION

Start-Up

When the LTC4307-1 first receives power on its V_{CC} pin during power-up, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until V_{CC} rises above 2V (typ). This is to ensure that the LTC4307-1 does not try to function until it has enough voltage to do so.

Once the LTC4307-1 comes out of UVLO, it monitors both 2-wire busses for either a stop bit or bus idle condition to indicate the completion of data transactions. When both sides are idle or one side has a stop bit condition while the other is idle, the input-to-output connection circuitry is activated, joining SDAIN to SDAOUT and SCLIN to SCLOUT.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. The LTC4307-1 is tolerant of I^2C bus DC logic low voltages up to the $0.3V_{CC}$ V_{IL} I^2C specification.

When the LTC4307-1 senses a rising edge on the bus, it deactivates its pull-down devices for bus voltages as low as 0.48V. Care must be taken to ensure that devices participating in clock stretching or arbitration force logic low voltages below 0.48V at the LTC4307-1 inputs.

SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4307-1.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the capacitances of the two 2-wire busses isolated from each other. Placing an LTC4307-1 close to an HDMI port inside an HDMI transmitter or receiver allows the HDMI device to pass the capacitance compliance specification. Because of this isolation, the waveforms on SDAIN and SCLIN look slightly different than the corresponding waveforms on SDAOUT and SCLOUT as described here.

Input to Output Offset Voltage

When a logic low voltage, V_{LOW1}, is driven on any of the LTC4307-1's data or clock pins, the LTC4307-1 regulates the voltage on the opposite data or clock pins to a slightly higher voltage, typically 60mV above V_{LOW1}. This offset is practically independent of pull-up current (see the Typical Performance curves).

Propagation Delays

During a rising edge, the rise time on each side is determined by the bus pull-up resistor and the equivalent capacitance on the line. If the pull-up resistors are the same, a difference in rise time occurs which is directly proportional to the difference in capacitance between the two sides. Users must account for differences in the RC time constants between the two 2-wire busses and ensure that all system timing specifications are met on both busses.

There is a finite propagation delay through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms for V_{CC} = 5.5V, a 10k pull-up resistor on each side, 150pF parasitic capacitance on the input bus and 50pF on the output pins. An external N-channel MOSFET device pulls down the voltage on the side with 150pF capacitance; the LTC4307-1 pulls down the voltage on the opposite side with a delay of 80ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows propagation delay as a function of temperature and voltage for 10k pull-up resistors and 50pF equivalent capacitance on both sides of the part. Also, the t_{PHL} vs C_{OUT} curve for V_{CC} = 5.5V shows that increasing the

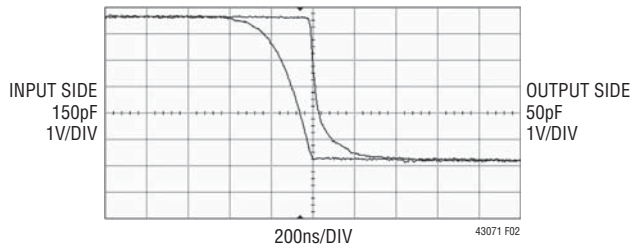


Figure 2. Input-Output Falling Edge Waveforms

OPERATION

capacitance from 50pF to 150pF results in a t_{PHL} increase from 81ns to 91ns. Larger output capacitances translate to longer delays (up to 125ns). Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

READY Digital Output

This pin provides a digital flag which is low when either ENABLE is low or the start-up sequence described earlier in this section has not been completed. READY goes high when ENABLE is high and the input and output 2-wire busses are connected. The pin is driven by an open-drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor to V_{CC} to provide the pull-up.

READY can be used to control the HDMI hot plug detect (HPD) signal to prevent the possibility of erroneous attempts by the source to contact the sink before the sink is ready to communicate.

ENABLE

When the ENABLE pin is driven below 0.8V with respect to the LTC4307-1's ground, the input 2-wire bus is disconnected from the output 2-wire bus and the READY pin is internally pulled low. When the pin is driven above 2V, the part waits for data transactions on both 2-wire busses to be complete (as described in the Start-Up section) before connecting the two sides. At this time the internal pull-down on READY releases.

LTC4307 and LTC4307-1 Feature Differences

The LTC4307-1 HDMI level-shifting 2-wire bus buffer is specifically intended for HDMI applications. Features in the general purpose LTC4307 device that are not required in HDMI systems have been removed. In addition, level-shifting functionality has been added to the LTC4307-1 to allow 3.3V HDMI devices to interface safely to the 5V HDMI DDC bus. See Table 1 for a list of the differences between the LTC4307 and LTC4307 -1.

Table 1. Differences Between the LTC4307 and the LTC4307-1

SPECIFICATION	LTC4307	LTC4307-1	COMMENTS ON LTC4307-1
Pre-charge	Yes	No	HDMI DDC Lines are Not Hot Swapped
Level Shifting	No	Yes, 2.2V to 5.5V	Provides Communication Between 3.3V and 5V DDC Busses, Protects 3.3V Devices from 5V Supply
Stuck Bus Disconnect and Recovery	Yes	No	Stuck Busses, Not an Issue in HDMI Systems
Rise Time Accelerators	Yes	No	Complies with HDMI Specification Version 1.3 DDC Capacitance Requirement

APPLICATIONS INFORMATION

Figure 3 shows the LTC4307-1 in a capacitance buffering application. Due to the LTC4307-1's capacitance buffering feature and sub-10pF input capacitance, this application circuit passes the HDMI 50pF maximum DDC capacitance specification easily when the LTC4307-1 is located right at the HDMI connector interface as shown. The capacitance of the internal bus connected to the SDAIN and SCLIN pins may be much larger than 50pF, but because of the LTC4307-1's capacitance buffering, the internal bus capacitance is isolated from the HDMI connector.

In HDMI, the sink device pulls the hot plug detect HPD signal high to tell the source that it is ready to accept commands through the DDC. This signal can be controlled through the READY pin of the LTC4307-1 to prevent the possibility of erroneous attempts by the source to contact the sink before the sink is ready to return its extended display identification data (EDID). The READY pin only goes high after 5V is applied and the LTC4307-1 ENABLE pin is pulled high by the HDMI receiver IC, a controller in the sink, or the 5V line itself.

APPLICATIONS INFORMATION

Figure 4 shows the LTC4307-1 being used for capacitance buffering and 5V to 3.3V level shifting. In this application, the EEPROM is powered by a backup 3.3V supply that is available when the component is turned off. The EDID in the EEPROM should be available for reading even when a component's power is off.

Although the applications shown in this section are for HDMI receive channels, the LTC4307-1 can also be used in HDMI transmit channels with equal success as shown in the Typical Application on the last page of this data sheet.

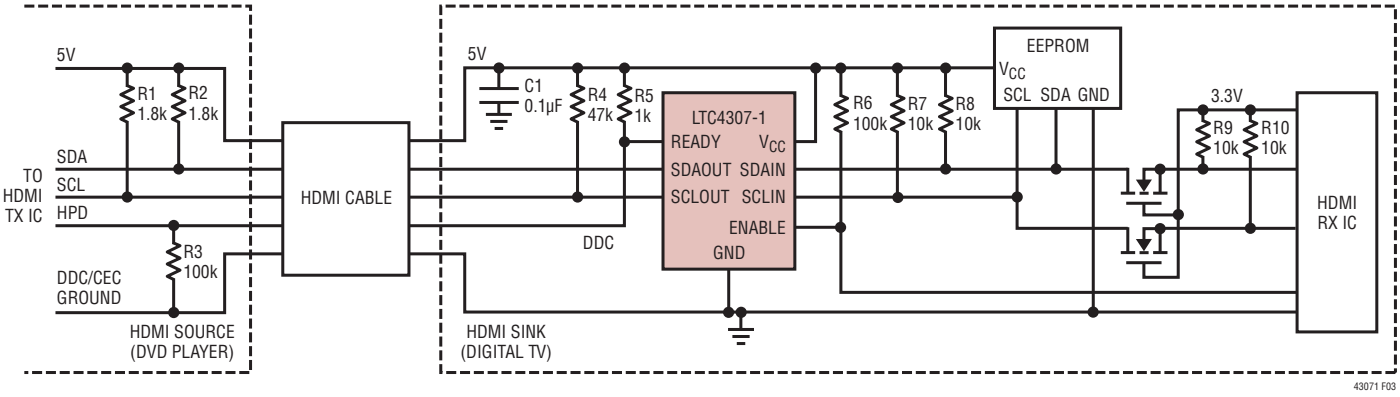


Figure 3. The LTC4307-1 in HDMI Capacitance Buffering Application

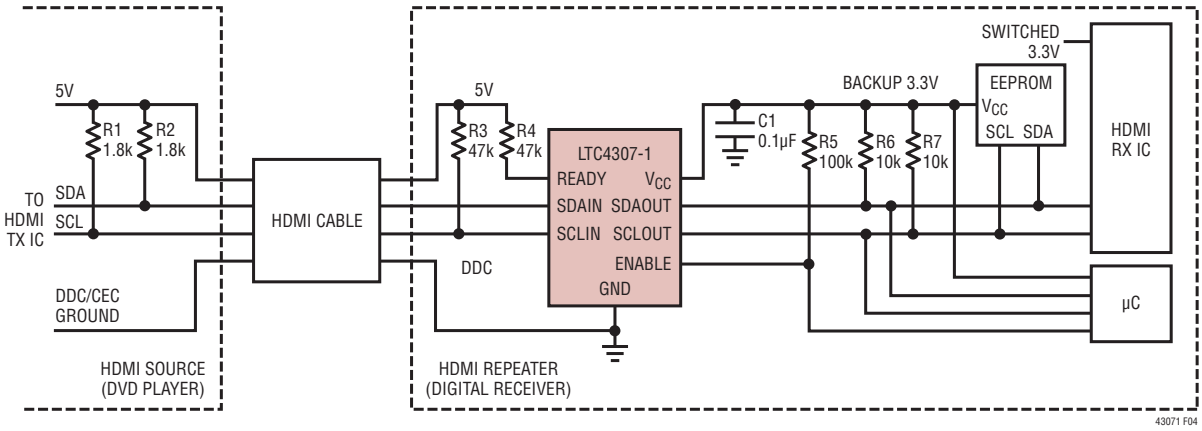
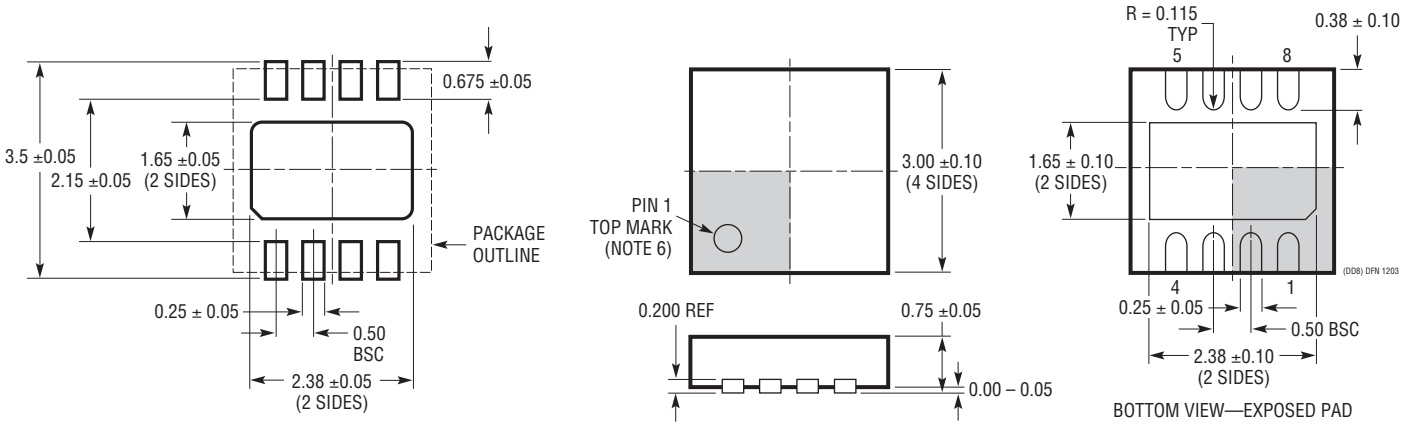


Figure 4. The LTC4307-1 in a Level Shifting and Capacitance Buffering HDMI Application with Backup 3.3V

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

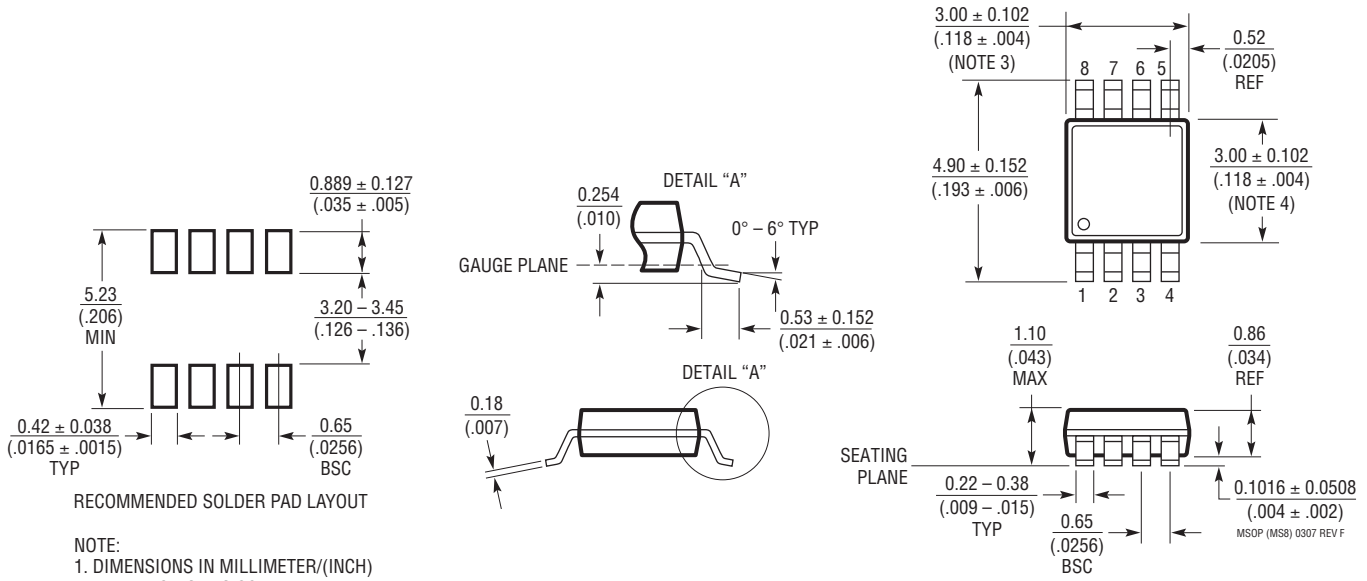


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX