Hot-Swappable I²C Isolators

FEATURES

- **Bidirectional I²C Communication Between Two Isolated Buses**
- **Full Isolation with Inexpensive Ethernet Transformers or Capacitors**
- **Low Voltage Level Shifting**
- **I²C Maximum Operating Frequency:**
  100kHz for LTC4310-1
  400kHz for LTC4310-2
- **I²C Specification Compliant V_{OL}, V_{IL}**
- ±5kV Human Body Model ESD Protection
- Rise Time Accelerators
- SDA, SCL Hot-Swapping
- Very Low Shutdown Current
- Stuck Bus Disconnect and Recovery
- Thermal Shutdown
- 10-Lead MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- Isolated I²C, SMBus and PMBus Interfaces
- Isolated Power Supplies
- Positive-to-Negative Rail Communications
- Power-over-Ethernet

DESCRIPTION

The LTC®4310 provides bidirectional I²C communications between two I²C buses whose grounds are isolated from one another. Each LTC4310 encodes I²C bus logic states into signals that are transmitted across an isolation barrier to another LTC4310. The receiving LTC4310 decodes the transmission and drives its I²C bus to the appropriate logic state. The isolation barrier can be bridged by an inexpensive Ethernet, or other transformer, to achieve communications across voltage differences reaching thousands of volts, or it can be bridged by capacitors for lower voltage isolation. The LTC4310-1 is intended for use in 100kHz I²C systems. The LTC4310-2 is intended for 400kHz I²C systems.

Rise time accelerators provide strong pull-up currents on SCL and SDA rising edges to meet rise time specifications for heavily loaded systems. Data and clock Hot Swap™ circuitry prevent data corruption when a card is inserted into or removed from a live bus. When a bus is stuck low for 37ms, the LTC4310 turns off its pull-down devices and generates up to sixteen clocks and a STOP bit in an attempt to free the bus. Driving EN low sets the LTC4310 in a very low current shutdown mode to conserve power.

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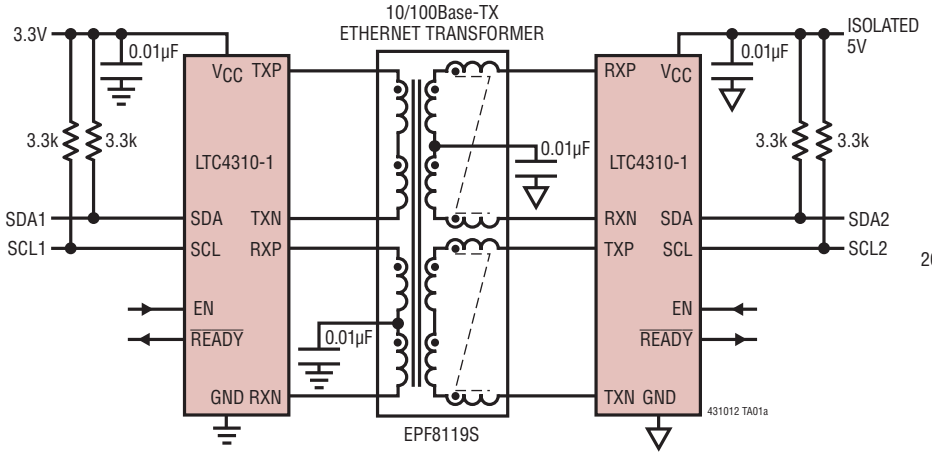
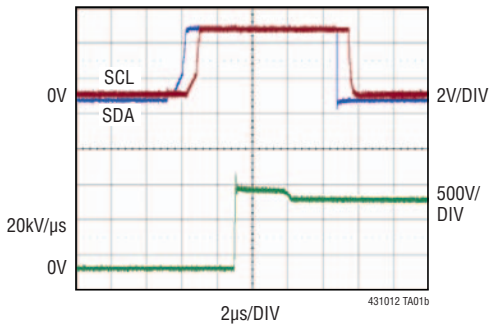
TYPICAL APPLICATION

1500V Isolated I²C System



LTC4310 Operating Through 20kV/µs Common Mode Transient

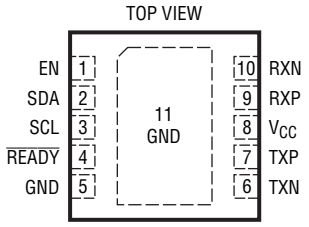


ABSOLUTE MAXIMUM RATINGS (Notes 1, 4)

Input Supply Voltage (V_{CC}) ..... –0.3V to 6V
Input and Bidirectional Pin Voltages
  SCL, SDA, EN, RXP, RXN..... –0.3V to 6V
Output Voltages
  $\overline{READY}$ ..... –0.3V to 6V
  TXP, TXN .....–0.3V to V_{CC} + 0.3V (6V Max)
Maximum Sink Current (SDA, SCL, $\overline{READY}$).....30mA

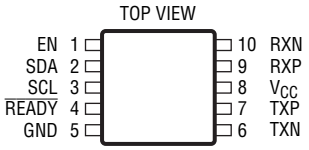
Operating Ambient Temperature Range
  LTC4310C ..... 0°C to 70°C
  LTC4310I..... –40°C to 85°C
Storage Temperature Range
  DD ..... –65°C to 125°C
  MS ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  MS Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) PCB CONNECTION TO GROUND IS OPTIONAL



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4310CDD-1#PBF	LTC4310CDD-1#TRPBF	LFCH	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4310IDD-1#PBF	LTC4310IDD-1#TRPBF	LFCH	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4310CMS-1#PBF	LTC4310CMS-1#TRPBF	LTFCG	10-Lead Plastic MSOP	0°C to 70°C
LTC4310IMS-1#PBF	LTC4310IMS-1#TRPBF	LTFCG	10-Lead Plastic MSOP	–40°C to 85°C
LTC4310CDD-2#PBF	LTC4310CDD-2#TRPBF	LFCK	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4310IDD-2#PBF	LTC4310IDD-2#TRPBF	LFCK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4310CMS-2#PBF	LTC4310CMS-2#TRPBF	LTFCJ	10-Lead Plastic MSOP	0°C to 70°C
LTC4310IMS-2#PBF	LTC4310IMS-2#TRPBF	LTFCJ	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	Input Supply Range		●	3		5.5	V
I_{CC}	Input Supply Current, LTC4310-1 Input Supply Current, LTC4310-2	EN = V_{CC} = 5.5V, SDA = SCL = $V_{SDA,SCL(OL)}$ EN = V_{CC} = 5.5V, SDA = SCL = $V_{SDA,SCL(OL)}$	● ●		6.5 7	8 8.5	mA mA
$I_{CC(SD)}$	Shutdown Input Supply Current	EN = 0V, V_{CC} = 5.5V	●		0.1	±10	µA
$V_{CCH(UVL)}$	Input Supply Undervoltage Lockout Rising Threshold Voltage		●	2.1	2.4	2.7	V
$V_{CC(UVL, HYST)}$	Input Supply Undervoltage Lockout Hysteresis		●	90	190	270	mV
I^2C Interface							
$V_{SDA,SCL(OL)}$	SDA, SCL Logic Low Output Voltage	$I_{(SDA,SCL)}$ = 4mA, 500µA; V_{CC} = 3V, 5.5V	●	310	350	380	mV
$V_{SDA,SCL(IL,R)}$	SDA, SCL Controlled Rising Edge Rate Turn-Off Threshold Voltage	V_{CC} = 3V, 5.5V (Note 5)	●	0.3 • V_{CC}	0.35 • V_{CC}	0.4 • V_{CC}	V
$V_{SDA,SCL(IL,F)}$	SDA, SCL Logic Low Falling Input Threshold Voltage	V_{CC} = 3V	●	0.4 • V_{CC}	0.45 • V_{CC}	0.5 • V_{CC}	V
$I_{SDA,SCL(OH)}$	SDA, SCL Input Current	SDA = SCL = 5.5V; V_{CC} = 0V, 5.5V	●		0	±5	µA
I^2C Interface Timing							
dV/dt_{RISE}	Bus Line Controlled Rising Edge Rate, LTC4310-1	0.35V < V_{BUS} < 0.35 • V_{CC}, V_{CC} = 3V 0.35V < V_{BUS} < 0.35 • V_{CC}, V_{CC} = 5.5V	● ●	0.8 1.5	1.16 2.14	1.4 2.6	V/µs V/µs
	Bus Line Controlled Rising Edge Rate, LTC4310-2	0.35V < V_{BUS} < 0.35 • V_{CC}, V_{CC} = 3V 0.35V < V_{BUS} < 0.35 • V_{CC}, V_{CC} = 5.5V	● ●	2 3.9	3 5.4	3.9 6.9	V/µs V/µs
$t_{PHL(SDA,SCL)}$	SDA, SCL High-to-Low Propagation Delay	V_{CC} = 5.5V (Note 3)	●		170	270	ns
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency	LTC4310-1 LTC4310-2	● ●	100 400			kHz kHz
C_{IN}	SCL, SDA Input Capacitance	SCL, SDA = V_{CC} (Note 2)				10	pF
Rise Time Accelerators							
V_{BOOST}	SDA, SCL Rise Time Accelerator Activation Threshold Voltage	V_{CC} = 3V (Note 5)	●	0.32 • V_{CC}	0.45 • V_{CC}	0.5 • V_{CC}	V
I_{BOOST}	SDA, SCL Rise Time Accelerator Current	V_{CC} = 3V	●	2	6		mA
$\overline{READY}$ Open-Drain Output							
$V_{\overline{READY}(OL)}$	$\overline{READY}$ Output Low Voltage	$I_{\overline{READY}}$ = 4mA	●		50	400	mV
$I_{\overline{READY}(OH)}$	$\overline{READY}$ Off-Current	$\overline{READY}$= V_{CC} = 5.5V, EN = 0V	●		0.1	±10	µA
Connection Control							
$V_{EN,RISE}$	EN Rising Threshold Voltage		●		0.6 • V_{CC}	0.9 • V_{CC}	V
$V_{EN,FALL}$	EN Falling Threshold Voltage		●	0.1 • V_{CC}	0.3 • V_{CC}		V
$I_{EN(OH)}$	EN Input Current	EN = V_{CC} = 5.5V	●		0.1	±10	µA
t_{IDLE}	Bus Idle Time		●	75	115	155	µs
t_{UVLO,EN_FILT}	Start-Up Filter Time		●	700	900	1200	µs
t_{STUCK}	SDA, SCL Bus Stuck Low Disconnect		●	27	37	47	ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{MAX(TX)}$	Maximum Time Between TXP, TXN Transmit Events		●	0.85	1.15	1.45	ms
$t_{MAX(RX)}$	Maximum Time Between RXP, RXN Receive Events		●	3.4	4.6	5.8	ms
Transmit Outputs							
$V_{TX(OL)}$	TXP, TXN Single-Ended Output Low	I_{SINK} = 100µA, V_{CC} = 3V	●		1.5	5	mV
$V_{TX(OH)}$	TXP, TXN Single-Ended Output High	15kΩ to GND on TXP, TXN; V_{CC} = 3V, 5.5V	●	0.95	1.25	1.52	V
$t_{R(TX)}$	TXP, TXN Output Rise Time	C_{TXP} , C_{TXN} = 20pF	●		1	3	ns
$t_{F(TX)}$	TXP, TXN Output Fall Time	C_{TXP} , C_{TXN} = 20pF	●		1	3	ns
$t_{PWMIN(TX)}$	TXP, TXN Minimum Transmission Pulse Width	V_{CC} = 3V, 5.5V	●	31.5	35	39	ns
Receive Inputs							
$V_{RX(TH)}$	RXP, RXN Differential High Level Threshold	RXP, RXN Pins; V_{CC} = 3V, 5.5V	●	0.3	0.5	0.875	V
$t_{PWMIN(RX)}$	RXP, RXN Minimum Received Pulse Width	V_{CC} = 3V, 5.5V	●	30			ns
$R_{RX(IN)}$	RXP, RXN Differential Input Resistance		●	13	16.5	20	kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. Guaranteed by design, not tested in production.

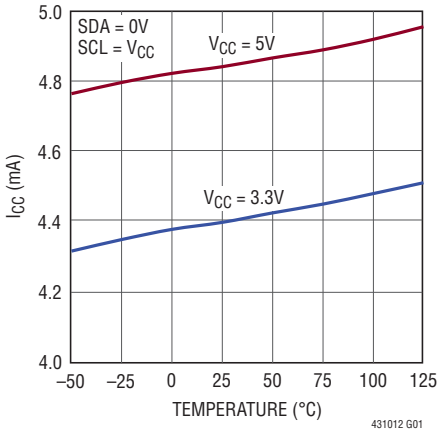
Note 3. SDA, SCL high-to-low propagation delay is measured from the beginning of a new received message telling the LTC4310 to drive its SDA, SCL pins from high to low, to when the SDA, SCL lines have fallen below 0.5 • V_{CC}. It includes approximately 87ns required for an LTC4310 to receive a message on the RXP and RXN pins, plus the time the LTC4310 requires to process the message and pass the low to the data and clock buffers, plus the time required by the buffers to drive their bus pins below 0.5 • V_{CC}.

Note 4. All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

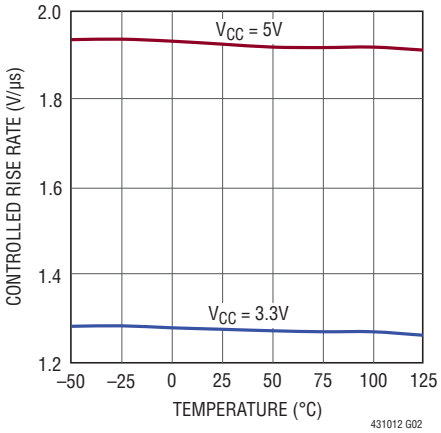
Note 5. Internal control circuitry prevents the rise time accelerators from activating until the rising edge rate control circuitry is off.

TYPICAL PERFORMANCE CHARACTERISTICS

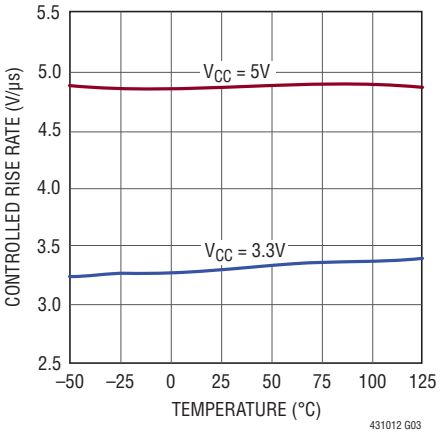
I_{CC} vs Temperature, LTC4310-1



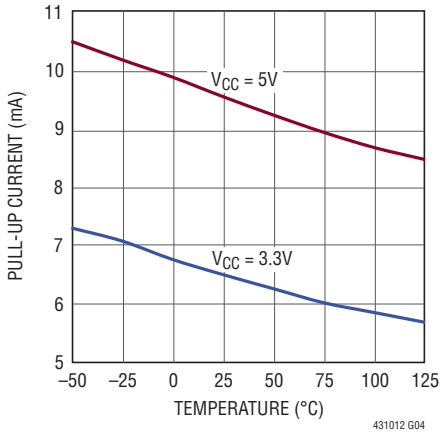
SDA, SCL Controlled Rising Edge Rate vs Temperature, LTC4310-1



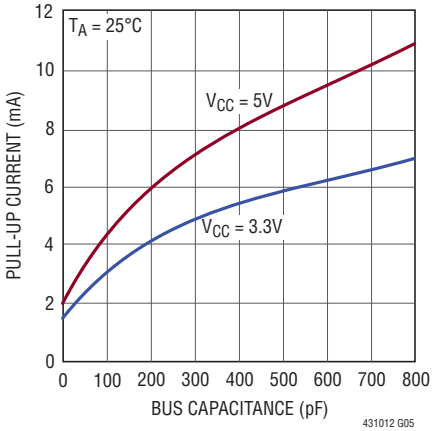
SDA, SCL Controlled Rising Edge Rate vs Temperature, LTC4310-2



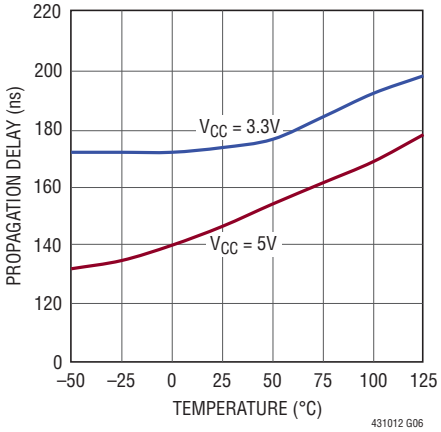
SDA, SCL Rise Time Accelerator Pull-Up Current vs Temperature



SDA, SCL Rise Time Accelerator Pull-Up Current vs Bus Capacitance



SDA,SCL Falling Propagation Delay vs Temperature



PIN FUNCTIONS

EN (Pin 1): Device Enable Input. Pulling EN up to V_{CC} sets the device in normal operation mode, allowing bus information to be sent and received across the barrier. Grounding EN disables communication across the barrier and debiases all internal circuitry, setting the device in a very low current shutdown mode. Connect to V_{CC} if unused.

SDA (Pin 2): Serial Bus Data Input/Output. This is the bidirectional data line for the two-wire bus. An external pull-up resistor or current source from SDA to a supply voltage greater than or equal to the V_{CC} voltage is required. See the Applications Information section for guidance on selecting the resistor or current source value. Do not leave open.

SCL (Pin 3): Serial Bus Clock Input/Output. This is the bidirectional clock line for the two-wire bus. An external pull-up resistor or current source from SCL to a supply voltage greater than or equal to the V_{CC} voltage is required. See the Applications Information section for guidance on selecting the resistor or current source value. Do not leave open.

$\overline{\text{READY}}$ (Pin 4): Device Receiving Indicator Output. $\overline{\text{READY}}$ is an open-drain digital output that pulls low when the LTC4310 is driving its SDA and SCL pins with the logic state information it is receiving on its RXP and RXN pins. Connect this pin to V_{CC} with a 10k resistor. This pin can be left open or tied to GND if unused.

GND (Pin 5): Device Ground.

TXN (Pin 6): Negative Transmit Output. Tie TXN to the negative side of the transformer primary winding or to the RXN pin of another LTC4310 through a ceramic capacitor. See the Applications Information section for guidance in selecting the capacitor value. Do not leave open.

TXP (Pin 7): Positive Transmit Output. Tie TXP to the positive side of the transformer primary winding or to the RXP pin of another LTC4310 through a ceramic capacitor. See the Applications Information section for guidance in selecting the capacitor value. Do not leave open.

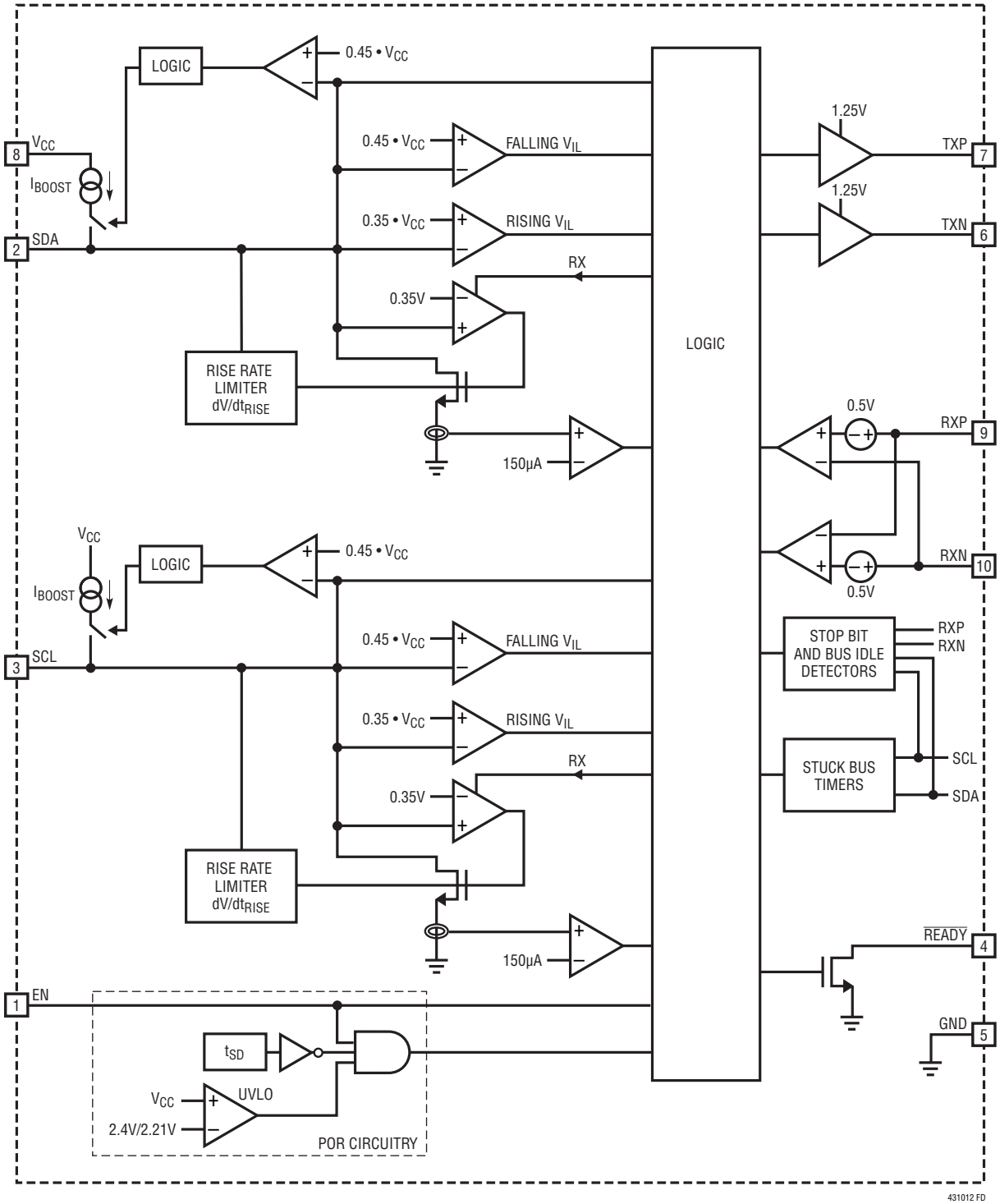
V_{CC} (Pin 8): Device Power Supply Input. Connect a bypass capacitor of at least 0.01µF directly between V_{CC} and GND.

RXP (Pin 9): Positive Receive Input. Tie RXP to the positive side of the transformer secondary winding or to the TXP pin of another LTC4310 through a ceramic capacitor. See the Applications Information section for guidance in selecting the capacitor value. Do not leave open.

RXN (Pin 10): Negative Receive Input. Tie RXN to the negative side of the transformer secondary winding or to the TXN pin of another LTC4310 through a ceramic capacitor. See the Applications Information section for guidance in selecting the capacitor value. Do not leave open.

Exposed Pad (Pin 11) DFN Package Only: The exposed pad may be left open or connected to device ground.

FUNCTIONAL DIAGRAM



OPERATION (LTC4310 refers to both LTC4310-1 and LTC4310-2)

The LTC4310 provides fully bidirectional communications between two I^2C or SMBus buses whose grounds are isolated from one another. Clock stretching, clock synchronization, arbitration and data acknowledging all work seamlessly across the barrier, regardless of the locations of the master(s) and slave(s).

Referring to the application circuit shown in Figure 1, an LTC4310 is located on each side of the isolation barrier. Each LTC4310 contains logic detection circuitry that can differentiate externally driven SDA and SCL logic signals from its own output signals. Each LTC4310 converts the logic state of the externally driven signals into a sequence of pulses that are then transmitted across the isolation barrier via an Ethernet transformer (or coupling capacitors for low isolation voltage applications) to the other LTC4310. Each LTC4310 also receives and decodes corresponding pulses from the other LTC4310 and drives its SDA and SCL pins accordingly.

Transmissions occur on the TXP and TXN pins in a sequence of 1.25V pulses. The LTC4310 receives messages on its RXP and RXN pins. Signals having less than 500mV differential voltages are rejected to provide noise immunity against common-mode transients.

When the LTC4310 receives a message to drive SDA low, it regulates SDA to 0.35V. If an external device pulls SDA below 0.35V during this time, the LTC4310 detects this condition and immediately transmits a LOW to the other LTC4310.

When an external pull-down device drives SDA below $0.45 \bullet V_{CC}$ from a logic high, TXP and TXN transmit a message across the isolation barrier instructing the other LTC4310 to drive its SDA line low.

When the external pull-down device turns off and SDA is rising between 0V and $0.35 \bullet V_{CC}$, the LTC4310 limits the bus rise rate to dV/dt_{RISE} via the rise rate limiter circuitry. It also transmits a high to the other LTC4310. If the SDA rise rate falls below the threshold, it is assumed that another pull-down on the bus has turned on and is pulling SDA low, and a command to pull the far side low is sent across the isolation barrier.

When SDA rises above $0.35 \bullet V_{CC}$, the rise rate limiter circuitry is deactivated. When SDA rises above $0.45 \bullet V_{CC}$, the rise time accelerator current I_{BOOST} is activated, which provides a strong, slew-limited pull-up current to reduce system rise time.

The LTC4310 contains power-on reset (POR) circuitry that sets the data and clock pins in a high impedance state and deactivates the transmit and receive circuitry until the EN voltage is high, the device is not in thermal shutdown and the V_{CC} voltage is above the 2.4V UVLO threshold voltage. The LTC4310 enters thermal shutdown when the die temperature exceeds 150°C. Grounding EN sets the LTC4310 in a near-zero current mode.

After the LTC4310 exits POR, STOP bit and bus idle detector circuitry monitors the logic state of its own SDA and SCL bus and of the other I^2C bus in the system via RXP and RXN. When a STOP bit or bus idle occurs simultaneously on both I^2C buses, the LTC4310 activates its SDA and SCL drivers, logic detection circuitry and rise time accelerators and drives $\overline{READY}$ low.

The stuck bus timer and recovery circuitry disable the SDA and SCL driver, logic detection circuitry and rise time accelerators if the bus is low for 37ms. A stuck bus also causes $\overline{READY}$ to be released high. If the stuck bus releases high, the I^2C driver and accelerator circuitry are reactivated when a STOP bit or bus idle occurs simultaneously on both I^2C buses, as previously described.

OPERATION

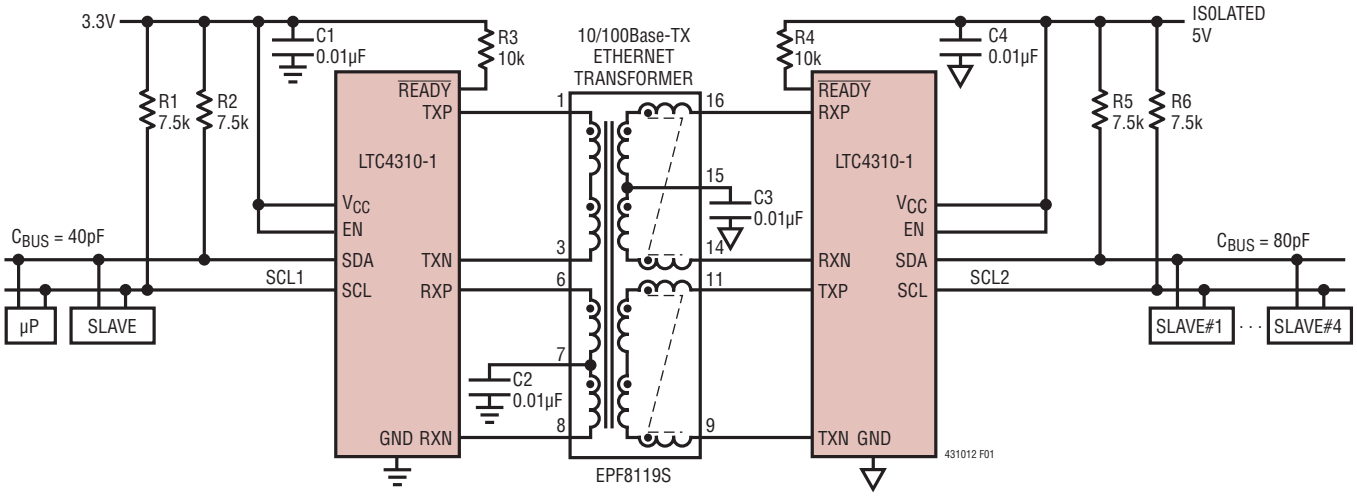


Figure 1. The LTC4310-1 in a Transformer Isolated Application

APPLICATIONS INFORMATION

SDA, SCL Bus Pull-Up Resistor Value Selection

When the SDA (or SCL) bus is rising between 0V and 0.35 • V_{CC}, the LTC4310 controls the bus rise rate to (0.35 • V_{CC})/900ns for the LTC4310-1 and to (0.35 • V_{CC})/300ns for the LTC4310-2. Users must quantify their parasitic bus capacitance, C_{BUS}, and choose a bus pull-up resistor, R_{BUS}, based on their bus pull-up supply voltage and maximum bus switching frequency to ensure that each bus rises faster than the controlled rise rate. For bus frequencies up to 100kHz, choose the LTC4310-1 and refer to Figure 2 for the maximum pull-up resistance to use. For bus frequencies between 100kHz and 400kHz, choose the LTC4310-2 and refer to Figure 3 for the maximum pull-up resistance to use. Be sure to include worst-case resistor tolerance when selecting resistor value.

Rise Time Accelerators

The LTC4310's rise time accelerator circuitry on the SDA and SCL lines turns on during rising edges to reduce the bus rise time. When the bus has risen above 0.45 • V_{CC}, the LTC4310 turns on a strong, slew-limited pull-up current, I_{BOOST}, to help even heavily loaded buses meet the rise time specifications. See the Typical Performance Characteristics section for the rise time accelerator pull-up current as a function of temperature and bus capacitance. When either the bus has risen above (V_{CC} – 1V) or 300ns after the pull-up current has turned on (whichever comes first), the LTC4310 deactivates its pull-up current to deter fighting with the subsequent falling edge. Users must ensure that the bus pull-up supply voltage $V_{BUS} \geq V_{CC}$, so that the accelerators do not overdrive the SDA, SCL bus and source current into V_{BUS}. The rise time accelerators are deactivated during start-up, thermal shutdown, shutdown and after disconnection due to a stuck bus or failure to receive a transmission within 4.6ms.

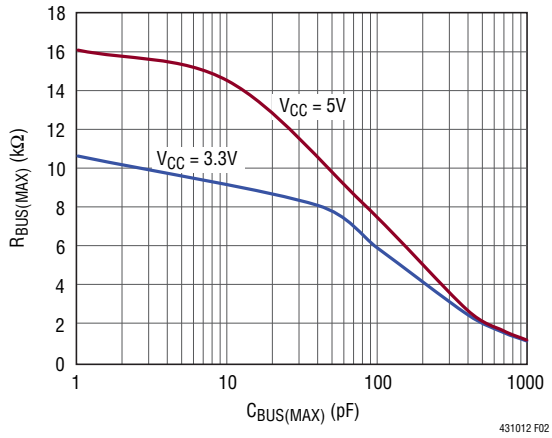


Figure 2. Maximum SDA,SCL Bus Pull-Up Resistor Value as a Function of Parasitic Bus Capacitance for the LTC4310-1

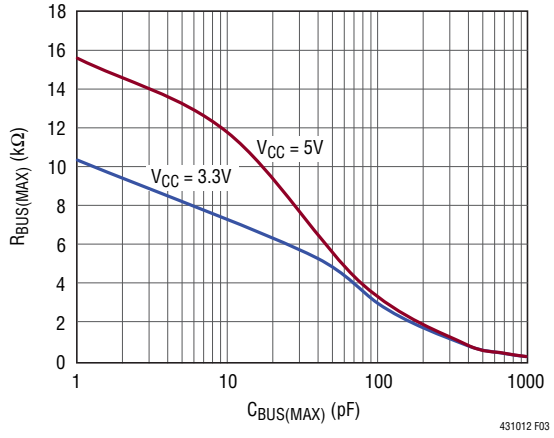


Figure 3. Maximum SDA,SCL Bus Pull-Up Resistor Value as a Function of Parasitic Bus Capacitance for the LTC4310-2

APPLICATIONS INFORMATION

Bus Rising Edge Waveform

When all external pull-downs on SCL1 (Figure 1) turn off, the SCL1 rising waveform will resemble that shown in Figure 4. The LTC4310-1 senses that SCL1 is rising and transmits a message to the other LTC4310-1 to release SCL2 high. During the transmission, the first LTC4310-1 also drives SCL1 to 0.35V, so that when the transmission is complete, both buses will rise simultaneously from 0.35V at a rate of $(0.35 \bullet V_{CC})/900ns$. This functionality minimizes the effective skew between the two buses. When SCL1 reaches $0.35 \bullet V_{CC}$, the LTC4310-1 deactivates its rise rate regulation circuitry. The bus then rises with a time constant of $(R_{BUS} \bullet C_{BUS})$ until it reaches $0.45 \bullet V_{CC}$, at which point the I_{BOOST} rise time accelerator pull-up current is activated.

Figure 5 shows SCL1 and SCL2 for an entire 100kHz switching cycle. Because the LTC4310-1 regulates the bus rise rate to $(0.35 \bullet V_{CC})/900ns$, the 5V bus signal rises more quickly than the 3.3V bus signal. Both buses reach $(0.35 \bullet V_{CC})$ in approximately 900ns, so the effective skew between the buses is nearly zero. The LTC4310-2 functions the same as the LTC4310-1, except the controlled rise rate is limited to $(0.35 \bullet V_{CC})/300ns$.

Start-Up, Data and Clock Hot Swap Circuitry

The LTC4310 contains power-on reset (POR) circuitry that sets the data and clock pins in a high impedance state and deactivates the transmit circuitry until the EN voltage is high, the device is not in thermal shutdown and the V_{CC} voltage is above 2.4V. After the LTC4310 exits the POR state, it activates its transmit circuitry and communicates its SDA, SCL logic states across the barrier to the other LTC4310 via its TXP and TXN pins.

The receive circuitry remains deactivated for an additional 900µs after the LTC4310 exits POR. The 900µs filter time is required for the LTC4310 to charge its RXP and RXN pins to their DC bias voltage, assuming a 0.01µF common-mode noise filtering capacitor at the center-tap of the secondary side of the external transformer. When the filter time has elapsed, the LTC4310 activates its receive circuitry and decodes the messages it receives on its RXP and RXN pins, registering the logic state of the remote I^2C bus.

When both the local and remote two-wire buses are "quiet" (i.e., no data transactions are occurring on either bus), the LTC4310 then drives its $\overline{READY}$ pin low to indicate that it has linked the logic state of the local I^2C bus with the logic state of the remote I^2C bus. This means that the LTC4310 will now drive its SDA and SCL pins to the logic state of the remote I^2C bus, as specified by the messages it receives on RXP and RXN. The LTC4310 considers a two-wire bus

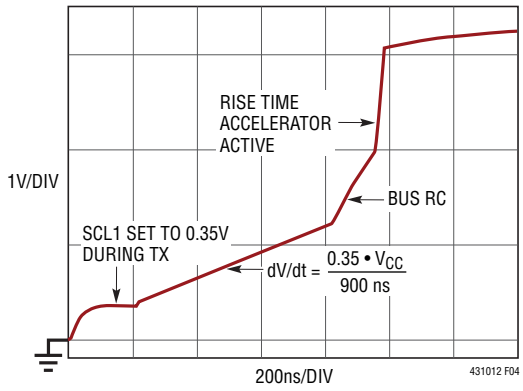


Figure 4. SCL1 Rising Waveform of SCL1 for Application Circuit Shown in Figure 1

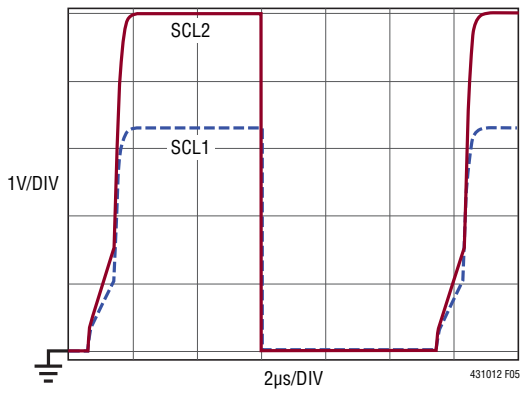


Figure 5. 100kHz SCL Waveforms for Application Circuit Shown in Figure 1

APPLICATIONS INFORMATION

quiet if it has been idle high for at least 115µs, or if a STOP bit has occurred and both data and clock have remained high since the STOP bit. This functionality makes the LTC4310 ideal for hot-swapping cards into and out of a live I^2C system. The threshold voltages for the STOP bit and bus idle comparators are $0.5 \bullet V_{CC}$.

Stuck Bus Disconnect and Recovery

An internal timer runs whenever SDA, SCL or both are low. The timer is only reset when both SDA and SCL are high. If the timer does not reset within 37ms, the LTC4310 assumes the bus is stuck low. Accordingly, it ceases driving its SDA and SCL pins and transmits a special message across the barrier to inform the other LTC4310. Upon receiving this message, the other LTC4310 also ceases driving its SDA and SCL pins. At least 40µs after determining the bus is stuck low, the LTC4310 generates up to sixteen clock cycles on SCL in an attempt to make the slave release the SDA line. The LTC4310 stops issuing clocks when the SDA line releases high, or after sixteen cycles, whichever comes first. Once the clock pulses have completed, the LTC4310 issues a STOP bit on SDA and SCL to reset all devices on the bus.

The LTC4310 reactivates its amplifiers and rise time accelerators when the bus releases high and a STOP bit or bus idle occurs on both the local and isolated buses, as previously described in the Start-Up, Data and Clock Hot Swap Circuitry section. The stuck bus disconnect and recovery circuitry is disabled when the LTC4310 is in UVLO, thermal shutdown and low current shutdown.

Transmit and Receive Circuitry

Transmissions occur on the TXP and TXN pins whenever the externally driven SDA or SCL logic state changes – in other words, transmissions are event driven. In addition, if SDA and SCL do not change state for 1.15ms, the LTC4310 retransmits the logic state. The TXP and TXN pins are driven in a pseudo differential fashion. Both pins are driven to ground when inactive and are driven to 1.25V (typical) in matched sets of alternating 35ns pulses to send information across the barrier to the other LTC4310.

The LTC4310 receives and decodes the pulses sent by the other LTC4310 on its RXP and RXN pins. Assuming the start-up sequence previously described has been completed, the LTC4310 drives its SDA and SCL lines to the logic state dictated by the decoded RXP and RXN signals. The LTC4310 rejects RXP and RXN signals having less than 500mV magnitude to provide noise immunity against common-mode transients. The parasitic capacitances of the LTC4310's RXP and RXN pins and their associated board traces form a capacitive divider with the transmit/receive coupling capacitors, as shown in Figure 6. To guarantee robust communications, minimize the parasitic capacitance CPAR by minimizing the trace length from the coupling capacitors to the RXP and RXN pins and choose coupling capacitor values, CRXP and CRXN, that are at least ten times larger than CPAR.

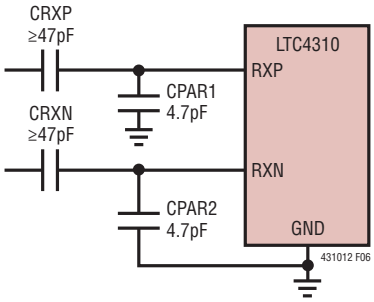


Figure 6. Parasitic Trace and Pin Capacitances Form a Capacitive Divider with C_{RXP} and C_{RXN}. Ensure C_{RXP} , $C_{RXN} \geq 10 \bullet C_{PAR}$

If the LTC4310 has not received a message in 4.6ms, it assumes there is a communication problem and ceases driving its SDA and SCL pins. It also transmits a special message to the other LTC4310 to inform it that it is no longer driving its SDA and SCL bus. Upon receiving this message, the other LTC4310 also ceases driving its SDA and SCL pins. Once the communication problem is resolved, both LTC4310's reactivate their amplifiers and rise time accelerators after a STOP bit or bus idle has occurred on both buses, as previously described in the Start-Up, Data and Clock Hot Swap Circuitry section.

Thermal Shutdown

If the die temperature of the LTC4310 exceeds 150°C, the LTC4310 enters a thermal shutdown mode. It sets TXP and TXN to a high impedance state, ceases driving SDA and SCL, and ignores the signals on RXP and RXN. When the temperature drops back below 130°C, the LTC4310 goes through the POR sequence previously described.

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Once a STOP bit or bus idle occurs on both the local and isolated buses, the LTC4310 reactivates its buffers and rise time accelerators.

$\overline{\text{READY}}$ Digital Output

The $\overline{\text{READY}}$ pin provides a digital output flag that pulls low to indicate that the LTC4310 is driving its SDA and SCL pins with the logic state information it is receiving on its RXP and RXN pins from the other LTC4310. $\overline{\text{READY}}$ is driven by an N-channel MOSFET open-drain pull-down that is capable of sinking 4mA while holding 0.4V maximum. The pull-down turns off whenever the LTC4310 is not driving its SDA and SCL pins—during start-up, thermal shutdown, low current shutdown and after disconnection due to a stuck bus or failure to receive a transmission within 4.6ms. Connect a resistor to the bus pull-up supply to provide the pull-up.

Design Example: High Voltage Isolation Using an Inexpensive Ethernet Transformer

Figure 1 shows the LTC4310-1 providing I^2C communications between two buses whose ground voltages can differ up to 1500V. An EPF8119S Ethernet transformer is used to bridge the isolation barrier. The left I^2C bus connects to the LTC4310-1 and two other devices, resulting in a bus parasitic capacitance of 40pF in this example set-up. Referring to the V_{CC} = 3.3V curve in Figure 2, 7.5k pull-up resistors are chosen for R1 and R2. The right I^2C bus connects to another LTC4310-1 and four slave devices, resulting in a bus parasitic capacitance of 80pF. Referring to the V_{CC} = 5V curve in Figure 2, 7.5k pull-up resistors are also chosen for R5 and R6. Standard 5% resistors are used.

Sudden changes in the ground differential across the isolation barrier can be effectively resisted by tying the center tap of the receive side of the transformer to the local ground through a 0.01µF capacitor, as shown by capacitors C2 and C3.

Figure 7 shows the same application as Figure 1, but with each LTC4310-1 replaced by an LTC4310-2, so that the bus can switch at frequencies up to 400kHz. To meet the requirements shown in the curves of Figure 3, R1 and R2 are changed from 7.5k to 4.3k, and R5 and R6 are changed from 7.5k to 3.3k.

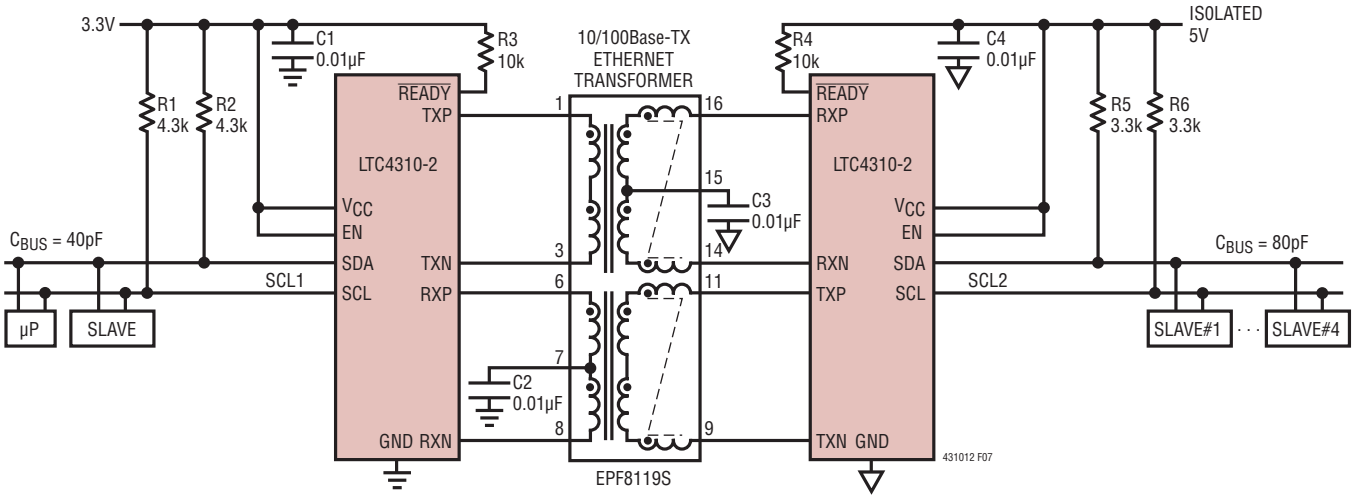

Figure 7. The LTC4310-2 in a 400kHz Application

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS

Figure 8 shows the LTC4310-1 providing I²C communications between an I²C bus referenced to system ground and an I²C bus using –5V for its ground reference. Ceramic coupling capacitors, C1-C5, are used to bridge the isolation barrier. This circuit is recommended for ground isolation voltages less than 100V and is limited by the voltage rating of C1-C5. Higher voltage ceramic capacitors may be used to achieve higher isolation voltages. Because the LTC4310 uses a pseudo-differential transmit scheme, capacitor C5 must be connected between ground and –5V to provide a return path for the transmitted current.

Figure 9 shows the LTC4310-1 in an application circuit using its zero current shutdown mode. A microprocessor only activates the left LTC4310-1 when it needs to communicate with the isolated I²C bus. Because the LTC4310-1 contains a STOP bit and bus idle detection circuitry, there is no danger of connecting in the middle of a message when the microprocessor asynchronously reenables the LTC4310-1.

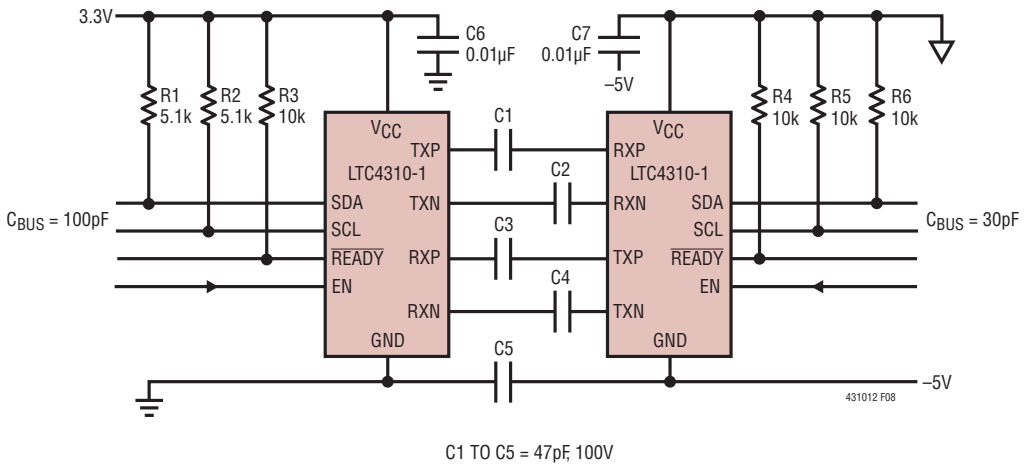

Figure 8. Low Voltage I²C Isolation Between a Ground Referenced Bus and a –5V Referenced Bus

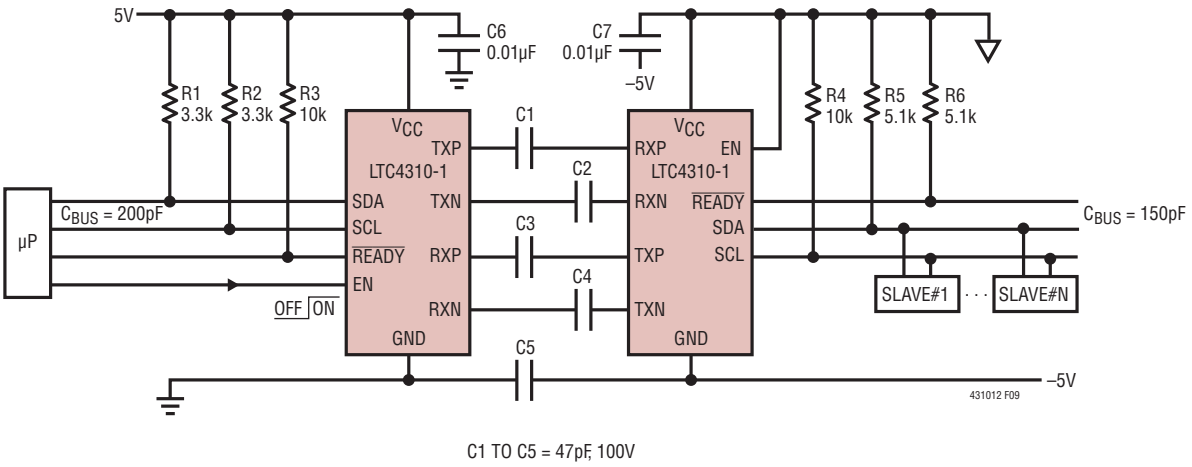

Figure 9. The LTC4310-1 in a Zero Current Shutdown Application

APPLICATIONS INFORMATION

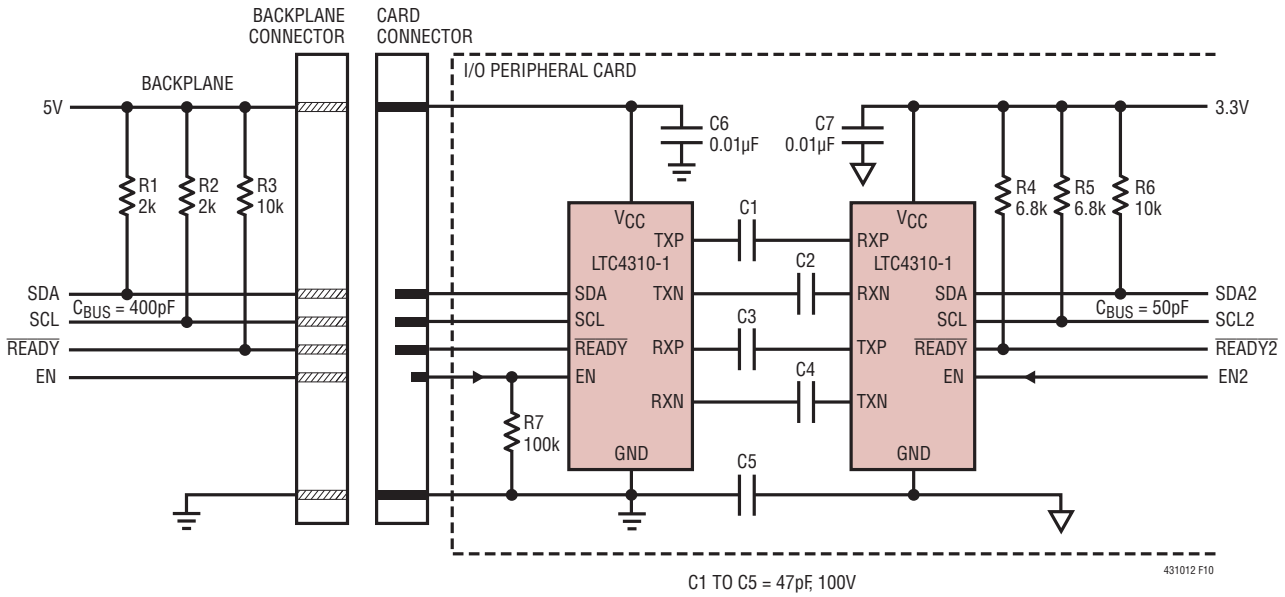

Figure 10. The LTC4310-1 in an I²C Hot-Swapping Application

Figure 10 shows the LTC4310-1 in a two-wire bus Hot Swap application. Using a staggered connector, make EN the shortest length pin to ensure that the transients associated with hot swapping have settled before the LTC4310-1 can be enabled. After connection is complete, a master on the backplane may drive EN high to bring the LTC4310-1 out of shutdown mode and into normal operation. Due to its STOP bit and bus idle detection circuitry, the LTC4310-1's driver circuitry is not activated until transactions on both buses are complete.

LTC4310 Compatibility with Other LTC Bus Buffers

The LTC4310 cannot be used on the same I²C bus with the LTC4300A-1, LTC4303 or LTC4307. During rising edges, the rise time accelerators of these buffers turn on before the LTC4310 disables its rise rate regulation circuitry, resulting in nonmonotonic bus edges.

The LTC4310-1 is compatible with the LTC4301 and LTC4301L. It is also compatible with the LTC4302, LTC4304, LTC4305 and LTC4306, provided that the rise time accelerators of these buffers are permanently disabled. All of the previously mentioned buffers are incompatible with the LTC4310-2 because the compensation networks of these buffers cause the bus to rise more slowly than (0.35 • V_{CC})/300ns, therefore the LTC4310-2 would not be able to control the bus rise rate.

LTC4310-1 Compatibility with LTC4310-2

In a typical application such as shown in Figure 1, an LTC4310-1 can be used on one bus and an LTC4310-2 can be used on the other, provided that the bus pull-up resistors connected to the LTC4310-1 meet the requirements of Figure 2, and the bus pull-up resistors connected to the LTC4310-2 meet the requirements of Figure 3. However, the bus switching frequency is limited by the rise rate regulation circuitry of the LTC4310-1. In addition, significant skew is introduced on the rising edges due to the large difference in the controlled rise rates of the two buses. For this reason, it is recommended to use two LTC4310-1's in SMBus and standard mode I²C applications and to use two LTC4310-2's in fast mode I²C applications.

The LTC4310-1 cannot be used on the same physical I²C bus with the LTC4310-2, because the LTC4310-1's rise rate regulation circuitry controls the bus rise rate to (0.35 • V_{CC})/900ns, therefore the LTC4310-2 would not be able to control the bus rise rate.

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Using the LTC4310-1 at Frequencies Above 100kHz

Users who implement custom two-wire buses may use the LTC4310-1 at bus frequencies above 100kHz provided that all other devices on the bus can tolerate the approximately 1µs bus rise times resulting from the LTC4310-1's bus rise rate regulation circuitry.

Transformer Selection Guide

As shown in Figure 1, a transformer passes transmit and receive signals between the two LTC4310's. The transmit signals have 1.25V magnitude and 35ns pulse width. The receive circuitry has an equivalent input impedance of 16.5kΩ and can receive differential signals ranging from 0.875V to 1.55V. To meet these requirements, choose a transformer having a magnetizing inductance ranging from 50µH to 350µH, a 1:1 turns ratio and a maximum insertion loss of –1.5dB. For optimal common mode noise rejection, choose a center-tapped transformer and connect the center tap on the receiving side to local ground using a 0.01µF capacitor. Ringing at the LTC4310's RXP and RXN pins can effectively be damped by inserting 50Ω series resistors between each LTC4310's TXP and TXN pins and the corresponding transformer primary windings.

Table 1 shows a recommended list of transformers for use with the LTC4310. 10/100BaseTX Ethernet transformers are inexpensive and work very well in this application for isolation voltages up to 1500V. For applications requiring 4000V isolation, the Würth Electronics Midcom 749014012 transformer is recommended.

RF Radiated Emissions

The LTC4310 evaluation board passes CISPR22 Class B requirements for radiated emissions. The results of CISPR22 testing are shown in the evaluation board manual. To reduce radiated emission levels further, enclose the LTC4310 application circuit in a shielded enclosure.

Common Mode Transient Immunity

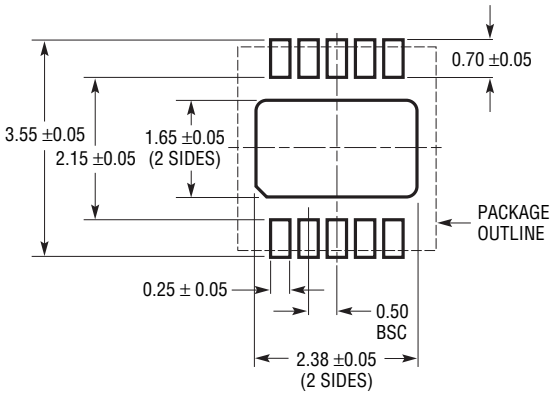
The LTC4310 has high immunity to common mode transients. This is tested by applying a square voltage pulse having very fast edges between the isolated grounds. The LTC4310 passes 20kV/us edges without corruption of the I^2C bus logic states.

Table 1. LTC4310 Recommended Transformers

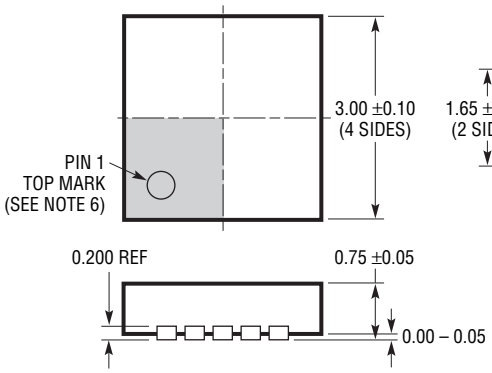
MANUFACTURER	PART NUMBER	ISOLATION VOLTAGE	FORM FACTOR (mm)			TURNS RATIO	CENTER TAP	OPERATING TEMPERATURE
			x	y	z			
PCA Electronics	EPF8119S	$1500V_{RMS}$	10.41	12.45	5.84	1:1	Yes	0°C TO 70°C
	EPF8119SE	$1500V_{RMS}$	10.2	12.7	5.96	1:1	Yes	–40°C TO 85°C
Pulse	E5017	$1500V_{RMS}$	9.4	12.7	5.08	1:1	Yes	0°C TO 70°C
Würth Electronics Midcom	000-7090-37R-LF1	$1500V_{RMS}$	9.4	12.95	5.33	1:1	Yes	–40°C TO 85°C
	749014012	$4000V_{RMS}$	17	24.55	10.85	1:1	Yes	0°C TO 70°C

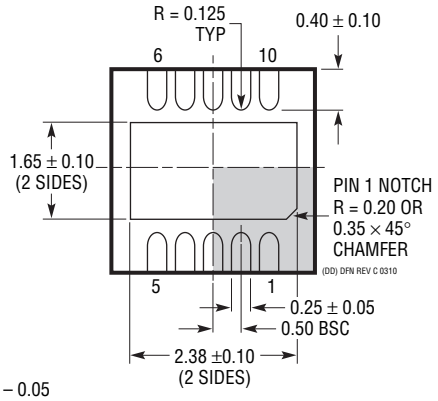
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



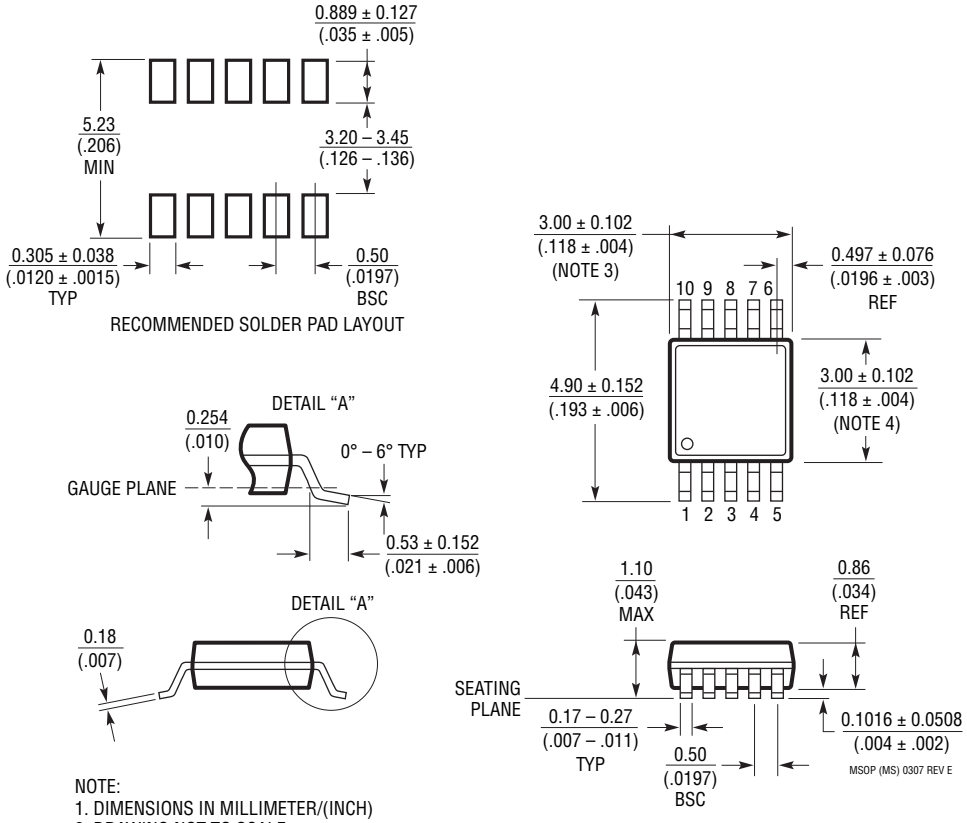


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/11	Revised conditions for $I_{SDD,SCL(OH)}$ in the Electrical Characteristics section.	3

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.