2-Wire Bus Buffer with High Noise Margin

FEATURES

- **Bidirectional Buffer Increases Fanout**
- **High Noise Margin with $V_{IL} = 0.3 \bullet V_{CC}$**
- **Compatible with Non-Compliant I^2C Devices That Drive a High V_{OL}**
- **Selectable Rise Time Accelerator Current**
- **Level Shift 1.5V, 1.8V, 2.5V, 3.3V and 5V Busses**
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane
- Stuck Bus Disconnect and Recovery
- Compatible with I^2C, I^2C Fast Mode and SMBus
- ±4kV Human Body Model ESD Ruggedness
- High Impedance SDA, SCL pins When Unpowered
- 12-Lead (4mm × 3mm) DFN and 12-Lead MSOP Packages

APPLICATIONS

- Capacitance Buffers/Bus Extender
- Live Board Insertion
- Telecommunications Systems Including ATCA
- Level Translation
- PMBus
- Servers

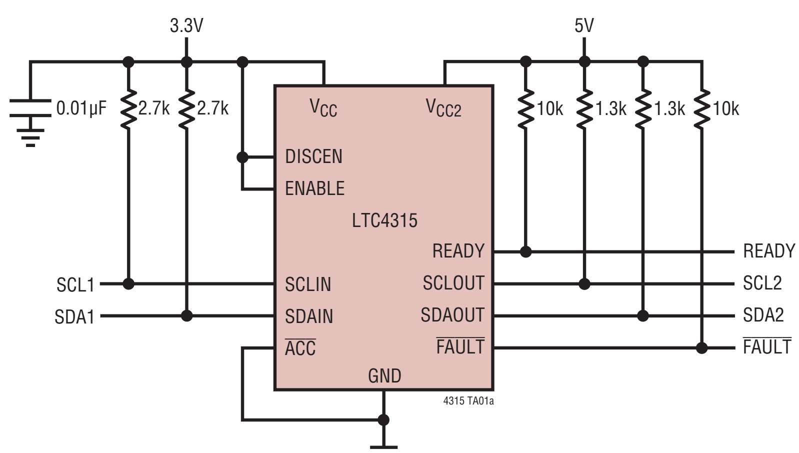
DESCRIPTION

The LTC4315 is a hot-swappable 2-wire bus buffer that provides bidirectional buffering, while maintaining a low offset voltage and high noise margin up to $0.3 \bullet V_{CC}$. The high noise margin allows the LTC4315 to be interoperable with devices that drive a high V_{OL} (>0.4V) and allows multiple LTC4315s to be cascaded. The LTC4315 supports level translation between 1.5V, 1.8V, 2.5V, 3.3V and 5V busses.

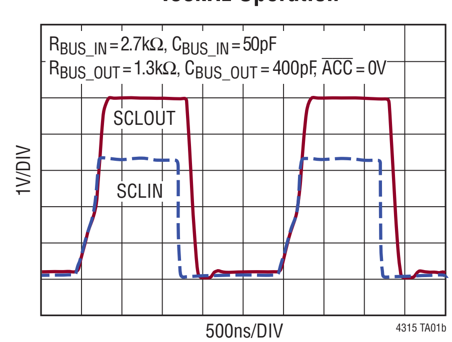
During insertion, the SDA and SCL lines are precharged to 1V to minimize bus disturbances. Connection is established between the input and output after ENABLE is asserted high and a stop bit or bus idle condition has been detected on the SDA and SCL pins.

If both data and clock are not simultaneously high at least once in 45ms and DISCEN is high, a $\overline{FAULT}$ signal is generated indicating a stuck bus low condition and the input is disconnected from the output. Up to 16 clock pulses are subsequently generated to free the stuck bus. A three state $\overline{ACC}$ pin enables input and output side rise time accelerators of various strengths.

TYPICAL APPLICATION



400kHz Operation



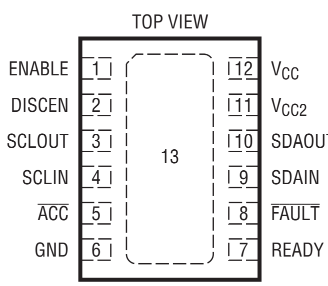
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

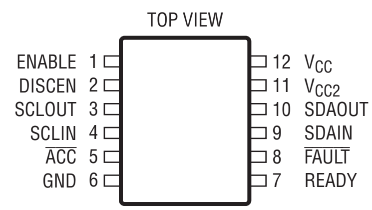
Supply Voltages V_{CC}, V_{CC2} .... –0.3V to 6V
Input Voltages $\overline{\text{ACC}}$, DISCEN, ENABLE......... –0.3V to 6V
Input/Output Voltages SDAIN, SCLIN, SCLOUT,
SDAOUT.. –0.3V to 6V
Output Voltages $\overline{\text{FAULT}}$, READY .... –0.3V to 6V
Output Sink Currents
$\overline{\text{FAULT}}$, READY 50mA

Operating Ambient Temperature Range
LTC4315C .... 0°C to 70°C
LTC4315I.. –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP .... 300°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) PCB CONNECTION TO GND IS OPTIONAL



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4315CDE#PBF	LTC4315CDE#TRPBF	4315	12-Lead (4mm × 3mm) DFN	0°C to 70°C
LTC4315IDE#PBF	LTC4315IDE#TRPBF	4315	12-Lead (4mm × 3mm) DFN	–40°C to 85°C
LTC4315CMS#PBF	LTC4315CMS#TRPBF	4315	12-Lead Plastic MSOP	0°C to 70°C
LTC4315IMS#PBF	LTC4315IMS#TRPBF	4315	12-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{CC2} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply/Start-Up							
V_{CC}	Input Supply Voltage		●	2.9		5.5	V
$V_{DD,BUS}$	2-Wire Bus Supply Voltage	(Note 3)	●	1.4		5.5	V
V_{CC2}	Output Side Accelerator Supply Voltage		●	2.25		5.5	V
I_{CC}	Input Supply Current	V_{ENABLE} = V_{CC} = V_{CC2} = 5.5V, $V_{SDAIN,SCLIN}$ = 0V (Note 4)	●	6	8.1	10	mA
$I_{CC(DISABLED)}$	Input Supply Current	V_{ENABLE} = 0V, V_{CC} = V_{CC2} = 5.5V, $V_{SDAIN,SCLIN}$ = 0V	●	2.3	3.3	4.3	mA
I_{CC2}	V_{CC2} Supply Current	V_{ENABLE} = V_{CC} = V_{CC2} = 5.5V, $V_{SDAIN,SCLIN}$ = 0V (Note 4)	●	0.2	0.31	0.4	mA
$I_{CC2(DISABLED)}$	V_{CC2} Supply Current	V_{ENABLE} = 0V, V_{CC} = V_{CC2} = 5.5V, $V_{SDAIN,SCLIN}$ = 0V	●	0.15	0.25	0.35	mA
V_{TH_UVLO}	V_{CC} UVLO Threshold	V_{CC} Rising	●	2.55	2.7	2.85	V
$V_{CC\_UVLO(HYST)}$	UVLO Threshold Hysteresis Voltage				200		mV
V_{PRE}	Precharge Voltage	SDA, SCL Pins Open	●	0.8	1	1.2	V
Buffers							
$V_{OS(SAT)}$	Buffer Offset Voltage	I_{OL} = 4mA, Driven $V_{SDA,SCL}$ = 50mV	●	100	190	280	mV
		I_{OL} = 500µA, Driven $V_{SDA,SCL}$ = 50mV	●	15	60	120	mV
V_{OS}	Buffer Offset Voltage	I_{OL} = 4mA, Driven $V_{SDA,SCL}$ = 200mV	●	50	120	180	mV
		I_{OL} = 500µA, Driven $V_{SDA,SCL}$ = 200mV	●	15	60	115	mV
$V_{IL(FALLING)}$	Buffer Input Logic Low Voltage	(Notes 5 and 6)	●	0.3 • V_{MIN}	0.33•V_{MIN}	0.36•V_{MIN}	V
$V_{IL(HYST)}$	V_{IL} Hysteresis Voltage				50		mV
I_{LEAK}	Input Leakage Current	SDA, SCL Pins = 5.5V, V_{CC} = 5.5V, 0V	●			±10	µA
C_{IN}	Input Capacitance	SDA, SCL Pins (Note 7)	●			10	pF
Rise Time Accelerators							
$\frac{dV}{dt}_{(RTA)}$	Minimum Slew Rate Requirement	SDA, SCL Pins, V_{CC} = V_{CC2} = 5V	●	0.1	0.2	0.4	V/µs
$V_{RTA(TH)}$	Rise Time Accelerator DC Threshold Voltage	V_{CC} = V_{CC2} = 5V (Note 5)	●	0.38•V_{MIN}	0.41•V_{MIN}	0.44•V_{MIN}	V
$\Delta V_{\overline{ACC}}$	Buffers Off to Accelerator On Voltage	SDA, SCL Pins, V_{CC} = V_{CC2} = 5V (Note 5)	●	0.05•V_{MIN}	0.07•V_{MIN}		V
I_{RTA}	Rise Time Accelerator Pull-Up Current	SDA, SCL Pins $\overline{ACC}$ Grounded, V_{CC} = V_{CC2} = 5V (Note 8)	●	15	25	40	mA
		$\overline{ACC}$ Open, V_{CC} = V_{CC2} = 5V (Note 8)	●	1.5	2.5	3.5	mA
Enable/Control							
$V_{EN(TH)}$	ENABLE Threshold Voltage		●	1	1.4	1.8	V
$V_{DISCEN(TH)}$	DISCEN Threshold Voltage		●	1	1.4	1.8	V
I_{LEAK}	Input Leakage Current	DISCEN, ENABLE Pins, V_{CC} = 5.5V	●		0.1	±1	µA
$V_{\overline{ACC}(L,TH)}$	$\overline{ACC}$ Input Low Threshold Voltage	V_{CC} = 5V	●	0.2 • V_{CC}	0.3 • V_{CC}	0.4 • V_{CC}	V
$V_{\overline{ACC}(H,TH)}$	$\overline{ACC}$ Input High Threshold Voltage	V_{CC} = 5V	●	0.7 • V_{CC}	0.8 • V_{CC}	0.9 • V_{CC}	V
$I_{\overline{ACC}(IN,HL)}$	$\overline{ACC}$ High, Low Input Current	V_{CC} = V_{CC2} = 5V, $V_{\overline{ACC}}$ = 5V, 0V	●		±23	±40	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{CC} = V_{CC2}$ = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{\overline{ACC}(IN, Z)}$	Allowable Leakage Current in the Open State	$V_{CC} = V_{CC2}$ = 5V	●			±5	μA
$V_{READY(OL)}$	READY Output Low Voltage	I_{READY} = 3mA, V_{CC} = 5V	●			0.4	V
$I_{READY(OH)}$	READY Off Leakage Current	$V_{CC} = V_{READY}$ = 5V	●		0.1	±5	μA
Stuck Low Timeout Circuitry							
$t_{TIMEOUT}$	Bus Stuck Low Timer	SDAOUT or SCLOUT < 0.3 • V_{MIN} (Note 5)	●	35	45	55	ms
$V_{\overline{FAULT}(OL)}$	$\overline{FAULT}$ Output Low voltage	$I_{\overline{FAULT}}$ = 3mA	●			0.4	V
$I_{\overline{FAULT}(OH)}$	$\overline{FAULT}$ Off Leakage Current	$V_{CC} = V_{\overline{FAULT}}$ = 5V	●		0.1	±5	μA
I^2C Interface Timing							
$f_{SCL(MAX)}$	I^2C Frequency Max		●	400			kHz
t_{PDHL}	SCL, SDA Fall Delay	$V_{CC} = V_{CC2} = V_{DD(BUS)}$ = 5V, C_{BUS} = 100pF, R_{BUS} = 10kΩ (Note 7)			130	250	ns
t_f	SCL, SDA Fall Times	$V_{CC} = V_{CC2} = V_{DD(BUS)}$ = 5V, C_{BUS} = 100pF, R_{BUS} = 10kΩ (Note 7)		20		300	ns
t_{IDLE}	Bus Idle Time		●	55	95	175	μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive and all voltages are referenced to GND unless otherwise indicated.

Note 3: The LTC4315 can level translate bus voltages ranging from 2.25V to 5.5V. In special cases, it can also level translate down to 1.4V. See the Applications Information section for more details.

Note 4: Test performed with SDA, SCL buffers active.

Note 5: V_{MIN} = minimum of V_{CC} and V_{CC2} if V_{CC2} > 2.25V, otherwise $V_{MIN} = V_{CC}$.

Note 6: V_{IL} is tested for the following (V_{CC}, V_{CC2}) combinations; (2.9V, 5.5V), (5.5V, 2.25V), (3.3V, 3.3V) and (5V, 0V).

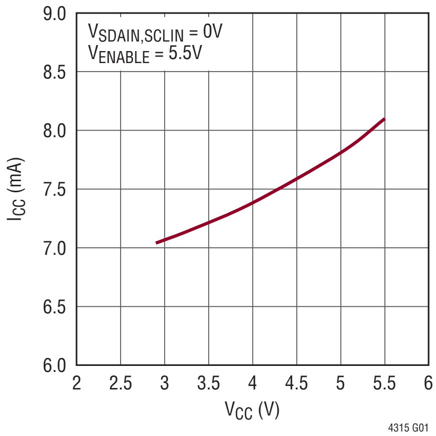
Note 7: Guaranteed by design and not tested.

Note 8: Measured in a special DC mode with $V_{SDA,SCL} = V_{RTA(TH)}$ + 1V. The transient I_{RTA} during rising edges, when $\overline{ACC}$ is LOW, will depend on the bus loading condition and the slew rate of the bus. The LTC4315's internal slew rate control circuitry limits the maximum bus rise rate to 75V/μs by controlling the transient I_{RTA}.

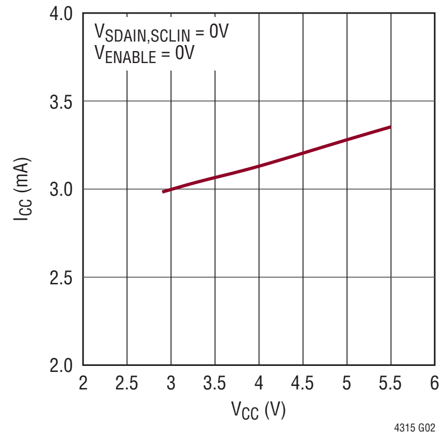
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = V_{CC2} = 3.3V$ unless otherwise noted.

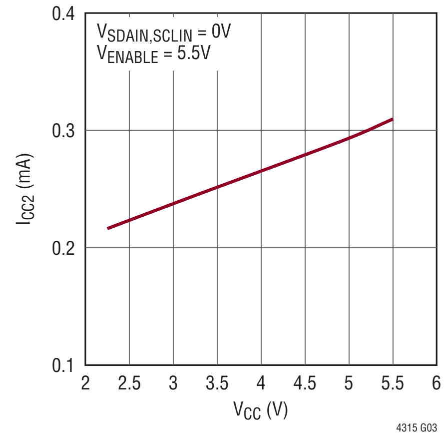
I_{CC} Enabled Current vs Supply Voltage



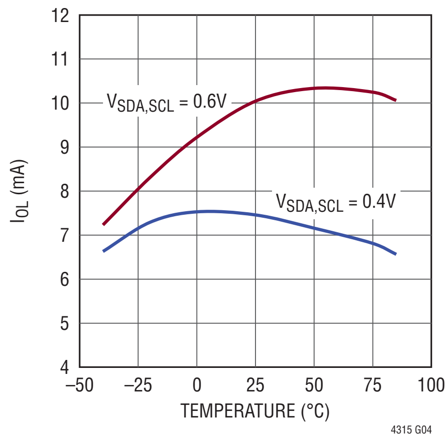
I_{CC} Disabled Current vs Supply Voltage



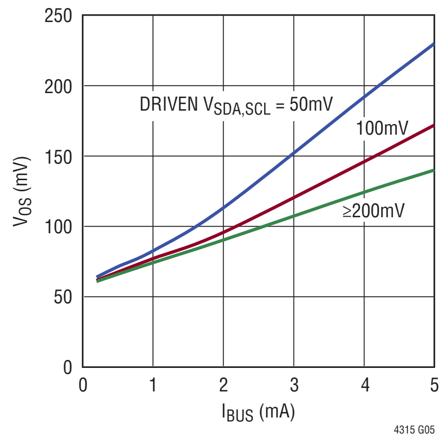
I_{CC2} Enabled Current vs Supply Voltage



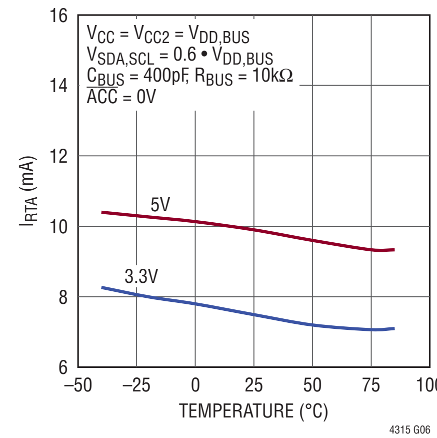
Buffer DC I_{OL} vs Temperature



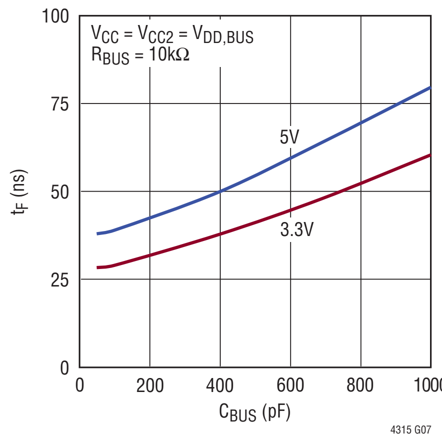
V_{OS} vs I_{BUS} Different Driven Voltage Levels



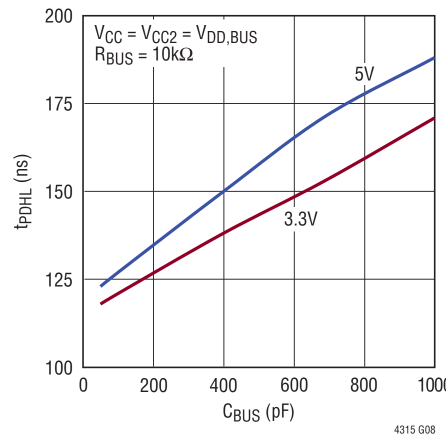
I_{RTA} vs Temperature



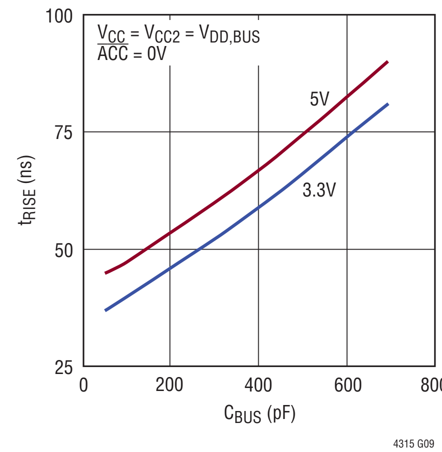
t_F (70% to 30%) vs Bus Capacitance



t_{PDHL} (50% to 50%) vs Bus Capacitance



Bus Rise Time (40% to 70%) vs C_{BUS}



PIN FUNCTIONS

$\overline{\text{ACC}}$ (Pin 5): Three-State Acceleration Strength Selector. This pin controls the current strength of the rise time accelerators on both the input and output sides. Rise time accelerators (RTAs) are disabled if $\overline{\text{ACC}}$ is high, in current source mode if $\overline{\text{ACC}}$ is open and in the slew limited switch mode if $\overline{\text{ACC}}$ is low. See Table 1 in the Applications Information section. Grounding V_{CC2} selectively disables the output side RTAs independent of the $\overline{\text{ACC}}$ setting.

DISCEN (Pin 2): Enable Input to Disconnect Stuck Bus. When this pin is high, stuck busses are automatically disconnected after a timeout period of 45ms and $\overline{\text{FAULT}}$ is pulled low. Up to sixteen clock pulses are subsequently applied to SCLOUT. When DISCEN is low, stuck busses are neither disconnected nor clocked but $\overline{\text{FAULT}}$ is pulled low. Connect to GND if unused.

ENABLE (Pin 1): Connection Enable Input. When driven low, the ENABLE pin isolates SDAIN and SCLIN from SDAOUT and SCLOUT, asserts READY low, disables rise time accelerators and inhibits automatic clock and stop bit generation during a bus stuck low fault condition. When driven high, the ENABLE pin connects SDAIN and SCLIN to SDAOUT and SCLOUT after a stop bit or bus idle has been detected on both busses. Driving ENABLE high also enables automatic clock generation during a fault condition, if DISCEN is tied high. During a fault condition, a rising edge on the ENABLE pin forces a connection between SDAIN and SDAOUT and SCLIN and SCLOUT. When using the LTC4315 in a Hot Swap™ application with staggered pins, connect a 10k resistor between ENABLE and GND to ensure correct functionality. Connect to V_{CC} if unused.

Exposed Pad (DE12 Package Only): Exposed pad may be left open or connected to device GND.

$\overline{\text{FAULT}}$ (Pin 8): Stuck Bus Fault Output. This open drain N-channel MOSFET output pulls low if a simultaneous high on SCLOUT and SDAOUT does not occur in 45ms. In normal operation $\overline{\text{FAULT}}$ is high. Connect a pull-up resistor, typically 10k, from this pin to the bus pull-up supply. Leave open or tie to GND if unused.

GND (Pin 6): Device Ground.

READY (Pin 7): Connection Ready Status Output. This open drain N-channel MOSFET output pulls low when the input and output sides are disconnected. READY is pulled high when ENABLE is high and a connection has been established between the input and output. Connect a pull-up resistor, typically 10k, from this pin to the bus pull-up supply. Leave open or tie to GND if unused.

SCLIN (Pin 4): Serial Bus 1 Clock Input/Output. Connect this pin to the SCL line on the upstream bus. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply must be $\geq V_{CC}$ if rise time accelerators are enabled. Do not leave open.

SCLOUT (Pin 3): Serial Bus 2 Clock Input/Output. Connect this pin to the SCL bus segment where stuck low recovery is desired. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply must be $\geq V_{CC2}$ if rise time accelerators are enabled. Do not leave open.

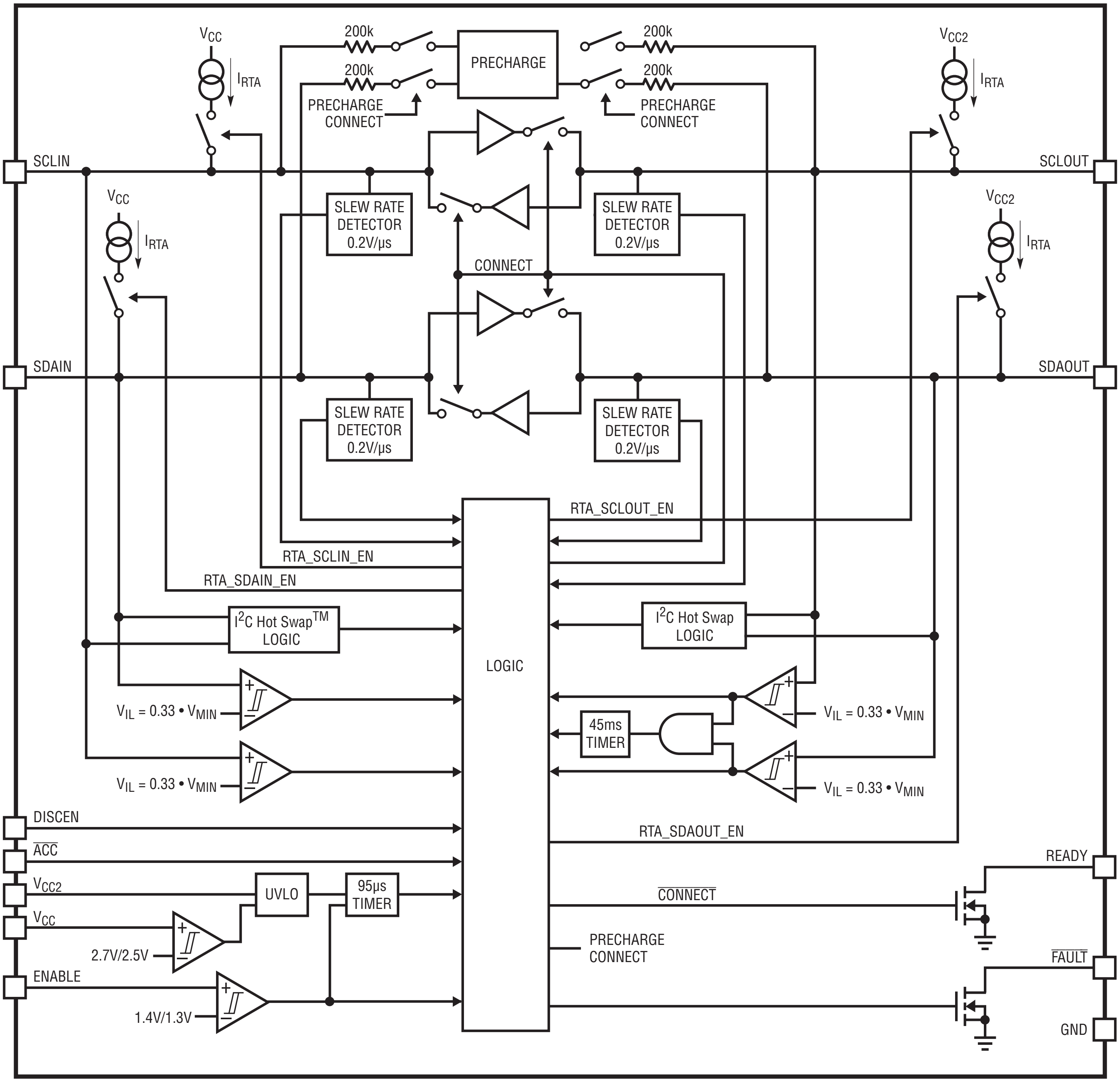
SDAIN (Pin 9): Serial Bus 1 Data Input/Output. Connect this pin to the SDA line on the upstream bus. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply must be $\geq V_{CC}$ if rise time accelerators are enabled. Do not leave open.

SDAOUT (Pin 10): Serial Bus 2 Data Input/Output. Connect this pin to the SDA bus segment where stuck low recovery is desired. Connect an external pull-up resistor or current source between this pin and the bus supply. The bus supply must be $\geq V_{CC2}$ if rise time accelerators are enabled. Do not leave open.

V_{CC} (Pin 12): Power Supply Voltage. Power this pin from a supply between 2.9V and 5.5V. Bypass with at least 0.01µF to GND.

V_{CC2} (Pin 11): SDAOUT, SCLOUT Rise Time Accelerator Power Supply Voltage. When powering V_{CC2}, use a supply voltage ranging from 2.25V to 5.5V and bypass with at least 0.01µF to GND. Output side rise time accelerators are active if $V_{CC2} \geq 2.25V$ and $\overline{\text{ACC}}$ is low or open. Grounding V_{CC2} disables output side rise time accelerators independent of the state of $\overline{\text{ACC}}$.

BLOCK DIAGRAM



OPERATION

The Block Diagram shows the major functional blocks of the LTC4315. The LTC4315 is a high noise margin bus buffer which provides capacitance buffering for I^2C signals. Capacitance buffering is achieved by using back to back buffers on the clock and data channels, which isolate the SDAIN and SCLIN capacitances from the SDAOUT and SCLOUT capacitances respectively. All SDA and SCL pins are fully bidirectional. The high noise margin allows the LTC4315 to operate with non-compliant I^2C devices that drive a high V_{OL}, permits a number of LTC4315s to be connected in series and improves the reliability of I^2C communications in large noisy systems. When enabled, rise time accelerator (RTA) pull-up currents (I_{RTA}) turn on during rising edges to reduce bus rise time. In a typical application, the input bus is pulled up to V_{CC} and the output bus is pulled up to V_{CC2}, although these are not requirements. V_{CC} is the primary power supply to the LTC4315. V_{CC} and V_{CC2} serve as the input and output side rise time accelerator supplies respectively. Grounding V_{CC2} selectively disables the output side RTAs.

When the LTC4315 first receives power on its V_{CC} pin, it starts out in an under voltage lockout mode (UVLO) until its V_{CC} exceeds 2.7V. The buffers and RTAs are disabled and the LTC4315 ignores the logic state of its clock and data pins. During this time the precharge circuit forces a nominal voltage of 1V on the SDA and SCL pins through 200k resistors.

Once the LTC4315 exits UVLO and its ENABLE pin has been asserted high, it monitors the clock and data pins for a stop bit or a bus idle condition. When a combination of either condition is detected simultaneously on the input and output sides, the LTC4315 activates the connections between SDAIN and SDAOUT, and SCLIN and SCLOUT respectively, asserts READY high and deactivates the precharge circuit. If $\overline{\text{ACC}}$ is low or open, RTAs are also enabled at this time. V_{CC2} transitions from a high to a low or vice versa across a 1.8V threshold cause the LTC4315 to disable the buffers and RTAs and to ignore the clock and data pins for 95µs after that transition. A stop bit or bus idle is required on both sides to reactivate the buffers and RTAs. The precharge circuit is not affected by V_{CC2}.

When a SDA/SCL pin is driven below the V_{IL} level, the buffers are turned on and the logic low level is propagated though the LTC4315 to the other side. A high occurs when all devices on the input and output sides release high. Once the bus voltages rise above the V_{IL} level, the buffers are turned off. The RTAs are turned on at a slightly higher voltage. The RTAs accelerate the rising edges of the SDA/SCL inputs and outputs up to voltages of $0.9 \bullet V_{CC}$ and $0.9 \bullet V_{CC2}$ respectively, provided that the busses on their own are rising at a minimum rate of 0.4V/µs as determined by internal slew rate detectors. $\overline{\text{ACC}}$ is a three-state input that controls the RTA pull-up current strength I_{RTA}.

The LTC4315 detects a bus stuck low (fault) condition when both clock and data busses are not simultaneously high at least once in 45ms. When a stuck bus occurs, the LTC4315 asserts the $\overline{\text{FAULT}}$ flag. If DISCEN is tied high, the LTC4315 also disconnects the input and output sides and after waiting at least 40µs, generates up to sixteen 5.5kHz clock pulses on the SCLOUT pin and a stop bit to attempt to free the stuck bus. Should the stuck bus release high during this period, clock generation is terminated and the $\overline{\text{FAULT}}$ flag is cleared.

If DISCEN is tied low, a stuck bus event only causes $\overline{\text{FAULT}}$ flag assertion. Disconnection of the input and output sides and clock generation are not done. Once the stuck bus recovers and $\overline{\text{FAULT}}$ flag has been cleared, connection is re-established between the input and output after a stop bit or bus idle condition is detected. Toggling the ENABLE pin after a fault condition has occurred forces a connection between the input and output. When powering into a stuck low condition, the input and output sides remain disconnected. After the timeout period, a stuck low fault condition is detected and the behavior is as described previously.

APPLICATIONS INFORMATION

The LTC4315 provides capacitance buffering, data and clock Hot Swap capability and level translation of I^2C signals on its clock and data pins. The high noise margin of the LTC4315 permits interoperability with I^2C devices that drive a high V_{OL}, permits series connection of multiple LTC4315s and provides improved I^2C communication reliability. The LTC4315 isolates backplane and card capacitances, provides slew limited acceleration of rising edges and slew control of falling edges while level translating 1.5V, 1.8V, 2.5V, 3.3V and 5V busses. These features are illustrated in the following subsections.

RISE TIME ACCELERATOR (RTA) PULL-UP CURRENT STRENGTH

After an input to output connection has been established the RTAs on both the input and output sides of the SDA and SCL busses are activated based on the state of the $\overline{ACC}$ pin and the V_{CC2} supply voltage. During positive bus transitions of at least 0.4V/µs, the RTAs provide pull-up currents to reduce rise time. Enabling the RTAs allows users to choose larger bus pull-up resistors to reduce power consumption and improve logic low noise margins, to design with bus capacitances outside of the I^2C specification and to operate at a higher clock frequency. The function of the $\overline{ACC}$ pin in setting I_{RTA} is summarized in Table 1. In the strong mode ($\overline{ACC}$ low) the acceleration is slew limited to a maximum bus rise rate of 75V/µs. The strong mode current is therefore directly proportional to the bus capacitance. The LTC4315 is capable of sourcing up to 40mA of current in the strong mode. If $\overline{ACC}$ is left open, rise time acceleration is provided by a 2.5mA pull up.

TABLE 1: $\overline{ACC}$ Control of the RTA Current I_{RTA}

$\overline{ACC}$	I_{RTA}
Low	Strong
Hi-Z	2.5mA
High	None

The $\overline{ACC}$ pin has a resistive divider between V_{CC} and ground to set its voltage to 0.5 • V_{CC} if left open.

Figures 1 and 2 show the rising waveforms of heavily loaded SDAIN and SDAOUT busses with the $\overline{ACC}$ pin set for strong mode and 2.5mA current source mode respectively. In both figures, during a rising edge, the buffers are active and the input and output sides connected, until the bus voltages on both the input and output sides are greater than 0.33 • V_{MIN}, where V_{MIN} is the lower of the V_{CC} and V_{CC2} voltages. When each individual bus voltage rises above 0.41 • V_{MIN}, the RTA on that bus turns on. The effect of the acceleration strength is shown in the SDA waveforms in Figures 1 and 2 for identical bus loads. The RTAs supply 10mA and 2.5mA of pull-up current I_{RTA} in the strong and current source modes respectively for the bus conditions shown in Figures 1 and 2. For identical bus loads, the bus rises faster in Figure 1 compared to Figure 2 because of the higher I_{RTA}.

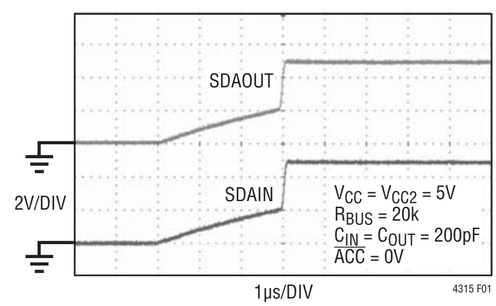


Figure 1. Bus Rising Edge for the Strong Acceleration Mode. $V_{CC} = V_{CC2} = 5V$

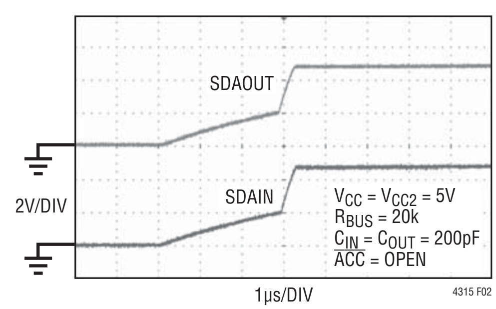


Figure 2. Bus Rising Edge for the Current Source Acceleration Mode. $V_{CC} = V_{CC2} = 5V$

APPLICATIONS INFORMATION

If V_{CC2} is tied low, output RTAs are disabled independent of the state of the $\overline{ACC}$ pin. Using a combination of the $\overline{ACC}$ pin and the V_{CC2} voltage, the input and output side RTAs can be controlled independently. The RTAs are also internally disabled during power up, V_{CC2} transitions described in the Operation section and during a bus stuck low event.

The RTAs when activated pull the bus up to 0.9 • V_{CC} and 0.9 • V_{CC2} on the input and output sides of the SDA and SCL pins. Independent supply voltages V_{CC} and V_{CC2} maximize acceleration range on both inputs and outputs by allowing the RTA turn-off voltage to be set independently on the two sides. In order to prevent bus overdrive by the RTA, the bus supplies on the input and output sides of the LTC4315 must be greater than or equal to 0.9 • V_{CC} and 0.9 • V_{CC2} respectively. An example is shown in Figure 3 where the input bus voltage is greater than V_{CC}. During a rising edge, the input bus rise rate will be accelerated by the RTA up to a voltage of 2.97V after which the bus rise rate will reduce to a value that is determined by the bus current and bus capacitance. The RTA turn-off voltage is less than the bus supply and the bus is not over driven. This can also be accomplished by tying V_{CC} to the input bus supply and V_{CC2} to the output bus supply as shown in Figure 4. In this case the input and output busses are accelerated to 2.97V and 2.25V respectively

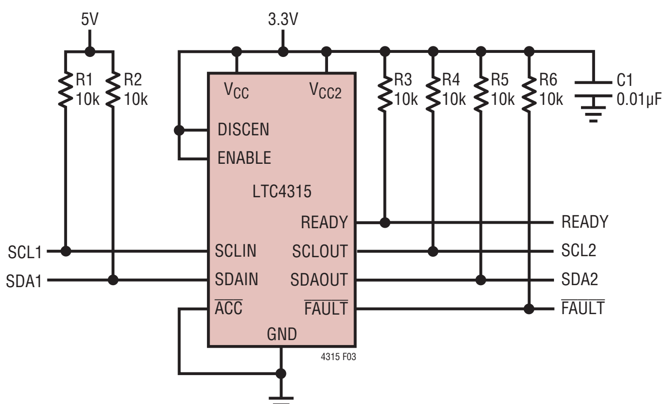


Figure 3. Level Shift Application Where the SDAIN, SCLIN Bus Pull-Up Supply Voltages are Higher Than the Supply Voltages of the LTC4315

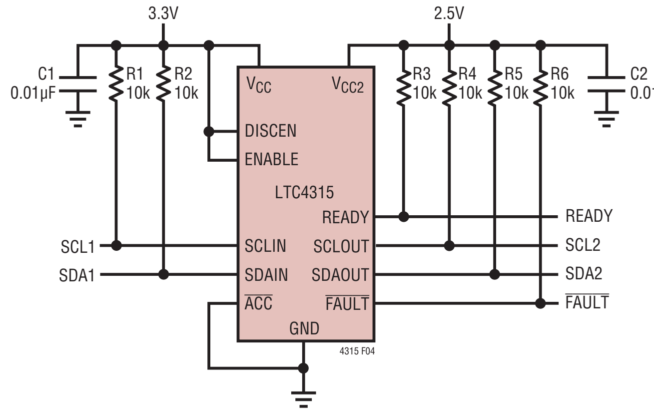


Figure 4. Level Shift Application Where the LTC4315 V_{CC} and V_{CC2} Pins are Connected to the Bus Pull-Up Supply Voltages

PULL-UP RESISTOR VALUE SELECTION

To guarantee that the RTAs are activated during a rising edge, the bus must rise on its own with a positive slew rate of at least 0.4V/µs. To achieve this, choose a maximum R_{BUS} using the formula:

$$R_{BUS} \le \frac{\left(V_{DD,BUS(MIN)} - V_{RTA(TH)}\right)}{0.4\dfrac{V}{\mu s} \bullet C_{BUS}} \quad (1)$$

R_{BUS} is the bus pull-up resistor, $V_{DD,BUS(MIN)}$ is the minimum bus pull-up supply voltage, $V_{RTA(TH)}$ is the maximum voltage at which the RTA turns on and C_{BUS} is the equivalent bus capacitance. R_{BUS} must also be large enough to guarantee that:

$$R_{BUS} \ge \frac{\left(V_{DD,BUS(MAX)} - 0.4V\right)}{4mA} \quad (2)$$

This criterion ensures that the maximum bus current is less than 4mA.

APPLICATIONS INFORMATION

INPUT TO OUTPUT OFFSET VOLTAGE

While propagating a logic low voltage on its SDA and SCL pins, the LTC4315 introduces a positive offset voltage between the input and output. When a logic low voltage ≥200mV is driven on any of the LTC4315's data or clock pins, the LTC4315 regulates the voltage on the opposite side to a slightly higher value. This is illustrated in Equation 3, which uses SDA as an example:

$$V_{SDAOUT} = V_{SDAIN} + 50mV + 15\Omega \bullet \frac{V_{DD,BUS}}{R_{BUS}} \quad (3)$$

In Equation 3, $V_{DD,BUS}$ is the output bus supply voltage and R_{BUS} is the SDAOUT bus pull-up resistance.

For driven logic low voltages < 200mV Equation 3 does not apply as the saturation voltage of the open collector output transistor results in a higher offset. However, for any input logic low below 220mV, the output is guaranteed to be below a V_{OL} of 400mV for bus pull-up currents up to 4mA. See the Typical Performance section for offset variation as a function of the driven logic low voltage and bus pull-up current.

FALLING EDGE CHARACTERISTICS

The LTC4315 introduces a propagation delay on falling edges due to the finite response time and finite current sink capability of its buffers. In addition the LTC4315 also slew limits the falling edge to an edge rate of 45V/µs. The slew limited falling edge eliminates fast transitions on the busses and minimizes transmission line effects in systems. Refer to the Typical Performance section for the propagation delay and fall times as a function of the bus capacitance.

STUCK BUS DISCONNECT AND RECOVERY

During an output bus stuck low condition (SCLOUT or SDAOUT stuck low for at least 45ms) if DISCEN is tied high, the LTC4315 attempts to unstick the bus by first breaking the connection between the input and output. The LTC4315 then asserts $\overline{\text{FAULT}}$ low and after 40µs, generates up to sixteen 5.5KHz clock pulses on the SCLOUT pin. Should the stuck bus release high during this period, clock generation is stopped, a stop bit is generated and the $\overline{\text{FAULT}}$ flag is cleared. This process is shown in Figure 5 for the case where SDAOUT starts out stuck low and then recovers. As seen from the figure, the LTC4315 pulls $\overline{\text{FAULT}}$ and READY low and breaks the connection between the input and output sides, when a stuck low condition on SDA is detected. Clock pulses are then issued on SCLOUT to attempt to unstick the SDAOUT bus. When SDAOUT recovers, clock pulsing is stopped, a stop bit is generated on the output and $\overline{\text{FAULT}}$ and READY are released high. If DISCEN is low and a stuck bus event occurs, the $\overline{\text{FAULT}}$ flag is driven low but the input and output sides stay connected and no clocking or stop bit generation occurs. When powering up into a stuck low condition, a connection is never made between the input and the output, as a stop bit or bus idle condition is never detected. After a timeout period of 45ms, the $\overline{\text{FAULT}}$ flag is asserted low and the behavior is the same as described previously.

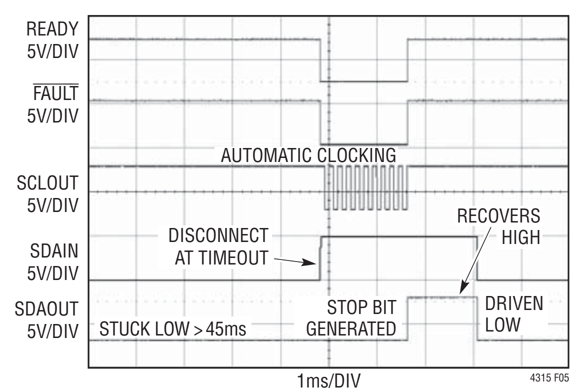


Figure 5. Bus Waveforms During SDAOUT Stuck Low and Recovery Event

APPLICATIONS INFORMATION

LIVE INSERTION, CAPACITANCE BUFFERING AND LEVEL TRANSLATION APPLICATION

Figures 6 illustrates an application of the LTC4315 that takes advantage of the LTC4315's Hot Swap, capacitance buffering and level translation features. If the I/O cards were plugged directly into the backplane without LTC4315 buffers, all of the backplane and card capacitances would directly add together, making rise time requirements difficult to meet. Placing an LTC4315 on the edge of each card isolates the card capacitance from the backplane. For a given I/O card, the LTC4315 drives the capacitance of everything on the card and devices on the backplane must drive only the small capacitance of the LTC4315 which is <10pF.

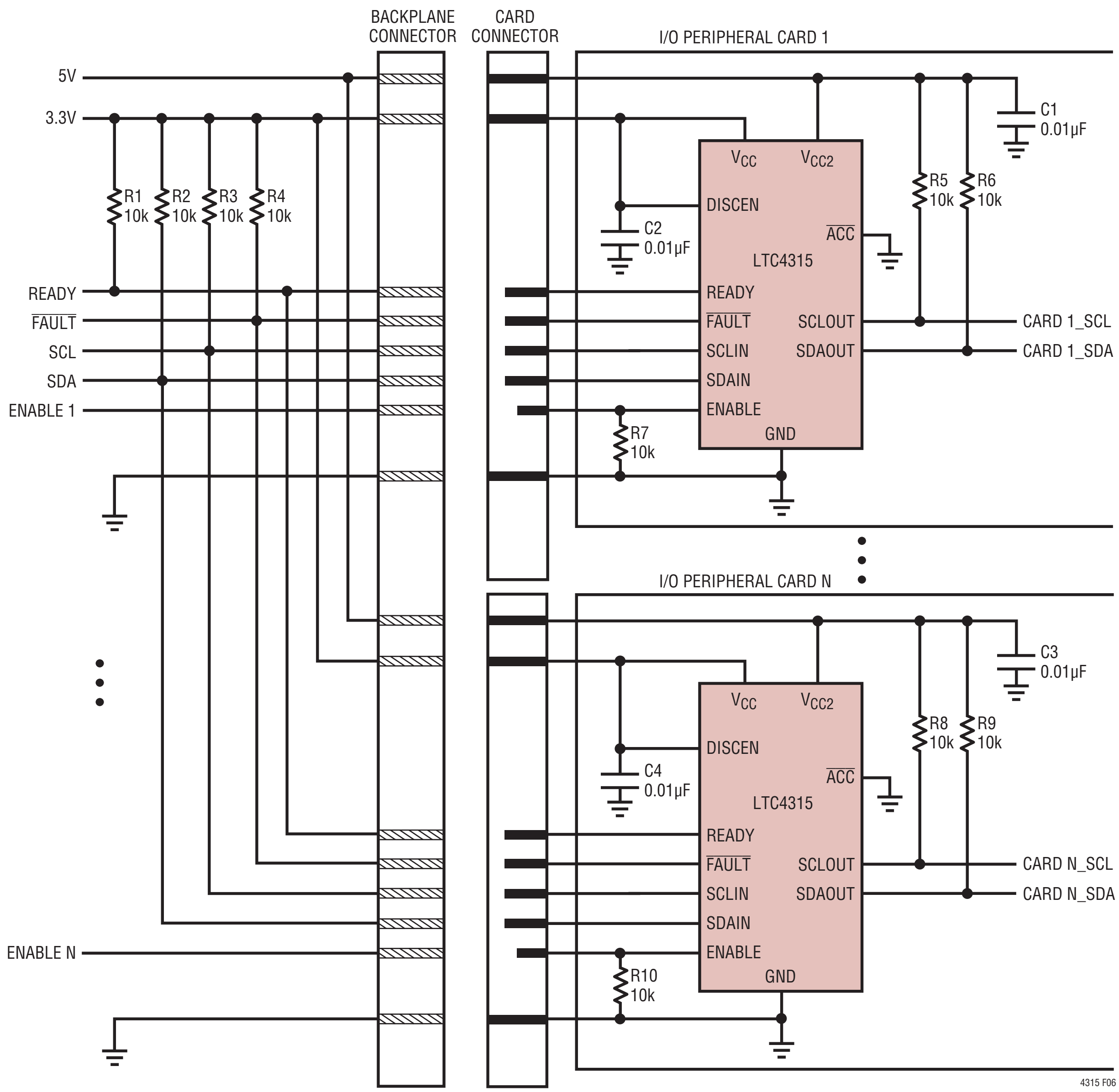


Figure 6. LTC4315 in an I²C Hot Swap Application with a Staggered Connector

APPLICATIONS INFORMATION

In Figure 6, a staggered connector is used to connect the LTC4315 to the backplane. V_{CC} and GND are the longest pins to ensure that the LTC4315 is powered and forcing a 1V precharge voltage on the medium length SDA and SCL pins before they contact the backplane. The 1V precharge voltage is applied to the SDA and SCL pins through 200k resistors. Since cards are being plugged into a live backplane whose SDA and SCL busses could be at any voltage between 0 and V_{CC}, precharging the LTC4315's SDA and SCL pins to 1V minimizes disturbances to the backplane bus when cards are being plugged in. The low (<10pF) input capacitance of the LTC4315 also contributes to minimizing bus disturbance as cards are being plugged in. With ENABLE being the shortest pin and also pulled to GND by a resistor, the staggered approach provides additional time for transients associated with live insertion to settle before the LTC4315 can be enabled. A 10k or lower pull-down resistor from ENABLE to GND is recommended.

If a connector is used where all pins are of equal length, the benefit of the precharge circuit is lost. Also, the ENABLE signal to the LTC4315 must be held low until all transients associated with the plugging in of a card into a live system die out.

LEVEL TRANSLATING TO VOLTAGES <2.25V

The LTC4315 can be used for level translation to bus voltages below 2.25V if certain conditions are met. In order to perform this level translation, RTAs on the low voltage side need to be disabled in order to prevent an overdrive of the low voltage bus. Since the maximum buffer turn-on and turn-off voltages are $0.36 \bullet V_{MIN}$, the minimum bus supply voltage is determined by the following equation,

$$V_{DD,BUS(MIN)} \geq \frac{0.36 \bullet V_{MIN}}{0.7} \quad (4)$$

in order to meet the $V_{IH} = 0.7 \bullet V_{DD,BUS}$ requirement and not impact the logic high noise margin. Voltage level translation down to 1.4V is allowed, but the logic high noise margin will be lowered. An example of voltage level translation from 3.3V to 1.8V is illustrated in Figure 7, where a 3.3V input voltage bus is translated to a 1.8V output voltage bus. Tying V_{CC} to 3.3V satisfies Equation 4. Grounding V_{CC2} disables the output RTAs. V_{MIN} defaults to V_{CC} under these conditions, making the buffer turn-off voltage 1.089V. A similar voltage translation can also be performed going from a 3.3V bus supply on the output side to a 1.8V bus supply on the input side if $\overline{ACC}$ is tied high to disable the input RTAs and if V_{CC} and V_{CC2} are tied to the 3.3V bus supply.

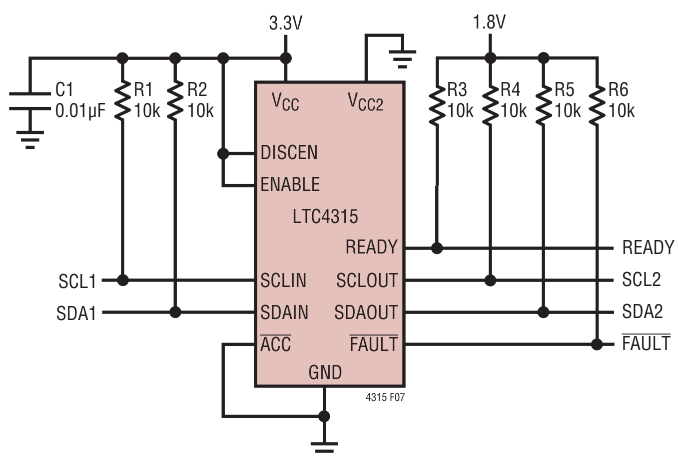


Figure 7. Voltage Level Translation from 3.3V to 1.8V Using the LTC4315

APPLICATIONS INFORMATION

TELECOMMUNICATIONS SYSTEMS

The LTC4315 has several features that make it an excellent choice for use in telecommunications systems such as ATCA. Referring to Figures 8 and 9, buffers are used on the edges of the field replaceable units (FRUs) and shelf managers to shield devices on these cards from the large backplane capacitance. The input capacitance of the LTC4315 is less than the 10pF maximum specification for buffers used in bussed ATCA applications. The LTC4315 buffers can drive capacitances >1nF, which is greater than the maximum backplane capacitance of 690pF in bused ATCA systems. The precharge feature, the low input capacitance of the LTC4315 and the high impedance of the SDA and SCL pins of the LTC4315 when it is unpowered, minimize disturbances to the bus when cards are being hot swapped. In Figure 8, the RTA of the LTC4315 on the shelf manager supplies 2.5mA of pull-up current, allowing the 1µs rise time requirement to be met on the heavily loaded backplane for loads well beyond the 690pF maximum specification. The 0.33 • V_{MIN} turn-off voltage of the LTC4315's buffers provides a large logic low noise margin in these systems.

In the bused ATCA application shown in Figure 8, the LTC4315s located on the shelf managers #1 and #2 and on the FRUs, drive the large backplane capacitance while the microcontrollers on the shelf managers and the I^2C slave devices on the FRUs drive the small input capacitance of the LTC4315. The LTC4315 on only one of the shelf managers is enabled at any given time. The hot insertion logic on the LTC4315 allows the FRUs to be plugged or unplugged

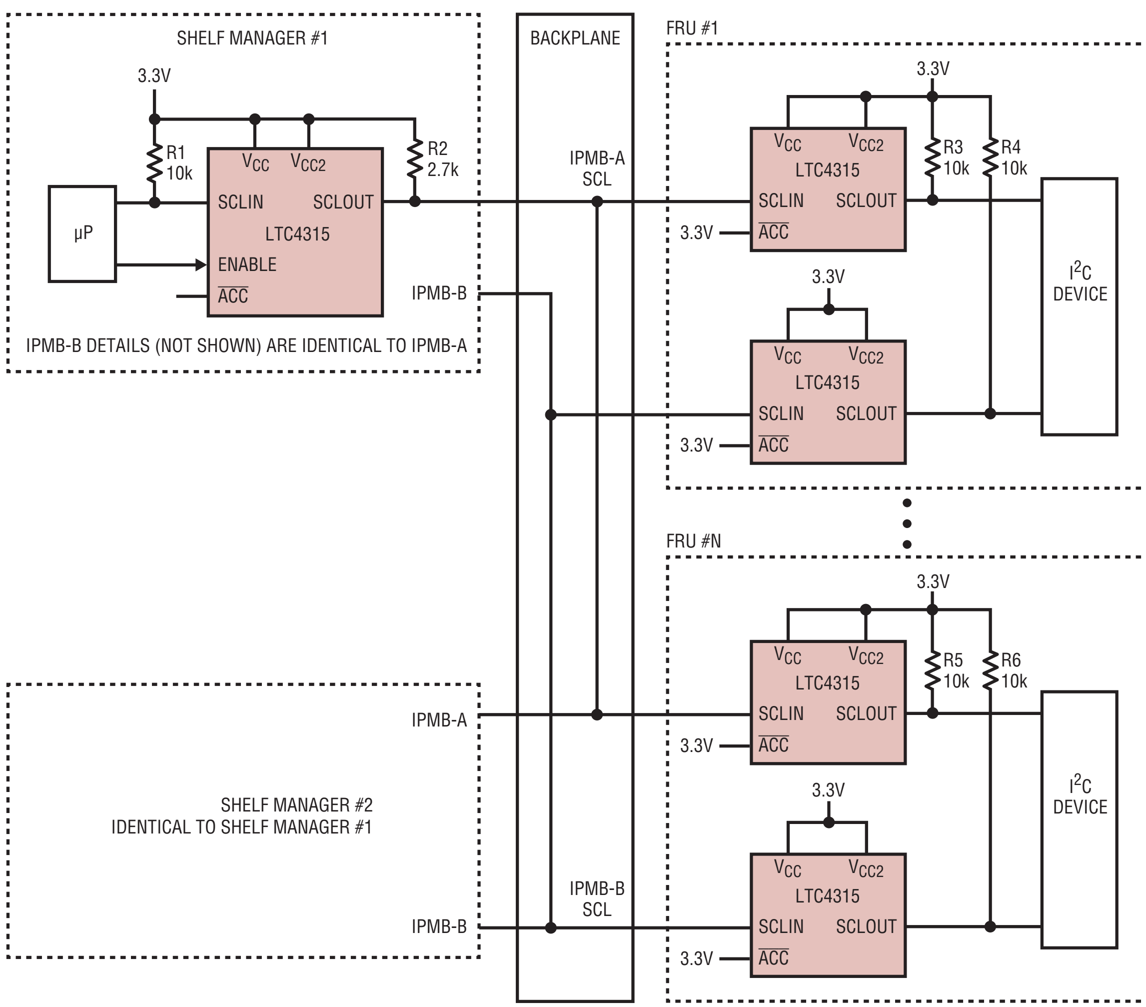


Figure 8. LTC4315s Used in a Bused ATCA Application. Only the Clock Path Is Shown for Simplicity.

APPLICATIONS INFORMATION

from a live backplane. The features mentioned previously provide noise immunity and allow timing specifications to be met for a wide range of backplane loading conditions.

In the 6 × 4 radial configuration shown in Figure 9, the LTC4314s on the shelf managers and the LTC4315s on the FRUs drive the large backplane capacitance while the I^2C slave devices on the FRUs only drive the small input capacitance of the LTC4315. The LTC4314s on only one of the shelf managers are enabled at a given time. All the benefits provided by the LTC4315 in Figure 8 apply to Figure 9 as well.

Cascading and Interoperability with Other LTC Buffers and Non-Compliant I^2C Devices

Multiple LTC4315s can be cascaded or the LTC4315 can be cascaded with other LTC bus buffers. Cascades often exist in large I^2C systems, where multiple I/O cards having bus buffers connect to a common backplane bus. Two issues need to be considered when using such cascades—the additive nature of the buffer logic low offset voltages and the impact of the RTA-buffer interaction on the noise margin.

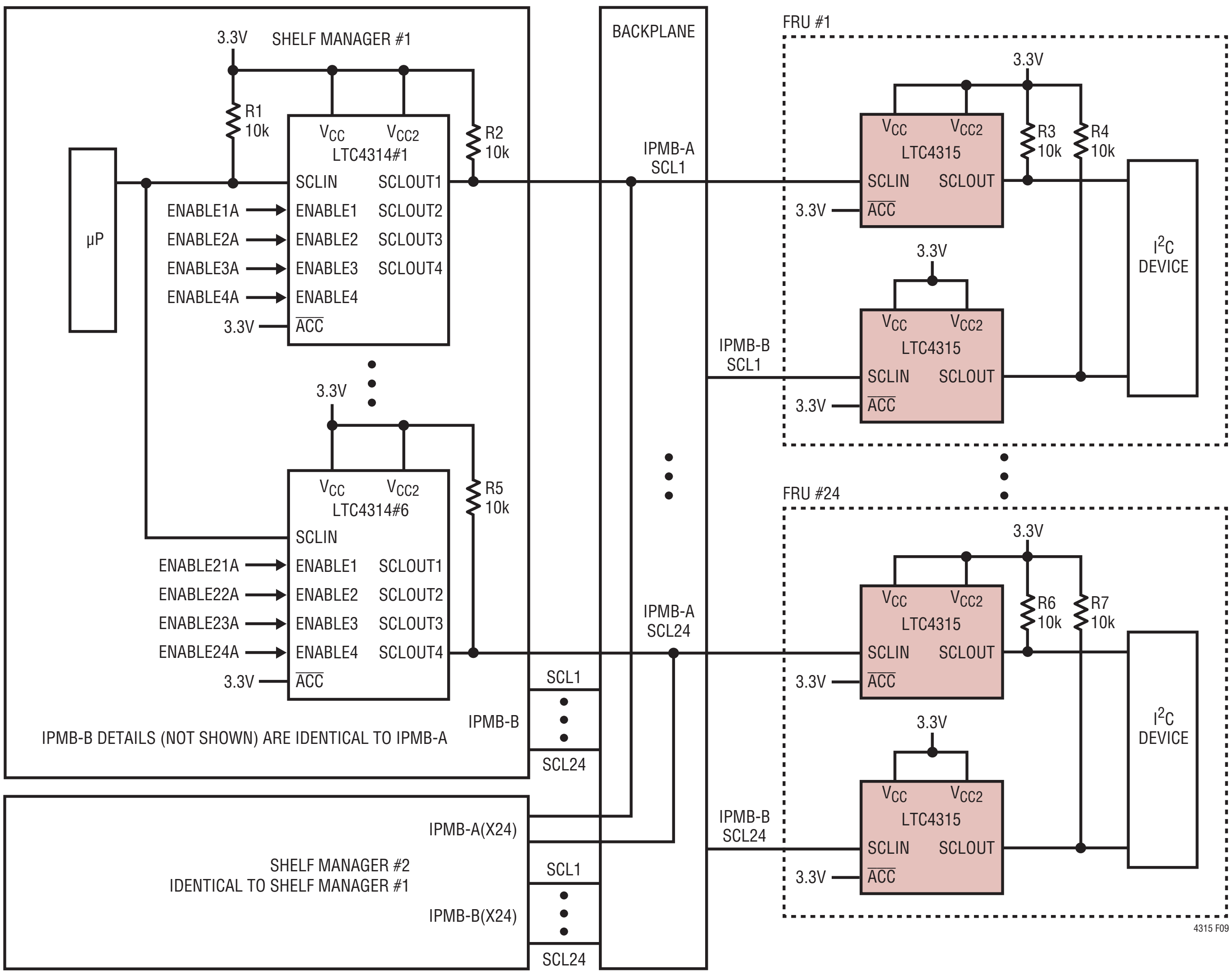


Figure 9. LTC4315s Used in a Radially Connected Telecommunications System in a 6 × 4 Arrangement. Only the Clock Path Is Shown for Simplicity. The Data Pathway Is Identical.

APPLICATIONS INFORMATION

First, when two or more buffers are connected in a cascade configuration, if the sum of the offsets across the cascade (refer to Equation 3 and the data sheets of the corresponding buffers) plus the worst-case driven logic low voltage exceeds the minimum buffer turn-off voltage, signals will not be propagated across the cascade. The maximum driven logic low voltage must be set accordingly, for correct operation in such cascades.

Second, noise margin is affected by cascading the LTC4315 with buffers whose RTA turn-on voltage is lower than the LTC4315 buffer turn-off voltage. The V_{IL} for the LTC4315 is set to $0.3 \cdot V_{MIN}$ to achieve high noise margin provided that the LTC4315 buffers do not contend with RTAs of other products. To maximize logic low noise margin, disable the RTAs of the other LTC buffers if possible and use the RTAs of the LTC4315 in cascading applications. To permit interoperability with other LTC buffers whose RTAs cannot be disabled, the LTC4315 senses the RTA current and turns off its buffers below $0.3 \cdot V_{MIN}$. This eliminates contention between the LTC4315 buffers and other RTAs, making the SDA/SCL waveforms monotonic.

Figure 10 shows the LTC4315 operating on a bus shared with LTC4300A and LTC4307 buffers. The corresponding SCL waveforms are shown in Figure 11. The RTAs on the LTC4300A and the LTC4307 cannot be disabled. The backplane in Figure 11 has five I/O cards connected to it. Each I/O card has a LTC bus buffer on its outside edge for SDA/SCL hot swap onto the backplane. In this

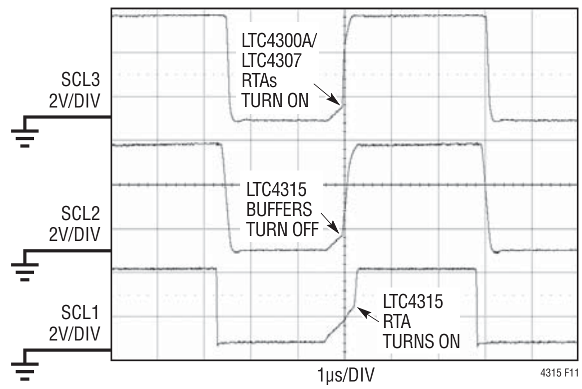


Figure 11. Corresponding SCL Switching Waveforms. No Glitches Are Seen.

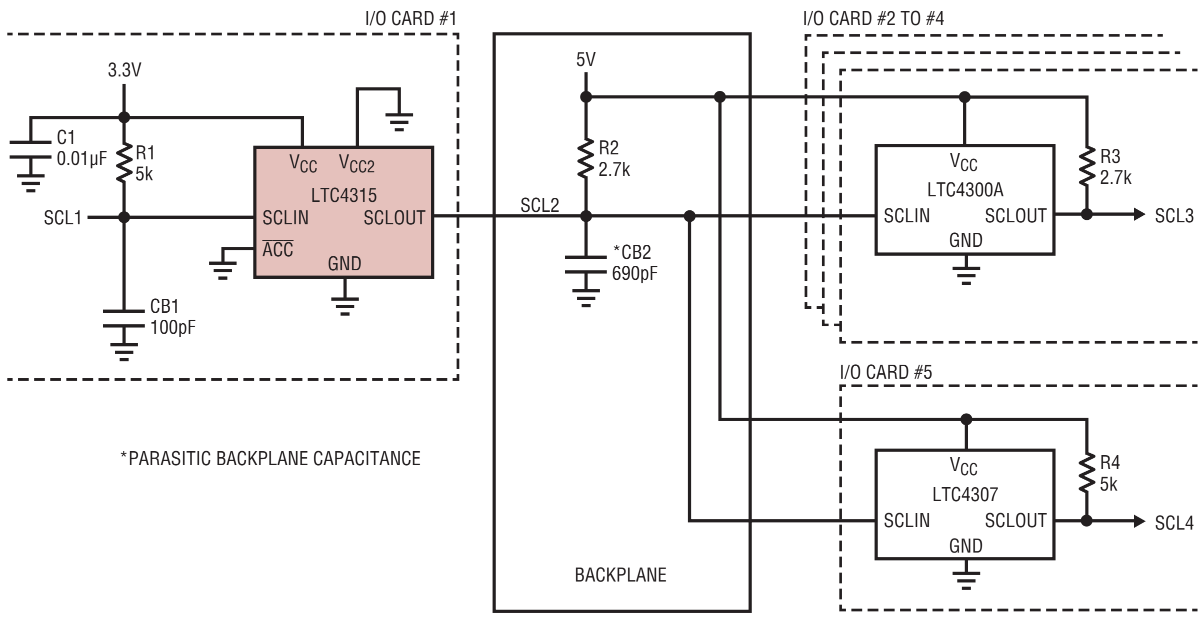


Figure 10. The LTC4315 Operating in a Cascade with Other LTC Buffers with Active RTAs. Only the Clock Pathway Is Shown for Simplicity

APPLICATIONS INFORMATION

example, there are three LTC4300As, one LTC4307 and one LTC4315. The SCL1 bus is driven by an I^2C master (master not shown). When the SCL2 voltage crosses 0.6V and 0.8V, the RTAs on the LTC4300A and LTC4307 turn on respectively and source current into SCL2. The LTC4315 detects this and turns off its buffers, releasing SCL1 and SCL2 high. Contention between the LTC4315 buffers and the LTC4300A and LTC4307 RTAs is prevented and the SCL1, SCL2 and SCL3 waveforms in Figure 11 are monotonic. The logic low noise margin is reduced because the LTC4315 buffers turn off when the SCL1 voltage is approximately 0.6V.

Generally, noise margin will be reduced if other RTAs turn on at a voltage less than $0.3 \cdot V_{MIN}$. The reduction in noise margin is a function of the number of LTC4315s and the number and turn-on voltage of other RTAs, whose current must be sunk by the LTC4315 buffers. The same arguments apply for non-LTC buffer products whose RTA turn-on voltage is less than $0.3 \cdot V_{MIN}$.

Interoperability is improved by reducing the interaction time between the LTC4315 buffers and other RTAs by reducing R1 and CB1. The following guidelines are recommended for single supply systems,

a. For 5V systems choose R1 < 20k and CB1 < 1nF. There are no other constraints.

b. For 3.3V systems, refer to Figures 12 and 13 for operation with LTC4300As and LTC4307s. In the figures:

$$M = \frac{\text{Number of LTC4300As or LTC4307s}}{\text{Number of LTC4315s}}$$

R1 and CB1 must be chosen to be below the curves for a specific value of M. For M greater than the values shown in the figures, non-idealities do not result. R1 < 20k and CB1 <1nF are still recommended.

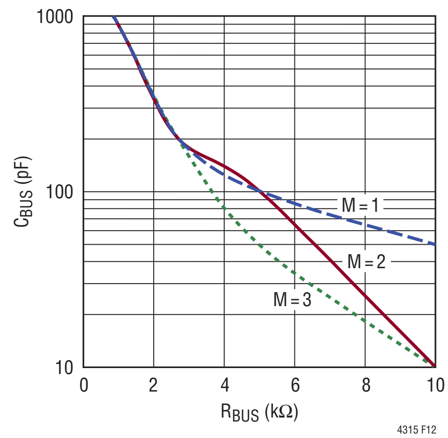


Figure 12. Recommended Maximum R1 and CB1 Values for the LTC4315 Operating with Multiple LTC4300As in a 3.3V System.

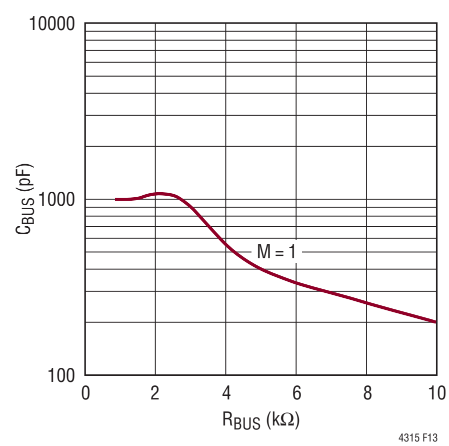


Figure 13. Recommended Maximum R1 and CB1 Values for the LTC4315 Operating with Multiple LTC4307s in a 3.3V System.

APPLICATIONS INFORMATION

The LTC4315 is interoperable with non-compliant I²C devices that drive a high V_{OL} > 0.4V. Figure 14 shows the LTC4315 in an application where a microcontroller communicates through the LTC4315 with a non-compliant I²C device that drives a V_{OL} of 0.6V. The LTC4313 buffers are active up to a bus voltage of 0.3 • V_{MIN} which is 1.089V in this case, yielding a noise margin of 0.489V.

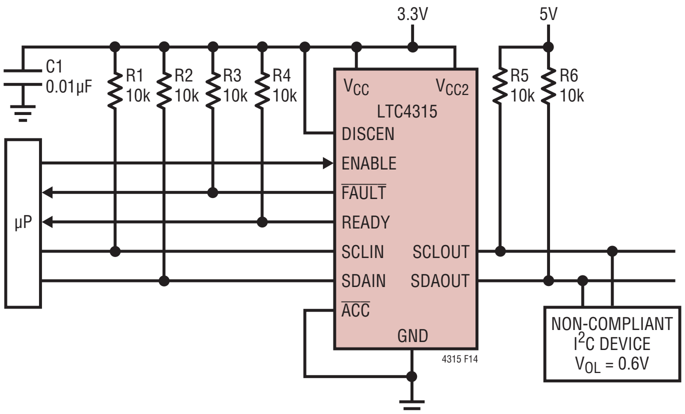


Figure 14. Communication with a Non-Compliant I²C Device Using the LTC4315.

Repeater Application

Multiple LTC4315s can be cascaded in a repeater application where a large 2-wire system is broken into smaller sections as shown in Figure 15. The high noise margin and low offset of the LTC4315 allows multiple devices to be cascaded while still providing good system level noise margin. In the repeater circuit shown in Figure 15, if SCL1/SDA1 is driven externally to 200mV, SCL2/SDA2 is regulated to ~440mV worst-case by the cascade of LTC4315s. The buffer turn-off voltage is 1.089V yielding a minimum logic low noise margin of ~650mV. In Figure 15, use of RTAs combined with an increased level of buffering reduces transition times and permits operation at a higher frequency.

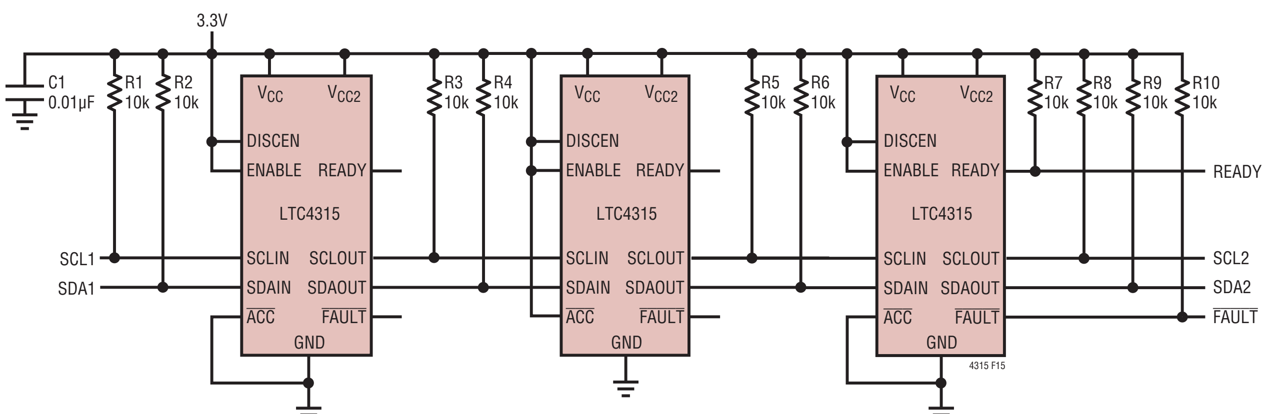
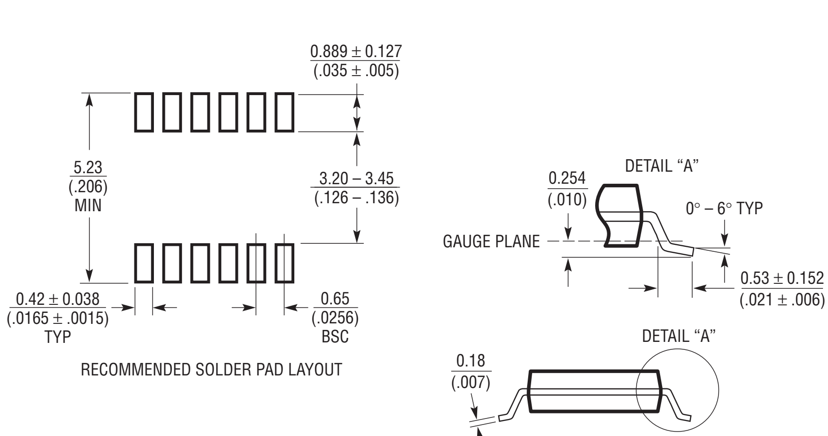


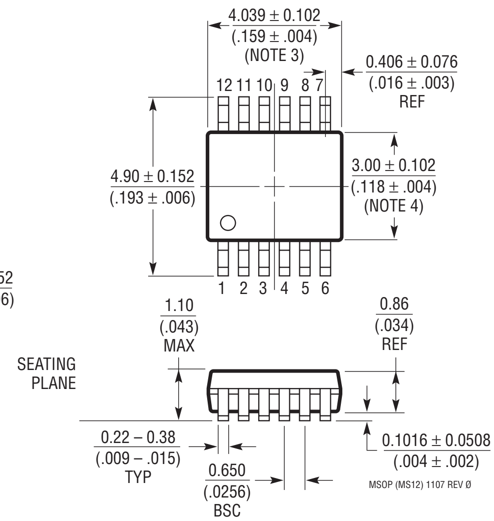
Figure 15. LTC4315s in a Repeater Application

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

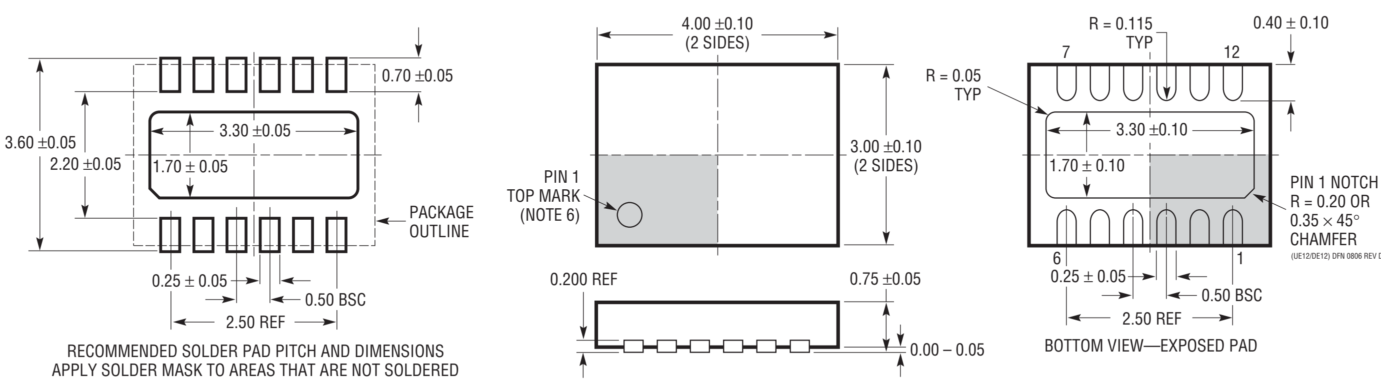
MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev Ø)





NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION
   (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE