I²C Slave Device Extender Over Rugged Differential Link

FEATURES

- **Up to 1MHz Serial Clock, Fast-mode Plus (Fm+)**
- **Selectable Link Baud Rates Extend I²C Up to 1200m**
- **Protected from Overvoltage Line Faults to ±60V**
- **±40kV ESD on Link Pins**
- **IEC Level 4 ESD ±8kV and EFT ±5kV on Link Pins**
- **Extended Common Mode Range: ±15V**
- Remote Interrupt/SMBALERT and Control Signals
- Low EMI Mode
- SMBus 3.0 Compatible
- I²C Idle Detection, and Stuck Bus Protection
- I²C Device Address Sharing
- 3V to 5.5V Supply Voltage
- 1.62V to 5.5V Logic Supply
- 4mm × 5mm 20-Lead QFN package

APPLICATIONS

- Industrial Control and Sensors
- Lighting and Sound System Control

DESCRIPTION

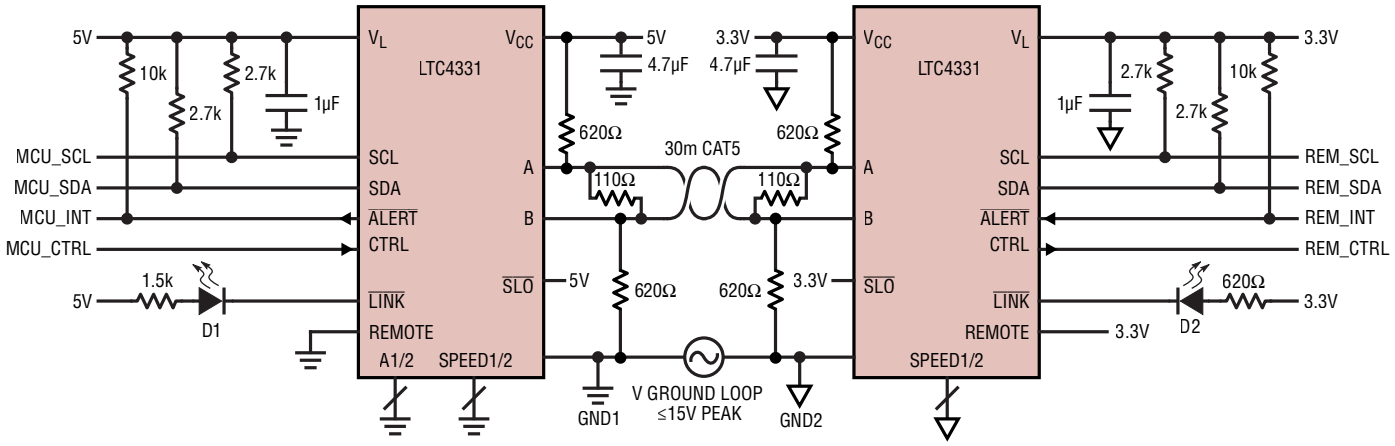
The LTC®4331 is a point-to-point SMBus compatible I²C slave device extender designed for operation in high noise industrial environments. Using a ±60V fault protected differential transceiver, the LTC4331 can extend an I²C/SMBus bus, including SMBALERT and a control signal, over a single twisted pair differential link up to 1200m. With an extended common mode operating range the solution provides tolerance to large ground differences between nodes. For EMI sensitive environments, a slew rate control pin reduces the EMI emitted from the differential link.

In addition, the LTC4331 can act as an I²C to I²C bridge allowing independent bus frequencies between the local and remote networks. The solution is completely transparent to the master requiring no additional code in most cases; however, a control interface is provided for additional configuration and fault monitoring.

A master controller fully supporting SCL clock-stretching is strongly recommended.

TYPICAL APPLICATION

Extended I²C Network Over 30m, 1MHz Fm+ SCL



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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- V_{CC} ..... –0.3V to 6V
- V_L ..... –0.3V to 6V

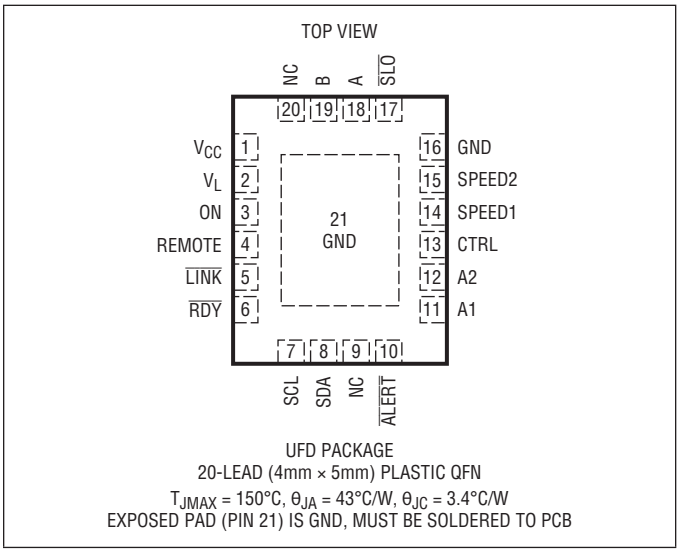
Logic Signals
- ON, $\overline{LINK}$, $\overline{RDY}$, SCL, SDA, $\overline{ALERT}$, $\overline{SLO}$ ..... –0.3V to 6V
- REMOTE, A1, A2, CTRL, SPEED1, SPEED2 ..... –0.3V to 6.3 or V_L + 0.3V

Interface I/O: A,B ..... –60V to 60V

Operating Ambient Temperature Range
- LTC4331C ..... 0°C to 70°C
- LTC4331I ..... –40°C to 85°C
- LTC4331H ..... –40°C to 125°C
- Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4331CUFD#PBF	LTC4331CUFD#TRPBF	4331	20-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4331IUFD#PBF	LTC4331IUFD#TRPBF	4331	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4331HUFD#PBF	LTC4331HUFD#TRPBF	4331	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, V_L = 3.3V, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	Operating Supply Range		●	3		5.5	V
I_{CC}	Operating Supply Current	Low Power: ON = 0	●		1	40	µA
		Idle: ON = 1, I^2C Bus Idle, Link = Fm+	●			12	mA
		Active: I^2C Transaction	●			65	mA
V_L	Logic Supply Range		●	1.62		5.5	V
I_L	Logic Supply Current		●			140	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, V_L = 3.3V, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver							
$\|V_{OD}\|$	Differential Driver Output Voltage	R = ∞ R = 27Ω (Figure 1)	● ●	1.5 1.5		V_{CC} 5	V V
I_{OSD}	Maximum Driver Short-Circuit Current	–60V ≤ (A or B) ≤ 60V (Figure 2)	●		±150	±250	mA
Differential Receiver							
R_{IN}	Receiver Input Resistance	0 ≤ V_{CC} ≤ 5.5V (Figure 3)			112		kΩ
V_{CM}	Receiver Common Mode Input Voltage		●			±15	V
V_{TH}	Differential Input Signal Threshold	–15V < V_{CM} < 15V (Note 2)	●			±200	mV
Logic							
V_{IH}	High Level Input Voltage (ON, CTRL, REMOTE)	1.62V < V_L < 5.5V	●	0.8 • V_L			V
	High Level Input Voltage (SCL, SDA, $\overline{ALERT}$)	1.62V < V_L < 5.5V	●	1.35			V
	High Level Input Voltage ($\overline{SLO}$)	3V < V_{CC} < 5.5V	●	0.67 • V_{CC}			V
V_{IH3ST}	High Level Input Voltage (A1, A2, SPEED1, SPEED2)		●	V_L – 0.25			V
V_{IM3ST}	Mid Level Input Voltage (A1, A2, SPEED1, SPEED2)		●	0.45 • V_L		0.55 • V_L	V
V_{IL3ST}	Low Level Input Voltage (A1, A2, SPEED1, SPEED2)		●			0.25	V
V_{IL}	Low Level Input Voltage (ON, CTRL, REMOTE)	1.62V < V_L < 5.5V	●			0.2 • V_L	V
	Low Level Input Voltage (SCL, SDA, $\overline{ALERT}$)	1.62V < V_L < 5.5V	●			0.8	V
	Low Level Input Voltage ($\overline{SLO}$)	3V < V_{CC} < 5.5V	●			0.33 • V_{CC}	V
	Digital Input Current (SCL, SDA, $\overline{ALERT}$)	V_{IN} = 0V to V_L	●			±5	µA
	Digital Input Current (ON, CTRL, A1, A2, REMOTE, SPEED1, SPEED2)	V_{IN} = 0V to V_L	●			±60	µA
	Digital Input Current ($\overline{SLO}$)		●		0	±5	µA
V_{OH}	High Level Output Voltage (CTRL)	I_{LOAD} = –500µA	●	V_L – 0.2			V
V_{OL}	Low Level Output Voltage ($\overline{LINK}$, $\overline{RDY}$, $\overline{ALERT}$, CTRL)	I_{LOAD} = 500µA	●			0.2	V
	Low Level Output Voltage (SCL, SDA)	I_{LOAD} = 20mA	●			0.4	V
I_{OZ}	High-Z Output Leakage Current (SCL, SDA, $\overline{ALERT}$, $\overline{LINK}$)		●			±5	µA
	High-Z Output Leakage Current ($\overline{RDY}$)		●			–60	µA
	Output Source Current (Short-Circuit) (CTRL)				–80		mA
	Output Sink Current (Short-Circuit) ($\overline{LINK}$, $\overline{RDY}$, $\overline{ALERT}$, CTRL)				80		mA
	Short-Circuit Current (SCL, SDA)				100		mA
C_{IN}	Input Pin Capacitance	SCL, SDA (Note 2)			10		pF

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, C_L = 20pF, V_{CC} = 5V, V_L = 3.3V, GND = 0V; unless otherwise noted. Conditions Fast-mode Plus, Fast-mode, and Standard-mode listed below as Fm+, Fm, and Sm respectively.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON_LOW}	Pulse Width of ON Low for Valid Reset Condition		●	1			µs
Local Mode (REMOTE = 0)							
t_{READY}	Delay From ON Rise to $\overline{RDY}$ Low	I²C Bus IDLE			65		µs
t_{REMOTE_RESET}	Delay From Local ON Low for Valid Remote Reset Condition		●	180			ms
$f_{SCL:SLAVE}$	Slave Device SCL Operating Frequency	(Note 3)	●	10	1000	2000	kHz
$t_{BUF:SLAVE}$	Bus free Time between STOP and START	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.5 1.3 4.7			µs µs µs
$t_{SU:STA:SLAVE}$	Repeated Start Condition Setup Time	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.26 0.6 4.7			µs µs µs
$t_{HD:STA:SLAVE}$	Hold Time after START Condition	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.26 0.6 4			µs µs µs
$t_{SU:STO:SLAVE}$	STOP Condition Setup Time	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.26 0.6 4			µs µs µs
$t_{SU:DAT:FSLAVE}$	Data Setup Time from LTC4331	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	50 100 250			ns ns ns
$t_{SU:DAT:TSLAVE}$	Data Setup Time to LTC4331		●	50			ns
$t_{HD:DAT:TSLAVE}$	Data Hold Time to LTC4331		●	0			ns
$t_{HD:DAT:FSLAVE}$	Data Hold Time from LTC4331		●	50			ns
$t_{TIMEOUT:SLAVE}$	SCL Low Timeout Detection		●	28	31.5	35	ms
$t_{LOW:SLAVE}$	SCL Low Time		●	0.25			µs
$t_{HIGH:SLAVE}$	SCL High Time		●	0.25		50	µs
$t_{HIGH:IDLE}$	SCL High for Bus Idle Detection		●	70			µs
Remote Mode (REMOTE = 1)							
$t_{SCL:MASTER}$	Master Device SCL Operating Period	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	1 2.5 10			µs µs µs
$t_{BUF:MASTER}$	Bus Free Time between STOP and START	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.5 1.3 4.7	0.6 1.5 5		µs µs µs
$t_{HD:STA:MASTER}$	Hold Time after START Condition	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.26 0.6 4	0.3 0.8 4.2		µs µs µs
$t_{SU:STA:MASTER}$	Repeated Start Condition Setup Time	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.26 0.6 4.7	0.3 0.8 4.8		µs µs µs
$t_{SU:STO:MASTER}$	Setup Time for STOP	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.26 0.6 4	0.3 0.8 4.2		µs µs µs

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, C_L = 20pF, V_{CC} = 5V, V_L = 3.3V, GND = 0V; unless otherwise noted. Conditions Fast-mode Plus, Fast-mode, and Standard-mode listed below as Fm+, Fm, and Sm respectively.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{HD:DAT:FMASTER}$	Data Hold from LTC4331		●	50			ns
$t_{HD:DAT:TMASTER}$	Data Hold to LTC4331	(Note 2)	●	0			ns
$t_{SU:DAT:FMASTER}$	Data Setup from LTC4331	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	50 100 250			ns ns ns
$t_{SU:DAT:TMASTER}$	Data Setup to LTC4331		●	50			ns
$t_{TIMEOUT:MASTER}$	SCL Low Timeout Detection		●	28	31.5	35	ms
$t_{LOW:MASTER}$	SCL Low Time	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.6 1.5 5.8			µs µs µs
$t_{HIGH:MASTER}$	SCL High Time	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm SPEED1/SPEED2 = Sm	● ● ●	0.4 1 3.8			µs µs µs
t_F	Fall Time (SDA, SCL) (Note 5)	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm, Sm C_L = 550pF, R_L = 1kΩ (Figure 5) (Note 2)	● ● ●			120 300 25	ns ns ns
t_R	Rise Time (SDA, SCL) (Note 5)	SPEED1/SPEED2 = Fm+ SPEED1/SPEED2 = Fm, Sm	● ●			120 300	ns ns
t_{SPIKE}	Noise Spike Suppression Time (SDA, SCL)		●	0		50	ns
Transceiver							
t_{RD}, t_{FD}	Driver Rise or Fall Time (Figure 4)	R_{DIFF} = 54Ω, C_L = 100pF, $\overline{SLO}$ = 1 R_{DIFF} = 54Ω, C_L = 100pF, $\overline{SLO}$ = 0	● ●	 500	4 800	15 1200	ns ns
$t_{LINK\_TIMEOUT}$	Response Time for $\overline{LINK}$ = 1 after Disconnection	REMOTE = 1 REMOTE = 0 (Note 4)			168 96 • SF		ms µs
System							
t_{ALT_PROP}	$\overline{ALERT}$ Propagation Delay, Remote to Local	I²C Bus idle (Note 4)		0.8 • SF	2 • SF	26 • SF	µs
t_{CTRL_PROP}	Local CTRL Propagation Delay to Remote CTRL	I²C Bus idle (Note 4)		0.8 • SF	2 • SF	26 • SF	µs
t_{START_PROP}	I²C START Link Propagation Delay, Local to Remote	(Note 4)			2 • SF		µs
t_{LDAT_PROP}	I²C DATA Link Propagation Delay, Local to Remote	(Note 4)			2 • SF		µs
t_{STOP_PROP}	I²C STOP Link Propagation Delay, Local to Remote	(Note 4)			2 • SF		µs
t_{RDAT_PROP}	I²C DATA Link Propagation Delay, Remote to Local	(Note 4)			2 • SF		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design, not production tested.

Note 3: Local SCL frequencies between 1000kHz and 2000kHz are allowed, however the effective link throughput maximum is 1000kHz. SCL low clock-stretching by the LTC4331 must be respected.

Note 4: SF = Speed Factor. See Table 3.

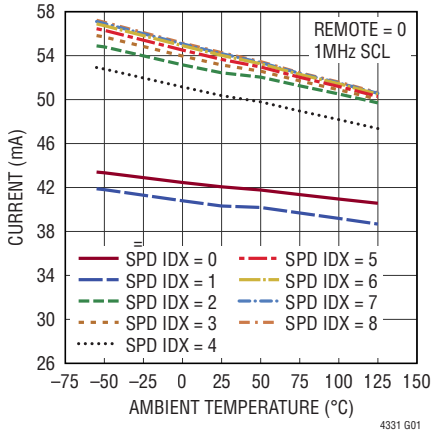
Note 5: SCL and SDA rise and fall time measurement limits are defined as follows:

Rise Time Limit: 0.65V to 1.5V
Fall Time Limit: 1.5V to 0.65V

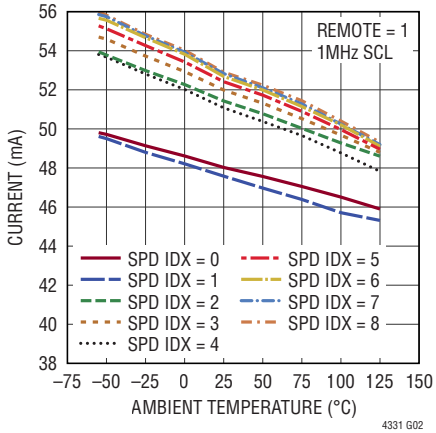
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, V_L = 3.3V, GND = 0V, unless otherwise noted.

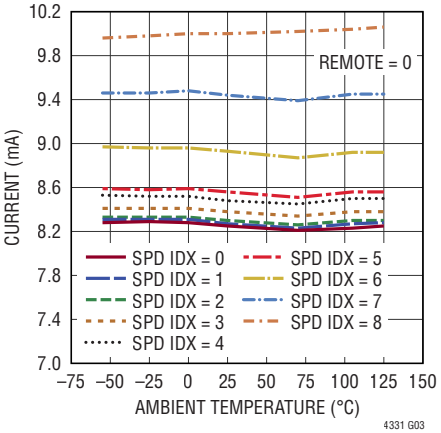
I_{CC} vs Temperature Burst I^2C Write Traffic



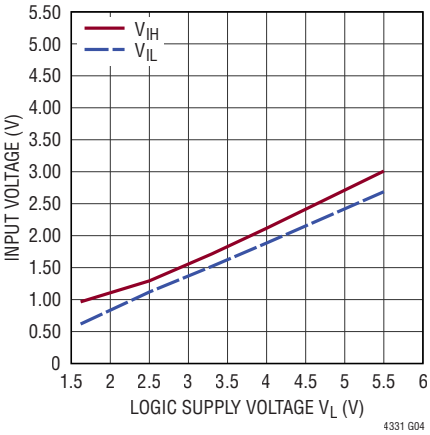
I_{CC} vs Temperature Burst I^2C Read Traffic



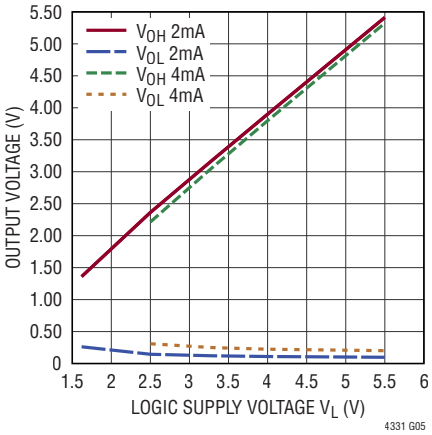
I_{CC} vs Temperature I^2C Bus Idle



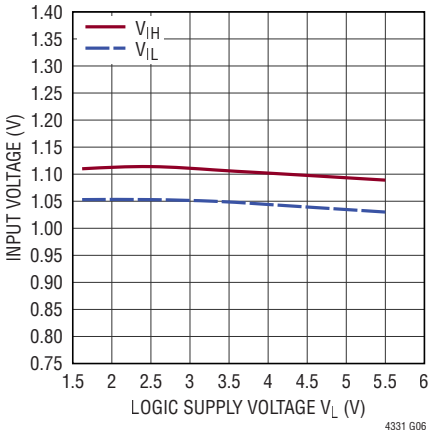
ON, CTRL, and REMOTE Inputs V_{IL} and V_{IH} vs V_L Supply



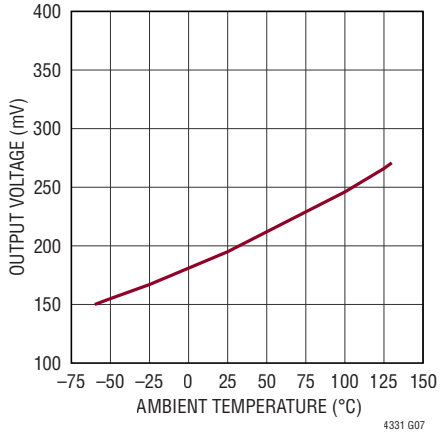
CTRL Output (2mA and 4mA) V_{OL} and V_{OH} vs V_L Supply



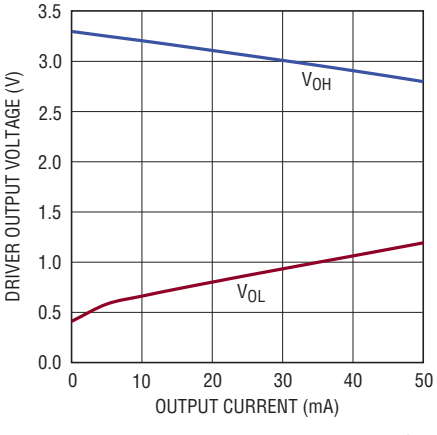
I^2C SCL and SDA Input V_{IL} and V_{IH} vs V_L Supply



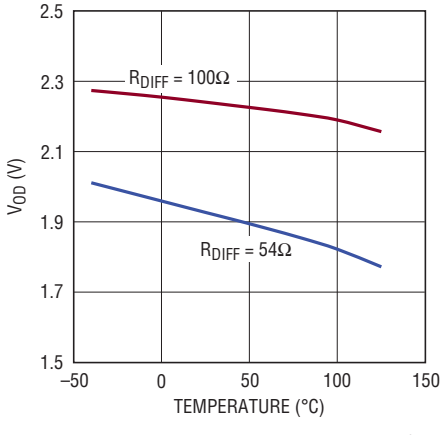
I^2C SCL and SDA Output V_{OL} at 20mA vs Temperature



A/B Driver Output Low/High Voltage vs Output Current



A/B Driver Differential Output Voltage vs Temperature



PIN FUNCTIONS

Logic (All Logic Side Inputs and Outputs Referenced to GND and V_L Except $\overline{SLO}$, which Is Referenced to GND and V_{CC})

V_{CC} (Pin 1): Supply Voltage. $3V < V_{CC} < 5.5V$. Bypass with 4.7µF ceramic capacitor to GND.

V_L (Pin 2): Logic Supply Voltage. $1.62V < V_L < 5.5V$. Bypass with 1µF ceramic capacitor to GND.

ON (Pin 3): Enable Input. Set high for operation. Set low for low power mode, in which the internal reset is held and outputs are disabled. Connect to V_L if unused.

REMOTE (Pin 4): Operating Mode Select Input. Set low for local I²C slave mode. Set high for I²C master mode when used on the remote side. REMOTE is weakly pulled to GND.

$\overline{LINK}$ (Pin 5): Link Status Open-Drain Output. When in remote mode, $\overline{LINK}$ is driven low when the device establishes link communication. When in local mode, $\overline{LINK}$ is driven low after the LTC4331's I²C interface has joined the I²C bus in addition to establishing link communication. The link status function is only valid when an LTC4331 configured to local mode (REMOTE set low) connects to a second LTC4331 configured to remote mode (REMOTE set high). Connect to an external pull-up to V_L to monitor status, otherwise float or connect to GND.

$\overline{RDY}$ (Pin 6): I²C Ready Status Open-Drain Output. $\overline{RDY}$ is driven low after the device's I²C interface has joined the bus. Use to detect when the LTC4331's control interface is available in the absence of a connected link. $\overline{RDY}$ has a weak internal pull-up to V_L and is only valid when in local mode. In remote mode the pin can be unconnected.

SCL (Pin 7): I²C Serial Clock. Low side output driver and input. Connect to an external pull-up.

SDA (Pin 8): I²C Serial Data. Low side output driver and input. Connect to an external pull-up.

NC (Pins 9, 20): Unconnected Pins. Float or connect to GND.

$\overline{ALERT}$ (Pin 10): SMBALERT/Interrupt. $\overline{ALERT}$ is an open-drain output in local mode and an input in remote mode. Values set on the remote side $\overline{ALERT}$ propagate to the local side $\overline{ALERT}$ pin. In addition, $\overline{ALERT}$ is the SMBALERT function for the local side's I²C control interface when enabled. The $\overline{ALERT}$ pin switches to a level-sensitive active low interrupt signal when register field INTR_MODE = 1. Connect to an external pull-up on the local side. Do not allow the $\overline{ALERT}$ pin to float on the remote side.

A1 (Pin 11): I²C Device Address Select 1. A1 is a 3-state input. A1 in conjunction with A2 selects one of eight possible I²C addresses assigned to the internal slave device. Float pins A1 and A2 to disable the internal I²C device. Set to high, low, or float as defined in Table 4.

A2 (Pin 12): I²C Device Address Select 2. A2 is a 3-State input. A2 in conjunction with A1 selects one of eight possible I²C addresses assigned to the internal slave device. Float pins A1 and A2 to disable the internal I²C device. Set to high, low, or float as defined in Table 4.

CTRL (Pin 13): Local to Remote Control. Values set on the local side CTRL pin propagate to the remote side CTRL pin over the differential link. On the remote side, CTRL is not driven at startup until the differential link is established. CTRL has a weak pull-up to V_L and can be unconnected if not used.

SPEED1 (Pin 14): Link and Interface Timing Select 1. SPEED1 is a 3-state input and in conjunction with SPEED2 selects link baud rate and I²C bus timing. Set to high, low, or float as defined in Table 2.

SPEED2 (Pin 15): Link and Interface Timing Select 2. SPEED2 is a 3-state input and in conjunction with SPEED1 selects link baud rate and I²C bus timing. Set to high, low, or float as defined in Table 2.

GND (Pin 16): Ground.

$\overline{SLO}$ (Pin 17): Link Slow Mode Input. Set low to limit the link transmitter slew rate which also limits the maximum link rate set by SPEED1 and SPEED2. Only valid for SPEED INDEX 0 and 1. $\overline{SLO}$ is referenced to GND and V_{CC}. Do not allow pin $\overline{SLO}$ to float.

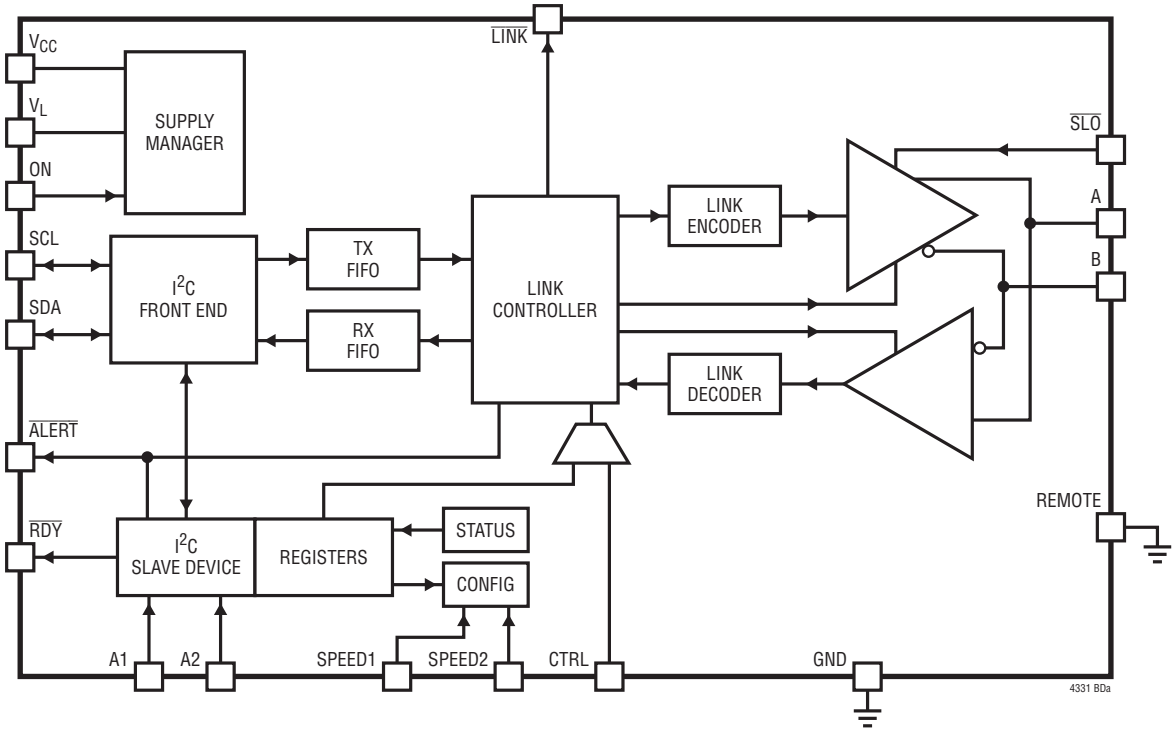
Link

A (Pin 18): Noninverting Link Transceiver Pin.

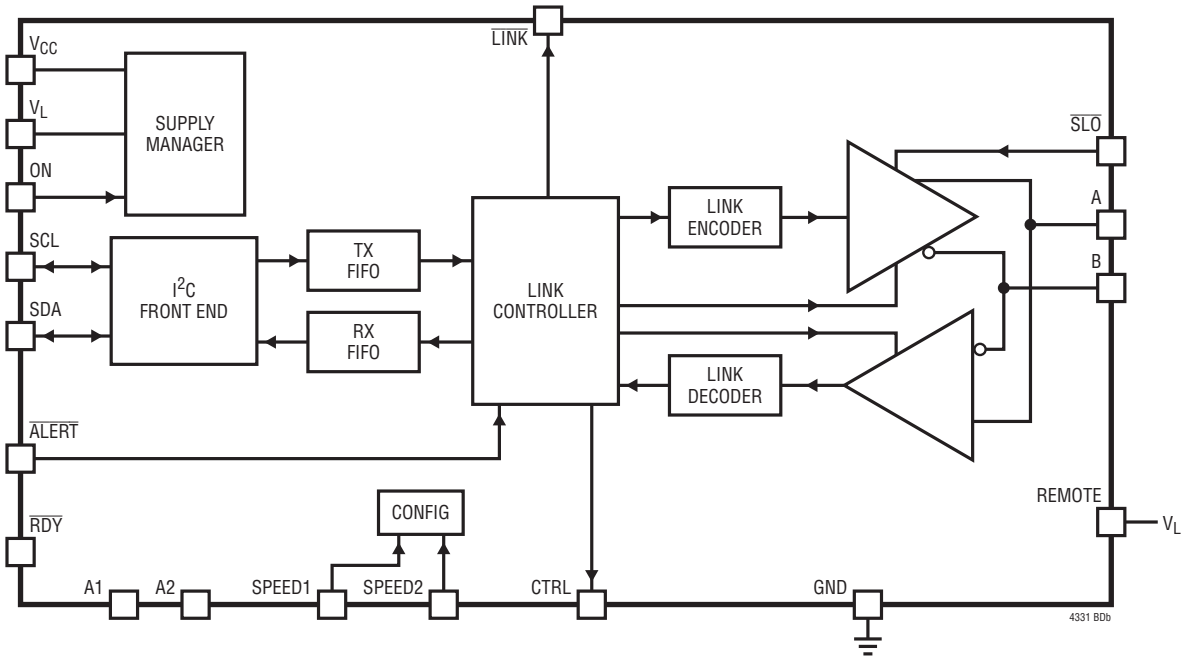
B (Pin 19): Inverting Link Transceiver Pin.

BLOCK DIAGRAM

Local Mode



Remote Mode



TEST CIRCUITS

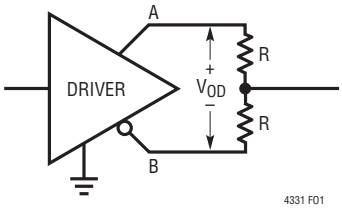


Figure 1. Driver DC Characteristics

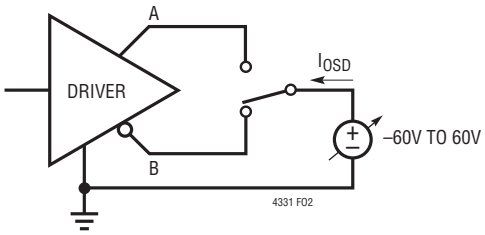


Figure 2. Driver Output Short-Circuit Current

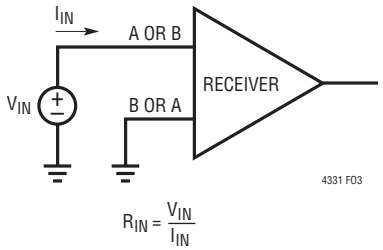


Figure 3. Receiver Input Current and Input Resistance

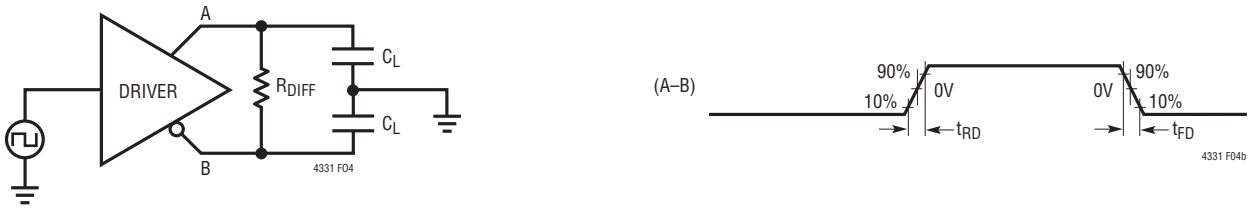


Figure 4. Driver Timing Measurement

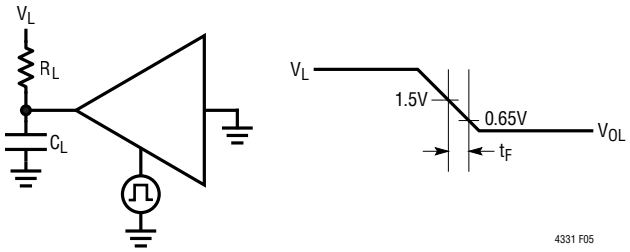


Figure 5. SCL and SDA Driver Timing Measurement

TIMING DIAGRAMS

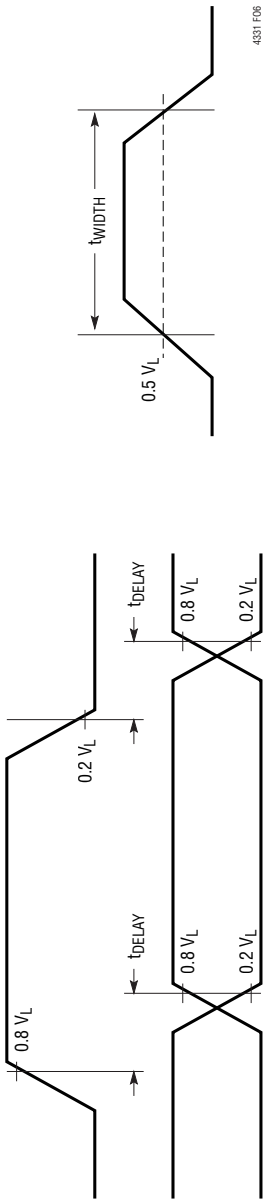


Figure 6. Logic I/O Voltage Levels for Timing Specification (Except SCL and SDA)

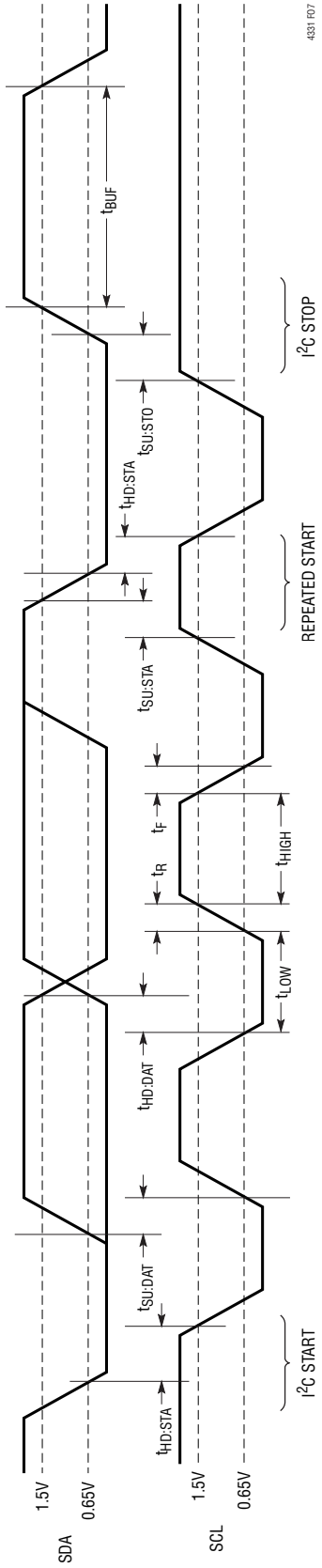


Figure 7. I²C Voltage Levels and Timing

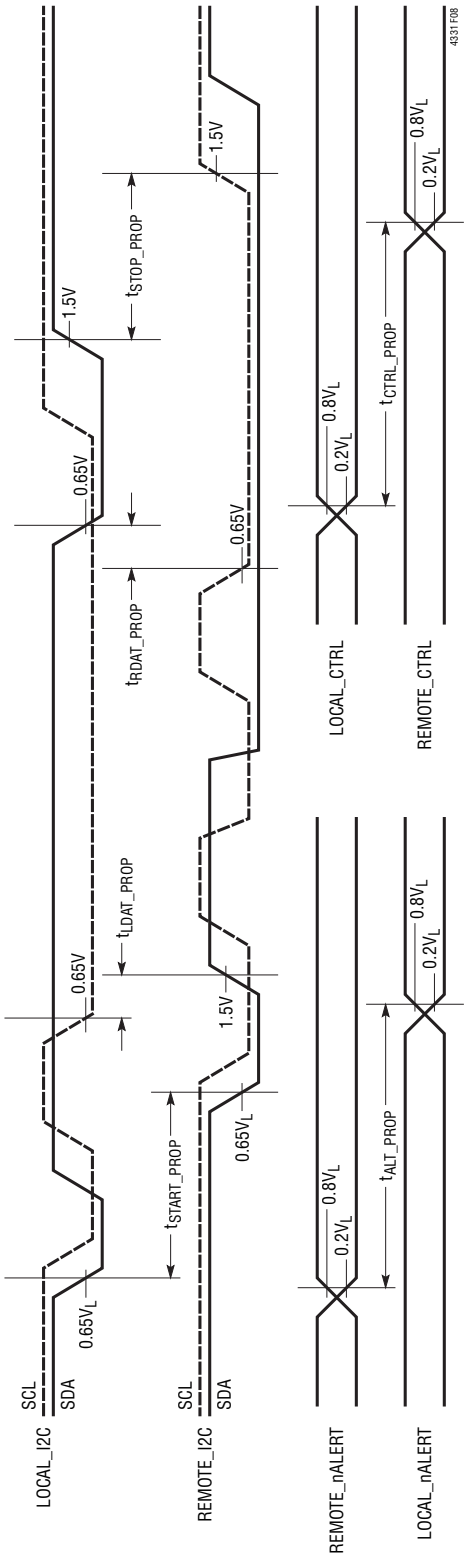


Figure 8. Propagation Timing

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Overview

Two LTC4331 devices are required for a complete extended I²C network. Using the REMOTE pin, one LTC4331 is configured to local mode and acts as a full-featured SMBus compatible I²C slave device. Through this local interface a master can address a remote slave device up to 1200m away along a differential cable. On the remote network a second LTC4331 configured to remote mode acts as an I²C master device connected to the remote slave devices. The master interface mirrors the local I²C transactions on the remote network and transmits the remote slave responses back to the local network. In most cases the link is transparent; the remote slave devices appear as local devices to a local master.

A separate addressable slave device contained in the local side LTC4331 provides a control interface for optional configuration and event monitoring of the link.

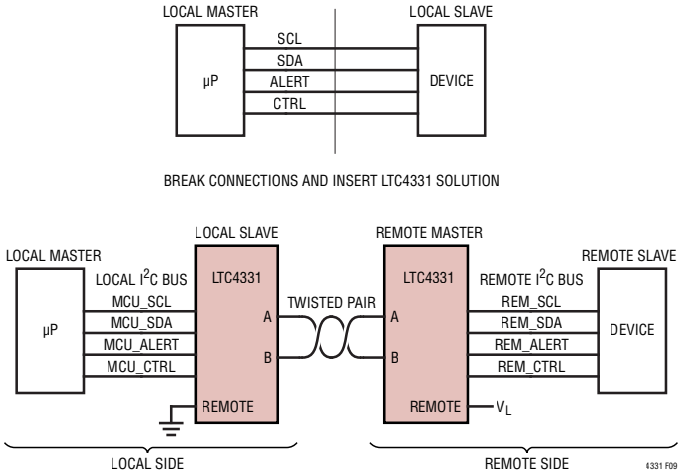

Figure 9. LTC4331 Solution Inserted Into an I²C Network.

Local Mode

On the local side, set the REMOTE pin low to put the LTC4331 in local mode. In this mode the LTC4331 operates as a slave device. The I²C interface is designed to be compatible with I²C Fast-mode Plus, Fast-mode, or Standard-mode class timing specifications selectable using pins SPEED1 and SPEED2.

When operating as a slave-receiver the LTC4331 captures I²C START, STOP, and data events sent by a local I²C master. The device transmits these events across the differential link as an encoded bit-stream to a second LTC4331 which is set to remote mode. After an I²C bus turnaround, the device operates as a slave-transmitter and the differential link direction is reversed. The remote LTC4331 transmits the response data measured from the remote I²C bus onto the twisted pair cable. The local side LTC4331 then decodes the transmitted bit-stream into I²C data events and drives them onto the local I²C bus.

When operating as a slave-transmitter, the local LTC4331 must periodically stall the local I²C bus to account for remote I²C bus and link latencies. It does this by clock-stretching whenever a valid response is not yet available. Therefore it is recommended that the local I²C master device fully support SCL clock-stretching for each response (N)ACK and data bit. See section Considerations.

By using SCL clock-stretching to account for link and remote device latency, the local I²C clock rate is decoupled from the link baud rate and remote I²C clock rate. This allows independent I²C bus rates between the local and remote networks.

Remote Mode

On the remote side, set the REMOTE pin high to put the LTC4331 in remote mode. In this mode the LTC4331 operates as an I²C master device. In normal operation the remote master mirrors the I²C events produced by the local I²C master. The device recreates the events using Fast-mode Plus, Fast-mode, or Standard-mode class timing specifications. The timing class is selected by pins SPEED1 and SPEED2.

The LTC4331 does not support multiple masters on the remote I²C networks. The LTC4331's I²C master device interface is the only allowed master on the remote side network. Remote slaves are also forbidden to switch to master mode, for example as part of a host-notify operation.

The LTC4331 master interface fully supports slave device clock-stretching for all data bits in the packet.

I²C Transactions

A local master initiates a transaction by sending an I²C START along with the slave address byte. The LTC4331

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device, configured for local mode, encodes and transmits the captured I²C events to the remote I²C network where they are recreated on the remote I²C bus. If additional LTC4331 devices configured as slaves, REMOTE set low, are connected to the remote I²C network, they also transmit the events to the 3rd tier I²C network, and so on. The local side LTC4331 always holds SCL low on the 9th bit waiting for an (N)ACK response from the remote slave device(s). When the local side LTC4331 receives the response, SCL is released with the response data set on the I²C bus. If the R/W bit is set to Write, the bus turns around after the ACK and the local LTC4331 switches back to slave-receive mode in order to capture the incoming write data. After the 8th SCL clock, the bus and link direction reverse in order to retrieve the (N)ACK response from the remote slave device. This sequence continues until the master sends a START or STOP condition. Data to be transferred across the link is stored in a buffer if the local I²C transaction is faster than the effective link rate. See Figure 10.

If a local LTC4331 detects that all remote slaves have NACK'd the slave address byte, it ceases transmitting further I²C data to the remote side until a STOP or REPEATED START condition is detected. This feature prevents the LTC4331 from stalling the bus unnecessarily when the transaction is addressed to a separate local slave device. Note that in this scenario, the remote side SCL is held low until a STOP or START condition is detected. Unusually long cycle times could activate the $t_{TIMEOUT}$ condition.

In the case of a read transaction to a remote slave device, the local LTC4331 slave device stalls the bus during the read data phase. During this time, the remote LTC4331 I²C master prefetches the next byte from the remote slave device. The read data byte is transmitted across the differential link and stored in a local buffer. As bits become available in the local buffer, the local LTC4331 drives them onto SDA and releases SCL according to the configured setup time $t_{SU:DAT:SLAVE}$. After the complete byte has been read, the I²C bus and differential link are turned around. The local I²C master either ACKs or NACKs during this time. If the master ACKs, the sequence is repeated. This bus and link direction is reversed, and the next byte is prefetched from the remote slave device. If the master then NACKs, the bus and link do not reverse direction. The master is then expected to send a STOP or START event. See Figure 11.

Differential Link

Internally, the LTC4331 utilizes a high performance RS485 compliant transceiver to communicate over the link. The A and B pins are fault protected to ±60V. In addition, the transceiver operates over an extended common mode range of ±15V making it suitable for noisy environments or systems with ground potential differences. Data is exchanged between the LTC4331 devices using a custom packet which has a selectable baud rate based on the configuration of the SPEED1 and SPEED2 pins. Selectable baud rates over the cable allow balancing performance with cable length specific to the application. Both sides of the link must be set to the same speed configuration in order to match the baud rates and allow communication.

The LTC4331 allows slew rate limiting over the differential link outputs to reduce EMI in sensitive applications. Setting the $\overline{SLO}$ pin low activates the slew rate limiting circuit. Once in slew limiting mode, SPEED1 and SPEED2 pins must only be configured for Speed Index 0 or 1. Setting SPEED1/2 to a speed index of 2 or higher when $\overline{SLO}$ is low results in link data corruption regardless of cable length.

The LTC4331 I²C slave device extension solution is point-to-point only. Multidrop or multipoint configurations on the differential link are not allowed.

±40kV ESD Protection

The LTC4331 features exceptionally robust ESD protection. The link interface pins (A, B) feature protection to ±40kV HBM with respect to GND, V_{CC} (with a 4.7µF capacitor to GND), A or B without latchup or damage, during all modes of operation or while unpowered.

Level 4 IEC ESD and EFT Protection

The improved ESD protection of the LTC4331 provides a high level of protection in the IEC ESD and EFT (Electrical Fast Transient) tests. The IEC ESD stress exceeds that of the HBM test in peak current, amplitude, and rise time, while the EFT test provides a prolonged repetitive stress. Combined with the HBM test, the IEC tests help ensure that the LTC4331 is robust under a wide range of real

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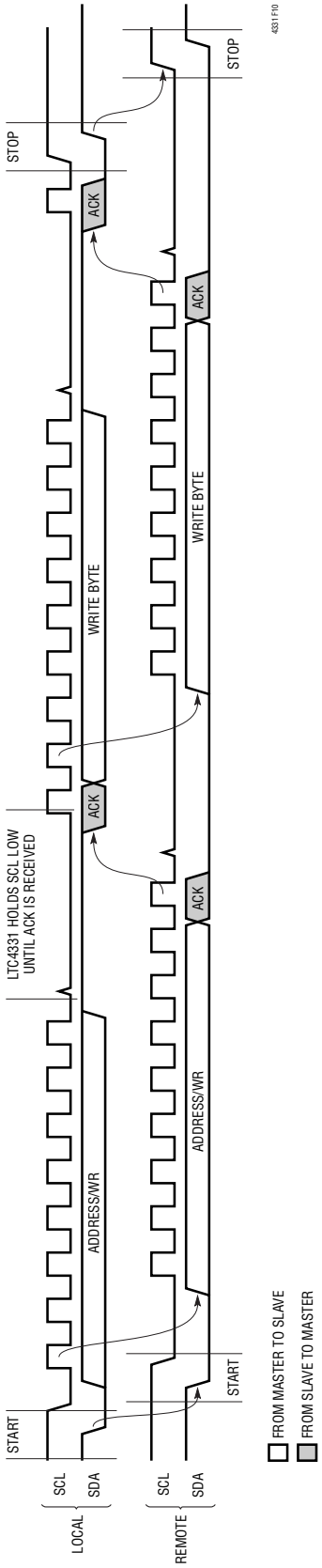

Figure 10. Full Write

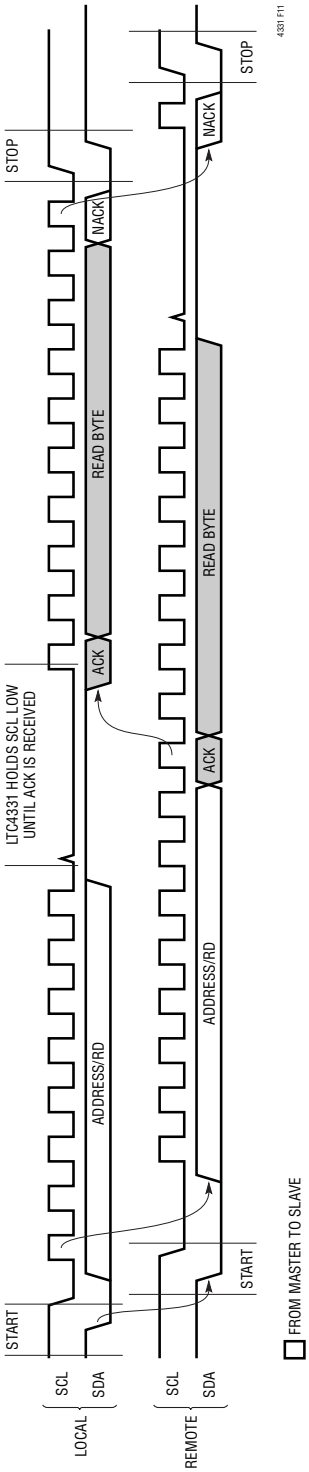

Figure 11. Full Read

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world hazards. The LTC4331 passes the following tests on the A, B pins:

- IEC 61000-4-2 Edition 2.0 2008-12 ESD Level 4: ±8kV contact (A or B to GND, direct discharge to bus pins with transceiver and protection circuit mounted on a test card with a low impedance ground discharge path from board GND to ESD gun return lead, per Figure 4 of the standard)
- IEC 61000-4-4 Second Edition 2004-07 EFT Level 4: ±5kV (A or B to GND, 5kHz repetition rate, 15ms burst duration, 60 second test duration, discharge coupled to bus pins through 100pF capacitor per paragraph 7.3.2 of the standard). V_{CC} pin requires a low inductance capacitor of at least 4.7µF to meet Level 4 rating.

Startup and Shutdown

Startup occurs when supply voltages are applied to pins V_{CC} and V_L and the ON pin is high. All output pins are tri-stated during the first part of startup. After an initialization sequence, the I^2C interface and other pins are functional. The local side LTC4331 monitors the I^2C bus for inactivity and probes the differential link. When the device detects an idle condition on the local I^2C bus, it drives pin $\overline{RDY}$ low to indicate that it is ready to respond to I^2C transactions. Thereafter a master can access the internal control interface. In addition, once the device establishes link communication with a remote LTC4331, it drives pin $\overline{LINK}$ low and the remote I^2C network can be accessed.

The ON pin can be used to set the LTC4331 to a lower power state. By setting ON low, the LTC4331 is held in reset, all programmed configuration is set to the default value, all output drivers are disabled, and the differential transceiver is put into low power mode. If not used, tie ON to V_L.

Link Status

The LTC4331 provides the $\overline{LINK}$ pin which indicates if the remote I^2C network has joined with the local I^2C network. $\overline{LINK}$ is driven low when bidirectional link communication is established and the I^2C interface is ready. It is an open-drain output and requires an external pull-up to V_L if used. At startup, the $\overline{LINK}$ pin output driver is disabled.

Link status can also be monitored using the control interface. See section Control Interface.

Ensure that the values set on local side SPEED1 and SPEED2 pins match the values set on remote side. Also, do not exceed the cable length listed in Table 2 for the given SPEED setting. The LTC4331 will not link if these conditions are not met.

Note that the link status is indeterminate if the REMOTE pin is incorrectly configured on either the local or remote side LTC4331 device.

Ready Status

The $\overline{RDY}$ pin is driven low when the local side LTC4331 control interface is ready for access. It is an open-drain output and only valid in local mode. When the device is first powered and pin ON is set high, the low output driver on $\overline{RDY}$ is disabled and the pin is weakly pulled to V_L. An internal I^2C bus idle detection circuit prevents the interface from interrupting an active transaction. This circuit drives $\overline{RDY}$ low when either pin SCL is high for $t_{READY:IDLE}$ or it detects an I^2C STOP which indicates the interface is ready and has joined the bus. The status of the link connection does not affect the ready function. If pin $\overline{LINK}$ is high when $\overline{RDY}$ is low, only the local side LTC4331 control interface is available for access. The $\overline{RDY}$ pin is internally pulled to V_L. It is valid only in local mode.

A secondary function of $\overline{RDY}$ indicates if the internal buffer has filled, see section Considerations for more detail.

Interrupt/SMBALERT

The LTC4331 supports an interrupt signal that is mirrored from the remote network to the local network using the differential link. On the remote side $\overline{ALERT}$ is an input pin that can be connected to remote I^2C slave devices. While on the local side $\overline{ALERT}$ operates as an open-drain type output that can be connected to a shared local interrupt line. $\overline{ALERT}$ is periodically sampled and has a propagation time of t_{ALT_PROP}.

If enabled, the local LTC4331's control interface uses the $\overline{ALERT}$ pin to report link and fault events. The local side $\overline{ALERT}$ output is the logical AND of the remote $\overline{ALERT}$ and the internal endpoint interrupt signal.

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By default the local addressable slave device in the LTC4331 recognizes the Alert Response Address (ARA) and participates in the Alert Response protocol. If an EVENT is triggered and its corresponding ALERT_EN bit is set high, $\overline{\text{ALERT}}$ is driven low. If the master transmits the Alert Response protocol and the LTC4331's internal slave address is the lowest numerically, then the LTC4331 releases its local alert output. Note that local $\overline{\text{ALERT}}$ could continue to be low due to a low value from a remote $\overline{\text{ALERT}}$ pin. The remote $\overline{\text{ALERT}}$ function in the LTC4331 is not directly affected by an Alert Response transaction. The signal on the remote $\overline{\text{ALERT}}$ pin is always propagated to the local side if connected. If using SMBus slave devices on both sides of the link that respond to the ARA, the remote slaves must have higher priority device addresses than the devices on the local side, see section Considerations.

The LTC4331's internal slave device can be programmed to ignore the ARA and switch the function of pin $\overline{\text{ALERT}}$ from SMBALERT to interrupt mode. To switch to interrupt mode set INTR_MODE in the CONFIG register to 1. To clear the interrupt set the triggered event or the corresponding event enable bit to 0. This method is also valid in SMBALERT mode in lieu of the ARA protocol.

Control

Through the CTRL pin, the LTC4331 provides an additional signal to control a remote device's input pin. When in remote mode, the CTRL pin is an output and reflects the value either on the local side CTRL pin or the value programmed into the bit field SW_CTRL. A separate bit field CTRL_SEL selects pin or register control. By default the value on local CTRL pin is used. Local CTRL values transfer to the remote side CTRL only when the communication link is established and pin $\overline{\text{LINK}}$ is low.

At startup the CTRL output driver is disabled and a weak internal pull-up prevents the pin from floating. The CTRL pin's output driver enables only when link communication is established. Thereafter, the remote CTRL pin's output driver is always enabled except after a remote reset event where it is disabled until link communication is reestablished.

I²C Address Translation

The address translation feature allows the use of multiple I²C slave devices with fixed or limited device address ranges on the same network. The LTC4331 I²C slave device automatically translates the incoming address using an XOR function against the internal register ADDR_TRANS. Address translation is enabled by setting this register to a non-zero value. ADDR_TRANS must be programmed before any accesses to the remote slave if that slave requires address translation or there will be a collision. See Figure 12.

Timeouts

The LTC4331 respects SMBus SMBCLK low timeouts on the SCL pin. When in local mode and SCL is held low for a minimum of $t_{TIMEOUT:SLAVE:MAX}$, the I²C Interface is reset and SCL and SDA are released if held low. On the remote

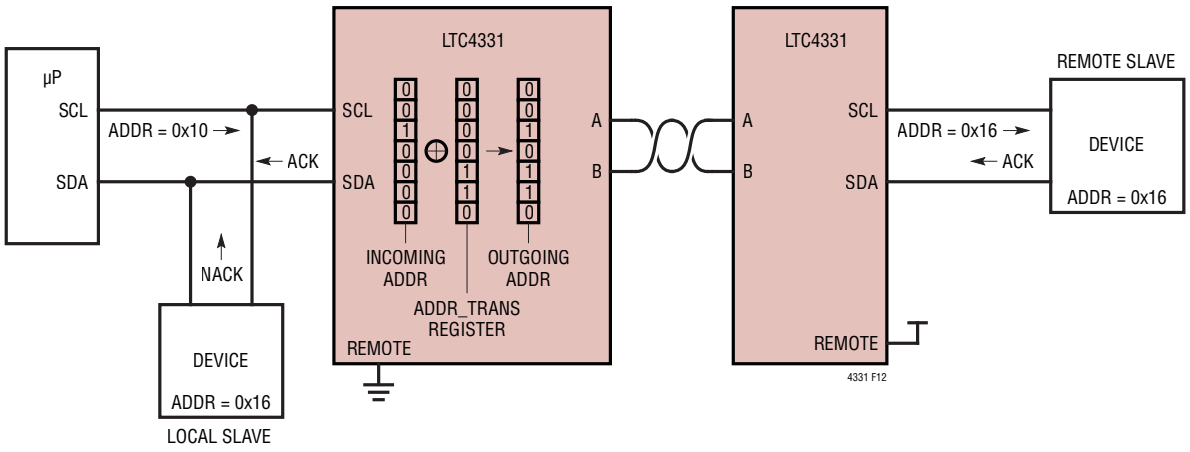

Figure 12. Address 0x10 Is Translated to 0x16 for the Remote Device

Rev A

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side, the LTC4331 acting as an I²C master also releases SCL and SDA if an remote slave is signaling a timeout. In addition, the LTC4331 master sends a STOP event and requires a local side STOP event before allowing further remote I²C transactions. This ensures the local and remote are synchronized.

In addition, the local side LTC4331 slave interface contains an SDA stuck-low prevention circuit which ensures the LTC4331 does not hold SDA low when the I²C bus is idle. This typically occurs when there is a loss of I²C protocol synchronization between the master and slave devices. If the LTC4331 is holding SDA low while SCL is high for 35ms, the interface is reset and SDA is released.

Remote Stuck Bus Protection

On the remote side, the LTC4331 master device can detect and attempt recovery from I²C bus faults. If the master device senses that SDA is low when it should be high, it considers SDA stuck by a slave device. The LTC4331 enters a bus recovery routine which drives 16 SCL clocks onto the bus and then issues a STOP event. This routine is also entered if SDA is sensed low after a startup. If successful, the LTC4331 master then ignores further local I²C bus transactions until the local bus transmits a STOP condition. If the routine is unsuccessful, it retries whenever a local side master initiates a new transaction.

If the remote LTC4331 detects that SCL is stuck, it automatically NACKs all I²C transactions from the local bus until it measures SCL high and receives a STOP command from a local I²C master.

For both SCL and SDA fault conditions, the remote LTC4331 sends a FAULT response to the local LTC4331 which sets the EXT_I2C_FAULT EVENT bit.

Remote Reset

The local side LTC4331 can trigger a remote side LTC4331 reset by holding the ON pin low for a minimum of t_{REMOTE_RESET}. In addition, the remote LTC4331 is automatically reset after t_{REMOTE_RESET} if the link is disconnected. A remote reset disables all remote side outputs, including pin CTRL, until link communication is reestablished.

Considerations

- The LTC4331 relies on SCL clock-stretching to account for link and remote bus latencies. Using a local master, either hardware or software based, that fully supports clock-stretching is highly recommended for best performance. Alternately, the SCL frequency can also be reduced such that the LTC4331's SCL configured low time and remote response time is less than the master's programmed SCL low time. The total clock-stretching time of the local LTC4331 I²C slave device depends on SPEED1 and SPEED2 pin settings and remote I²C Slave device timing requirements. This is not recommended. See Figure 13.

Table 1. Known I²C Master Devices Incompatible with LTC4331 SCL Clock-Stretching

DEVICE	ISSUE	WORKAROUND
All Raspberry Pi models (Broadcom BCM283X)	Hardware I²C peripheral clock-stretching issues	Use software based I²C that fully supports SCL clock-stretching
Analog Devices DC590B QuikEval controller	SCL signal path is not bidirectional	Use Analog Devices Linduino® w/DC590 sketch

- The LTC4331 I²C Slave Extender does not support remote I²C devices acting as masters. Therefore the SMBus Address Resolution Protocol and Host Notify Protocol are not supported.
- When using SMBus ARA, if there are SMBus slave devices on the local and remote side of the extender,

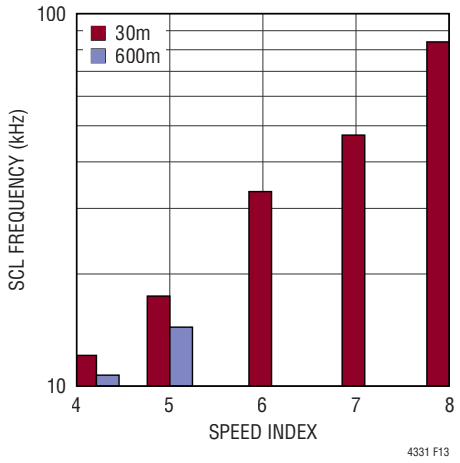

Figure 13. SCL Frequency Range when the I²C Master Ignores Slave SCL Low Stretching

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all local slave device addresses must be greater (lower priority) than the remote slave device address. This is to allow proper slave address negotiation.

- Care must be taken when interrupting an I^2C transaction with a START or STOP. A START or STOP can only be issued when the local side LTC4331 is in slave-receive mode. Since internally the data is sampled on the rising edge, the local I^2C bus is considered slave driven after the last rising edge of SCL in a master driven data cycle.
- The LTC4331 supports a faster local I^2C clock rate relative to the effective link rate. The device has a fixed length internal buffer to hold a complete byte as it is transferred across the link at the rate set by SPEED1 and SPEED2. During this time the local I^2C bus stalls preventing further I^2C data from entering the buffer. If however, a local master sends multiple consecutive START/STOP commands faster than the effective link rate, this buffer can overflow. The LTC4331 provides two status indicators for this event. First, if the buffer is full, then $\overline{RDY}$ rises indicating that the local I^2C interface is not ready and further START, STOP, or write data event can be lost. Second, a TX_BUFFER_OVERFLOW FAULT event occurs if a local master writes additional I^2C events while $\overline{RDY}$ is high.
- A remote slave device will not see a SCL timeout condition (bus reset) initiated by a local slave device if a remote device is not the target of the local Master.
- New I^2C transactions should not start in the time window of 28ms to 35ms following the end of the last transaction. New transactions starting in this window may fail with a local side NAK. In many cases, the extender link self recovers, and subsequent transactions occurs normally after waiting a short time, 28ms to 35ms. In some situations, the link cannot recover without a reset. See Remote Reset.

Link Speed

The link baud rate is set using the SPEED1 and SPEED2 pins as shown in Table 2. Column I^2C Class shows the timing mode set on the local and remote I^2C interfaces. The Effective I^2C Link Rate shows the rate I^2C data propagates across the link. The local SCL frequency can exceed this rate though increased clock-stretching times occur as the Effective Link Rate decreases relative to the local SCL frequency. The SPEED INDEX must be set to the same value on each side of the link.

Table 3. Speed Factors

SPEED INDEX	SPEED FACTOR (SF)
8	1×
7	2×
6	4×
5	8×
4	10×
3	16×
2	32×
1	50×
0	80×

Table 2. Link Speed

SPEED1 (Note 1)	SPEED2 (Note 1)	SPEED INDEX	I^2C CLASS	EFFECTIVE I^2C LINK RATE	MAX CABLE LENGTH (m) (Note 2)	SLEW RATE LIMITING OPTION (Note 3)
L	L	8	Fm+	1MHz	30	No
Float	L	7	Fm	500kHz	60	No
H	L	6	Fm	250kHz	200	No
L	Float	5	Fm	125kHz	600	No
L	H	4	Sm	100kHz	1200	No
H	Float	3	Sm	63kHz	1200+	No
Float	Float	2	Sm	31kHz	1200+	No
Float	H	1	Sm	20kHz	1200+	Yes
H	H	0	Sm	12.5kHz	1200+	Yes

Note 1: For assignments to float, 0.5 • V_L can also be applied to pin.
Note 2: Evaluated with Cat5E Ethernet cable in a lab environment. Actual maximum cable length depends on type of cable and application environment.
Note 3: Using $\overline{SLO}$.
Propagation times across the link for the SYSTEM timing specifications are based on the SPEED1 and SPEED2 pins.

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Control Interface

The LTC4331 contains an addressable slave device providing a control interface for configuration and monitoring.

The internal slave is enabled by configuring pins A1 and A2 to assign the device a unique I^2C address. When both pins are unconnected, the internal slave is disabled. The internal slave device recognizes the SMBus Write Byte and

S	DEVICE ADDR	$\overline{W}$	A	REGISTER	A	DATA	A	P
	3Eh	0	0	00h	0	01h	0	

4331 F14

DEVICE ADDRESS = 3Eh. ACCESSING THE CONFIG REGISTER

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

S: START
Sr: REPEATED START
$\overline{W}$: WRITE BIT (ACTIVE LOW)
A: (N)ACK BIT
P: STOP

Figure 14. Write Byte

S	DEVICE ADDR	$\overline{W}$	A	REGISTER	A	DATA	A	PEC	A	P
	3Eh	0	0	00h	0	01h	0	9Ah	0	

4331 F15

Figure 15. Write Byte + PEC

S	DEVICE ADDR	$\overline{W}$	A	REGISTER	A	Sr	DEVICE ADDR	$\overline{W}$	A	DATA	A	P
	3Eh	0	0	00h	0		3Eh	1	0	01h	1	

4331 F16

Figure 16. Read Byte

S	DEVICE ADDR	$\overline{W}$	A	REGISTER	A	Sr	DEVICE ADDR	$\overline{W}$	A	DATA	A	PEC	A	P
	3Eh	0	0	00h	0		3Eh	1	0	01h	0	96h	1	

4331 F17

Figure 17. Read Byte + PEC

S	DEVICE ADDR	$\overline{W}$	A	DATA	A	P
	3Eh	1	0	01h	1	

4331 F18

Figure 18. Receive Byte

S	DEVICE ADDR	$\overline{W}$	A	DATA	A	PEC	A	P
	3Eh	1	0	01h	0	4Ch	1	

4331 F19

Figure 19. Receive Byte + PEC

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Read/Receive Byte protocols with or without Packet Error Correction (PEC) as shown in Figures 14 to 19.

The PEC byte is calculated as a CRC-8 checksum over all bytes between the START and STOP conditions excluding the ACK/NACK and Sr bits and last CRC byte. The polynomial used is $x^8 + x^2 + x + 1$ initialized to zero.

PEC transfers are recommended in high noise environments or high reliability systems.

Table 4. Device Address

A1 (Note 1)	A2 (Note 1)	DEVICE ADDR (7-Bit)
L	L	3Eh
Float	L	3Ch
H	L	3Fh
L	Float	3Dh
H	Float	75h
L	H	76h
Float	H	74h
H	H	77h
Float	Float	Internal Slave Device is Disabled

Note 1: For assignments to Float, 0.5 • V_L can also be applied to pin.

Register Naming Conventions

RW Read-Write

RO Read Only

W0C Write Zero to Clear

Table 5. Register Map

REGISTER	NAME	DATA								DEFAULT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00h	CONFIG	–	–	–	–	–	–	CTRL_SEL	INTR_MODE	0x00
01h	STATUS	SPEED_IDX				Reserved	EXT_NALERT	NALERT	NLINK	–
02h	EVENT	–	–	–	–	–	FAULT	LINK_LOST	LINK_GOOD	0x00
03h	ALERT_EN	–	–	–	–	–	FAULT_EN	LINK_LOST_EN	LINK_GOOD_EN	0x00
04h	FAULT	–	–	–	–	TX_BUF_OVERFLOW	EXT_I2C_FAULT	LINK_FAULT	I2C_WRITE_FAULT	0x00
05h	SCRATCH	SCRATCH								0x08
06h	ADDR_TRANS	–	I2C_TRANS							0x00
07h	CTRL	–	–	–	–	–	–	–	SW_CTRL	0x00

CONFIG Register (RW)

FIELD	DESCRIPTION
INTR_MODE	When low, the internal slave interrupt behavior on pin $\overline{\text{ALERT}}$ is SMBALERT. The internal slave device recognizes and responses to an ARA. When high, the internal slave device ignores the ARA.
CTRL_SEL	When low, the local CTRL pin input is mirrored to the remote CTRL output pin. When high, the value in register CTRL is used instead.

STATUS (RO)

FIELD	DESCRIPTION
NLINK	The level driven by pin $\overline{\text{LINK}}$. High impedance is interpreted as 1.
NALERT	The level driven by the local side pin $\overline{\text{ALERT}}$. High impedance is interpreted as 1.
EXT_NALERT	The level driven into the remote $\overline{\text{ALERT}}$ pin. Link must be established.
SPEED_IDX	<0-8>. Encoded index from values set on SPEED1 and SPEED2. See Table 2. Link Speed.

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EVENT (W0C): Events Are Set by the System and Cleared by the User

FIELD	DESCRIPTION
LINK_GOOD	The local and remote I^2C networks are connected.
LINK_LOST	The local and remote I^2C networks have lost link communication.
FAULT	Set if any field in the FAULT register is set by the system. Clearing this bit clears all bits in the FAULT register.

ALERT_EN (RW): Asserts $\overline{ALERT}$ if Corresponding EVENT Bit Is Set

FAULT (RO): If the FAULT EVENT Bit Is Set, at Least One of the Following Bits Is Set. To Clear, Clear the FAULT Event Bit

FIELD	DESCRIPTION
I2C_WRITE_FAULT	An incomplete write transaction after the internal address byte or PEC error detected.
LINK_FAULT	Link communication corruption detected.
EXT_I2C_FAULT	A fault, or stuck bus recovery occurred on the remote I^2C bus.
TX_BUF_OVERFLOW	The transmit buffer overflowed, I^2C events lost.

SCRATCH (RW)

FIELD	DESCRIPTION
SCRATCH	Used to test read/write access to the control interface.

ADDR_TRANS (RW)

FIELD	DESCRIPTION
I2C_TRANS	Incoming 7-bit I^2C addresses are translated to the remote network by: $Address_{OUT}$ = I2C_TRANS XOR $Address_{IN}$

CTRL (RW)

FIELD	DESCRIPTION
SW_CTRL	Sets the output value of the remote CTRL pin when CTRL_SEL is high.

PCB Layout

A ground plane layout is recommended. A 4.7µF bypass capacitor should be placed no more than 7mm away from the V_{CC} pin. The PC board traces connected to signals A and B should be symmetrical and as short as possible to maintain good differential signal integrity. Route the differential signals A and B as an edge coupled microstrip with a differential impedance approximately matching the cable impedance.

Link Termination and Biasing

To minimize the transmission line reflections over the link, a termination resistor should be connected between pins A and B at each node. Each resistor's value should closely match the characteristic impedance of the differential cable to reduce reflections.

A bias resistor network should also be inserted at each node to maintain the idle state during link turnaround when all drivers are momentarily disabled. See Figure 20. For DC-coupled (non-isolated) link applications, select R_B and R_{T2} such that $200\Omega \le R_B \le 620\Omega$ and $100\Omega \le R_{T2} \le 110\Omega$.

Isolation

Galvanically isolating the link is supported with the LTC4331 allowing applications with safety requirements or applications with independent ground potentials. A bias network along with termination resistors must be used

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on both sides of the link. For transformer applications, series resistors must be added to the A and B pins on each side of the link. Use resistor values from 25Ω to 50Ω. See Figure 21.

Table 6. Typical Resistor Values for Transformer Applications

V_{CC} (V)	R_B (Ω)	R_S (Ω)	R_{T2} (Ω)
3.3	200	25	110
5.0	270	50	110

For capacitive isolation, select R_B such that 200Ω ≤ R_B ≤ 320Ω. C = 1µF rated capacitors support all SPEED INDEX values. Smaller value capacitors can be used if the application only utilizes higher SPEED INDEX values. Ensure the capacitors' working voltages are much higher than the expected ground offset voltage. See Figure 25.

Multiple Local Extender Network

Multiple LTC4331 devices operating in slave device mode can be connected to the same local SMBus network unlike other extension solutions which typically restrict usage to one extender device. This allows a star network of parallel LTC4331 devices extending separate remote SMBus networks.

$\overline{LINK}$ indicates when the remote system is ready. Optionally $\overline{RDY}$ can also be monitored to determine when the local side control interface is ready to access in the absence of a link. See Figure 23.

Multi-Tier Extender Network

The LTC4331 also supports chaining remote segments into a single multi-tiered network. The maximum depth of the I^2C link network is limited only by the $t_{TIMEOUT}$ parameters of the I^2C devices on the network. As the depth increases, the clock-stretched low time of the devices increases. No other I^2C timing parameter is affected by depth. See Figure 24.

Auxiliary Protection for 5kV Surge, 5kV EFT, and 30kV IEC ESD

An interface transceiver used in an industrial setting may be exposed to extremely high levels of electrical overstress due to phenomena such as lightning surge, electrical fast transient (EFT) from switching high current inductive loads, and electrostatic discharge (ESD) from the discharge of electrically charged personnel or equipment. The LTC4331 is designed for high robustness against ESD, but the on-chip protection is not able to absorb the energy associated with the 61000-4-5 surge transients. Therefore, a properly designed external protection network is necessary to achieve a high level of surge protection, and can also extend the ESD and EFT performance of the LTC4331 to extremely high levels.

Refer to section Auxiliary Protection for IEC Surge, EFT and ESD on page 17 of Analog Devices LTC2862A Datasheet for a detailed description and diagram of the external protection network.

The network provides the following protection:

- EC 61000-4-2 ESD Level 4: ±30kV contact, ±30kV air (line to GND, direct discharge to bus pins with transceiver and protection circuit mounted on a ground referenced test card per Figure 4 of the standard)
- IEC 61000-4-4 EFT Level 4: ±5kV (line to GND, 5kHz repetition rate, 15ms burst duration, 60 second test duration, discharge coupled to bus pins through 100pF capacitor per paragraph 7.3.2 of the standard)
- IEC 61000-4-5 Surge Level 4: ±5kV (line to GND, line to line, 8/20µs waveform, each line coupled to generator through 80Ω resistor per Figure 14 of the standard)

Table 7. Recommended Transformers

MANUFACTURER	PART NUMBER	ISOLATION VOLTAGE	CENTER TAP	CM CHOKE	SPEED INDEX SUPPORTED
Murata	78601/9JC	$1kV_{RMS}$	No	No	ALL
Pulse	PE-68386NL	$1500V_{RMS}$	No	No	3, 4, 5, 6, 7, 8

APPLICATIONS INFORMATION

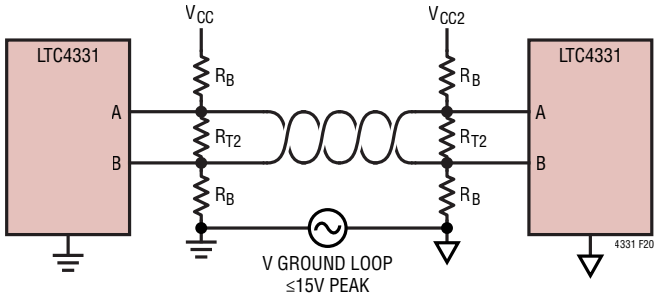


Figure 20. Resistor Bias Network

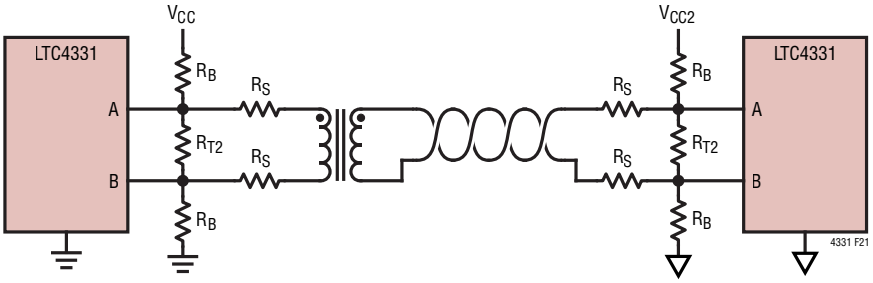


Figure 21. Transformer Application Resistor Network

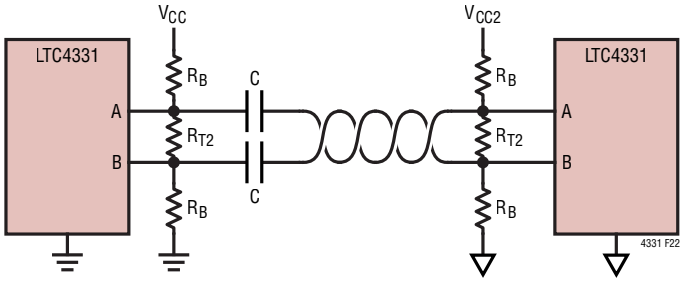


Figure 22. Capacitive Isolation Resistor Network

TYPICAL APPLICATIONS

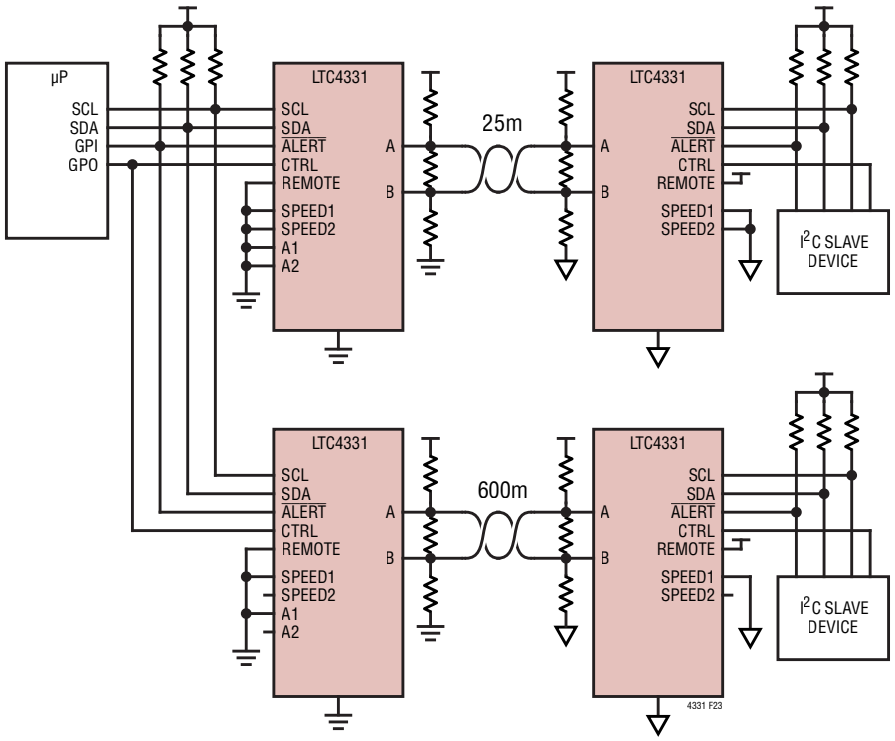


Figure 23. Multiple Local Extender Network

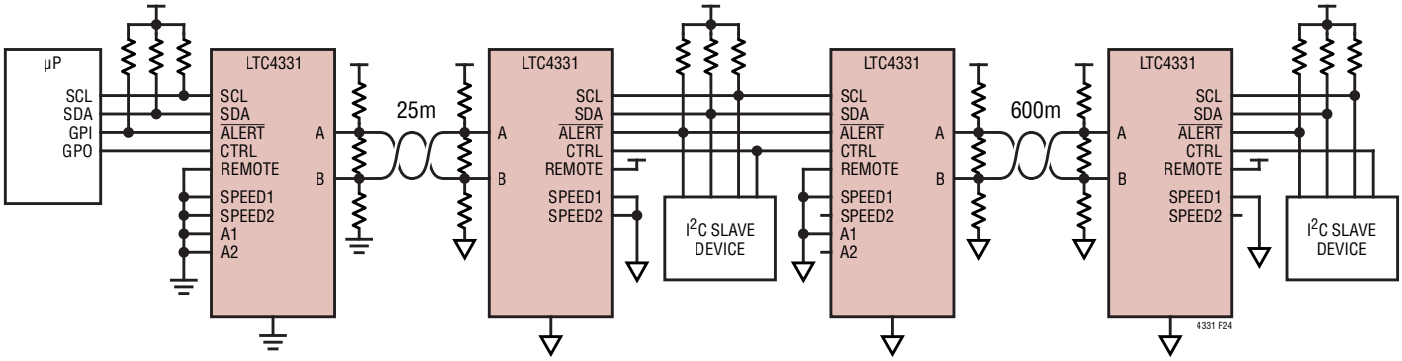
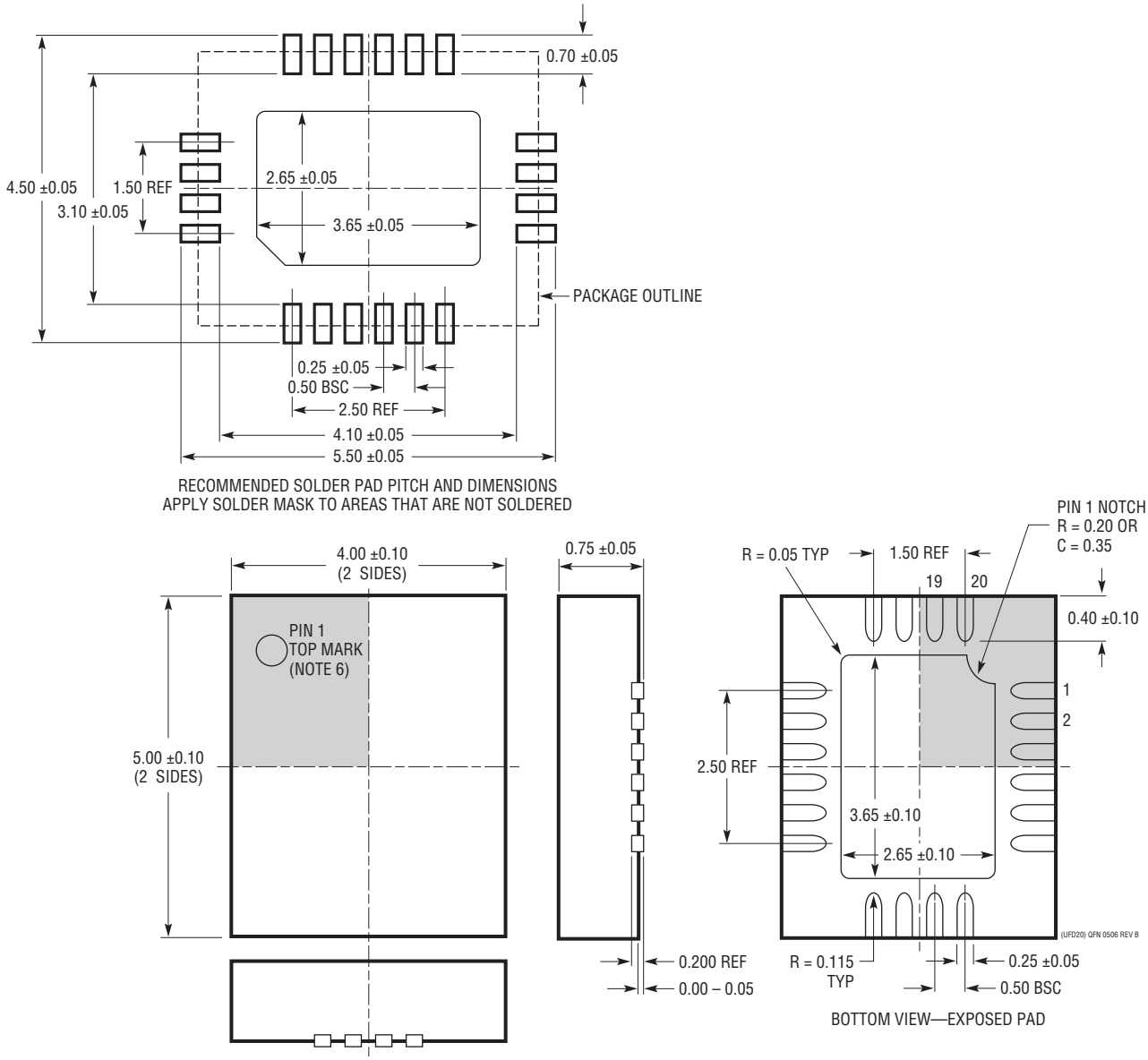


Figure 24. Multi-Tier Extender Network

PACKAGE DESCRIPTION

UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/23	Updated Considerations	18