# Hot Swappable Load Share Controller

**NOT RECOMMENDED FOR NEW DESIGNS**
Contact Linear Technology for Potential Replacement

## FEATURES

- **Build N + 1 Redundant Supply**
- **Hot Swap™ Power Supplies**
- **Isolates Supply Failures from Output**
- **Eliminates ORing Diodes**
- **Identifies and Localizes Output Low, Output High and Open-Circuit Faults**
- Output Voltages from 1.5V to 12V
- 16-Lead Narrow SSOP Package

## APPLICATIONS

- Servers and Network Equipment
- Telecom and Base Station Equipment
- Distributed Power Systems

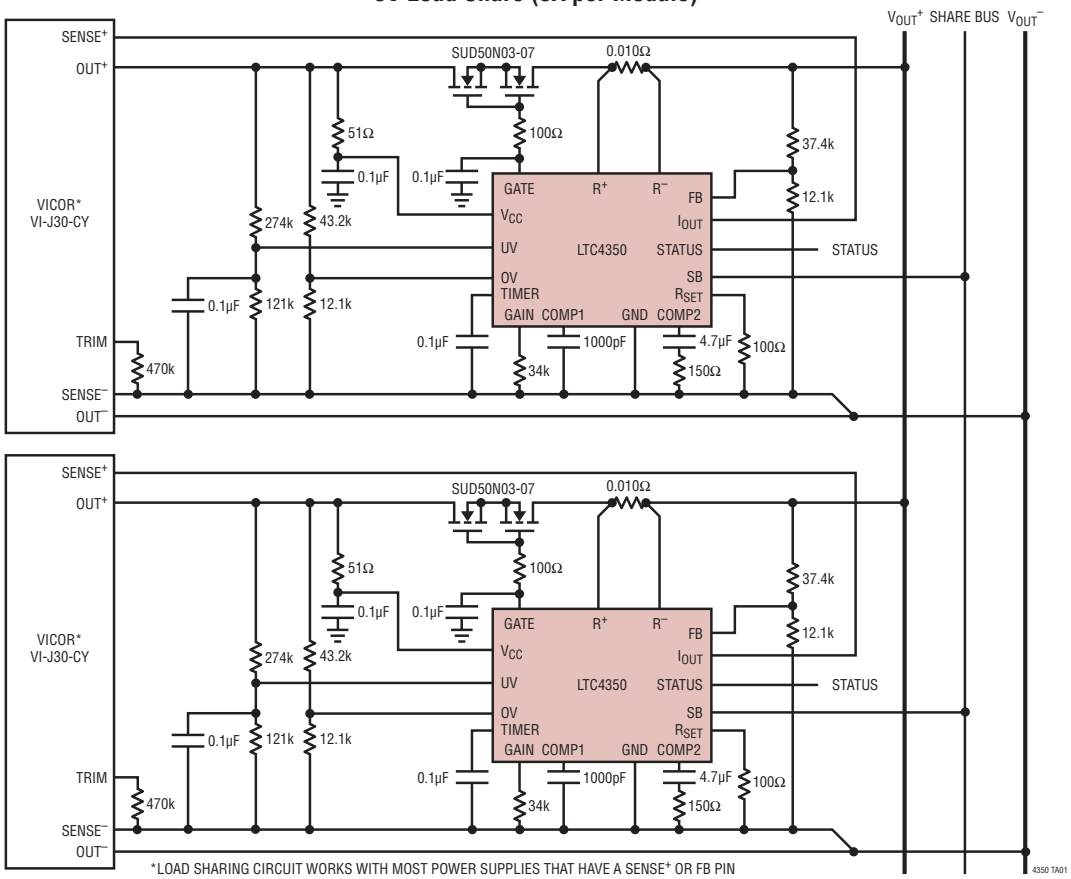
## DESCRIPTION

The LTC®4350 is a load share controller that allows systems to equally load multiple power supplies connected in parallel. The output voltage of each supply is adjusted using the SENSE⁺ input until all currents match the share bus. The LTC4350 also isolates supply failures by turning off the series pass transistors and identifying the failed supply. The failed supply can then be removed and replaced with a new unit without turning off the system power. The LTC4350 is available in a 16-pin narrow SSOP package.



## TYPICAL APPLICATION

**5V Load Share (5A per Module)**



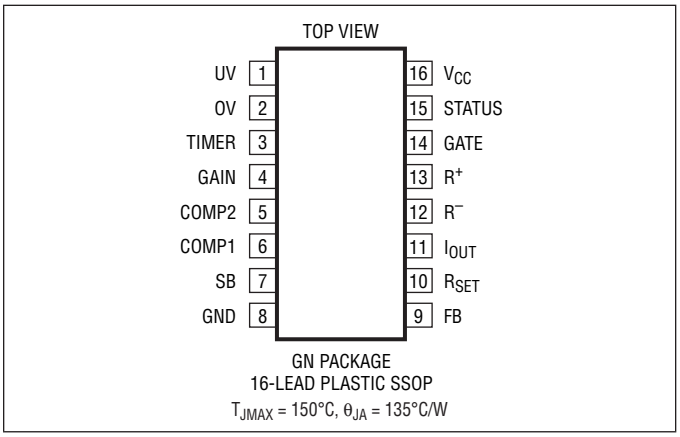

*LOAD SHARING CIRCUIT WORKS WITH MOST POWER SUPPLIES THAT HAVE A SENSE⁺ OR FB PIN

## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage ($V_{CC}$) ..... 17V
Input Voltage
  TIMER ..... –0.3V to 1.2V
  $R^+$, $R^-$ (Note 2) ..... –0.3V to 17V
  FB ..... –0.3V to 5.3V
OV, UV ..... –0.3V to 17V
Output Voltage
  COMP1 ..... –0.3V to 6V
  COMP2 ..... –0.3V to 3V
  GAIN, SB ..... –0.3V to 5.6V
GATE (Note 3) ..... –0.3V to 20V
$I_{OUT}$, STATUS ..... –0.3V to 17V
$R_{SET}$ ..... –0.3V to 1V
Operating Temperature Range
  LTC4350C ..... 0°C to 70°C
  LTC4350I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION




GN PACKAGE
16-LEAD PLASTIC SSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 135°C/W

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC4350CGN#PBF | LTC4350CGN#TRPBF | 4350 | 16-Lead Plastic SSOP | 0°C to 70°C |
| LTC4350IGN#PBF | LTC4350IGN#TRPBF | 4350I | 16-Lead Plastic SSOP | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | | |
| $I_{CC}$ | $V_{CC}$ Supply Current | UV = $V_{CC}$ | ● | 1.0 | 1.6 | 2.0 | mA |
| $V_{LKOH}$ | $V_{CC}$ Undervoltage Lockout High | | ● | 2.36 | 2.45 | 2.52 | V |
| $V_{LKOL}$ | $V_{CC}$ Undervoltage Lockout Low | | ● | 2.24 | 2.34 | 2.44 | V |
| $V_{FB}$ | FB Pin Voltage | 0°C to 85°C (LTC4350I) or 0°C to 70°C (LTC4350C)<br>–40°C to 85°C (LTC4350I) | | 1.208<br>1.196 | 1.220<br>1.220 | 1.236<br>1.244 | V<br>V |
| $V_{FBLIR}$ | FB Line Regulation | $V_{CC}$ = 3.3V to 12V, COMP1 = 1.240V | | | 0.02 | 0.05 | %/V |
| $V_{FBLOR}$ | FB Load Regulation | COMP1 = 2V<br>COMP1 = 0.64V | ●<br>● | | –0.0008<br>0.003 | –0.1<br>0.1 | %<br>% |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | | |
| $V_{UVTH}$ | UV Pin Threshold | High Going Threshold<br>Low Going Threshold | ●<br>● | 1.215<br>1.205 | 1.244<br>1.220 | 1.258<br>1.237 | V<br>V |
| $V_{OVTH}$ | OV Pin Threshold | High Going Threshold<br>Low Going Threshold | ●<br>● | 1.203<br>1.180 | 1.220<br>1.205 | 1.250<br>1.229 | V<br>V |
| $V_{TM}$ | TIMER Pin Threshold | | ● | 1.18 | 1.22 | 1.26 | V |
| $I_{TM}$ | TIMER Pin Current | TIMER On, $V_{TIMER}$ = 0V<br>TIMER On, $V_{TIMER}$ = 0V, $V_{OV} > V_{OVTH}$ | ●<br>● | –1.75<br>–5.30 | –2<br>–6 | –2.3<br>–6.7 | µA<br>µA |
| $V_G$ | GAIN Pin Voltage | $R_{GAIN}$ = 25k, ($V_R^+ – V_R^–$) = 100mV | ● | 2.3 | 2.5 | 2.7 | V |
| $V_{GO}$ | GAIN Pin Offset | $R_{GAIN}$ = 25k, ($V_R^+ – V_R^–$) = 0mV | ● | 0 | 0.02 | 0.20 | V |
| $V_{SB(MIN)}$ | SB Pin Minimum Voltage | | | | 2 | 8 | mV |
| $V_{SB(MAX)}$ | SB Pin Maximum Voltage | $V_{CC}$ = 3.3V<br>$V_{CC}$ = 12V | ●<br>● | 2.4<br>5.6 | 2.7<br>7.8 | 2.9<br>10.5 | V<br>V |
| $I_{SB(MAX)}$ | SB Pin Maximum Current | $V_{SB}$ = 0V | ● | –8 | –33 | –41 | mA |
| $R_{SB}$ | SB Pin Resistor Value | | ● | 14 | 20 | 33 | kΩ |
| $V_{E/A2OFF}$ | E/A2 Offset | $V_{SB} – V_{GAIN}$ | ● | 8 | 25 | 50 | mV |
| $V_{RSET(MAX)}$ | $R_{SET}$ Pin Maximum Voltage | $V_{CC}$ = 3.3V, $R_{SET}$ = 100Ω<br>$V_{CC}$ = 12V, $R_{SET}$ = 100Ω | ●<br>● | 0.94<br>0.94 | 1<br>1 | 1.03<br>1.03 | V<br>V |
| $V_{RSET(MIN)}$ | $R_{SET}$ Pin Minimum Voltage | $V_{CC}$ = 5V, $R_{SET}$ = 1000Ω<br>$V_{CC}$ = 5V, $R_{SET}$ = 100Ω | ●<br>● | | 0.001<br>0.001 | 0.5<br>0.5 | V<br>V |
| $I_{RSET(MAX)}$ | $R_{SET}$ Pin Maximum Current | $R_{SET}$ = 50Ω, $V_{IOUT}$ = 1.1V | ● | 18 | 20 | 21 | mA |
| $V_{RCTH}$ | Reverse Current Threshold | $V_R^+ – V_R^+$ | ● | 10 | 30 | 40 | mV |
| $\Delta V_{GATE}$ | External N-Channel Gate Drive | $V_{GATE} – V_{CC}$ | ● | 10.8 | 12 | 12.7 | V |
| $I_{GATE}$ | GATE Pin Current | Gate On, $V_{GATE}$ = 0V | ● | –8 | –10 | –12 | µA |
| $V_{SOL}$ | STATUS Pin Output Low | $I_{OUT}$ = 3mA | ● | 0.1 | 0.3 | 1.2 | V |

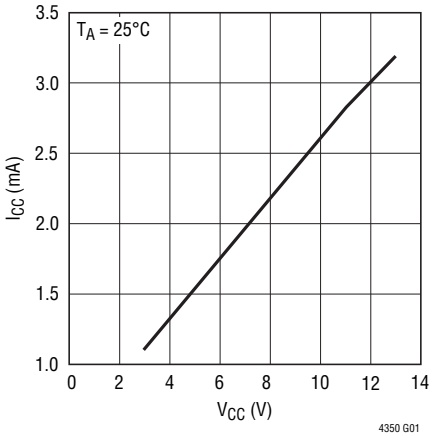
**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** $R^+$ and $R^–$ could be at 17V while $V_{CC}$ = 0V.

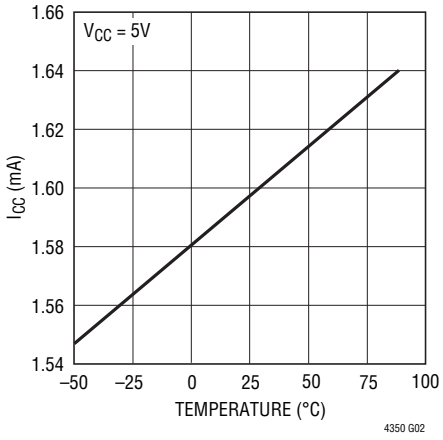
**Note 3:** An internal clamp limits the GATE pin to a minimum of 10.8V above $V_{CC}$. Driving this pin to voltages beyond the clamp may damage the part.

## TYPICAL PERFORMANCE CHARACTERISTICS

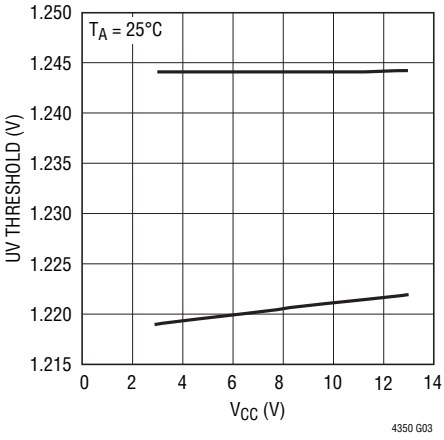
**$I_{CC}$ vs $V_{CC}$**



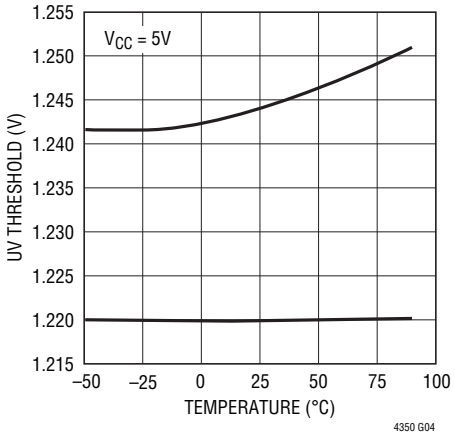

**$I_{CC}$ vs Temperature**



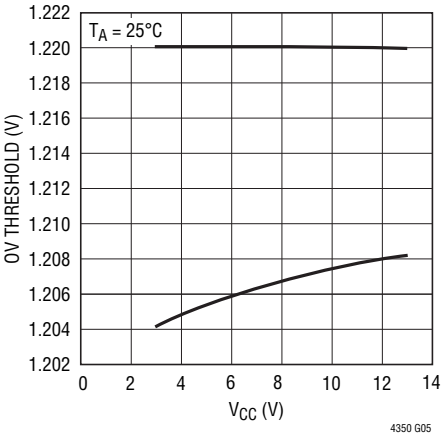

**UV Threshold vs $V_{CC}$**



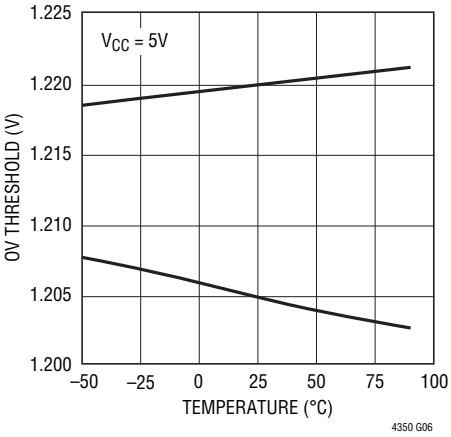

**UV Threshold vs Temperature**



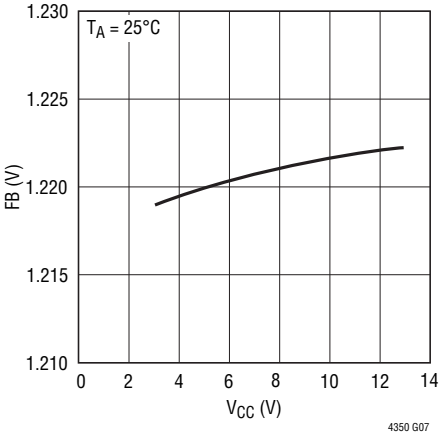

**OV Threshold vs $V_{CC}$**



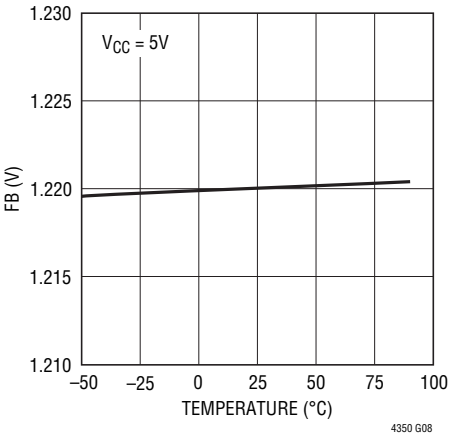

**OV Threshold vs Temperature**



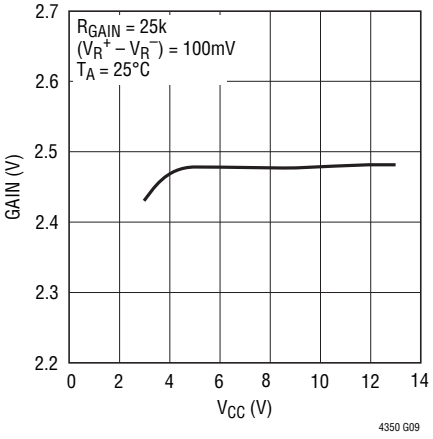

**FB vs $V_{CC}$**




**FB vs Temperature**

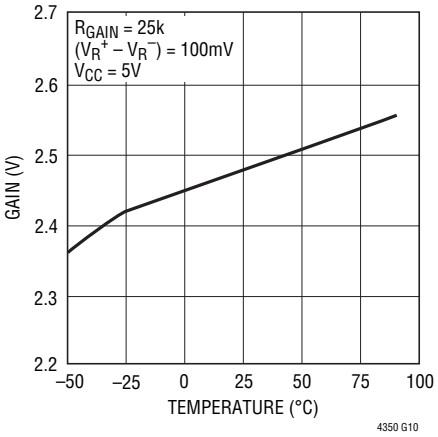



**Gain PIn Voltage vs $V_{CC}$**

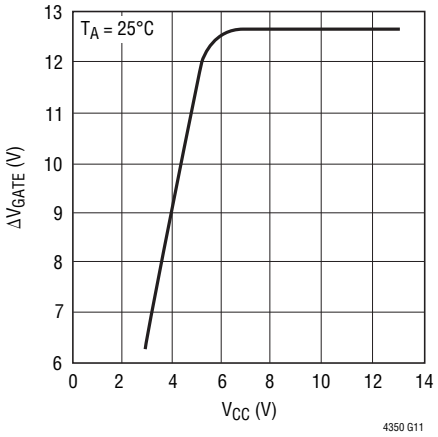


## TYPICAL PERFORMANCE CHARACTERISTICS

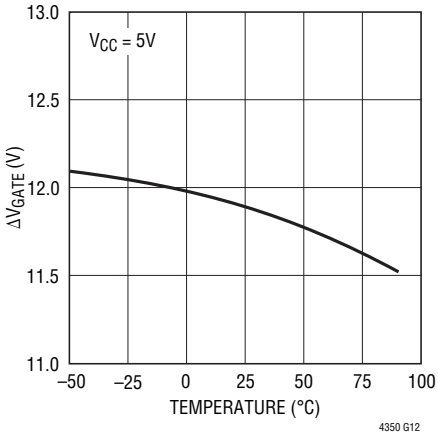
**Gain Pin Voltage vs Temperature**




**$\Delta V_{GATE}$ vs $V_{CC}$**




**$\Delta V_{GATE}$ vs Temperature**




## PIN FUNCTIONS

**UV (Pin 1):** Undervoltage Pin. The threshold is set at 1.244V with a 24mV hysteresis. When the UV pin is pulled high, the charge pump ramps the GATE pin. When the UV pin is pulled low, the GATE pin will be pulled low.

**OV (Pin 2):** Overvoltage Pin. The threshold is set at 1.220V with a 15mV hysteresis. When the OV pin is pulled high, the GATE pin is pulled low. After a timer cycle, the STATUS pin is pulled low until the OV pin is pulled low.

**TIMER (Pin 3):** Analog System Timing Generator Pin. This pin is used to set the delay before the load sharing turns on after the UV pin goes high. The other use for the TIMER pin is to delay the indication of a fault on the STATUS pin.

When the timer is off, an internal N-channel shorts the TIMER pin to ground. When the timer is turned on, a 2µA or 6µA timer current ($I_{TIMER}$) from $V_{CC}$ is connected to the TIMER pin and the voltage starts to ramp up with a slope given by: $dV/dt = I_{TIMER}/C_T$. When the voltage reaches the trip point (1.220V), the timer will be reset by pulling the TIMER pin back to ground. The timer period is given by: $(1.220V \bullet C_T)/I_{TIMER}$.

**GAIN (Pin 4):** Analog Output Pin. The voltage across the $R^+$ and $R^-$ pins is divided by a 1k resistor and sourced as a current from the GAIN pin. An external resistor on the GAIN pin determines the voltage gain from the current sense resistor to the GAIN pin.

**COMP2 (Pin 5):** Analog Output Pin. This pin is the output of the share bus error amplifier E/A2. (A compensation capacitor between this pin and ground sets the crossover frequency for the power supply adjustment loop.) In most cases, this pin operates between 0.5V to 1.5V and represents a diode voltage up from the voltage at the $R_{SET}$ pin. It is clamped at 3V. During start-up, this pin is clamped to ground. After a timer cycle (and if the GATE pin is high), the COMP2 pin is released.

**COMP1 (Pin 6):** Analog Output Pin. This pin is the output of the voltage regulating error amplifier E/A1. A compensation capacitor between this pin and ground sets the crossover frequency of the share bus loop. This pin operates a diode voltage up from the voltage at the SB pin and is clamped at 8.4V.

**SB (Pin 7):** Analog Output Pin. This pin drives the share bus used to communicate the value of shared load current between several power supplies. There is an amplifier that drives this pin a diode below the COMP1 pin using an internal NPN as a pull-up and a 20k resistor as a pull-down.

## PIN FUNCTIONS

**GND (Pin 8):** Chip Ground.

**FB (Pin 9):** Analog Error Amplifier Input (E/A1). This pin is used to monitor the output supply voltage with an external resistive divider. The FB pin voltage is compared to 1.220V reference. The difference between the FB pin voltage and the reference is amplified and output on the COMP1 pin.

**$R_{SET}$ (Pin 10):** Analog Output Pin. The $I_{OUT}$ amplifier converts the voltage at the COMP2 pin (down a diode voltage) to the $R_{SET}$ pin. Therefore, the current through the external resistor ($R_{SET}$) placed between the $R_{SET}$ pin and ground is (COMP2 – $V_{DIODE}$)/$R_{SET}$. This current is used to adjust the output voltage.

**$I_{OUT}$ (Pin 11):** Analog Output Pin. The current flowing into the $I_{OUT}$ pin is equal to the current flowing out of the $R_{SET}$ pin that was set by the external resistor $R_{SET}$. This current is used to adjust the output supply voltage by modifying the voltage sensed by the power supply's internal voltage feedback circuitry.

**$R^-$ (Pin 12):** Analog Input Pin. With a sense resistor placed in the supply path between the $R^+$ and $R^-$ pins, the power supply current is measured as a voltage drop between $R^+$ and $R^-$. This voltage is measured by the $I_{SENSE}$ block and multiplied at the GAIN pin.

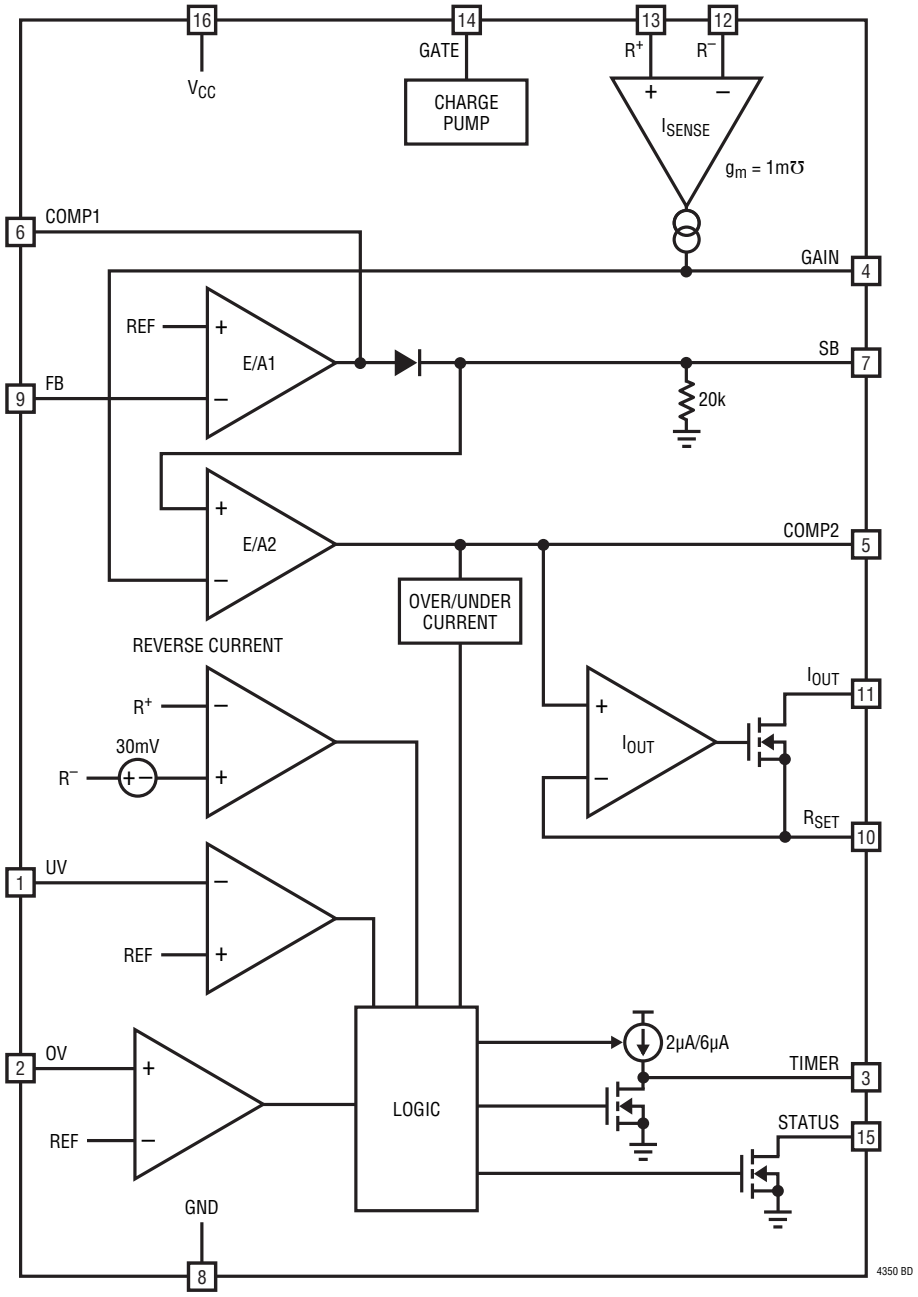
**$R^+$ (Pin 13):** Analog Input Pin. With a sense resistor placed in the supply path between the $R^+$ and $R^-$ pins, the power supply current is measured as a voltage drop between $R^+$ and $R^-$. This voltage is measured by the $I_{SENSE}$ block and multiplied at the GAIN pin.

**GATE (Pin14):** The high side gate drive for the external N-Channel power FET. An internal charge pump provides the gate drive necessary to drive the FETs. The slope of the voltage rise or fall at the GATE is set by an external capacitor connected between GATE and GND, and the 10µA charge pump output current. When the undervoltage lockout circuit monitoring $V_{CC}$ trips, the OV pin is pulled high or the UV pin is pulled low, the GATE pin is immediately pulled to GND.

**STATUS (Pin 15):** Open-Drain Digital Output. The STATUS pin has an open-drain output to GND. This pin is pulled low to indicate a fault has occurred in the system. There are three types of faults. The first is a undervoltage lockout on $V_{CC}$ or the UV pin is low while the output voltage is active. The second is when the COMP2 pin is above 1.5V or below 0.5V and the voltage on the GAIN pin is greater than 100mV. The final failure is when the OV pin is high. The three faults will activate the pull-down on the STATUS pin after a timing cycle.

**$V_{CC}$ (Pin 16):** The Positive Supply Input, Ranging from 3.3V to 12V for Normal Operation. $I_{CC}$ is typically 1.6mA. An undervoltage lockout circuit disables the chip until the voltage at $V_{CC}$ is greater than 2.47V. A 0.1µF bypass capacitor is required on the $V_{CC}$ pin. If the $V_{CC}$ pin is tied to the same power supply output that is being adjusted, then a 51Ω decoupling resistor is needed to hold up the supply during a short to ground on the supply output. $V_{CC}$ must be greater than or equal to the supply that is connected to the $R^+$ and $R^-$ pins.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### INTRODUCTION

Many system designers find it economically feasible to parallel power supplies to achieve redundancy. The second trend is providing some load sharing between the many supplies. In some cases, a failure in any one supply will trigger a sequence that disconnects the faulty supply and sends a flag to the system. Then, a service technician will swap in a good supply. For systems that are continuously powered, there is Hot Swap circuitry to prevent glitches on the power buses when power cards are swapped. A block diagram of this system is shown in Figure 1.

By combining the features of a load share and a Hot Swap controller into one IC, the LTC4350 simplifies the design of redundant power supplies. A complete redundant power supply is a combination of a power module and the LTC4350 as shown in Figure 2. Note that the power module must have accessible feedback network or a remote sensing pin (SENSE$^+$) to interface to the LTC4350.

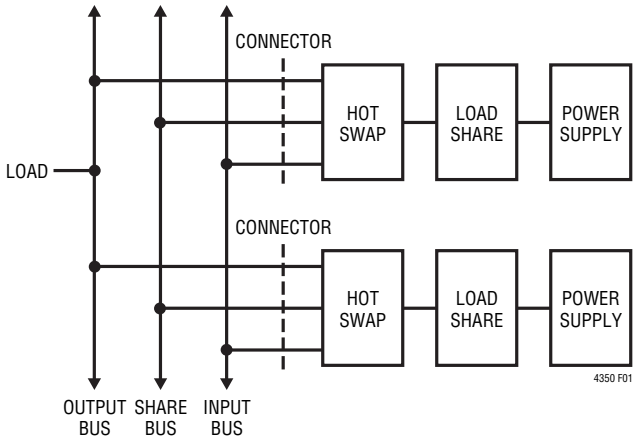



**Figure 1. Redundant Power Card System**

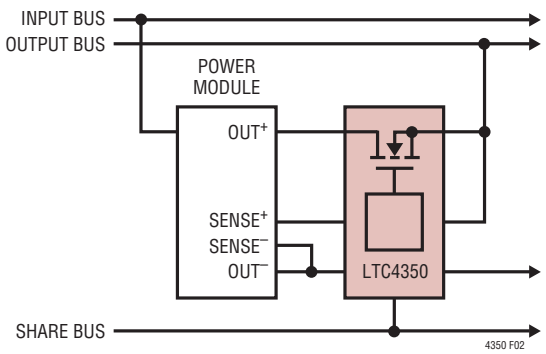



**Figure 2. Redundant Power Supply**

The LTC4350 provides a means for paralleling power supplies. It also provides for load sharing, fault isolation and power supply hot insertion and removal. The power supply current is accurately measured and then compared to a share bus signal. The power supply's output voltage is adjusted until the load current matches the share bus, which results in load sharing. There are two optional power FETs in series with the load that provide a quick disconnect between a load and a failed power supply. These same power FETs allow a power supply to be connected into a powered backplane in a controlled manner or removed without disruption.

### CURRENT SHARING

The current sharing components will now be discussed. Figure 3 shows a simplified block diagram of these components. The $I_{SENSE}$ block measures the power supply current by amplifying the voltage drop across the sense resistor. An external resistor on the GAIN pin determines the gain of the $I_{SENSE}$ block. The voltage drop across the sense resistor is divided by a precision 1k resistor to produce a current at the GAIN pin. For example, a 10mV sense voltage translates to a 10µA current. If a 10k resistor is on the GAIN pin, then the voltage gain is 10k/1k or 10.

The voltage at the GAIN pin is compared to the current share bus using the E/A2 block. The output of E/A2 is used to adjust the output voltage of the power supply using the $I_{OUT}$ block. The objective of the E/A2 block is forcing the GAIN pin voltage to equal the SB pin voltage. When the GAIN pin voltages of all the LTC4350s in the system equal the SB pin voltage, the load current is shared.

### VOLTAGE MONITOR

Unique to the LTC4350 is tight output voltage regulation. This is handled by the LTC4350's error amplifier and reference and not the power supply's error amplifier and reference. The E/A1 amplifier monitors the output voltage via the feedback divider connected to the FB pin. The FB pin is compared to the internal reference of the LTC4350. If the FB pin is at or below the reference, then the output of E/A1 drives the

## APPLICATIONS INFORMATION

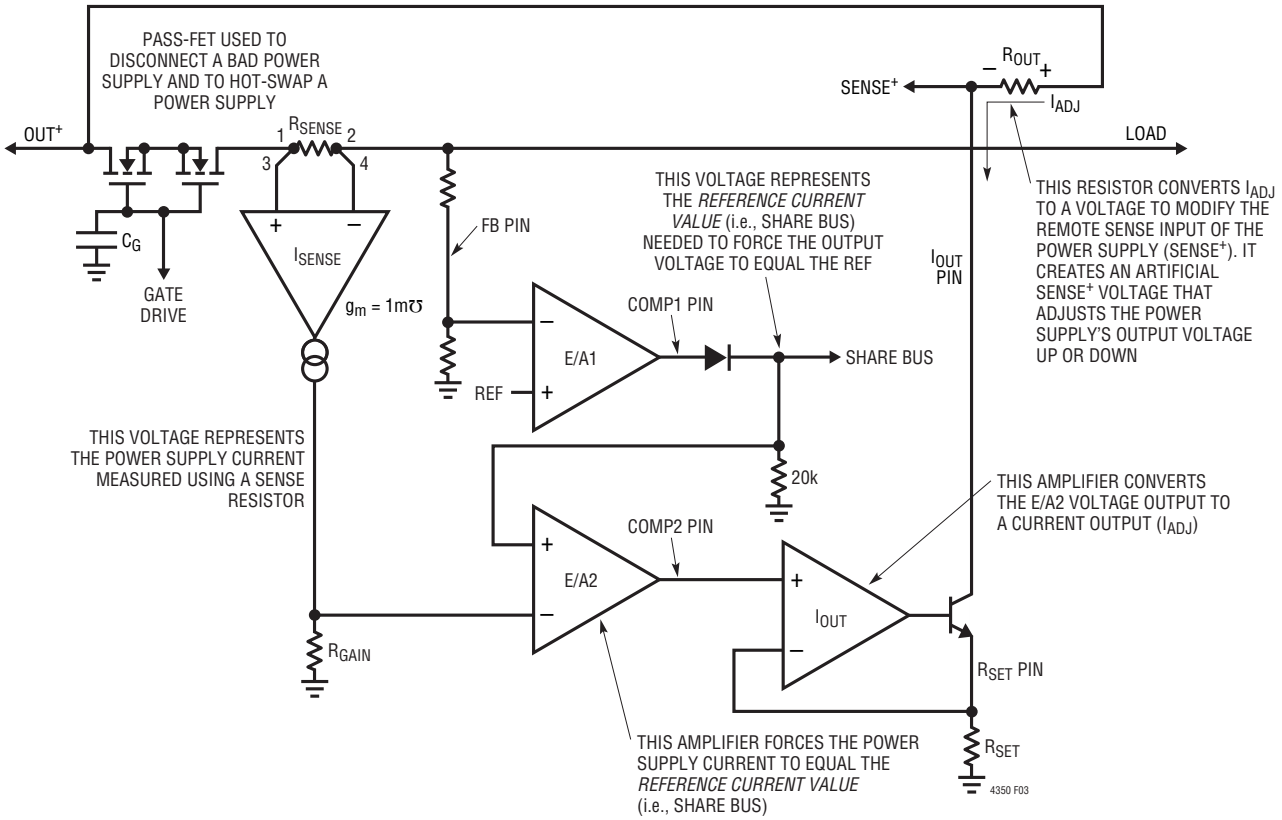



**Figure 3. Simplified Block Diagram**

SB pin (or share bus). If the FB pin is above the reference, the COMP1 pin is grounded and the SB pin is disconnected from the COMP1 pin using the series diode.

The LTC4350 with the highest reference will drive the SB pin and the 20k loads connected to the SB pin. All of the other LTC4350's COMP1 pins are pulled low because their FB pins are at a higher voltage than their references. The series diode between the COMP1 pin and the SB pin is actually a low impedance buffer amplifier with a diode in the output stage. Therefore, the master LTC4350's E/A1 drives the share bus to the proper value that keeps the output voltage tightly regulated. The buffer amplifier is capable of driving at least fifty 20k loads (each 20k load represents an LTC4350).

### OUTPUT VOLTAGE ADJUSTMENT

The LTC4350 is designed to work with supplies featuring remote sense. The output voltage of each power supply needs to be adjusted below the final output voltage at the common load. For example, a 5V system would require the power supply output be set to 4.90V or some value below 5V. This is normally done using the trim pin of the module. The power supply output is then increased by artificially reducing the positive sense voltage by a small amount. The LTC4350 would then adjust the output voltage to 5V, an increase of 2%. The maximum range of adjustment can be set from 2% to 5% to compensate for voltage drops in the wiring, but no more than 300mV.

In most power supplies, the voltage sense is tied directly to the output voltage. If a small valued resistor, $R_{OUT}$, is placed in series with the power supply sense line, a voltage drop across $R_{OUT}$ appears as a lower sensed voltage. This requires the power supply to increase its output voltage to compensate. Thus, the LTC4350 exercises complete control of the final output voltage.

The $I_{OUT}$ block converts the E/A2 output (COMP2 pin) to a current that flows through $R_{OUT}$ (see Figure 3). As the voltage at COMP2 increases, the current in $R_{OUT}$

## APPLICATIONS INFORMATION

increases. The output voltage will then increase by an amount equal to the voltage drop across $R_{OUT}$. The external resistor, $R_{SET}$, sets the voltage to current relationship in the $I_{OUT}$ block. The current in $R_{OUT}$ is defined as $I_{ADJ} = (V_{COMP2} – 0.58V)/R_{SET}$.

The maximum voltage that can be applied across $R_{SET}$ is 1V. The range of the output voltage adjustment is set to be $V_{MAXADJ} = R_{OUT}/R_{SET}$. This sets the worst-case output voltage if the share bus is accidentally shorted to $V_{CC}$. As mentioned previously, this range is set to be 2% to 10% in value.

The compensation elements, $C_{CP1}$ and $C_{CP2}$, are used to set the crossover frequencies of the two error amplifiers E/A1 and E/A2. In the Design Example section, the calculations for choosing all of the components will be discussed.

### Output Adjust Soft-Start

In the LTC4350, there is soft-start circuitry that holds the COMP2 pin at ground until both the GATE pin is 4V above the $V_{CC}$ pin and a timer cycle is completed following the UV pin becoming active.

Upon power-up, most of the circuitry is active including the circuits that monitor and adjust the output voltage. The external power FETs are initially open circuit when power is applied. It takes about 10ms to 100ms for the FETs to transition from the off to the fully on state (as discussed in the following Hot Swapping section). During this time the FB pin is near ground which forces the SB to the positive rail. The COMP2 pin is then forced to the positive rail, which forces the $R_{SET}$ pin to 1V. The voltage at the output of the power supply is now adjusted to its maximum adjusted value, which can be 10% above nominal. Once the power FETs are turned on, the load will see this adjusted output voltage. This appears to be a voltage overshoot at the load that exists until the loop can correct itself. The dominant pole in the loop exists on the COMP2 pin. Therefore, the overshoot duration is determined by the discharge time of the COMP2 pin.

In order to eliminate this overshoot, the COMP2 pin is clamped at ground until the GATE pin is 4V above the $V_{CC}$ pin (power FETs are turned on). Now, the COMP2 pin will begin to charge up until the FB pin regulates at 1.220V.

In cases where the power FETs are turned on but the power supply is still ramping up, the load voltage may overshoot. For these cases, the COMP2 pin is clamped to ground during one timing cycle. If the UV pin is greater than 1.244V, the chip begins the timer cycle. The timer cycle uses a 2µA current source into an external capacitor on the TIMER pin. As soon as the voltage at the TIMER pin exceeds 1.220V, the timer cycle is over. The time-out is defined as $t = C_T \bullet 1.220V/2\mu A$. At the end of the timer cycle, the power supply ramping should be complete.

### Faults

There are several types of power supply output faults. Shorts from the output to ground or to a positive voltage greater than the normal output voltage are considered “hard faults.” These faults require the bad power supply to be immediately disconnected from the load in order to prevent disruption of the system. “Soft faults” include power supply failed open-circuit or load current sharing failure where the output voltage is normal but load sharing between several supplies is not equal. The LTC4350 can isolate soft and hard faults and signal a system controller using the STATUS pin.

### HARD FAULTS

The LTC4350 can identify faults in the power supply and isolate them from the load if optional external power FETs are included between the power supply and the load. In the case of a power supply output short to ground, the reverse current block will sense that the voltage across the current sense resistor has changed directions and has exceeded 30mV for more than 5µs. The gate of the external power FETs is immediately pulled low disconnecting the short from the load. The gate is allowed to ramp-up and turn-on the power FETs as soon as the reverse voltage across the sense resistor is less than 30mV.

The condition where a power supply output shorts to a high voltage is referred to as an overvoltage fault. In this case, the gate of the power FETs is pulled low disconnecting the overvoltage from the load. This feature uses the OV pin to monitor the power supply output voltage. Once the voltage on the OV pin exceeds the 1.220V threshold, the gate of the external power FETs is pulled low.

## APPLICATIONS INFORMATION

A timer is started as soon as the OV pin exceeds 1.220V. The timer consists of a 6µA current source into an external capacitor on the TIMER pin. As soon as the voltage on the TIMER pin exceeds 1.220V, the STATUS pin is pulled low.

There are two external power FETs in Figure 3. The FET with its drain on the power supply side (left) and its source on the load side (right) is used to block high voltage faults from the load. If overvoltage protection is not needed, this FET is omitted. Likewise, the FET with its drain on the load side (right) can be eliminated if protection from a ground short is not needed. The other use for the power FETs is to allow hot swapping of the power supply. Hot swapping will be discussed in a later section.

### SOFT FAULTS

The existence of a share bus that forces tight regulation of the system output voltage allows the system to detect if the load current is not sharing properly. As mentioned previously, the output of E/A2 will adjust until the measured current equals the share bus value. If the power supply output fails to share properly, the E/A2 output will hit the plus or minus supply. The LTC4350 uses the over/under current block to monitor the E/A2 output. This block signals the logic that a soft fault has occurred if the E/A2 output goes out of the normal 0.5V to 1.5V range where the $I_{OUT}$ block is active. After a timer cycle, the STATUS pin indicates a soft fault. The timer consists of a 2µA current source into an external capacitor on the TIMER pin. As soon as the voltage on the TIMER pin exceeds 1.220V, the STATUS pin is pulled low.

The fault indication at the STATUS pin is disabled under one condition. The E/A2 output can be less than 0.5V when the load currents are low. In this case, it is desired to disable the soft fault indication until the current is higher. Higher current is defined as when the GAIN pin is greater than 100mV.

The most common situations for soft faults are a disconnected power supply and the share bus shorts to $V_{CC}$ or ground.

### HOT SWAPPING

The LTC4350 controls external power FETs to allow power supplies to be hot swapped in and out of the powered system without disturbing the power buses. The gate of the power FETs are slowly ramped up. This slowly charges the power supply input and output capacitors, preventing the large inrush currents associated with capacitors being hot plugged into power buses.

When power is first applied to the $V_{CC}$ pin, the gate of the power FET is pulled low. As soon as $V_{CC}$ rises above the undervoltage lockout threshold, the chip's UV pin is functional. A 0.1µF bypass capacitor is required on the $V_{CC}$ pin. If the $V_{CC}$ pin is tied to the same power supply output that is being adjusted, then a 51Ω decoupling resistor is needed to hold up the supply during a short to ground on the supply output.

If the UV pin is greater than 1.244V, the gate of the external FETs is charged with a 10µA current source. The voltage at the GATE pin begins to rise with a slope equal to $10µA/C_G$ (Figure 4), where $C_G$ is the external capacitor connected between the GATE pin and GND. This slow charging allows the power supply output to begin load sharing in a nondisruptive manner.

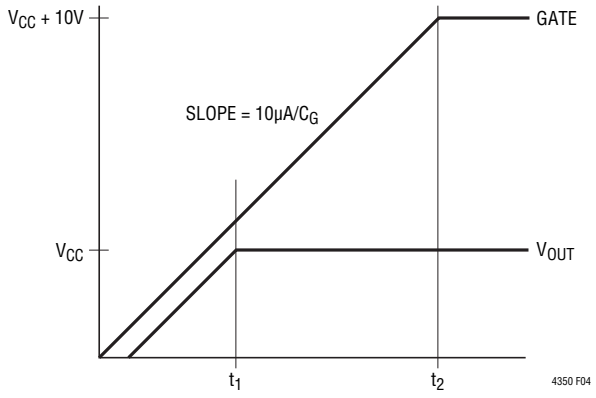



**Figure 4. Supply Turn-On**

## APPLICATIONS INFORMATION

When the power supply is disconnected, the UV pin will drop below 1.220V if the supply is loaded. The LTC4350 then discharges the gate of the power FET isolating the load from the power supply.

### DESIGN EXAMPLE

#### Load Share Components

This section demonstrates the calculations involved in selecting the component values. The design example in Figure 5 is a 5V output. This design can be extended to each of the parallel sections.

The first step is to determine the final output voltage and the amount of adjustment on the output voltage. The power supply voltage before the load sharing needs to be lower than the final output voltage. If the load is expecting to see a 5V output, then all of the shared power supplies need to be trimmed to 4.90V or lower. This allows 2% variation in component and reference tolerances so that the output always starts below 5V.

Now that the output voltage is preset below the desired output, the LTC4350 will be responsible for increasing the output utilizing the SENSE$^+$ input to the power supply. If a SENSE$^+$ line is not available, then the feedback divider at the module's error amplifier can be used. The next step is to determine the maximum positive adjustment needed for each power supply. This adjustment includes any I • R drops across sense resistors, power FETs, wiring and connectors in the supply path between the power supply and the load. For example, if the maximum current is 10A and the parasitic resistance between the power supply and load is 0.01Ω, then the positive adjustment range for I • R drops is 0.1V. Since the starting voltage is 4.9V ±0.1V, then the lowest starting voltage can be 4.8V. This voltage is 0.2V below the target. The total adjustment range that the LTC4350 will need for this example is 0.1V + 0.2V = 0.3V. Note that the lowest starting voltage should not be lower than 300mV below the target voltage.

The I • R drops should be designed to be low to eliminate the need for additional bulk capacitance at the load. In most cases the bulk capacitance exists at the power supply output before the I • R drops. If a 0.002Ω sense resistor is used and the FET resistance is below 0.003Ω, then a total 0.005Ω series resistance is acceptable for loads to 20A. Obviously, the FB pin compensates for the DC output impedance, but the AC output impedance is the I • R drops plus the ESR of the capacitors.

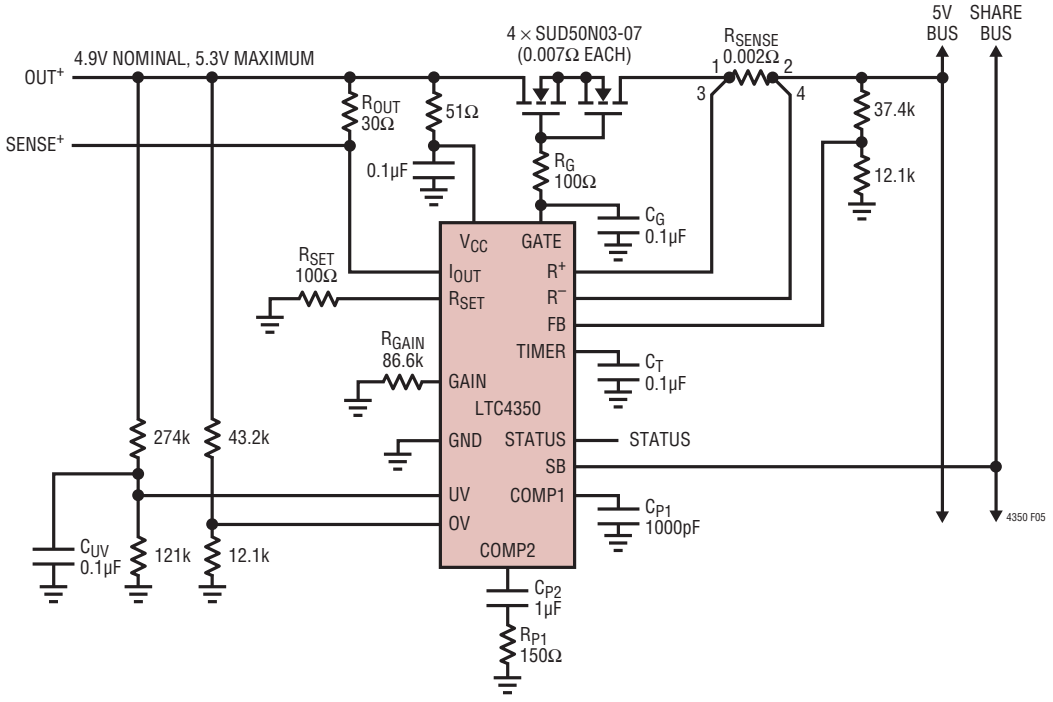



**Figure 5. 5V Load Share (20A per Module)**

## APPLICATIONS INFORMATION

The resistors $R_{OUT}$ and $R_{SET}$ set the adjustment range. The voltage on $R_{SET}$ is translated to a voltage on $R_{OUT}$ by the ratio of $R_{OUT}/R_{SET}$. Therefore, the adjustment on the output voltage will track the voltage at the $R_{SET}$ pin which is also the voltage on the COMP2 pin minus a diode voltage. The expression is $V_{ADJ} = (V_{RSET}) \bullet R_{OUT}/R_{SET} = (V_{COMP2} – V_{DIODE}) \bullet R_{OUT}/R_{SET}$. The maximum voltage at $V_{RSET}$ is limited to 1V. The maximum adjustment on the output is expressed as $V_{ADJMAX} = R_{OUT}/R_{SET}$. A normal value for $R_{SET}$ is in the 50Ω to 100Ω range.

If we set $R_{SET}$ to be 100Ω, then an $R_{OUT}$ of 100Ω allows the output voltage a full 1V adjustment. For the 0.3V range in this example, the $R_{OUT}$ is 30Ω. In some power modules, there already exists a resistor between the SENSE$^+$ line and the power output. In this case, the value of $R_{OUT}$ is the parallel combination of two resistors, one in the module and one placed between the SENSE$^+$ and output terminals of the module.

The value of the gain setting resistor, $R_{GAIN}$, depends on the maximum voltage drop across the sense resistor and the supply voltage $V_{CC}$ for the chip. The highest possible voltage at the GAIN pin is 1.5V from the $V_{CC}$ voltage. The maximum voltage on the GAIN pin is expressed as: $V_{GAINMAX} = R_{SENSE} \bullet I_{MAX} \bullet R_{GAIN}/1k = V_{CC} – 1.5V$. The expression for $R_{GAIN}$: $R_{GAIN} = (V_{CC} – 1.5V) \bullet 1k/(R_{SENSE} \bullet I_{MAX})$. In this example, $V_{CC}$ is 5V, $I_{MAX}$ is 20A and $R_{SENSE}$ is 0.002Ω. Therefore, $R_{GAIN}$ is 87.5k but using 1% values results in 86.6k.

The FB pin divider provides a 1.220V output for a 5V input. The precision of the FB pin divider resistors will impact the accuracy of the final output voltage. The UV resistive divider in this example, turns on the gate when $V_{CC}$ increases above 4V. This corresponds to the UV pin at 1.220V. The capacitor $C_{UV}$ prevents false activation during load steps. The OV set point needs to occur above the adjustment max for $V_{CC}$. The power supply output (which also is $V_{CC}$), can start as high as 5V and adjust upwards to 5.3V. The OV set point in this example is 5.5V on $V_{CC}$ when the OV pin is at 1.220V.

The timer capacitor $C_T$ is set to be 0.1µF for a 61ms timer cycle. The expression is $t = C_T \bullet 1.22V/2µA$. The gate capacitor $C_G$ is set to be 0.1µF which sets a slope of 10µA/$C_G$ or 1V every 10ms. In this case, the GATE pin must charge up to 9V before the output can ramp to 5V which happens in 90ms. In this case, the output adjust soft-start turns on when the gate ramps above 9V. The soft-start circuitry releases the COMP2 pin allowing the load sharing loop to function. A 100Ω resistor $R_G$ prevents high frequency oscillations from the power FETs at their turn-on threshold. A 0.1µF bypass capacitor is required on the $V_{CC}$ pin. If the $V_{CC}$ pin is tied to the same power supply output that is being adjusted, then a 51Ω decoupling resistor is needed to hold up the supply during a short to ground on the supply output.

### COMPENSATION

The compensation capacitor, $C_{P1}$, is needed to set the crossover frequency of the feedback error amplifier E/A1. The crossover frequency of 200kHz is adequate for most applications and requires $C_{P1}$ to be 1000pF (0.001µF).

The design of the other compensation capacitor will require some knowledge about the power supply's bandwidth. The bandwidth can be measured easily. First, use a storage oscilloscope to monitor the power supply output voltage. Then place a 1A resistive fixed load and switch in a second resistive load that increases the total load current close to rated maximum. Tapping the second resistor (with the correct power rating) to the power supply output creates this load step. Trigger the scope on the falling edge of the output voltage as it drops more than 100mV (for example from 5V to 4.8V). The recovery time, $t_R$, from the step needs to be measured. $t_R$ is defined as the 10% to 90% time measurement (see Figure 6). The

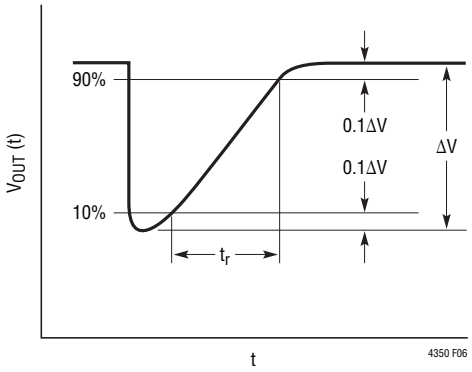



**Figure 6. $t_R$ Measurement**

## APPLICATIONS INFORMATION

compensation capacitor $C_{P2}$ can be looked up in Table 1 using $t_R$. The value for the zero setting resistor, $R_{P1}$, is 150Ω. This value guarantees the zero is at or above the crossover frequency.

**Table 1**

| $t_R$ | $f_C = 0.35/t_R$ | $C_{P2}$ |
|---|---|---|
| 5µs | 70kHz | 0.1µF |
| 10µs | 35kHz | 0.22µF |
| 20µs | 17.5kHz | 0.47µF |
| 40µs | 8.8kHz | 1µF |
| 60µs | 5.8kHz | 1.5µF |
| 80µs | 4.4kHz | 2.2µF |
| 100µs | 3.5kHz | 2.7µF |
| 150µs | 2.3kHz | 3.3µF |
| 200µs | 1.8kHz | 4.7µF |
| 300µs | 1.2kHz | 6.8µF |
| 400µs | 0.9kHz | 10µF |
| 500µs | 0.7kHz | 12µF |

### OTHER APPLICATIONS

The application shown on the first page of this data sheet assumes that the power supplies and the load reside on one main board. If the system is a true N + 1 hot swappable power supply, then the LTC4350 will reside with the power supply on a daughter card that plugs into the main board. In this case, the input and output capacitors need to be hot swapped (see Figure 7). The output capacitors are Hot Swap protected by the LTC4350. The input capacitors are Hot Swap protected using the LT®4250. Other Hot Swap parts are described in Table 2.

**Table 2**

| VOLTAGE RANGE | PART NUMBER |
|---|---|
| 3.3V to 12V | LTC1422 Single Channel<br>LTC1645 Dual Chanel |
| 3.3V to 15V | LTC1642 Overvoltage Protection |
| 2.7V to 16.5V | LTC1647 Dual Channel |
| 9V to 80V | LT1641 Positive High Voltage |
| –20V to –80V | LT4250 Negative High Voltage |

In some cases, the output voltage is below the undervoltage lockout of the LTC4350. In this case, an external supply of 3.3V or greater needs to provide for the chip. Figure 8 shows a 1.5V output redundant power supply that uses 24V to 1.5V switching power supplies. The $V_{CC}$ pin of the LTC4350 can be driven from the $INTV_{CC}$ pin of the LTC1629.

## APPLICATIONS INFORMATION

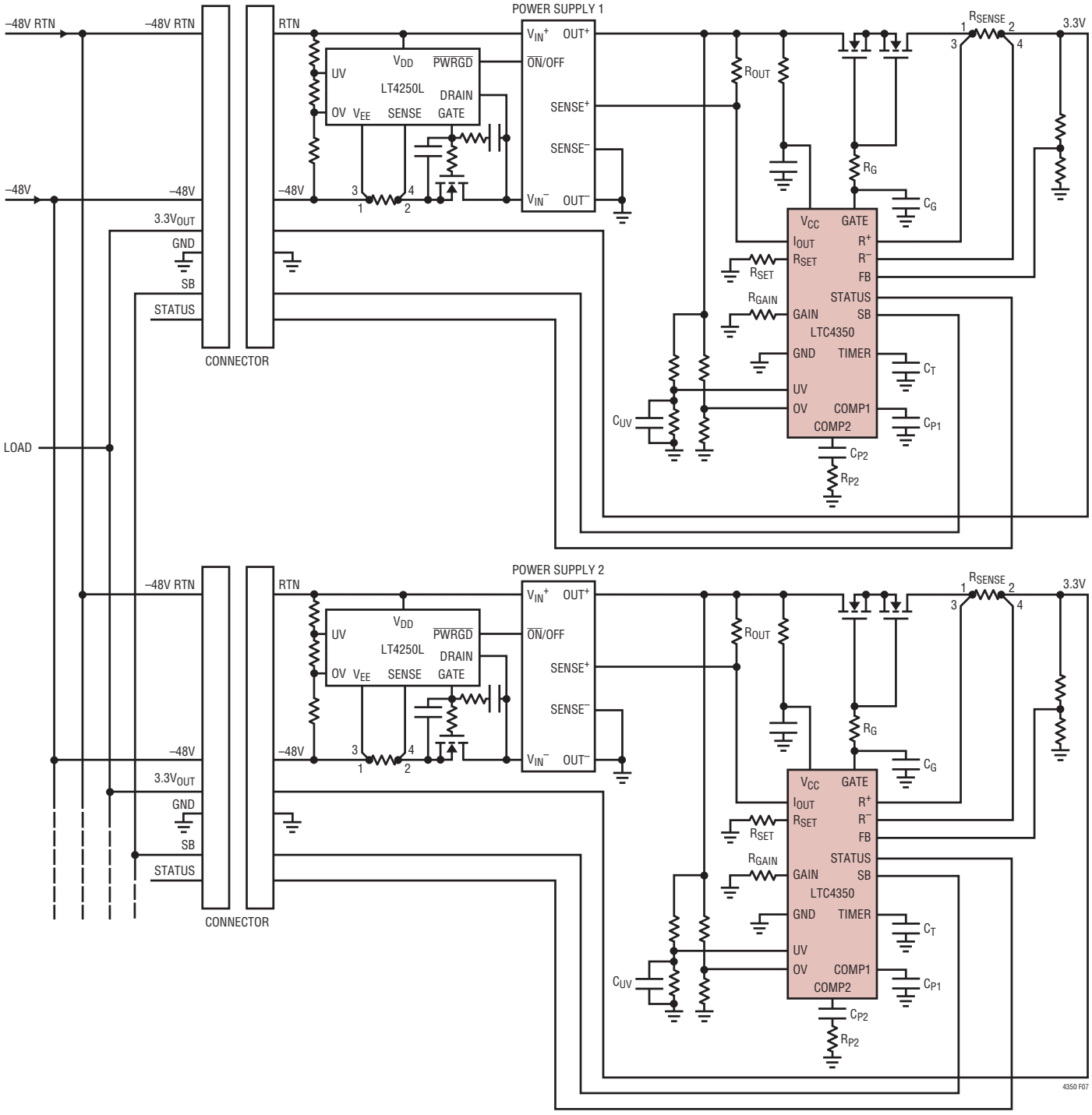
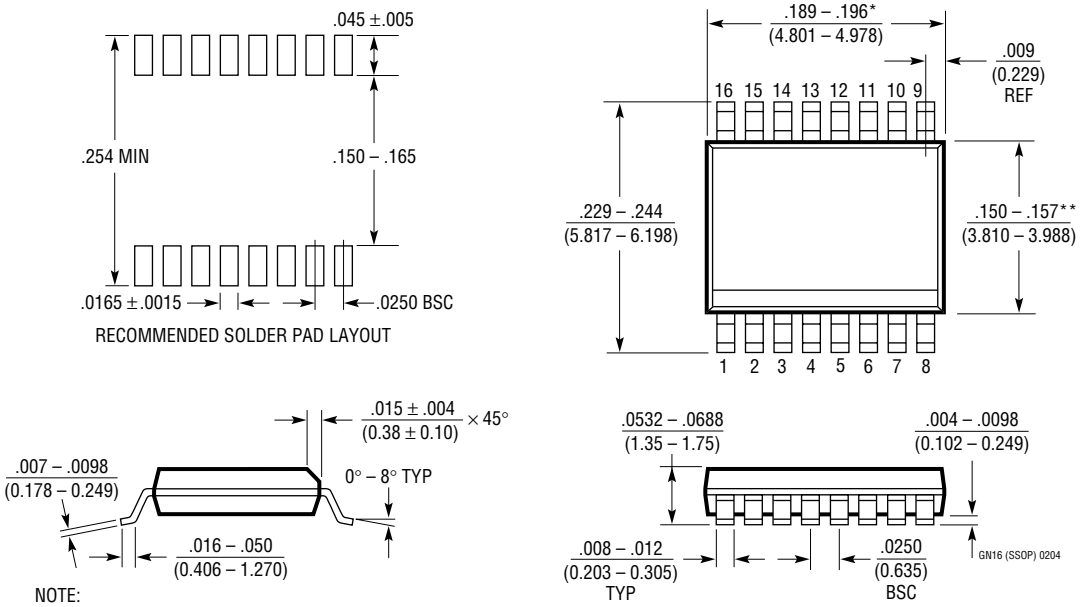



**Figure 7. –48V to 3.3V Hot Swap Power Supply**

# PACKAGE DESCRIPTION

**GN Package**
**16-Lead Plastic SSOP (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1641)




NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## REVISION HISTORY (Revision history begins at Rev B)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| B | 3/10 | Not Recommended for New Designs | 1 |