Negative Voltage Diode-OR Controller and Monitor

FEATURES

- **Controls N-Channel MOSFETs**
- **Replaces Power Schottky Diodes**
- **Less Than 1µs Turn-off Time Limits Peak Fault Current**
- **80V Operation**
- **Smooth Switchover without Oscillation**
- **No Reverse DC Current**
- Fault Output
- Selectable Fault Thresholds
- Available in 8-Lead (3mm × 2mm) DFN and 8-Lead SO Packages

APPLICATIONS

- AdvancedTCA Systems
- –48V Distributed Power Systems
- Computer Systems/Servers
- Telecom Infrastructure
- Optical Networks

DESCRIPTION

The LTC®4354 is a negative voltage diode-OR controller that drives two external N-channel MOSFETs. It replaces two Schottky diodes and the associated heat sink, saving power and area. The power dissipation is greatly reduced by using N-channel MOSFETs as the pass transistors. Power sources can easily be ORed together to increase total system power and reliability.

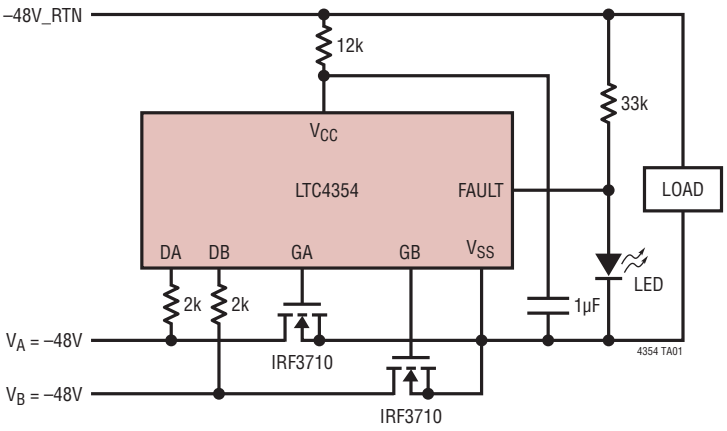
When first powered up, the MOSFET body diode conducts the load current until the pass transistor is turned on. The LTC4354 servos the voltage drop across the pass transistors to ensure smooth transfer of current from one transistor to the other without oscillation.

The MOSFETs are turned off in less than 1µs whenever the corresponding power source fails or is shorted. Fast turn-off prevents the reverse current from reaching a level that could damage the pass transistors.

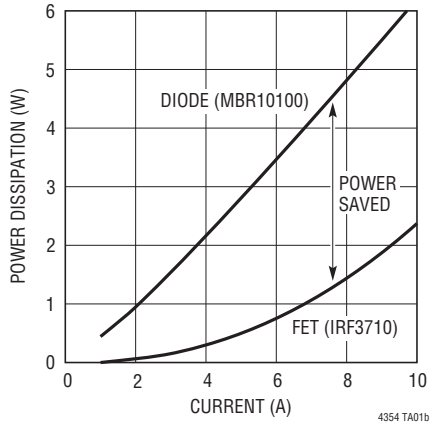
A fault detection circuit with an open-drain output capable of driving an LED or opto-coupler indicates either MOSFET short, MOSFET open or supply failed.

TYPICAL APPLICATION

–48V Diode-OR



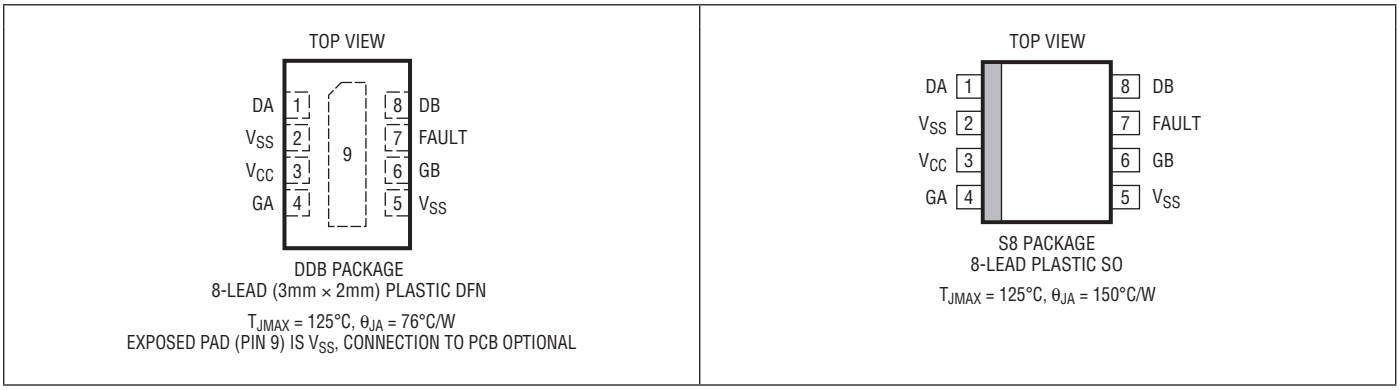
Power Dissipation vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

I_{CC} (100µs duration).....50mA
Output Voltages
GA, GB.....–0.3V to V_{CC} + 0.3V
FAULT.....–0.3V to 7V
Input Voltages
DA, DB.....–0.3V to 80V
Input Current
DA, DB Current.....–1mA to 20mA
Operating Temperature Range
LTC4354C.....0°C to 70°C
LTC4354I.....–40°C to 85°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS V_{SS}, CONNECTION TO PCB OPTIONAL

S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4354CDDB#TRMPBF	LTC4354CDDB#TRPBF	LBBK	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC4354IDDB#TRMPBF	LTC4354IDDB#TRPBF	LBMB	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4354CS8#PBF	LTC4354CS8#TRPBF	4354	8-Lead Plastic SO	0°C to 70°C
LTC4354IS8#PBF	LTC4354IS8#TRPBF	4354I	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. I_{CC} = 5mA, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_Z	Internal Shunt Regulator Voltage	I_{CC} = 5mA	●	10.25	11	11.75	V
ΔV_Z	Internal Shunt Regulator Load Regulation	I_{CC} = 2mA to 10mA			200	300	mV
V_{CC}	Operating Voltage Range		●	4.5		V_Z	V
I_{CC}	V_{CC} Supply Current	V_{CC} = (V_Z – 0.1V), Note 2 V_{CC} = 5V	● ●	 0.5	1.2 0.8	2 1.1	mA mA
V_{GATE}	GATE Pins Output High Voltage	V_{CC} = 10.25V V_{CC} = 5V		10 4.75		10.25	V V
I_{GATE}	GATE Pins Pull-Up Current	V_{SD} = 60mV; V_{GATE} = 5.5V V_{SD} = 0V; V_{GATE} = 5.5V		–15 15	–30 30	–60 60	µA µA
ΔV_{SD}	Source Drain Sense Threshold Voltage	(V_{SS} – V_{DX})	●	10	30	55	mV
$\Delta V_{SD(FLT)}$	Source Drain Fault Detection Threshold	(V_{SS} – V_{DX}); V_{CC} = 7V to V_Z	●	200	260	320	mV
t_{OFF}	Gate Turn-Off Time in Fault Condition	C_{GATE} = 3300pF; V_{GATE} ≤ 2V; V_{SD} = –0.4V			0.7	1.2	µs
V_{FAULT}	FAULT Pin Output Low	I_{FAULT} = 5mA	●		200	400	mV
I_{FAULT}	FAULT Pin Leakage Current	V_{FAULT} = 5V	●			±1	µA
I_D	Drain Pin Input Current	V_{DX} = 0V V_{DX} = 80V		–3.5 1.1	–2.5 1.5	–1.5 1.9	µA mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: I_{CC} is defined as the current level where the V_{CC} voltage is lower by 100mV from the value with 2mA of current.

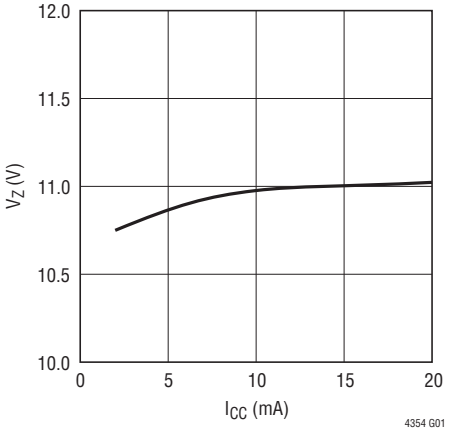
Note 3: An internal shunt regulator limits the V_{CC} pin to less than 12V above V_{SS}. Driving this pin to voltages beyond the clamp may damage the part.

Note 4: All currents into pins are positive; all voltages are referenced to V_{SS} unless otherwise specified.

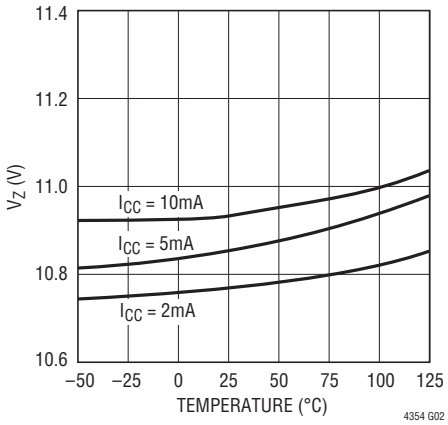
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, I_{CC} = 5mA, V_{SS} = 0V, unless otherwise noted.

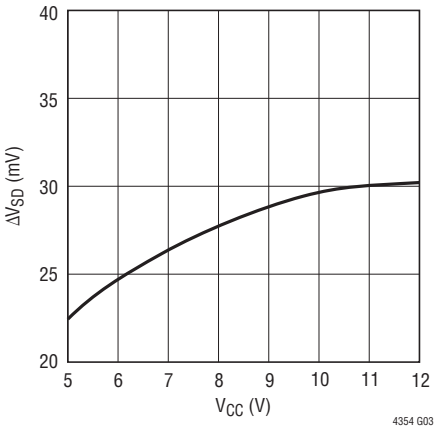
Shunt Regulator Voltage vs Input Current



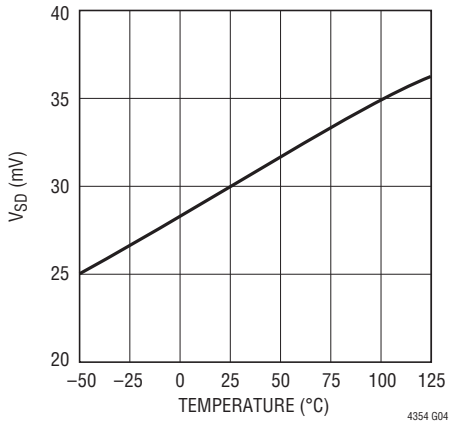
Shunt Regulator Voltage vs Input Current at Temperature



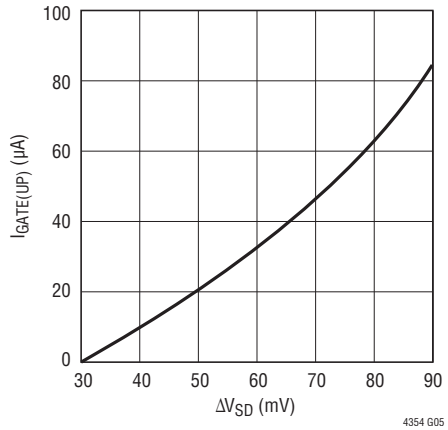
Source Drain Sense Voltage vs Supply Voltage



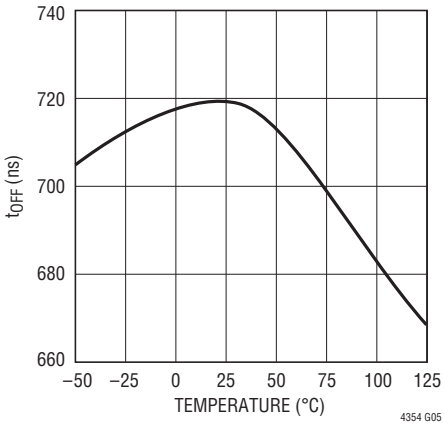
Source Drain Sense Voltage vs Temperature



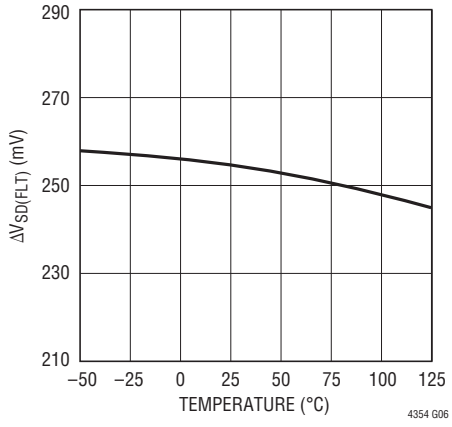
$I_{GATE(UP)}$ vs ΔV_{SD}



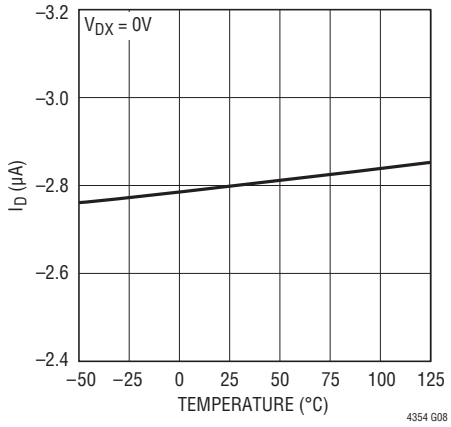
Gate Turn-Off Time vs Temperature



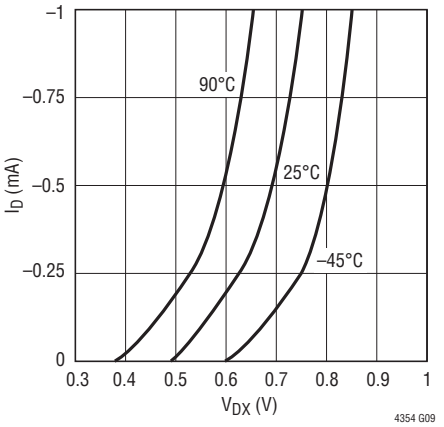
Fault Threshold Voltage vs Temperature



Drain Pin Current vs Temperature



Drain Pin Current vs Voltage



PIN FUNCTIONS

DA, DB (Pins 1, 8): Drain Voltage Sense Inputs. These pins sense source drain voltage drop across the N-channel MOSFETs. An external resistor is recommended to protect these pins from transient voltages exceeding 80V in extreme fault conditions. For Kelvin sensing, connect these pins as close to the drains as possible. Connect to V_{SS} if unused.

V_{CC} (Pin 3): Positive Supply Voltage Input. Connect this pin to the positive side of the supply through a resistor. An internal shunt regulator that can sink up to 20mA typically clamps V_{CC} at 11V. Bypass this pin with a 1µF capacitor to V_{SS}.

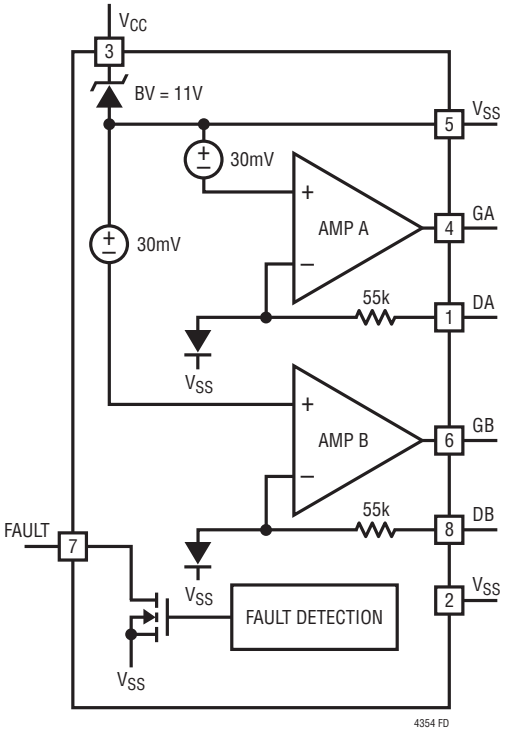
GA, GB (Pins 4, 6): Gate Drive Outputs. Gate pins pull high to 10V minimum, fully enhancing the N-channel MOSFET, when the load current creates more than 30mV of drop across the MOSFET. When the load current is small, the gates are actively servoed to maintain a 30mV drop across the MOSFET. If reverse current develops more than –140mV of voltage drop across the MOSFET, the pins pull low to V_{SS} in less than 1µs. Quickly turning off the pass transistors prevents excessive reverse currents. Leave the pins open if unused.

V_{SS} (Pins 2, 5): Negative Supply Voltage Input. This is the device negative supply input and connects to the common source connection of the N-channel MOSFETs. It also connects to the source voltage sense input of the servo amplifiers. For Kelvin sensing, connect Pin 5 as close to the common source terminal of the MOSFETs as possible.

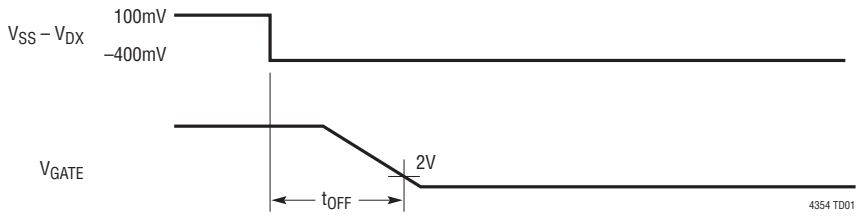
FAULT (Pin 7): Fault Output. Open-drain output that normally pulls the FAULT pin to V_{SS} and shunts current to turn off an external LED or opto-coupler. In the fault condition, where the pass transistor is fully on and the voltage drop across it is higher than the fault threshold, the FAULT pin goes high impedance, turning on the LED or opto-coupler. This indicates that one or both of the pass transistors have failed open or failed short creating a cross conduction current in between the two power supplies. Connect to V_{SS} if unused.

EXPOSED PAD (Pin 9): Exposed pad is common to V_{SS} and may be left open or connected to Pins 2 and 5.

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



OPERATION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. ORing diodes have been a popular means of connecting these supplies at the point-of-load. The disadvantage of this approach is the significant forward-voltage drop and resulting efficiency loss. This drop reduces the available supply voltage and dissipates significant power. A desirable circuit would behave like diodes but without the voltage drop and the resulting power dissipation.

The LTC4354 is a negative voltage diode-OR controller that drives two external N-channel MOSFETs as pass transistors to replace ORing diodes. The MOSFETs are connected together at the source pins. The common source node is connected to the V_{SS} pin which is the negative supply of the device. It is also connected to the positive inputs of the amplifiers that control the gates to regulate the voltage drop across the pass transistors. Using N-channel MOSFETs to replace Schottky diodes reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layouts in high power applications.

At power-up, the initial load current flows through the body diode of the MOSFET and returns to the supply with the lower terminal voltage. The associated gate pin will immediately start ramping up and turn on the MOSFET. The amplifier tries to regulate the voltage drop between the source and drain connections to 30mV. If the load current causes more than 30mV of drop, the gate rises to further enhance the MOSFET. Eventually the MOSFET gate is driven fully on and the voltage drop is equal to the $R_{DS(ON)} \bullet I_{LOAD}$.

When the power supply voltages are nearly equal, this regulation technique ensures that the load current is smoothly shared between them without oscillation. The current level flowing through each pass transistor depends on the $R_{DS(ON)}$ of the MOSFET and the output impedance of the supplies.

In the case of supply failure, such as if the supply that is conducting most or all of the current is shorted to the return side, a large reverse current starts flowing through the MOSFET that is on, from any load capacitance and through the body diode of the other MOSFET, to the second supply. The LTC4354 detects this failure condition as soon as it appears and turns off the MOSFET in less than 1µs. This fast turn-off prevents the reverse current from ramping up to a damaging level.

In the case where the pass transistor is fully on but the voltage drop across it exceeds the fault threshold, the FAULT pin goes high impedance. This allows an LED or opto-coupler to turn on indicating that one or both of the pass transistors have failed.

The LTC4354 is powered from system ground through a current limiting resistor. An internal shunt regulator that can sink up to 20mA clamps the V_{CC} pin to 11V above V_{SS}. A 1µF bypass capacitor across V_{CC} and V_{SS} pins filters supply transients and supplies AC current to the device.

APPLICATIONS INFORMATION

Input Power Supply

The power supply for the device is derived from –48_RTN through an external current limiting resistor (R_{IN}). An internal shunt regulator clamps the voltage at V_{CC} pin to 11V. A 1µF decoupling capacitor to V_{SS} is recommended. It also provides a soft-start to the part.

R_{IN} should be chosen to accommodate the maximum supply current requirement of 2mA at the expected input operating voltage.

$$R_{IN} \leq \frac{(V_{IN(MIN)} - V_{Z(MAX)})}{I_{CC(MAX)}}$$

The power dissipation of the resistor is calculated at the maximum DC input voltage:

$$P = \frac{(V_{IN(MAX)} - V_{CC(MIN)})^2}{R_{IN}}$$

If the power dissipation is too high for a single resistor, use multiple low power resistors in series instead of a single high power component.

MOSFET SELECTION

The LTC4354 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are on-resistance $R_{DS(ON)}$, the maximum drain-source voltage V_{DSS}, and the threshold voltage.

The gate drive for the MOSFET is guaranteed to be more than 10V and less than 12V. This allows the use of standard threshold voltage N-channel MOSFETs. An external zener diode can be used to clamp the potential at the V_{CC} pin to as low as 4.5V if the gate to source rated breakdown voltage is less than 12V.

The maximum allowable drain-source voltage, $V_{(BR)DSS}$, must be higher than the supply voltages. If the inputs are shorted, the full supply voltage will appear across the MOSFETs.

The LTC4354 tries to servo the voltage drop across the MOSFET to 30mV in the forward direction by controlling the gate voltage and sends out a fault signal when the voltage drop exceeds the 260mV fault threshold. The $R_{DS(ON)}$ should be small enough to conduct the maximum load current while not triggering a fault, and to stay within the MOSFET's power rating at the maximum load current ($I^2 \bullet R_{DS(ON)}$).

Fault Conditions

LTC4354 monitors fault conditions and turns on an LED or opto-coupler to indicate a fault. When the voltage drop across the pass transistor is higher than the 260mV fault threshold, the internal pull-down at the FAULT pin turns off and allows the current to flow through the LED or opto-coupler. Conditions that cause high voltage across the pass transistor include: short in the load circuitry, excessive load current, FET open while conducting current, and FET short on the channel with the higher supply voltage. The fault threshold is internally set to 260mV.

In the event of FET open on the channel with the more negative supply voltage, if the voltage difference is high enough, the substrate diode on the DA or DB pins will forward bias. The current flowing out of the pins must be limited to a safe level (<1mA) to prevent device latch up. Schottky diodes can be used to clamp the voltage at the DA and DB pins, as shown in Figure 1.

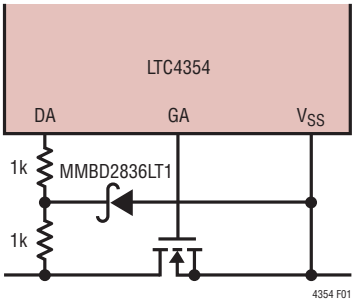


Figure 1. Method of Protecting the DA and DB Pins from Negative Inputs. One Channel Shown

APPLICATIONS INFORMATION

System Power Supply Failure

LTC4354 automatically supplies load current from the system supply with the more negative input potential. If this supply is shorted to the return side, a large reverse current flows from its pass transistor. When this reverse current creates –140mV of voltage drop across the drain and source pins of the pass transistor, the LTC4354 drives the gate low fast and turns it off.

The remaining system power supply will deliver the load current through the body diode of its pass transistor until the channel turns on. The LTC4354 ramps the gate up and turns on the N-channel MOSFET to reduce the voltage drop across it, a process that takes less than 1ms depending on the gate charge of the MOSFET.

Drain Resistor

Two resistors are required to protect the DA and DB pins from transient voltages higher than 80V. In the case when the supply with the lower potential is shorted to the return side due to supply failure, a reverse current flows briefly through the pass transistor to the other supply to discharge the output capacitor. This current stores energy in the stray inductance along the current path. Once the pass transistor is turned off, this energy forces the drain terminal of the FET high until it reaches the breakdown voltage. If this voltage is higher than 80V, the internal ESD devices at the DA and DB pins might break down and become damaged. The external drain resistors limit the current into the pins and protect the ESD devices. A 2k resistor is recommended for 48V applications. Larger resistor values increase the source drain sense threshold voltage due to the input current at the drain pins.

Loop Stability

The servo loop is compensated by the parasitic capacitance of the power N-channel MOSFET. No further compensation components are normally required. In the case when a MOSFET with very small parasitic capacitance is chosen, a 1000pF compensation capacitor connected across the gate and source pins might be required.

Design Example

The following demonstrates the calculations involved for selecting components in a –36V to –72V system with 5A maximum load current, see Figure 2.

First, select the input dropping resistor. The resistor should allow 2mA of current with the supply at –36V.

$$R_{IN} \le \frac{(36V - 11.5V)}{2mA} = 12.25k$$

The nearest lower 5% value is 12k.

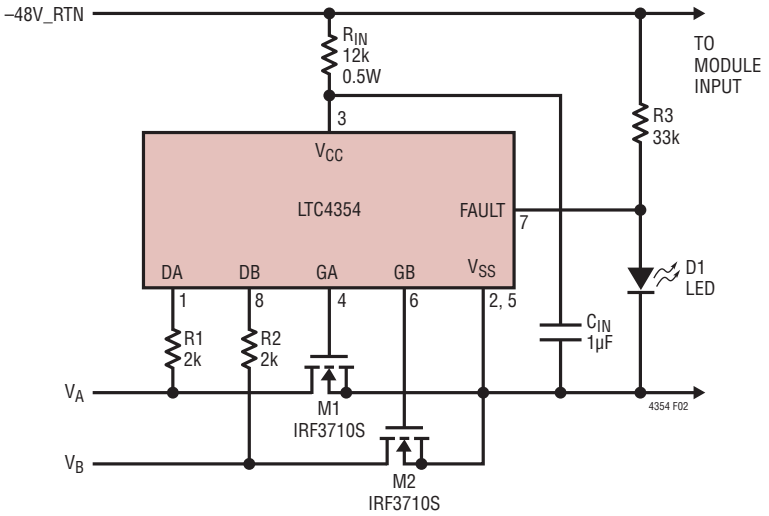


Figure 2. –36V to –72V/5A Design Example

APPLICATIONS INFORMATION

The worst-case power dissipation in R_{IN}:

$$P = \frac{(72V - 10.5V)^2}{12k} = 0.315W$$

Choose a 12k 0.5W resistor or use two 5.6k 0.25W resistors in series.

Next, choose the N-channel MOSFET. The 100V, IRF3710S in DD-Pak package with $R_{DS(ON)}$ = 23mΩ (max) offers a good solution. The maximum voltage drop across it is:

$\Delta V = (5A)(23m\Omega) = 115mV$

The maximum power dissipation in the MOSFET is a mere:

$P = (5A)(115mV) = 0.6W$

R1 and R2 are chosen to be 2k to protect DA and DB pins from being damaged by high voltage spikes that can occur during an input supply fault.

The LED, D1, requires at least 1mA of current to fully turn on, therefore R3 is set to 33k to accommodate lowest input supply voltage of –36V.

Layout Considerations

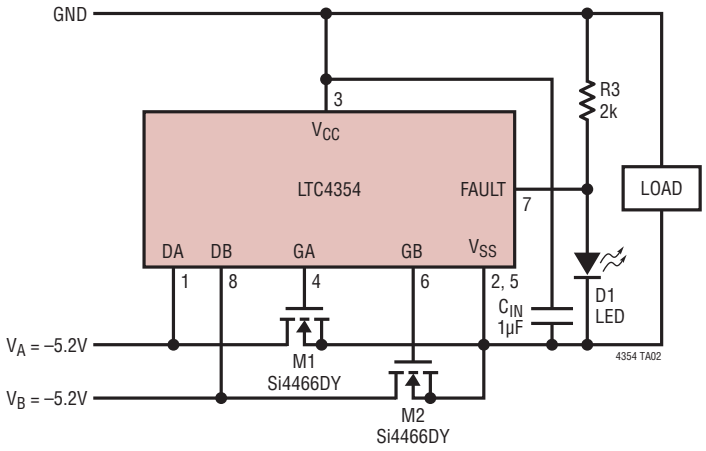
The following advice should be considered when laying out a printed circuit board for the LTC4354.

The bypass capacitor provides AC current to the device so place it as close to the V_{CC} and V_{SS} pins as possible. The inputs to the servo amplifiers, DA, DB and V_{SS} pins, should be connected directly to the MOSFETs' terminals using Kelvin connections for good accuracy.

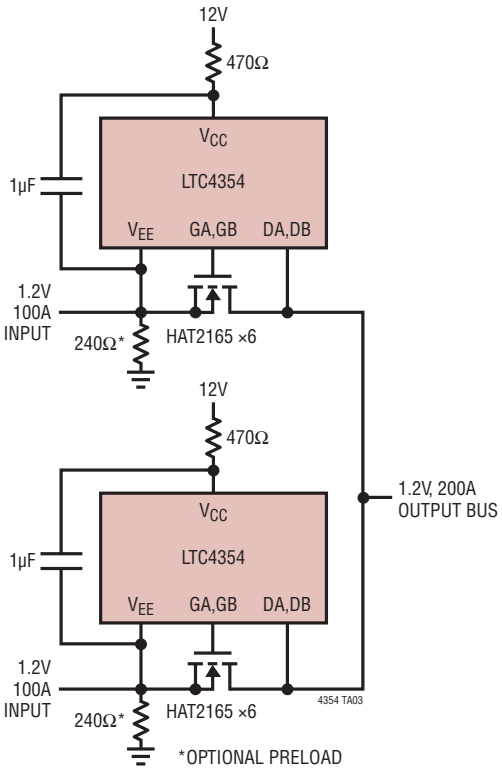
Keep the traces to the MOSFETs wide and short. The PCB traces associated with the power path through the MOSFETs should have low resistance.

TYPICAL APPLICATIONS

–5.2V Diode-Or Controller

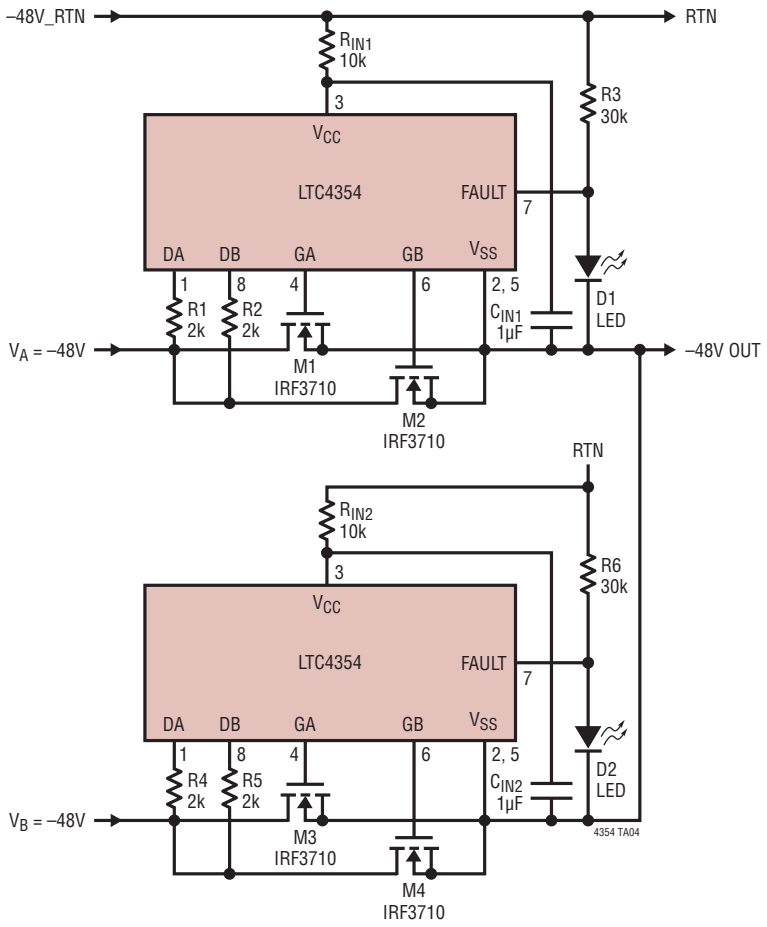


Positive Low Voltage Diode-OR Combines Multiple Switching Converters

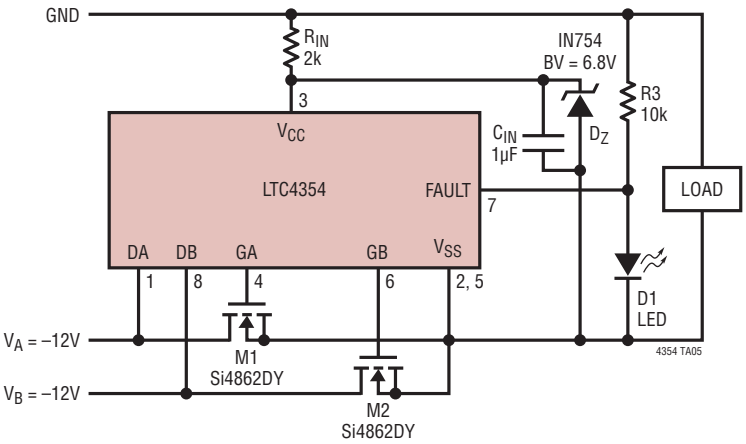


TYPICAL APPLICATIONS

–36V to –72V/20A High Current with Parallel FETs



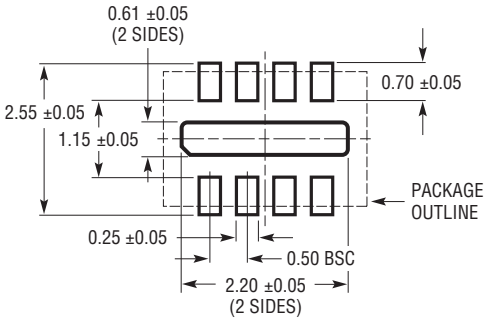
–12V Diode-OR Controller



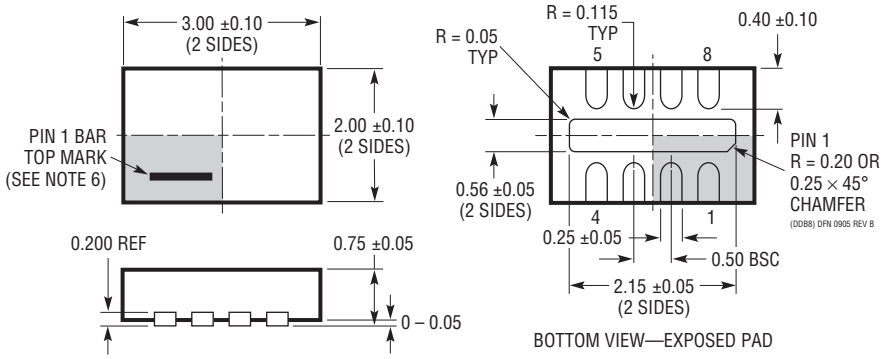
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



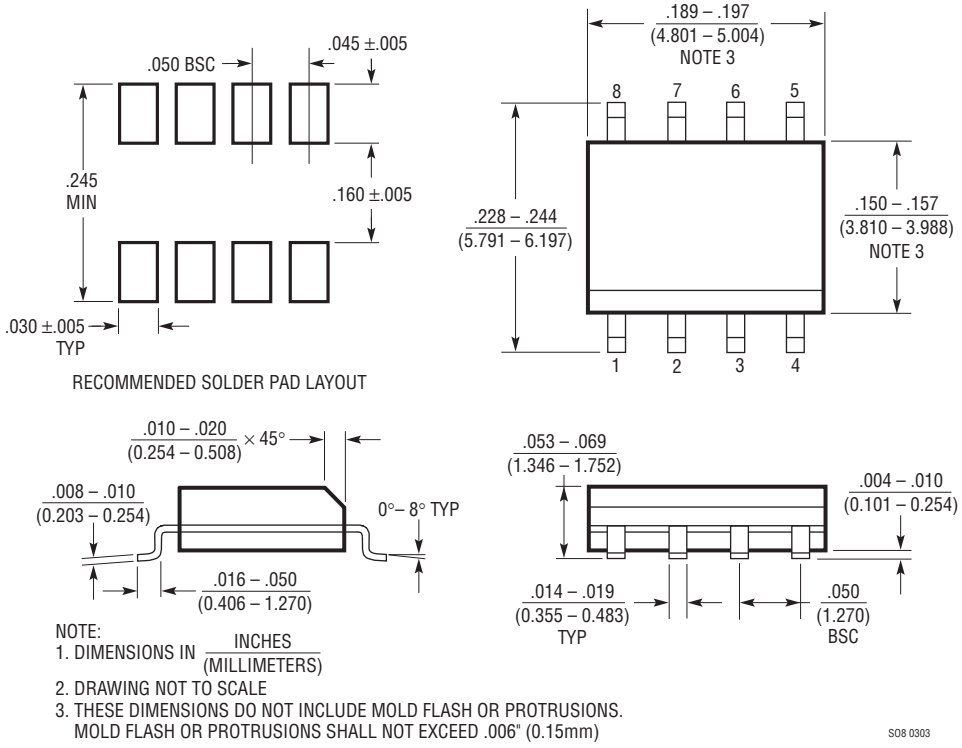
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	04/12	Updated package/Order Information format	2
		Changed Figure 2	8
		Updated DDB package drawing	11