Positive High Voltage Ideal Diode-OR with Input Supply and Fuse Monitors

FEATURES

- **Replaces Power Schottky Diodes**
- **Controls N-Channel MOSFETs**
- **0.3µs Turn-Off Time Limits Peak Fault Current**
- **Wide Operating Voltage Range: 9V to 80V**
- Smooth Switchover without Oscillation
- No Reverse DC Current
- Monitors V_{IN}, Fuse, and MOSFET Diode
- Available in 14-Lead (4mm × 3mm) DFN, 16-Lead MS and SO Packages

APPLICATIONS

- High Availability Systems
- AdvancedTCA® (ATCA) Systems
- +48V and –48V Distributed Power Systems
- Telecom Infrastructure

DESCRIPTION

The LTC®4355 is a positive voltage ideal diode-OR controller that drives two external N-channel MOSFETs. Forming the diode-OR with N-channel MOSFETs instead of Schottky diodes reduces power consumption, heat dissipation and PC board area.

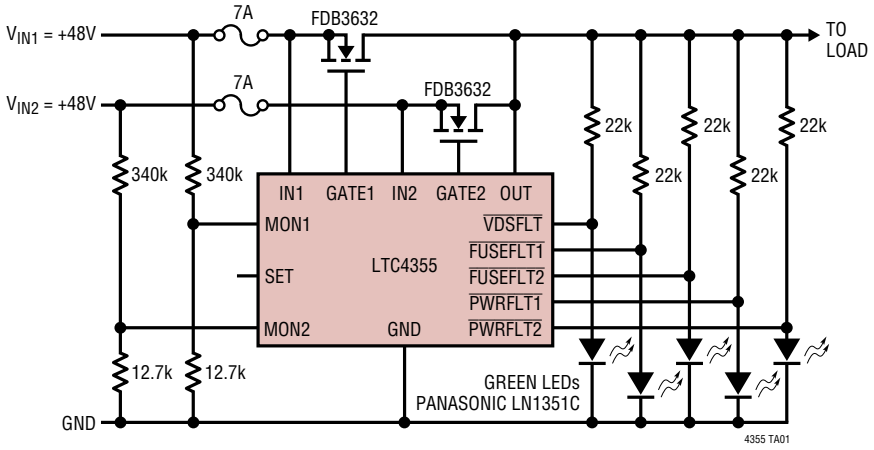
With the LTC4355, power sources can easily be ORed together to increase total system reliability. The LTC4355 can diode-OR two positive supplies or the return paths of two negative supplies, such as in a –48V system.

In the forward direction the LTC4355 controls the voltage drop across the MOSFET to ensure smooth current transfer from one path to the other without oscillation. If a power source fails or is shorted, fast turnoff minimizes reverse current transients.

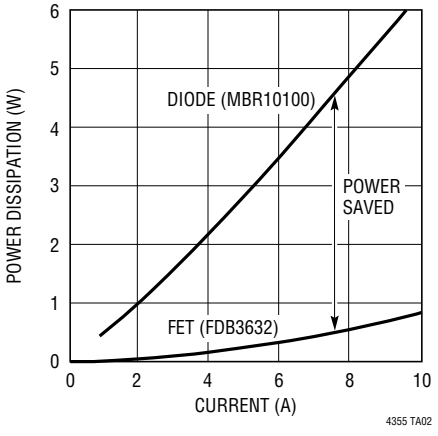
Power fault detection indicates if the input supplies are not in regulation, the inline fuses are blown, or the voltages across the MOSFETs are greater than the fault threshold.

TYPICAL APPLICATION

+48V Diode-OR



Power Dissipation vs Load Current



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
- IN1, IN2 ..... –1V to 100V
- OUT ..... –0.3V to 100V

Input Voltages
- MON1, MON2, SET ..... –0.3V to 7V

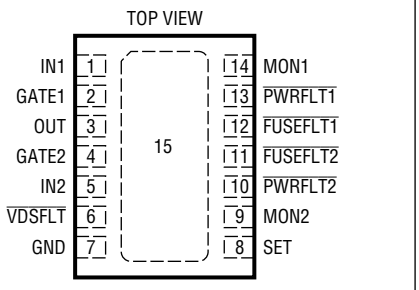
Output Voltages
- GATE1 (Note 3) ..... V_{IN1} – 0.2V to V_{IN1} + 13V
- GATE2 (Note 3) ..... V_{IN2} – 0.2V to V_{IN2} + 13V
- $\overline{PWRFLT1}$, $\overline{PWRFLT2}$, $\overline{VDSFLT}$, $\overline{FUSEFLT1}$, $\overline{FUSEFLT2}$ ..... –0.3V to 8V

Operating Ambient Temperature Range
- LTC4355C ..... 0°C to 70°C
- LTC4355I ..... –40°C to 85°C
- LTC4355H ..... –40°C to 125°C

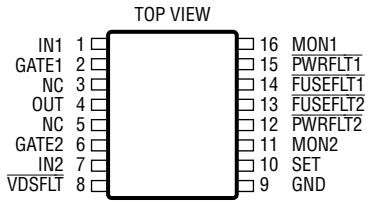
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- MS, SO Packages ..... 300°C

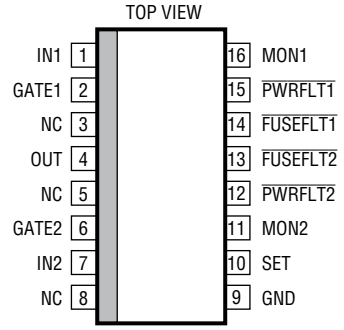
PIN CONFIGURATION



DE14 PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 15) PCB GND CONNECTION OPTIONAL



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 120°C/W



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 80°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4355CDE#PBF	LTC4355CDE#TRPBF	4355	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4355IDE#PBF	LTC4355IDE#TRPBF	4355	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4355CS#PBF	LTC4355CS#TRPBF	LTC4355CS	16-Lead Plastic SO	0°C to 70°C
LTC4355IS#PBF	LTC4355IS#TRPBF	LTC4355IS	16-Lead Plastic SO	–40°C to 85°C
LTC4355CMS#PBF	LTC4355CMS#TRPBF	4355	16-Lead Plastic MSOP	0°C to 70°C
LTC4355IMS#PBF	LTC4355IMS#TRPBF	4355	16-Lead Plastic MSOP	–40°C to 85°C
LTC4355HMS#PBF	LTC4355HMS#TRPBF	4355	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 9V < V_{OUT} < 80V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Operating Supply Range		●	9		80	V
I_{OUT}	Supply Current		●		2	3	mA
I_{INx}	INx Pin Input Current	GATE High	●	0.5	0.6	1.2	mA
ΔV_{GATEx}	External N-Channel Gate Drive ($V_{GATEx} - V_{INx}$) V_{OUT} = 20V to 80V V_{OUT} = 9V to 20V		● ●	10 4.5	14 6	18 18	V V
$I_{GATEx(UP)}$	External N-Channel Gate Pull-Up Current	$V_{GATEx} = V_{INx}$, $V_{INx} - V_{OUT}$ = 100mV	●	–14	–20	–26	µA
$I_{GATEx(DN)}$	External N-Channel Gate Pull-Down in Fault Condition	Gate Drive Off, $V_{GATEx} = V_{INx}$ +5V	●	1	2		A
t_{OFF}	Gate Turn-Off Time	$V_{INx} - V_{OUT}$ = 55mV ⎾–1V, C_{GATE} = 0 $V_{GATEx} - V_{INx}$ < 1V	●		0.3	0.4	µs
$V_{MONx(TH)}$	MONx Pin Threshold Voltage	V_{MONx} Rising	●	1.209	1.227	1.245	V
$V_{MONx(HYST)}$	MONx Pin Hysteresis Voltage		●	10	30	45	mV
$I_{MONx(IN)}$	MONx Pin Input Current	V_{MONx} = 1.23V	●		0	±1	µA
$V_{INx(TH)}$	INx Pin Threshold Voltage	V_{INx} Rising	●	3	3.5	4	V
$V_{INx(HYST)}$	INx Pin Hysteresis Voltage		●	25	75	150	mV
ΔV_{SD}	Source-Drain Regulation Voltage ($V_{INx} - V_{OUT}$)	$V_{GATEx} - V_{INx}$ = 2.5V	●	10	25	55	mV
$\Delta V_{SD(FLT)}$	Short-Circuit Fault Voltage ($V_{INx} - V_{OUT}$) Rising SET = 0V SET = 100kΩ SET = Hi-Z		● ● ●	0.2 0.4 1.3	0.25 0.5 1.5	0.3 0.6 1.6	V V V
$\Delta V_{SD(FLT)(HYST)}$	Short-Circuit Fault Hysteresis Voltage				30		mV
$V_{\overline{FLT}}$	$\overline{PWRFLTx}$, $\overline{FUSEFLTx}$, $\overline{VDSFLT}$ Pins Output Low	$I_{\overline{PWRFLTx}}$, $I_{\overline{FUSEFLTx}}$, $I_{\overline{VDSFLT}}$ = 5mA	●		100	200	mV
$I_{\overline{FLT}}$	$\overline{PWRFLTx}$, $\overline{FUSEFLTx}$, $\overline{VDSFLT}$ Pins Leakage Current	$V_{\overline{PWRFLTx}}$, $V_{\overline{FUSEFLTx}}$, $V_{\overline{VDSFLT}}$ = 5V	●		0	±1	µA
$R_{SET(L)}$	SET Resistance Range for $\Delta V_{SD(FLT)}$ = 0.25V		●	0		5	kΩ
$R_{SET(M)}$	SET Resistance Range for $\Delta V_{SD(FLT)}$ = 0.5V		●	50		150	kΩ
$R_{SET(H)}$	SET Resistance Range for $\Delta V_{SD(FLT)}$ = 1.5V		●	1			MΩ

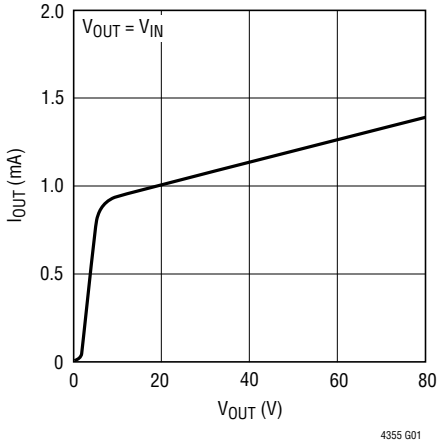
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

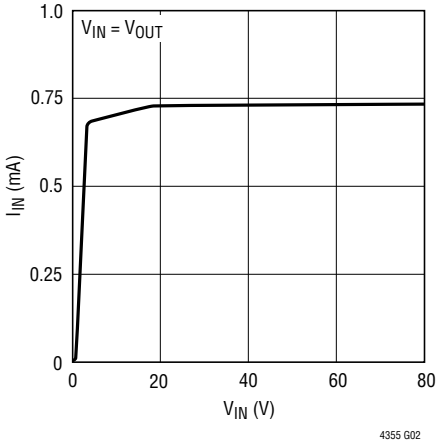
Note 3: The GATEx pins are internally limited to a minimum of 13V above INx. Driving these pins beyond the clamp may damage the part.

TYPICAL PERFORMANCE CHARACTERISTICS

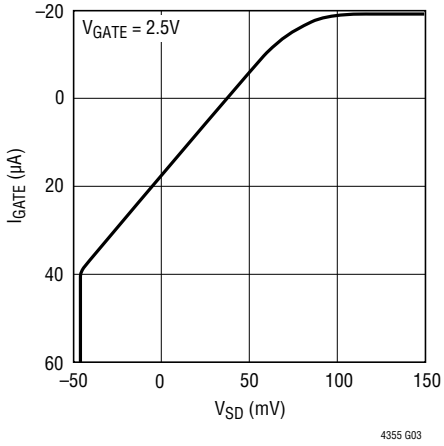
I_{OUT} vs V_{OUT}



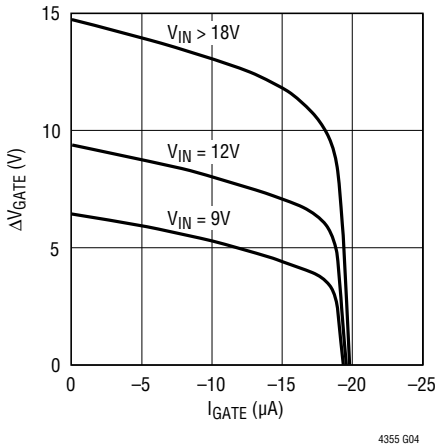
I_{IN} vs V_{IN}



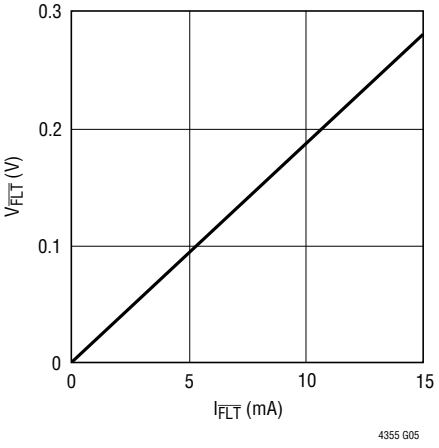
I_{GATE} vs ΔV_{SD}



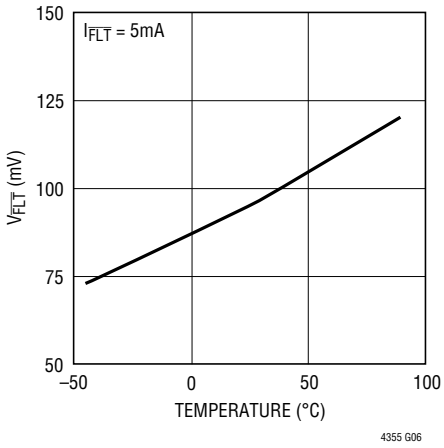
ΔV_{GATE} vs I_{GATE}



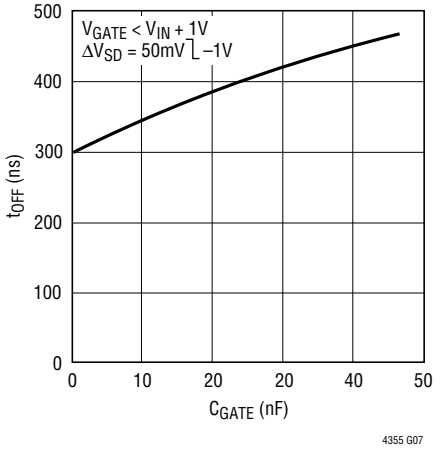
Fault Output Low vs Load Current



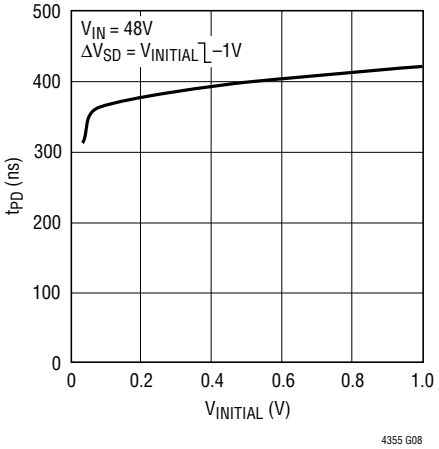
Fault Output Low vs Temperature



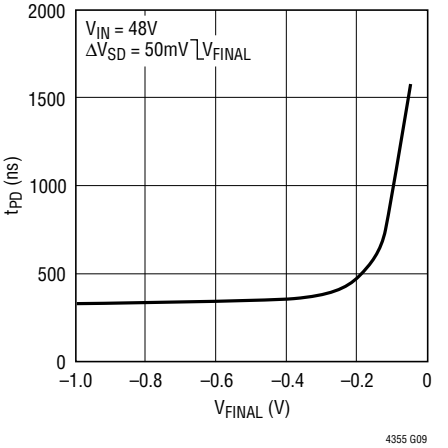
FET Turn-Off Time vs GATE Capacitance



FET Turn-Off Time vs Initial Overdrive



FET Turn-Off Time vs Final Overdrive



PIN FUNCTIONS

Exposed Pad: Exposed pad may be left open or connected to GND.

$\overline{\text{FUSEFLTx}}$: Fuse Fault Outputs. Open-drain output that pulls to GND when V_{INx} < 3.5V, indicating that the fuse has blown open. Otherwise, this output is high impedance. Connect to GND if unused.

GATEx: Gate Drive Outputs. The GATE pins pull high, enhancing the N-channel MOSFET when the load current creates more than 25mV of voltage drop across the MOSFET. When the load current is small, the gates are actively driven to maintain 25mV across the MOSFET. If the reverse current develops more than –25mV of voltage drop across a MOSFET, a fast pull-down circuit quickly connects the GATE pin to the IN pin, turning off the MOSFET. Limit the capacitance between the GATE and IN pins to less than 0.1µF.

GND: Device Ground.

INx: Input Voltages and GATE Fast Pull-Down Returns. The IN pins are the anodes of the ideal diodes and connect to the sources of the N-channel MOSFETs. The voltages sensed at these pins are used to control the source-drain voltages across the MOSFETs and are used by the fault detection circuits that drive the $\overline{\text{PWRFLT}}$, $\overline{\text{FUSEFLT}}$, and $\overline{\text{VDSFLT}}$ pins. The GATE fast pull-down current is returned through the IN pins. Connect these pins as close to the MOSFET sources as possible. Connect to OUT if unused.

MONx: Input Supply Monitors. These pins are used to sense the input supply voltages. Connect these pins to external resistive dividers between the input supplies and GND. If V_{MONx} falls below 1.23V, the $\overline{\text{PWRFLTx}}$ pin pulls to GND. Connect to GND if unused.

NC: No Connection. Not internally connected. These pins provide extra distance between high and low voltage pins.

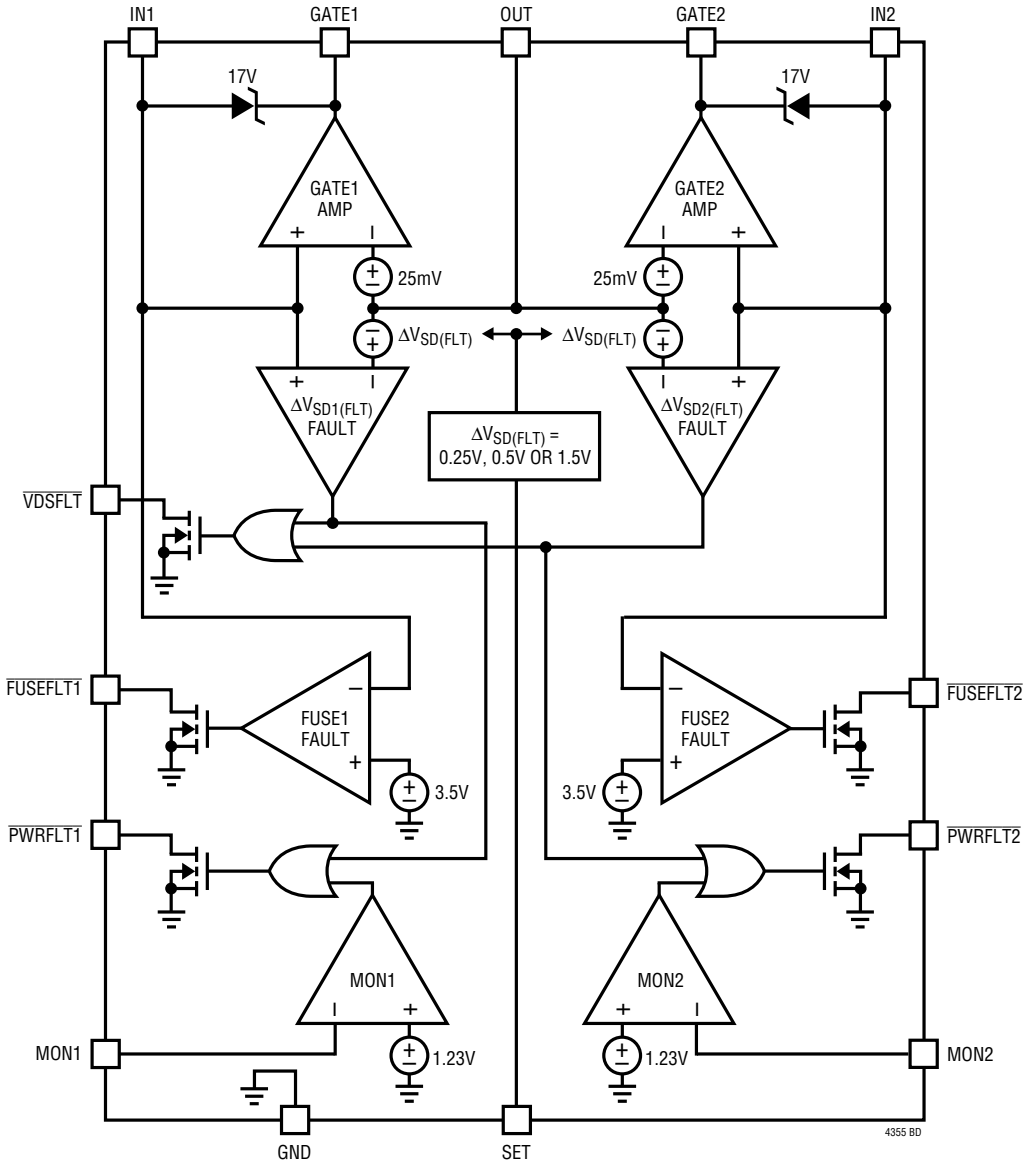
OUT: Drain Voltage Sense and Positive Supply Input. OUT is the diode-OR output of IN1 and IN2. It connects to the common drain connection of the N-channel MOSFETs. The voltage sensed at this pin is used to control the source-drain voltages across the MOSFETs and is used by the fault detection circuits that drive the $\overline{\text{PWRFLT}}$ and $\overline{\text{VDSFLT}}$ pins. The LTC4355 is powered from the OUT pin.

$\overline{\text{PWRFLTx}}$: Power Fault Outputs. Open-drain output that pulls to GND when V_{MONx} falls below 1.23V or the forward voltage across the MOSFET exceeds $\Delta V_{SD(FLT)}$. When V_{MONx} is above 1.23V and the forward voltage across the MOSFET is less than $\Delta V_{SD(FLT)}$, $\overline{\text{PWRFLTx}}$ is high impedance. Connect to GND if unused.

SET: $\Delta V_{SD(FLT)}$ Threshold Configuration Input. Tying SET to GND, to a 100k resistor connected to GND, or leaving SET open configures the $\Delta V_{SD(FLT)}$ forward voltage fault threshold to 250mV, 500mV, or 1.5V, respectively. When the voltage across a MOSFET exceeds $\Delta V_{SD(FLT)}$, the $\overline{\text{VSDFLT}}$ pin and at least one of the $\overline{\text{PWRFLT}}$ pins pull to GND.

$\overline{\text{VDSFLT}}$: MOSFET Fault Output. Open-drain output that pulls to GND when the forward voltage across either MOSFET exceeds $\Delta V_{SD(FLT)}$. $\overline{\text{PWRFLT1}}$ or $\overline{\text{PWRFLT2}}$ also pulls low to indicate which MOSFET's forward voltage drop exceeds $\Delta V_{SD(FLT)}$. Otherwise, this pin is high impedance. Connect to GND if unused.

BLOCK DIAGRAM



OPERATION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. ORing diodes have been a popular means of connecting these supplies at the point of load. The disadvantage of this approach is the forward voltage drop and resulting efficiency loss. This drop reduces the available supply voltage and dissipates significant power. Using N-channel MOSFETs to replace Schottky diodes reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layouts in high power applications.

The LTC4355 is a positive voltage diode-OR controller that drives two external N-channel MOSFETs as pass transistors to replace ORing diodes. The IN and OUT pins form the anodes and cathodes of the ideal diodes. The source pins of the external MOSFETs are connected to the IN pins. The drains of the MOSFETs are connected together at the OUT pin, which is the positive supply of the device. The gates of the external MOSFETs are driven by the LTC4355 to regulate the voltage drop across the pass transistors.

At power-up, the initial load current flows through the body diode of the MOSFET with the higher INx voltage. The associated GATEx pin immediately ramps up and turns on the MOSFET. The amplifier tries to regulate the voltage drop across the source and drain connections to 25mV. If the load current causes more than 25mV of drop, the MOSFET gate is driven fully on and the voltage drop is equal to $R_{DS(ON)} \bullet I_{LOAD}$.

When the power supply voltages are nearly equal, this regulation technique ensures that the load current is smoothly shared between the MOSFETs without oscillation. The current flowing through each pass transistor depends on the $R_{DS(ON)}$ of each MOSFET and the output impedances of the supplies.

In the event of a supply failure, such as if the supply that is conducting most or all of the current is shorted to GND, reverse current flows temporarily through the MOSFET that is on. This current is sourced from any load capacitance and from the second supply through the body diode of the other MOSFET. The LTC4355 quickly responds to this condition, turning off the MOSFET in about 500ns. This fast turn-off prevents the reverse current from ramping up to a damaging level.

In the case where the forward voltage drop exceeds the configurable fault threshold, $\Delta V_{SD(FLT)}$, the $\overline{VDSFLT}$ pin pulls low. Using this pin to shunt current away from an LED or opto-coupler provides an indication that a pass transistor has either failed or has excessive forward current. Additionally, in this condition the $\overline{PWRFLT1}$ or $\overline{PWRFLT2}$ pin pulls low to identify the faulting channel.

The $\overline{PWRFLT}$ pins also indicate if an input supply is within regulation. When $V_{MON1} < 1.23V$ or $V_{MON2} < 1.23V$, the corresponding $\overline{PWRFLT}$ pin pulls low to indicate that the input supply is low, turning off an optional LED or opto-coupler.

The $\overline{FUSEFLT}$ pins indicate the status of input fuses. If the voltage at one of the IN pins is less than 3.5V, the corresponding $\overline{FUSEFLT}$ pin pulls low. The IN pins sink a minimum of 0.5mA to guarantee that the IN pin will pull low when the input fuse is blown open. Note that the $\overline{FUSEFLT}$ pin will activate if the input supply is less than 3.5V even if the fuse is intact.

APPLICATIONS INFORMATION

MOSFET Selection

The LTC4355 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are on-resistance $R_{DS(ON)}$, the maximum drain-source voltage V_{DSS}, and the threshold voltage.

The gate drive for the MOSFET is guaranteed to be greater than 4.5V when the supply voltage at V_{OUT} is between 9V and 20V. When the supply voltage at V_{OUT} is greater than 20V, the gate drive is guaranteed to be greater than 10V. The gate drive is limited to less than 18V. This allows the use of logic level threshold N-channel MOSFETs and standard N-channel MOSFETs above 20V. An external Zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 18V. See the Typical Applications section for an example.

The maximum allowable drain-source voltage, BV_{DSS}, must be higher than the supply voltages. If an input is connected to GND, the full supply voltage will appear across the MOSFET.

If the voltage drop across either MOSFET exceeds the configurable $\Delta V_{SD(FLT)}$ fault threshold, the $\overline{VDSFLT}$ pin and the $\overline{PWRFLT}$ pin corresponding to the faulting channel pull low. The $R_{DS(ON)}$ should be small enough to conduct the maximum load current while not triggering a fault, and to stay within the MOSFET's power rating at the maximum load current ($I^2 \bullet R_{DS(ON)}$).

Fault Conditions

The LTC4355 monitors fault conditions and shunts current away from LEDs or opto-couplers, turning each one off to indicate a specific fault condition (see Table 1).

When the voltage drop across the pass transistor is higher than the configurable $\Delta V_{SD(FLT)}$ fault threshold, the internal pull-down at the $\overline{VDSFLT}$ pin and the $\overline{PWRFLT1}$ or $\overline{PWRFLT2}$ pin corresponding to the faulting channel turns on. The $\Delta V_{SD(FLT)}$ threshold is configured by the SET pin. Tying SET to GND, tying SET to a 100k resistor connected to GND, or floating SET configures $\Delta V_{SD(FLT)}$ to 250mV, 500mV, or 1.5V respectively.

Fault conditions that may cause a high voltage across the pass transistor include: a MOSFET open on the higher supply, excessive MOSFET current due to overcurrent on the load or a shorted MOSFET on the lower supply. During startup or when a switchover between supplies occurs, the $\overline{VDSFLT}$ pin and $\overline{PWRFLT1}$ or $\overline{PWRFLT2}$ pin may momentarily indicate that the forward voltage has exceeded the programmed threshold during the short interval when the MOSFET gate ramps up and the body diode conducts.

The $\overline{PWRFLT}$ pins are additionally used to indicate if either input supply is below its normal regulation range. If the voltage at the MON1 or MON2 pin is less than $V_{MON(TH)}$, typically 1.23V, the corresponding $\overline{PWRFLT1}$ or $\overline{PWRFLT2}$ pin will pull low. A resistive divider connected to the input supply drives the MON pin for the corresponding supply, configuring the $\overline{PWRFLT}$ threshold for that supply. Be sure to account for the tolerance of the MON pin threshold, the resistor tolerances, and the regulation range of the supply being monitored. Also, ensure that the voltage on the MON pin will not exceed 7V.

The $\overline{FUSEFLT}$ pins are used to indicate the status of the input fuses. If one of the IN pins falls below $V_{INx(TH)}$, typically 3.5V, the $\overline{FUSEFLT}$ pin corresponding to that supply will pull low. The IN pins each sink a minimum of 0.5mA, enough to pull the pin low after an input fuse blows open. If there is a possibility that the MOSFET leakage current can be greater than 0.5mA, a resistor can be connected between the IN pin and GND to sink more current. Note that if the input supply voltage is less than $V_{INx(TH)}$ the $\overline{FUSEFLT}$ pin will pull low.

Table 1. Fault Table

$\Delta V_{SD1} < \Delta V_{SD(FLT)}$	$V_{IN1} > 3.5V$	$V_{MON1} > 1.23V$	$\overline{VDSFLT}$*	$\overline{FUSEFLT1}$	$\overline{PWRFLT1}$
True	True	True	Hi-Z	Hi-Z	Hi-Z
True	True	False	Hi-Z	Hi-Z	Pull-Down
True	False	True	Hi-Z	Pull-Down	Hi-Z
True	False	False	Hi-Z	Pull-Down	Pull-Down
False	True	True	Pull-Down	Hi-Z	Pull-Down
False	True	False	Pull-Down	Hi-Z	Pull-Down
False	False	True	Pull-Down	Pull-Down	Pull-Down
False	False	False	Pull-Down	Pull-Down	Pull-Down

*$\Delta V_{SD2} < \Delta V_{SD(FLT)}$

APPLICATIONS INFORMATION

System Power Supply Failure

The LTC4355 automatically supplies load current from the system input supply with the higher voltage. If this supply shorts to ground, reverse current begins to flow through the pass transistor temporarily and the transistor begins to turn off. When this reverse current creates –25mV of voltage drop across the drain and source pins of the pass transistor, a fast pull-down circuit engages to drive the gate low faster.

The remaining system power supply delivers the load current through the body diode of its pass transistor until the channel turns on. The LTC4355 ramps the gate up with 20µA, turning on the N-channel MOSFET to reduce the voltage drop across it.

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/µs or higher.

High slew rates coupled with parasitic inductances in series with the input and output paths may cause potentially destructive transients to appear at the IN and OUT pins of the LTC4355 during reverse recovery. A zero impedance short-circuit directly across an input that is supplying current is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the MOSFET finally commutates the reverse current the LTC4355 IN pin experiences a negative voltage spike, while the OUT pin spikes in the positive direction.

To prevent damage to the LTC4355 under conditions of input short-circuit, protect the IN pins and OUT pin as shown in Figure 1. The IN pins are protected by clamping to the GND pin in the negative direction. Protect the OUT pin with a clamp, such as with a TVS or TransZorb, or with a local bypass capacitor of at least 10µF. In low voltage applications the MOSFET's drain-source breakdown may be sufficient to protect the OUT pin, provided BV_{DSS} + V_{IN} < 100V.

Parasitic inductance between the load bypass or the second supply and the LTC4355 allows a zero impedance input short to collapse the voltage at the OUT pin, which increases the total turn-off time (t_{OFF}). For applications up to 30V, bypass the OUT pin with 39µF; above 30V use at least 100µF. One capacitor serves to guard against OUT collapse and also protect OUT from voltage spikes.

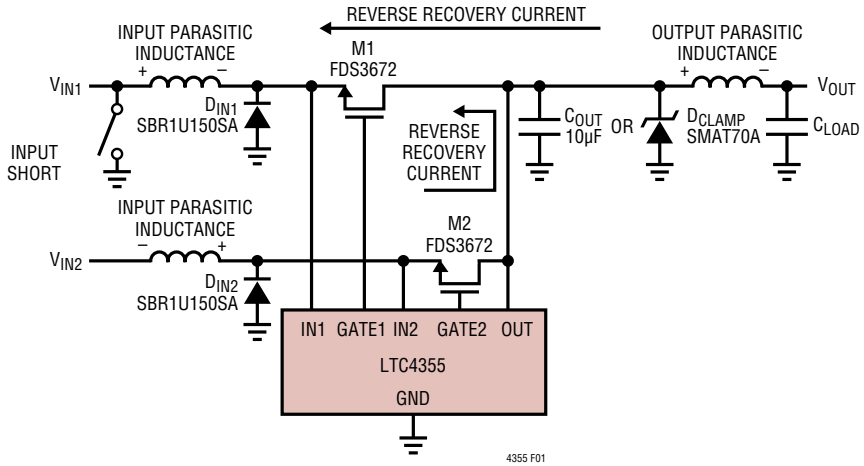


Figure 1. Reverse Recovery Produces Inductive Spikes at the IN and OUT Pins. The Polarity of Step Recovery Spikes Is Shown Across Parasitic Inductances

APPLICATIONS INFORMATION

Loop Stability

The servo loop is compensated by the parasitic capacitance of the power N-channel MOSFET. No further compensation components are normally required. In the case when a MOSFET with less than 1000pF gate capacitance is chosen, a 1000pF compensation capacitor connected across the gate and source pins might be required.

Design Example

The following design example demonstrates the calculations involved for selecting components in a 36V to 72V system with 5A maximum load current (see Figure 2).

First, choose the N-channel MOSFET. The 100V, FDS3672 in the SO-8 package with $R_{DS(ON)}$ = 22mΩ(max) offers a good solution. The maximum voltage drop across it is:

$\Delta V = 5A \bullet 22m\Omega = 110mV$

The maximum power dissipation in the MOSFET is a mere:

$P = 5A \bullet 110mV = 0.55W$

Next, select the resistive dividers that guarantee the $\overline{PWRFLT}$ pins will not assert when the input supplies are above 36V. The maximum $V_{MONx(TH)}$ is 1.245V and the maximum $I_{MONx(IN)}$ is 1µA. Choose a 1% tolerance resistor R1 = 12.7k. Then,

$$I_{R2} = \frac{V_{MONx(TH)}}{R1(MIN)} + I_{MONx(TH)(MAX)}$$

$$= \frac{1.245V}{12.7k\Omega(-1\%)} + 1\mu A = 100\mu A$$

Use I_{R2} to choose R2.

$$R2 = \frac{36V - 1.245V}{100\mu A} = 348k\Omega$$

Adjust R2 down by 1% to 344k to account for its tolerance. The next lower standard resistor value is R2 = 340k.

The LED D1, a Panasonic Green LN1351C, requires at least 1mA of current to fully turn on. Therefore, R5 is set to 33k to accommodate the lowest input supply voltage of 36V.

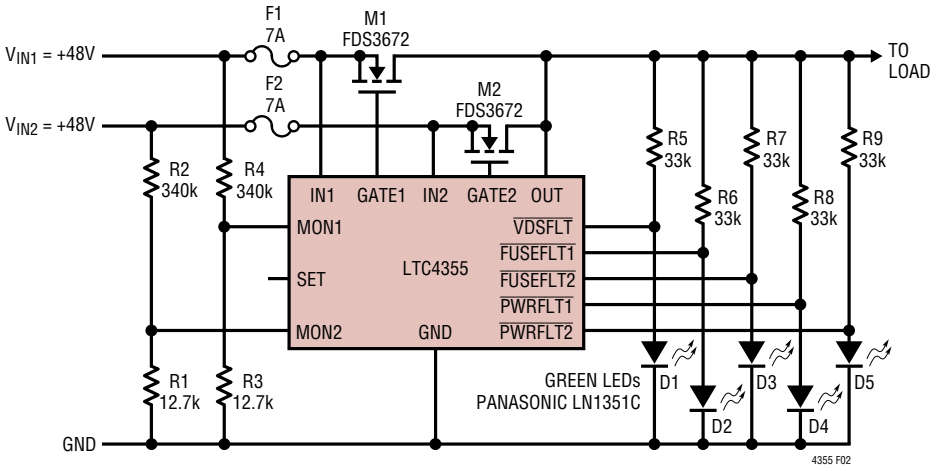


Figure 2. 36V to 72V/5A Design Example

APPLICATIONS INFORMATION

Layout Considerations

The following advice should be considered when laying out a printed circuit board for the LTC4355.

The inputs to the servo amplifiers, IN1, IN2, and OUT should be connected as closely as possible to the MOSFETs' terminals for good accuracy.

Keep the traces to the MOSFETs wide and short. The PCB traces associated with the power path through the MOSFETs should have low resistance (see Figure 3).

For the DFN package, pin spacing may be a concern at voltages greater than 30V. Check creepage and clearance guidelines to determine if this is an issue. Use no-clean solder to minimize PCB contamination.

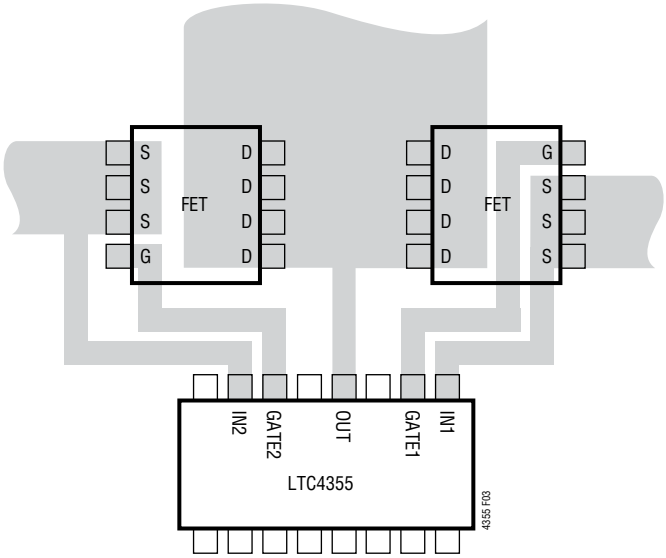
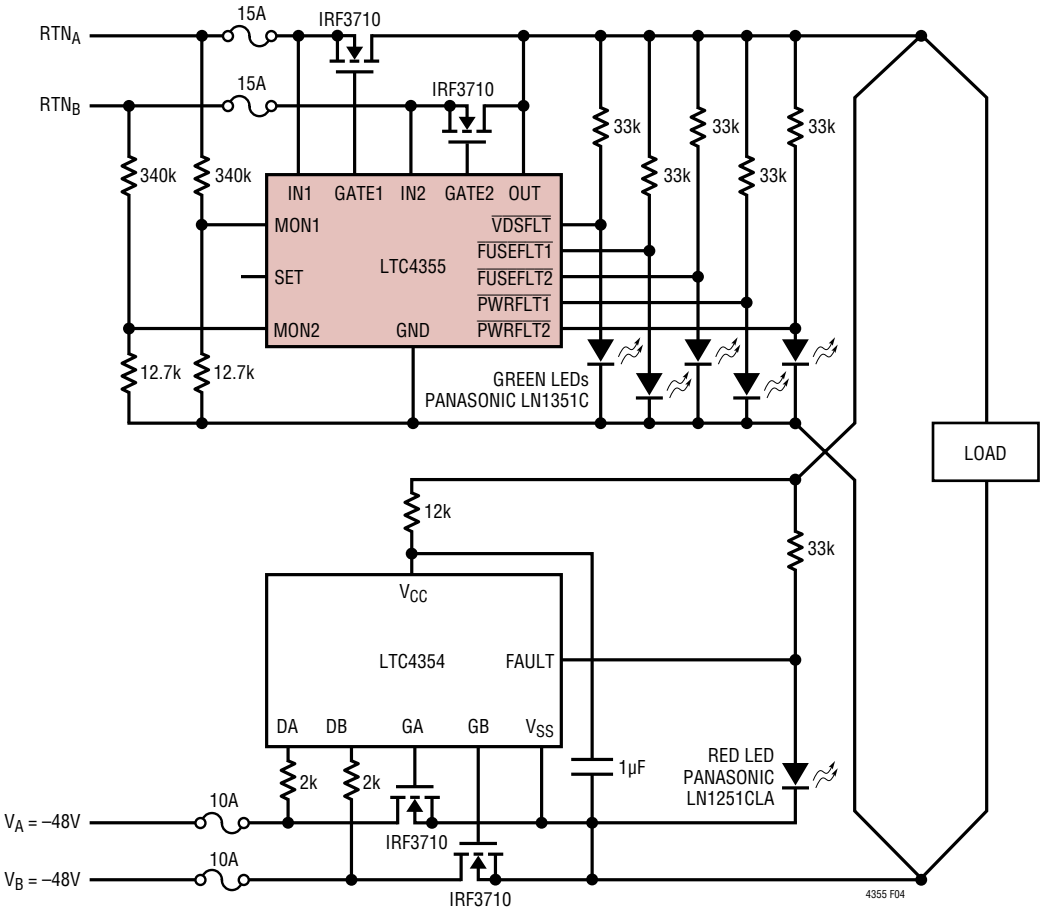


Figure 3. Layout Considerations

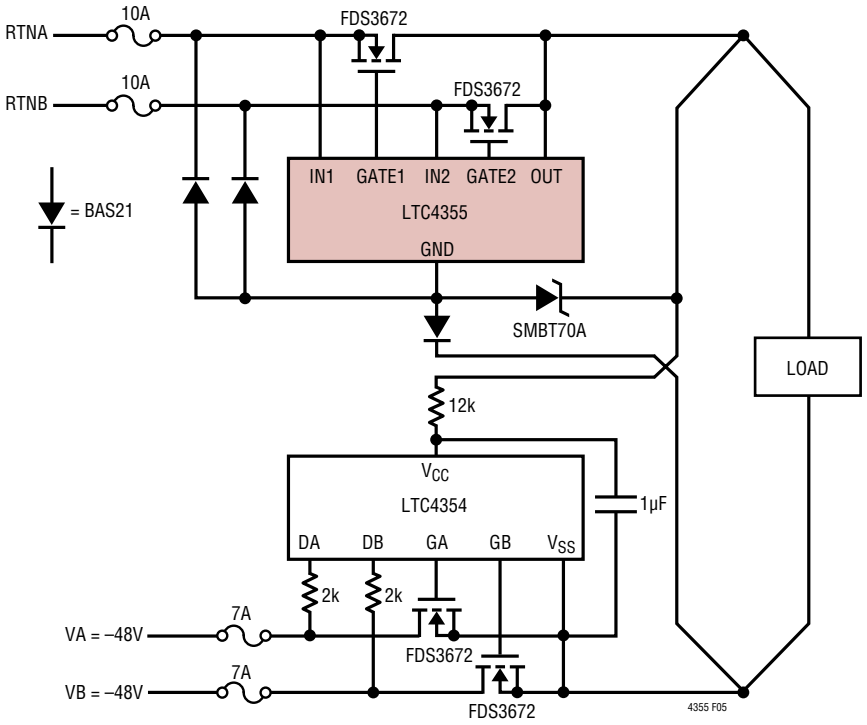
TYPICAL APPLICATIONS

–36V to –72V/10A with Positive Supply and Negative Supply Diode-ORing



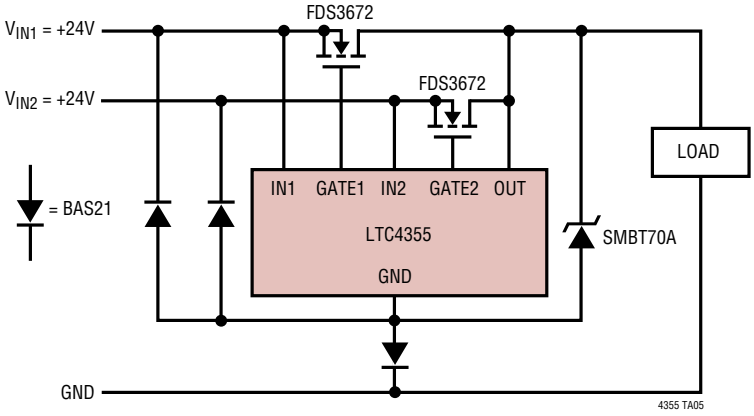
TYPICAL APPLICATIONS

–48V/5A with Positive Supply and Negative Supply Diode-ORing with Reverse Input Protection



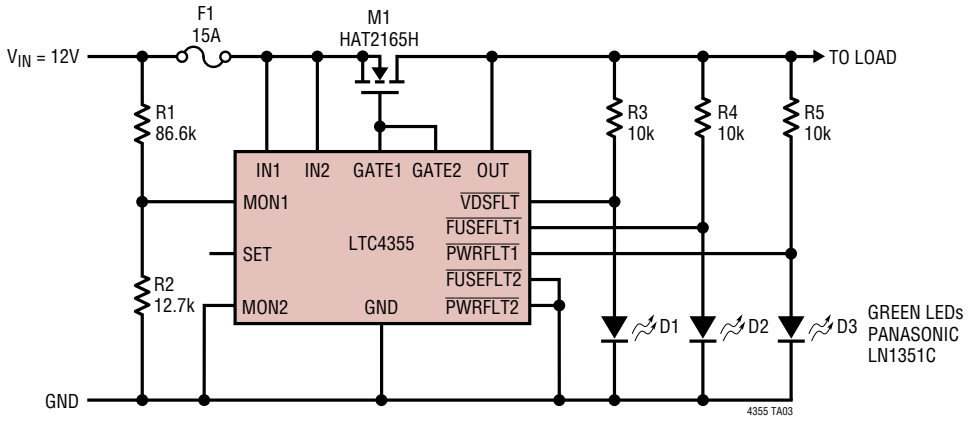
NOTE: MAXIMUM VOLTAGE BETWEEN ANY TWO INPUTS = $80V_{DC}$

+24V Diode-OR With Reverse Input Protection

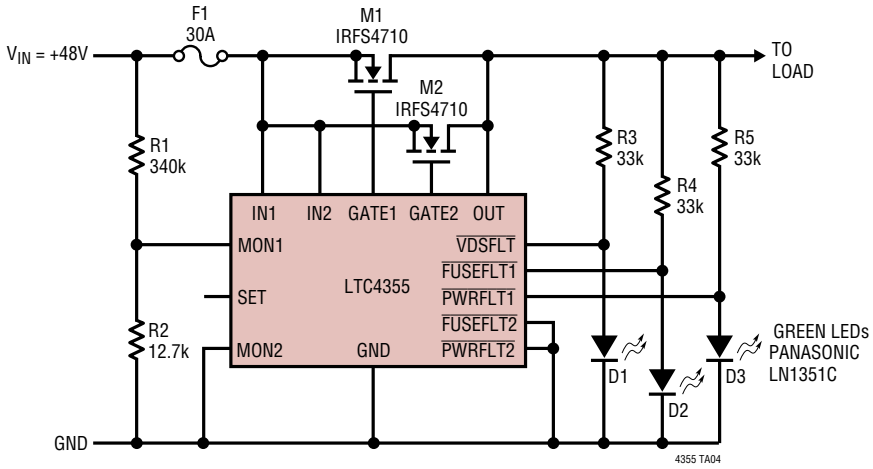


TYPICAL APPLICATIONS

Single 12V/15A Ideal Diode with Parallel Drivers

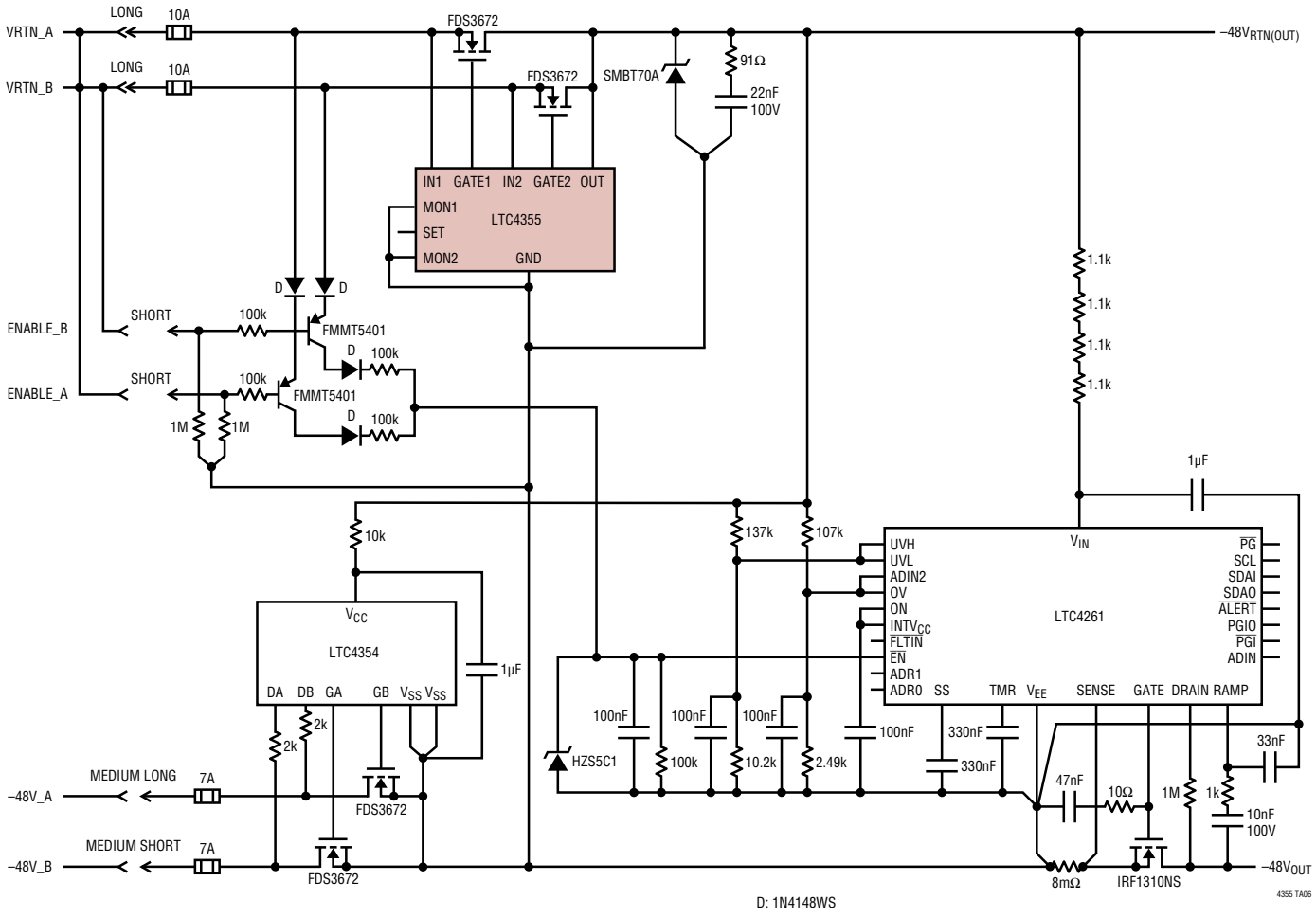


Single 36V to 72V/30A Ideal Diode Using Parallel MOSFETs



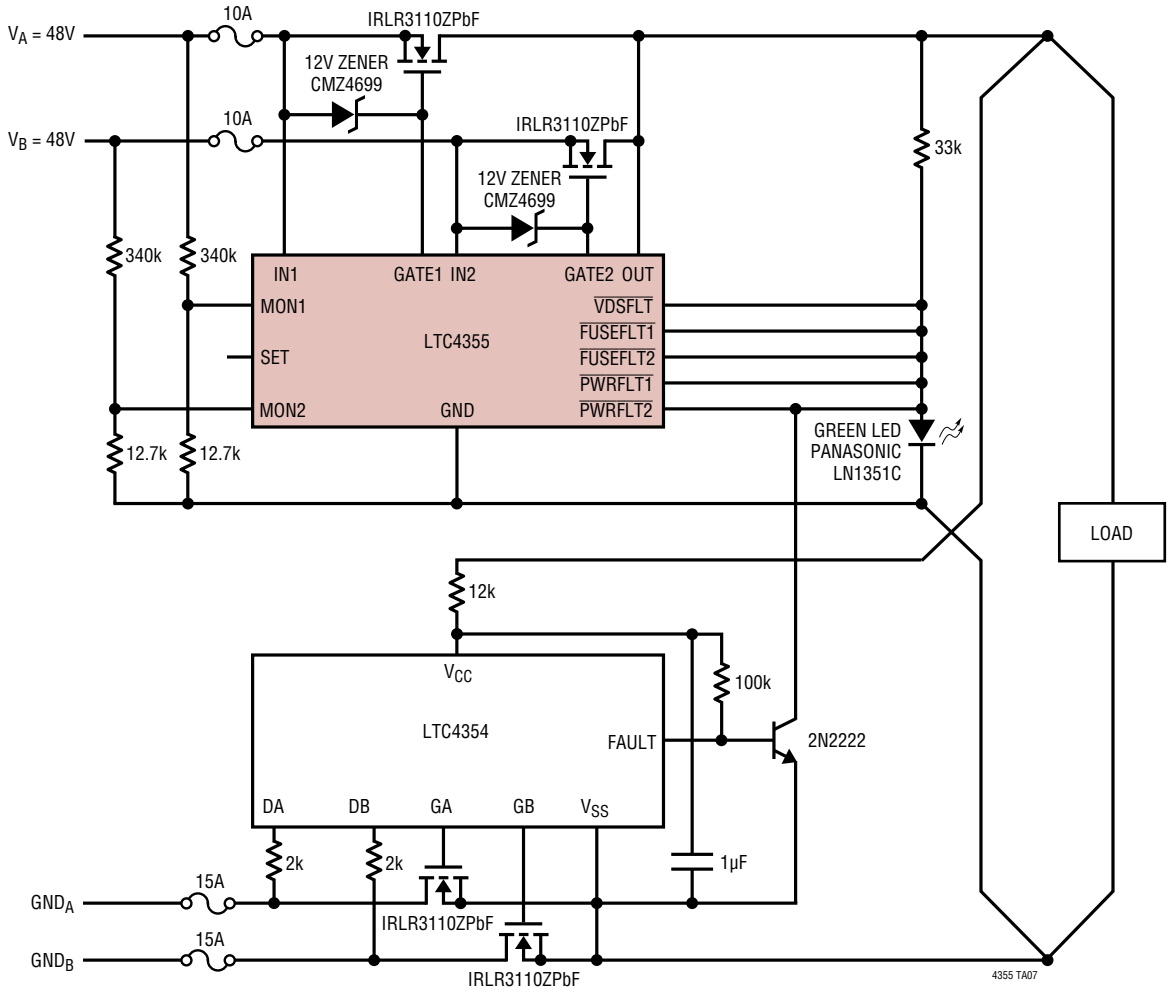
TYPICAL APPLICATIONS

AdvancedTCA with High Side and Low Side Ideal Diode-OR and Hot Swap™ Controller with I²C Current and Voltage Monitor



TYPICAL APPLICATIONS

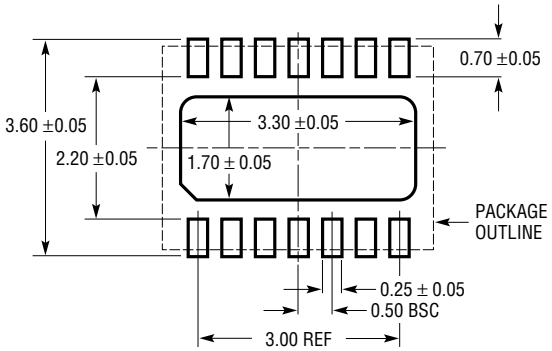
36V to 72V/10A with Positive Supply and Negative Supply Diode-ORing, Combined Fault Outputs, and Zener Clamps on MOSFET Gates



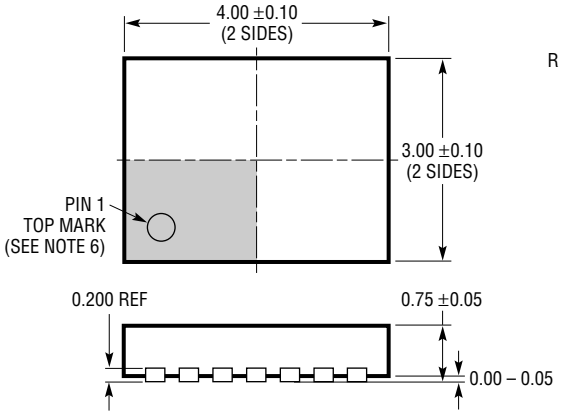
PACKAGE DESCRIPTION

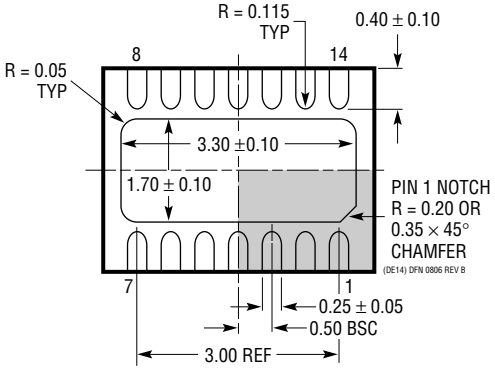
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





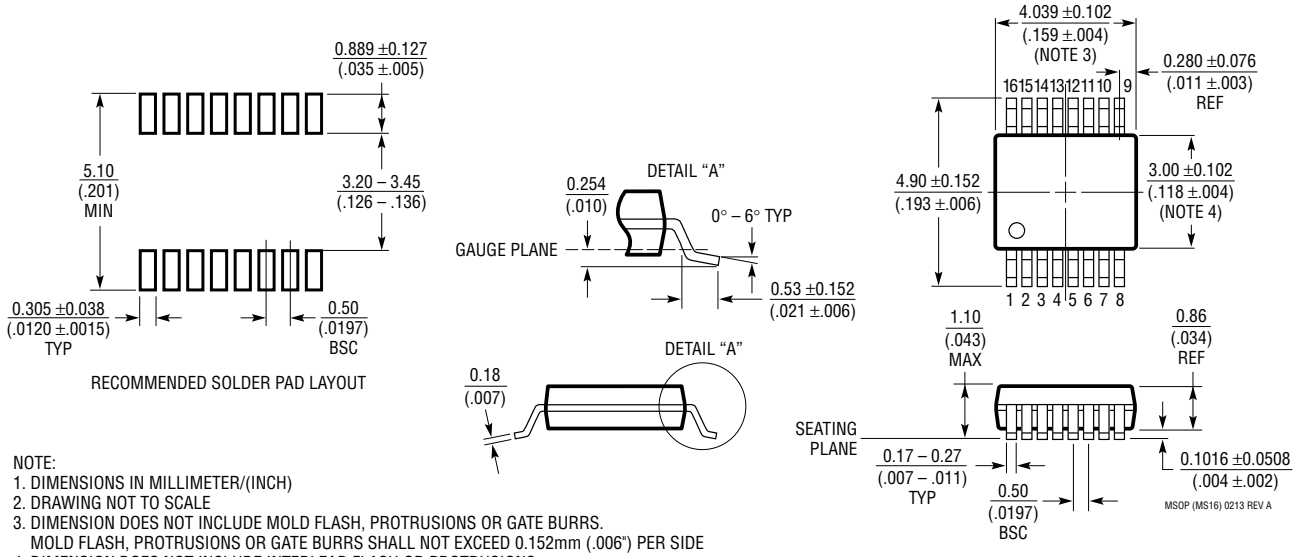
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

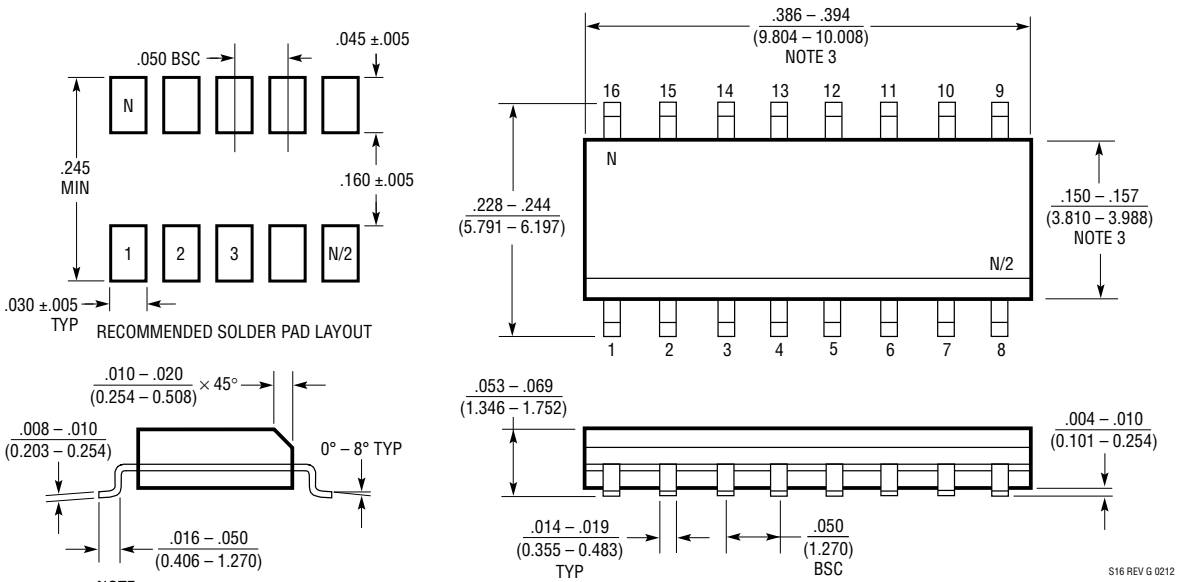
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

REVISION HISTORY (Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	2/10	Updated Features section and removed patent	1
		Revised t_{OFF} conditions	3
		Revised NC pin description	5
		Revised Typical Application drawings	13, 15, 16
		Corrected part number LTC4352 in Related Parts	20
F	8/13	Added H-grade (LTC4355H) information	2
		Changed θ_{JA}: MS package from 125°C/W to 120°C/W, S package from 75°C/W to 80°C/W	2
		Swapped ampere ratings between the two sets of fuses	12