Positive High Voltage Ideal Diode Controller

FEATURES

- **Reduces Power Dissipation by Replacing a Power Schottky Diode with an N-Channel MOSFET**
- **0.5µs Turn-Off Time Limits Peak Fault Current**
- **Wide Operating Voltage Range: 9V to 80V**
- Smooth Switchover without Oscillation
- No Reverse DC Current
- Available in 6-Lead (2mm × 3mm) DFN and 8-Lead MSOP Packages

APPLICATIONS

- N + 1 Redundant Power Supplies
- High Availability Systems
- AdvancedTCA Systems
- Telecom Infrastructure
- Automotive Systems

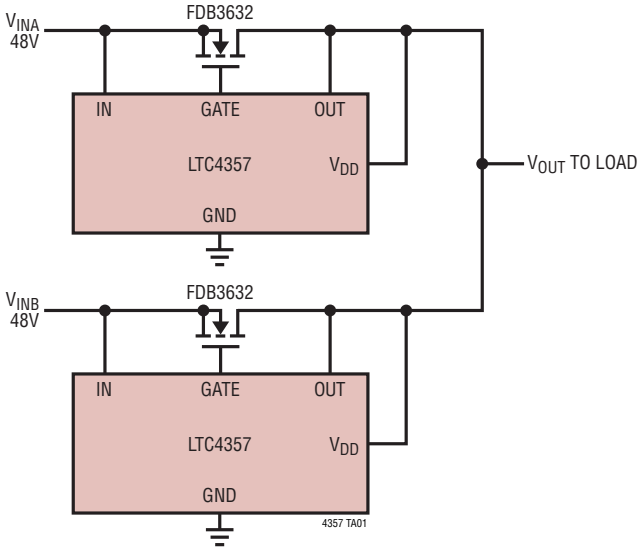
DESCRIPTION

The LTC®4357 is a positive high voltage ideal diode controller that drives an external N-channel MOSFET to replace a Schottky diode. When used in diode-OR and high current diode applications, the LTC4357 reduces power consumption, heat dissipation, voltage loss and PC board area.

The LTC4357 easily ORs power sources to increase total system reliability. In diode-OR applications, the LTC4357 controls the forward voltage drop across the MOSFET to ensure smooth current transfer from one path to the other without oscillation. If the power source fails or is shorted, a fast turn-off minimizes reverse current transients.

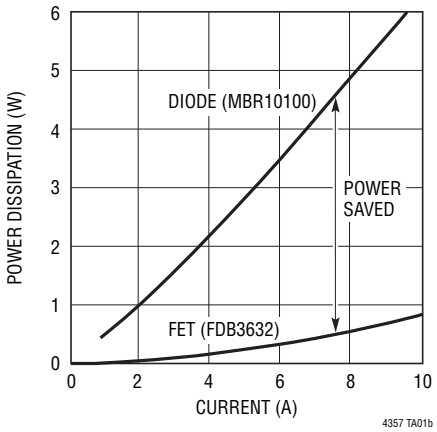
TYPICAL APPLICATION

48V, 10A Diode-OR



*SEE FIGURES 2 AND 3 FOR ADDITIONAL OPTIONAL COMPONENTS

Power Dissipation vs Load Current



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages
- IN ..... –1V to 100V
- OUT, V_{DD} ..... –0.3V to 100V

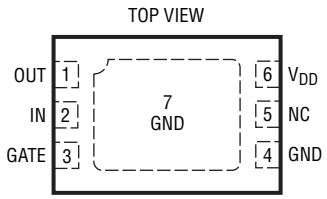
Output Voltage
- GATE (Note 3) ..... V_{IN} – 0.2V to V_{IN} + 10V

Operating Ambient Temperature Range
- LTC4357C ..... 0°C to 70°C
- LTC4357I ..... –40°C to 85°C
- LTC4357H ..... –40°C to 125°C
- LTC4357MP ..... –55°C to 125°C

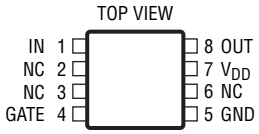
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- MS Package ..... 300°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLATIC DFN
T_{JMAX} = 125°C, θ_{JA} = 90°C/W
EXPOSED PAD (PIN 7) PCB GND CONNECTION OPTIONAL



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 163°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4357CMS8#PBF	LTC4357CMS8#TRPBF	LTCXD	8-Lead Plastic MSOP	0°C to 70°C
LTC4357IMS8#PBF	LTC4357IMS8#TRPBF	LTCXD	8-Lead Plastic MSOP	–40°C to 85°C
LTC4357HMS8#PBF	LTC4357HMS8#TRPBF	LTCXD	8-Lead Plastic MSOP	–40°C to 125°C
LTC4357MPMS8#PBF	LTC4357MPMS8#TRPBF	LTFWZ	8-Lead Plastic MSOP	–55°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4357MPMS8	LTC4357MPMS8#TR	LTFWZ	8-Lead Plastic MSOP	–55°C to 125°C

LEAD FREE FINISH TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4357CDCB#TRMPBF	LTC4357CDCB#TRPBF	LCXF	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC4357IDCB#TRMPBF	LTC4357IDCB#TRPBF	LCXF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4357HDCB#TRMPBF	LTC4357HDCB#TRPBF	LCXF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = V_{DD}, V_{DD} = 9V to 80V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Operating Supply Range		●	9		80	V
I_{DD}	Supply Current		●		0.5	1.25	mA
I_{IN}	IN Pin Current	V_{IN} = V_{OUT} ±1V	●	150	350	500	µA
I_{OUT}	OUT Pin Current	V_{IN} = V_{OUT} ±1V	●		80	210	µA
ΔV_{GATE}	External N-Channel Gate Drive (V_{GATE} – V_{IN})	V_{DD}, V_{OUT} = 20V to 80V V_{DD}, V_{OUT} = 9V to 20V	● ●	10 4.5	12 6	15 15	V V
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	V_{GATE} = V_{IN}, V_{IN} – V_{OUT} = 0.1V	●	–14	–20	–26	µA
$I_{GATE(DOWN)}$	External N-Channel Gate Pull-Down Current in Fault Condition	V_{GATE} = V_{IN} + 5V	●	1	2		A
t_{OFF}	Gate Turn-Off Time	V_{IN} – V_{OUT} = 55mV ⎾–1V, V_{GATE} – V_{IN} < 1V, C_{GATE} = 0pF	●		300	500	ns
ΔV_{SD}	Source-Drain Regulation Voltage (V_{IN} – V_{OUT})	V_{GATE} – V_{IN} = 2.5V	●	10	25	55	mV

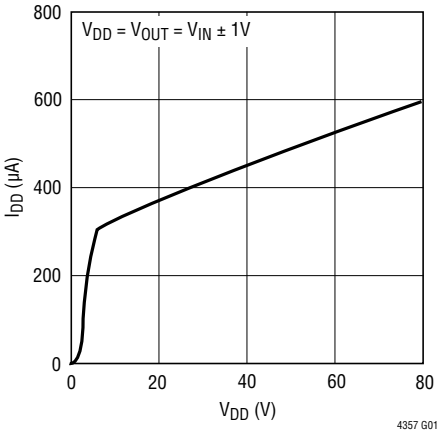
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

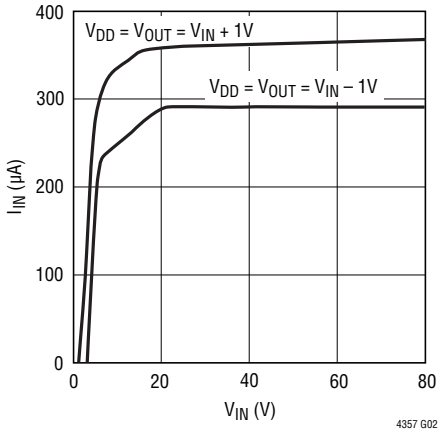
Note 3: An internal clamp limits the GATE pin to a minimum of 10V above IN or 100V above GND. Driving this pin to voltages beyond this clamp may damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

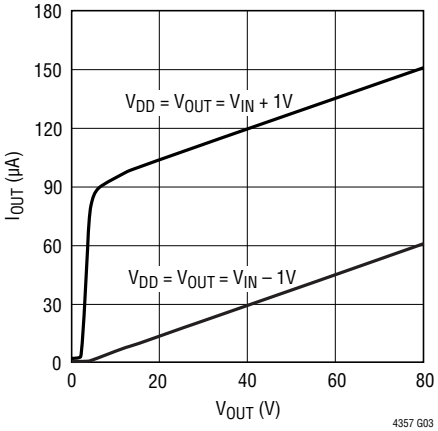
V_{DD} Current (I_{DD} vs V_{DD})



IN Current (I_{IN} vs V_{IN})

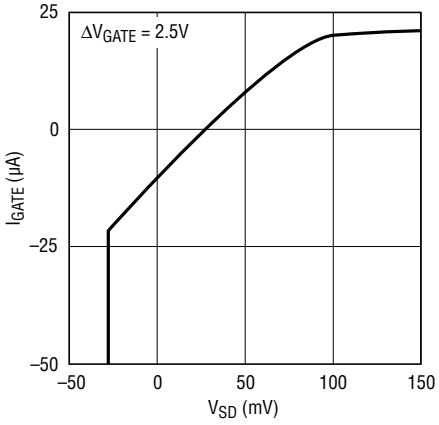


OUT Current (I_{OUT} vs V_{OUT})



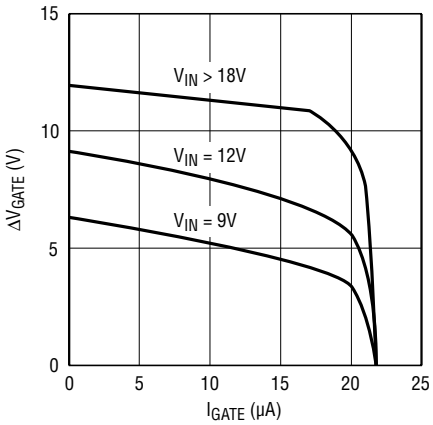
TYPICAL PERFORMANCE CHARACTERISTICS

GATE Current vs Forward Drop (I_{GATE} vs ΔV_{SD})



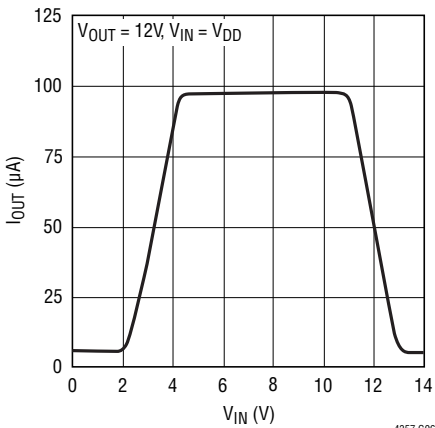
4357 G04

ΔV_{GATE} vs GATE Current (ΔV_{GATE} vs I_{GATE})



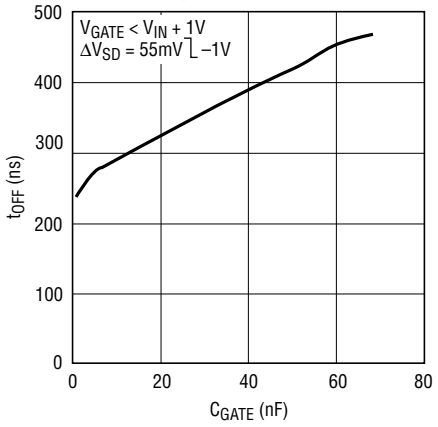
4357 G05

OUT Current (I_{OUT} vs V_{IN})



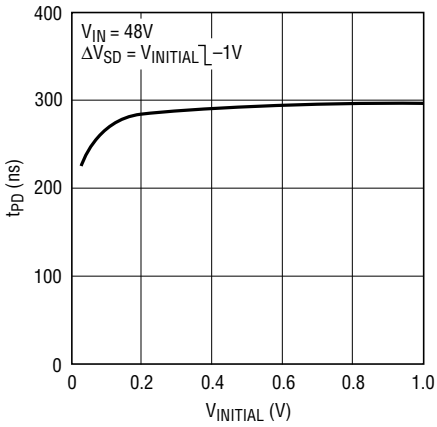
4357 G06

FET Turn-Off Time vs GATE Capacitance



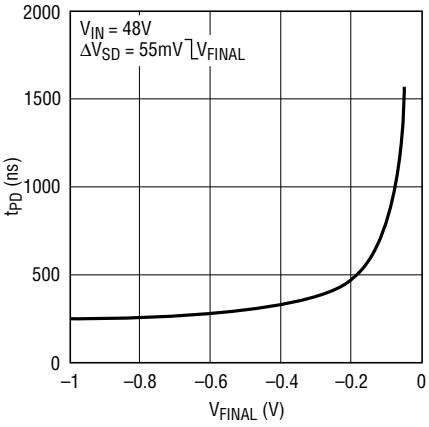
4357 G07

FET Turn-Off Time vs Initial Overdrive



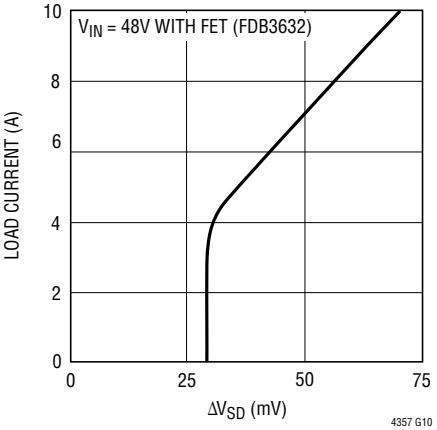
4357 G08

FET Turn-Off Time vs Final Overdrive



4357 G09

FET Load Current vs ΔVSD



4357 G10

PIN FUNCTIONS

Exposed Pad: Exposed pad may be left open or connected to GND.

GATE: Gate Drive Output. The GATE pin pulls high, enhancing the N-channel MOSFET when the load current creates more than 25mV of voltage drop across the MOSFET. When the load current is small, the gate is actively driven to maintain 25mV across the MOSFET. If reverse current develops more than –25mV of voltage drop across the MOSFET, a fast pull-down circuit quickly connects the GATE pin to the IN pin, turning off the MOSFET.

GND: Device Ground.

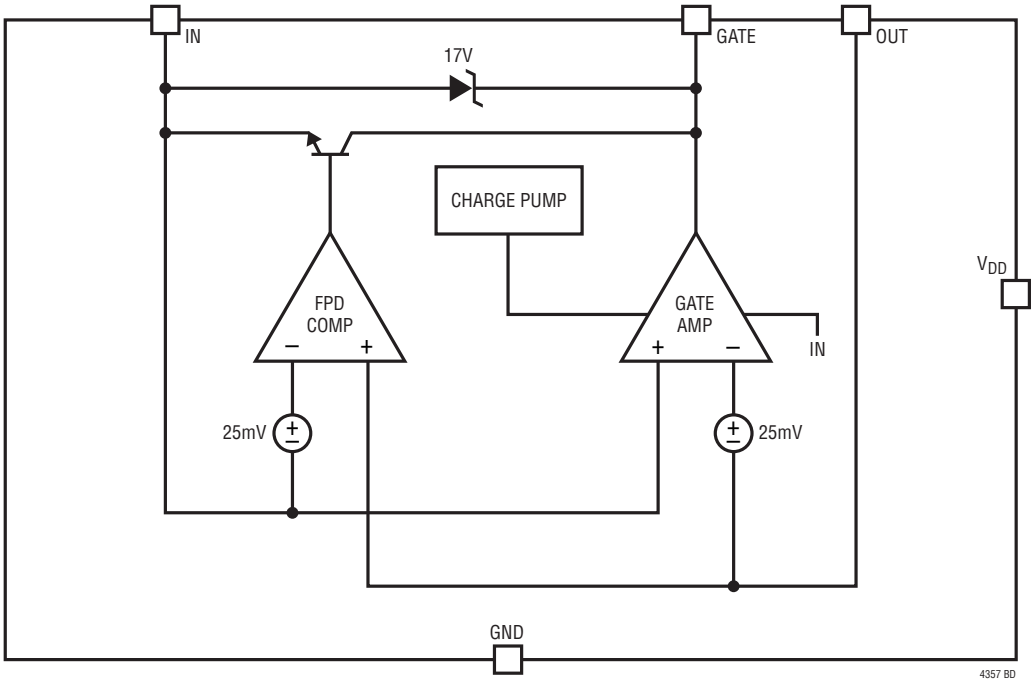
IN: Input Voltage and GATE Fast Pull-Down Return. IN is the anode of the ideal diode and connects to the source of the N-channel MOSFET. The voltage sensed at this pin is used to control the source-drain voltage across the MOSFET. The GATE fast pull-down current is returned through the IN pin. Connect this pin as close as possible to the MOSFET source.

NC: No Connection. Not internally connected.

OUT: Drain Voltage Sense. OUT is the cathode of the ideal diode and the common output when multiple LTC4357s are configured as an ideal diode-OR. It connects to the drain of the N-channel MOSFET. The voltage sensed at this pin is used to control the source-drain voltage across the MOSFET.

V_{DD}: Positive Supply Input. The LTC4357 is powered from the V_{DD} pin. Connect this pin to OUT either directly or through an RC hold-up circuit.

BLOCK DIAGRAM



OPERATION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. ORing diodes have been a popular means of connecting these supplies at the point of load. The disadvantage of this approach is the forward voltage drop and resulting efficiency loss. This drop reduces the available supply voltage and dissipates significant power. Using an N-channel MOSFET to replace a Schottky diode reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layouts in high power applications.

The LTC4357 controls an external N-channel MOSFET to form an ideal diode. The voltage across the source and drain is monitored by the IN and OUT pins, and the GATE pin drives the MOSFET to control its operation. In effect the MOSFET source and drain serve as the anode and cathode of an ideal diode.

At power-up, the load current initially flows through the body diode of the MOSFET. The resulting high forward voltage is detected at the IN and OUT pins, and the LTC4357 drives the GATE pin to servo the forward drop to 25mV. If the load current causes more than 25mV of voltage drop when the MOSFET gate is driven fully on, the forward voltage is equal to $R_{DS(ON)} \bullet I_{LOAD}$.

If the load current is reduced causing the forward drop to fall below 25mV, the MOSFET gate is driven lower by a weak pull-down in an attempt to maintain the drop at 25mV. If the load current reverses and the voltage across IN to OUT is more negative than –25mV the LTC4357 responds by pulling the MOSFET gate low with a strong pull-down.

In the event of a power supply failure, such as if the output of a fully loaded supply is suddenly shorted to ground, reverse current temporarily flows through the MOSFET that is on. This current is sourced from any load capacitance and from the other supplies. The LTC4357 quickly responds to this condition turning off the MOSFET in about 500ns, thus minimizing the disturbance to the output bus.

APPLICATIONS INFORMATION

MOSFET Selection

The LTC4357 drives an N-channel MOSFET to conduct the load current. The important features of the MOSFET are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, V_{DSS}, and the gate threshold voltage.

Gate drive is compatible with 4.5V logic-level MOSFETs in low voltage applications (V_{DD} = 9V to 20V). At higher voltages (V_{DD} = 20V to 80V) standard 10V threshold MOSFETs may be used. An internal clamp limits the gate drive to 15V between the GATE and IN pins. An external Zener clamp may be added between GATE and IN for MOSFETs with a $V_{GS(MAX)}$ of less than 15V.

The maximum allowable drain-source voltage, BV_{DSS}, must be higher than the power supply voltage. If an input is connected to GND, the full supply voltage will appear across the MOSFET.

ORing Two-Supply Outputs

Where LTC4357s are used to combine the outputs of two power supplies, the supply with the highest output voltage sources most or all of the load current. If this supply's output is quickly shorted to ground while delivering load current, the flow of current temporarily reverses and flows backwards through the LTC4357's MOSFET. When the reverse current produces a voltage drop across the MOSFET of more than –25mV, the LTC4357's fast pull-down activates and quickly turns off the MOSFET.

If the other, initially lower, supply was not delivering load current at the time of the fault, the output falls until the body diode of its ORing MOSFET conducts. Meanwhile, the LTC4357 charges its MOSFET gate with 20µA until the forward drop is reduced to 25mV. If instead this supply was delivering load current at the time of the fault, its associated ORing MOSFET was already driven at least partially on, and the LTC4357 will simply drive the MOSFET gate harder in an effort to maintain a drop of 25mV.

APPLICATIONS INFORMATION

Load Sharing

The application in Figure 1 combines the outputs of multiple, redundant supplies using a simple technique known as droop sharing. Load current is first taken from the highest output, with the low outputs contributing as the output voltage falls under increased loading. The 25mV regulation technique ensures smooth load sharing between outputs without oscillation. The degree of sharing is a function of $R_{DS(ON)}$, the output impedance of the supplies and their initial output voltages.

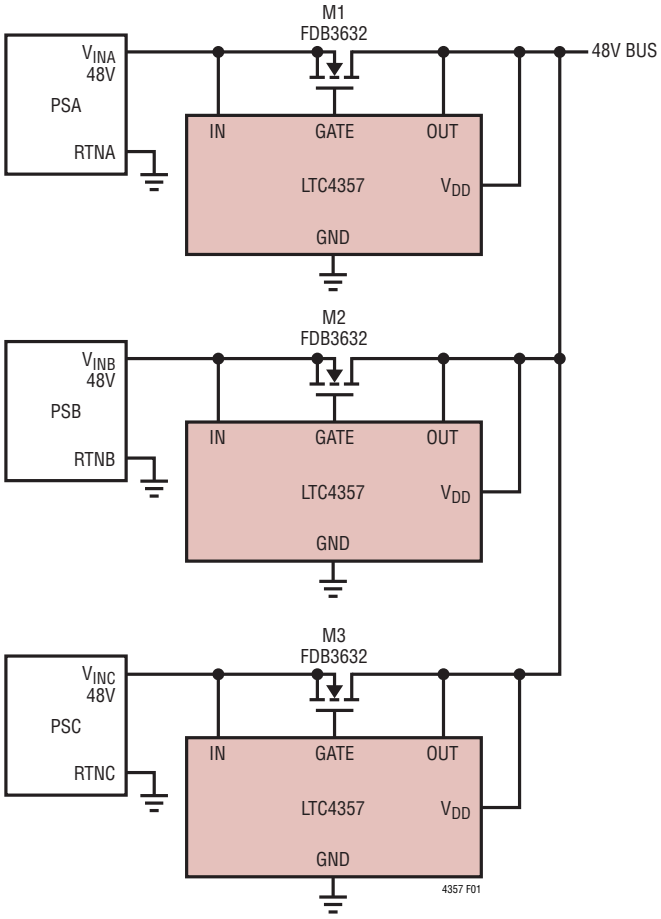


Figure 1. Droop Sharing Redundant Supplies

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/µs or higher.

High slew rates coupled with parasitic inductances in series with the input and output paths may cause potentially destructive transients to appear at the IN and OUT pins of the LTC4357 during reverse recovery. A zero impedance short-circuit directly across the input of the circuit is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the MOSFET finally commutates the reverse current the LTC4357 IN pin experiences a negative voltage spike, while the OUT pin spikes in the positive direction.

To prevent damage to the LTC4357 under conditions of input short-circuit, protect the IN pin and OUT pin as shown in Figure 2. The IN pin is protected by clamping to the GND pin in the negative direction. Protect the OUT pin with a clamp, such as with a TVS or TransZorb, or with a local bypass capacitor of at least 10µF. In low voltage applications the MOSFET's drain-source breakdown may be sufficient to protect the OUT pin, provided $BV_{DSS} + V_{IN} < 100V$.

Parasitic inductance between the load bypass and the LTC4357 allows a zero impedance input short to collapse the voltage at the V_{DD} pin, which increases the total turn-off time (t_{OFF}). For applications up to 30V, bypass the V_{DD} pin with 39µF; above 30V use at least 100µF. If V_{DD} is powered from the output side, one capacitor serves to guard against V_{DD} collapse and also protect OUT from voltage spikes. If the OUT pin is protected by a diode clamp or if V_{DD} is powered from the input side, decouple the V_{DD} pin with a separate 100Ω, 100nF filter (see Figure 3). In applications above 10A increase the filter capacitor to 1µF.

APPLICATIONS INFORMATION

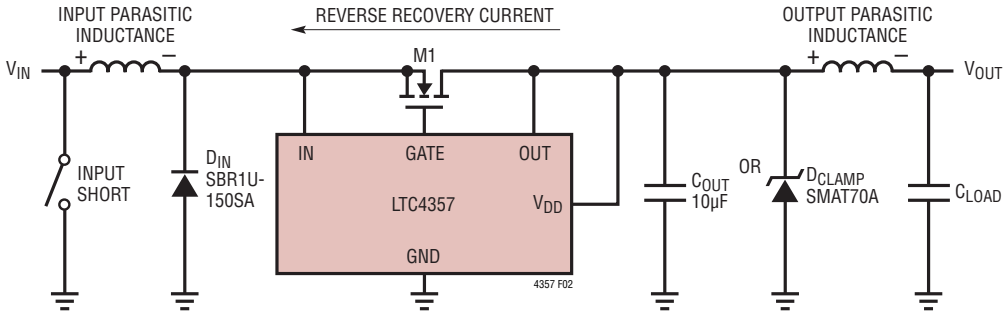


Figure 2. Reverse Recovery Produces Inductive Spikes at the IN and OUT Pin. The Polarity of Step Recovery Spikes is Shown Across Parasitic Inductances

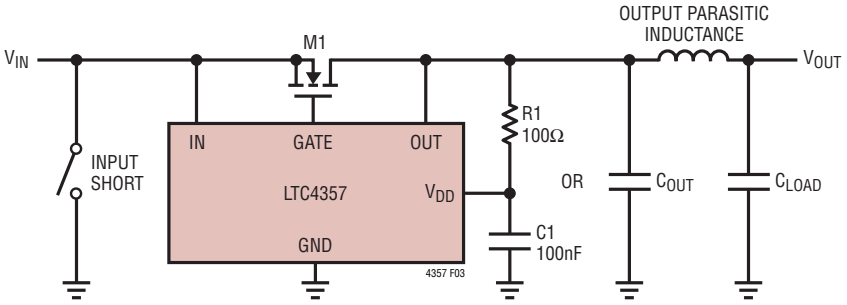


Figure 3. Protecting Against Collapse of V_{DD} During Reverse Recovery

Design Example

The following design example demonstrates the calculations involved for selecting components in a 12V system with 10A maximum load current (see Figure 4).

First, calculate the $R_{DS(ON)}$ of the MOSFET to achieve the desired forward drop at full load. Assuming V_{DROP} = 0.1V,

$$R_{DS(ON)} \leq \frac{V_{DROP}}{I_{LOAD}} = \frac{0.1V}{10A}$$

$$R_{DS(ON)} \leq 10m\Omega$$

The Si4874DY offers a good solution, in an S8 package with $R_{DS(ON)}$ = 10mΩ(max) and BV_{DSS} of 30V.

The maximum power dissipation in the MOSFET is:

$$P = I_{LOAD}^2 \bullet R_{DS(ON)} = (10A)^2 \bullet 10m\Omega = 1W$$

With less than 39µF of local bypass, the recommended RC values of 100Ω and 0.1µF were used in Figure 4.

Since $BV_{DSS} + V_{IN}$ is much less than 100V, output clamping is unnecessary.

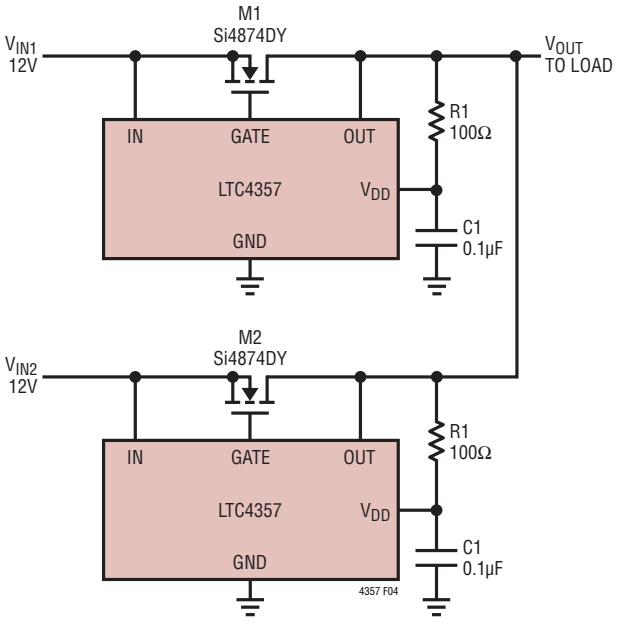


Figure 4. 12V, 10A Diode-OR

APPLICATIONS INFORMATION

Layout Considerations

Connect the IN and OUT pins as close as possible to the MOSFET's source and drain pins. Keep the traces to the MOSFET wide and short to minimize resistive losses. See Figure 5.

For the DFN package, pin spacing may be a concern at voltages greater than 30V. Check creepage and clearance guidelines to determine if this is an issue. To increase the pin spacing between high voltage and ground pins, leave the exposed pad connection open. Use no-clean solder to minimize PCB contamination.

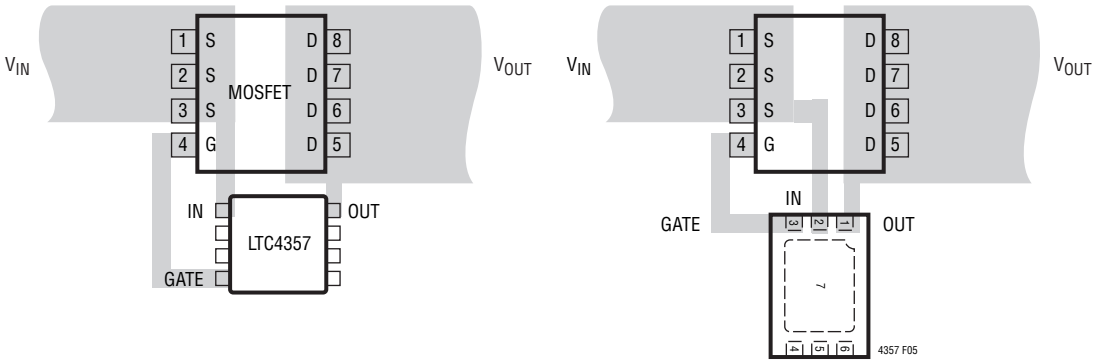
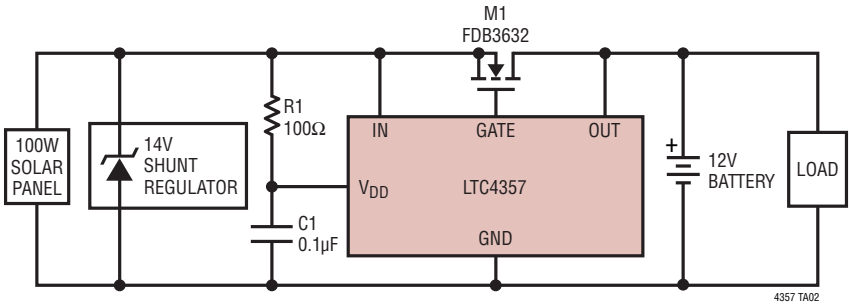


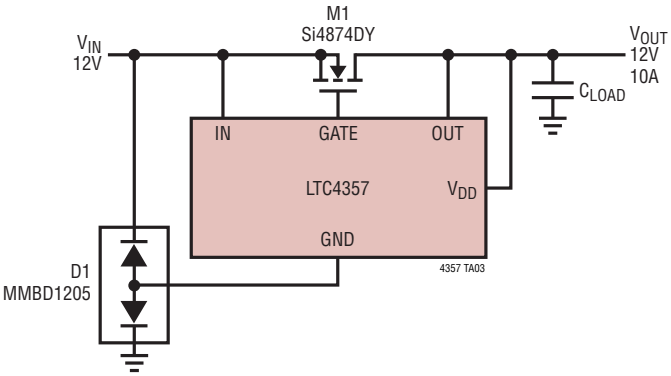
Figure 5. Layout Considerations

TYPICAL APPLICATIONS

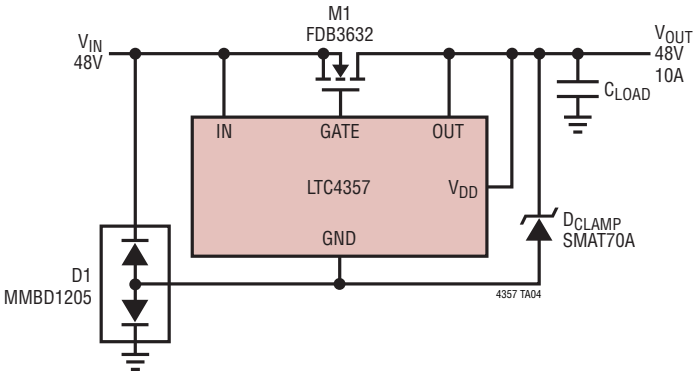
Solar Panel Charging a Battery



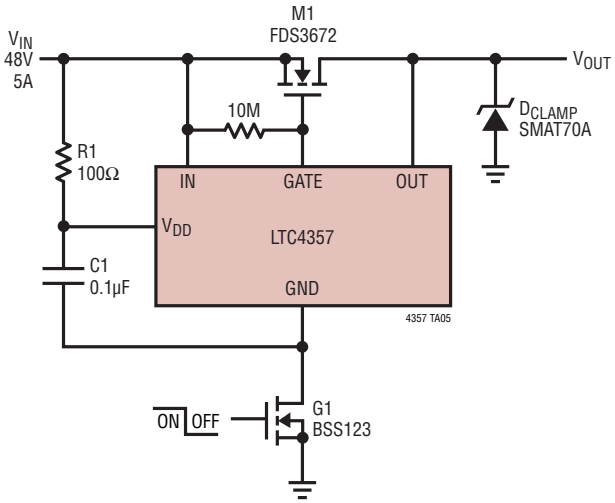
–12V Reverse Input Protection



–48V Reverse Input Protection

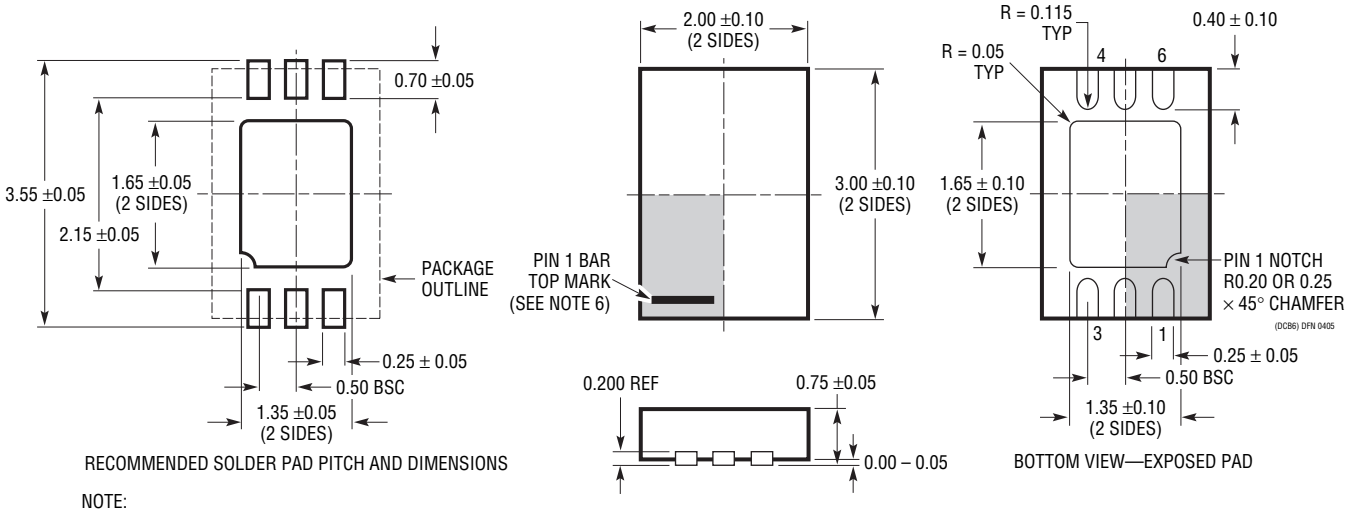


Low Current Shutdown



PACKAGE DESCRIPTION

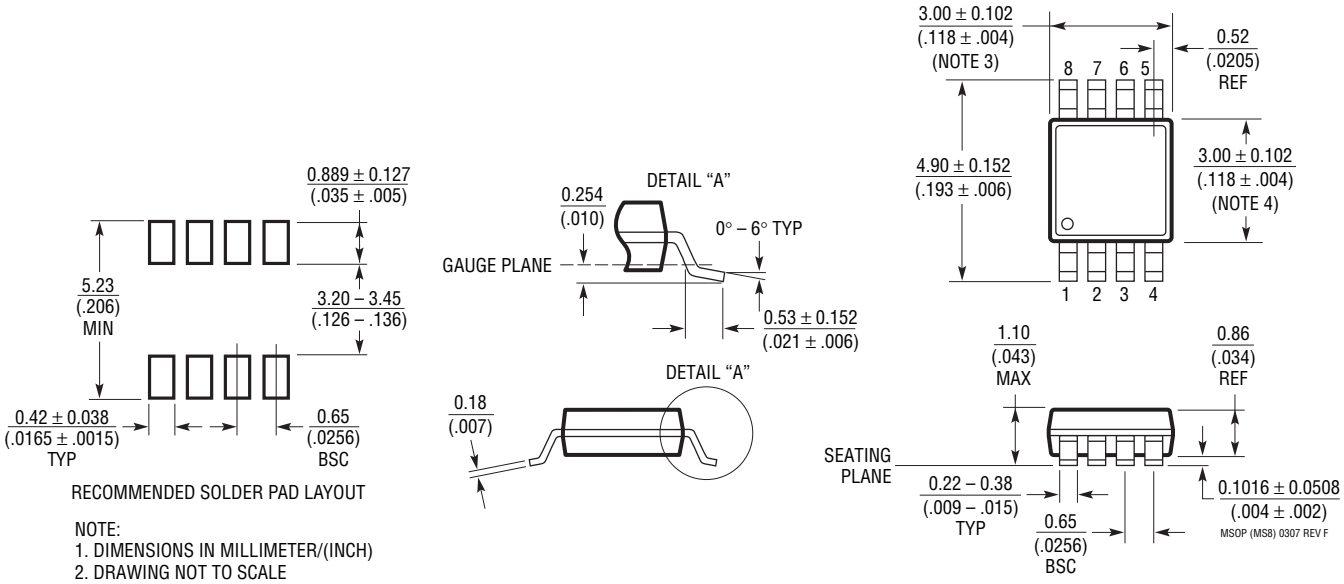
DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	09/10	Revised θ_{JA} value for MS8 package in Pin Configuration section and added MP-grade to Order Information section	2
		Added two new plots and revised remaining curves in Typical Performance Characteristics section	3, 4
		Updated Electrical Characteristics section	4
		Revised Figure 2 and Figure 4 in Applications Information section	8