# Overvoltage/Overcurrent Protection Controller

## FEATURES

- **2.5V to 5.5V Operation**
- **Overvoltage Protection Up to 80V**
- **No Input Capacitor or TVS Required for Most Applications**
- **2% Accurate 5.8V Overvoltage Threshold**
- **10% Accurate 50mV Overcurrent Circuit Breaker**
- **<1µs Overvoltage Turn-Off, Gentle Shutdown**
- Controls N-Channel MOSFET
- Adjustable Power-Up dV/dt Limits Inrush Current
- Reverse Voltage Protection
- Power Good Output
- Low Current Shutdown
- Latchoff (LTC4361-1) or Auto-Retry (LTC4361-2) After Overcurrent
- Available in 8-Lead ThinSOT™ and 8-Lead (2mm × 2mm) DFN Packages

## APPLICATIONS

- USB Protection
- Handheld Computers
- Cell/Smart Phones
- MP3/MP4 Players
- Digital Cameras

## DESCRIPTION

The LTC®4361 overvoltage/overcurrent protection controller safeguards 2.5V to 5.5V systems from input supply overvoltage. It is designed for portable devices with multiple power supply options including wall adaptors, car battery adaptors and USB ports.

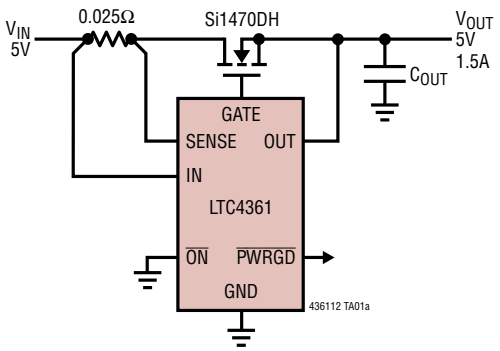
The LTC4361 controls an external N-channel MOSFET in series with the input power supply. During overvoltage transients, the LTC4361 turns off the MOSFET within 1µs, isolating downstream components from the input supply. Inductive cable transients are absorbed by the MOSFET and load capacitance. In most applications, the LTC4361 provides protection from transients up to 80V without requiring transient voltage suppressors or other external components.

The LTC4361 has a delayed start-up and adjustable dV/dt ramp-up for inrush current limiting. A $\overline{\text{PWRGD}}$ pin provides power good monitoring for $V_{IN}$. The LTC4361 features a soft shutdown controlled by the $\overline{\text{ON}}$ pin and drives an optional external P-channel MOSFET for negative voltage protection. Following an overvoltage condition, the LTC4361 automatically restarts with a start-up delay. After an overcurrent fault, the LTC4361-1 remains off while the LTC4361-2 automatically restarts after a 130ms start-up delay.

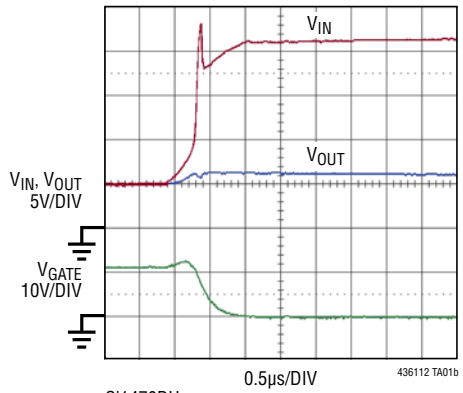


## TYPICAL APPLICATION

**Protection from Overvoltage and Overcurrent**




**Output Protected from Overvoltage at Input**




Rev C

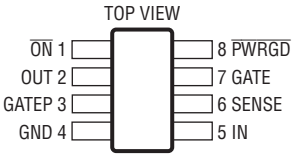
## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

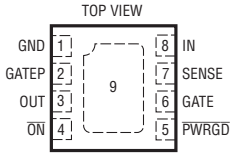
Bias Supply Voltage (IN) ..... –0.3V to 85V
Input Voltages
  SENSE ..... –0.3V to 85V
  OUT, $\overline{ON}$ ..... –0.3V to 9V
Output Voltages
  $\overline{PWRGD}$ ..... –0.3V to 9V
  GATE (Note 3) ..... –0.3V to 15V
  GATEP ..... –0.3V to 85V
  IN to GATEP ..... –0.3V to 10V

Operating Temperature Range
  LTC4361C ..... 0°C to 70°C
  LTC4361I ..... –40°C to 85°C
  LTC4361H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  TSOT ..... 300°C

## PIN CONFIGURATION




TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 195°C/W




DC PACKAGE
8-LEAD (2mm × 2mm) PLASTIC DFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 102°C/W
EXPOSED PAD (PIN 9) IS GND, CONNECTION OPT

## ORDER INFORMATION

**Lead Free Finish**

| TAPE AND REEL (MINI) | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC4361CTS8-1#TRMPBF | LTC4361CTS8-1#TRPBF | LTDWN | 8-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC4361CTS8-2#TRMPBF | LTC4361CTS8-2#TRPBF | LTFMN | 8-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC4361ITS8-1#TRMPBF | LTC4361ITS8-1#TRPBF | LTDWN | 8-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC4361ITS8-2#TRMPBF | LTC4361ITS8-2#TRPBF | LTFMN | 8-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC4361HTS8-1#TRMPBF | LTC4361HTS8-1#TRPBF | LTDWN | 8-Lead Plastic TSOT-23 | –40°C to 125°C |
| LTC4361HTS8-2#TRMPBF | LTC4361HTS8-2#TRPBF | LTFMN | 8-Lead Plastic TSOT-23 | –40°C to 125°C |
| LTC4361CDC-1#TRMPBF | LTC4361CDC-1#TRPBF | LDWP | 8-Lead (2mm × 2mm) Plastic DFN | 0°C to 70°C |
| LTC4361CDC-2#TRMPBF | LTC4361CDC-2#TRPBF | LFMP | 8-Lead (2mm × 2mm) Plastic DFN | 0°C to 70°C |
| LTC4361IDC-1#TRMPBF | LTC4361IDC-1#TRPBF | LDWP | 8-Lead (2mm × 2mm) Plastic DFN | –40°C to 85°C |
| LTC4361IDC-2#TRMPBF | LTC4361IDC-2#TRPBF | LFMP | 8-Lead (2mm × 2mm) Plastic DFN | –40°C to 85°C |
| LTC4361HDC-1#TRMPBF | LTC4361HDC-1#TRPBF | LDWP | 8-Lead (2mm × 2mm) Plastic DFN | –40°C to 125°C |
| LTC4361HDC-2#TRMPBF | LTC4361HDC-2#TRPBF | LFMP | 8-Lead (2mm × 2mm) Plastic DFN | –40°C to 125°C |

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult ADI Marketing for parts specified with wider operating temperature ranges.
Consult ADI Marketing for information on lead based finish parts.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 5V, $V_{\overline{ON}}$ = 0V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{IN}$ | Input Voltage Range | | ● | 2.5 | | 80 | V |
| $V_{IN(UVL)}$ | Input Undervoltage Lockout | $V_{IN}$ Rising | ● | 1.8 | 2.1 | 2.47 | V |
| $I_{IN}$ | Input Supply Current | $V_{\overline{ON}}$ = 0V | ● | | 220 | 400 | µA |
| | | $V_{\overline{ON}}$ = 2.5V | ● | | 1.5 | 10 | µA |
| **Thresholds** | | | | | | | |
| $V_{IN(OV)}$ | IN Pin Overvoltage Threshold | $V_{IN}$ Rising | ● | 5.684 | 5.8 | 5.916 | V |
| $V_{IN(OVL)}$ | IN Pin Overvoltage Recovery Threshold | $V_{IN}$ Falling | ● | 5.51 | 5.7 | 5.85 | V |
| $\Delta V_{OV}$ | Overvoltage Hysteresis | | ● | 25 | 100 | 300 | mV |
| $\Delta V_{OC}$ | Overcurrent Threshold | $V_{IN} - V_{SENSE}$ | ● | 45 | 50 | 55 | mV |
| **External Gate Drive** | | | | | | | |
| $\Delta V_{GATE}$ | External N-Channel MOSFET Gate Drive ($V_{GATE} - V_{OUT}$) | 2.5V ≤ $V_{IN}$ < 3V, $I_{GATE}$ = –1µA<br>3V ≤ $V_{IN}$ < 5.5V, $I_{GATE}$ = –1µA | ●<br>● | 3.5<br>4.5 | 4.5<br>6 | 6<br>7.9 | V<br>V |
| $V_{GATE(TH)}$ | GATE High Threshold for $\overline{PWRGD}$ Status | $V_{IN}$ = 3.3V<br>$V_{IN}$ = 5V | ●<br>● | 5.7<br>6.7 | 6.3<br>7.2 | 6.8<br>7.8 | V<br>V |
| $I_{GATE(UP)}$ | GATE Pull-Up Current | $V_{GATE}$ = 1V | ● | –4.5 | –10 | –15 | µA |
| $V_{GATE(UP)}$ | GATE Ramp-Up | $V_{GATE}$ = 1V to 7V | ● | 1.3 | 3 | 4.5 | V/ms |
| $I_{GATE(FST)}$ | GATE Pull-Down Current | Fast Turn-Off, $V_{IN}$ = 6V, $V_{GATE}$ = 9V (C-, I-Grade)<br>(H-Grade) | ●<br>● | 15<br>12 | 30<br>30 | 60<br>60 | mA<br>mA |
| $I_{GATE(DN)}$ | GATE Pull-Down Current | $V_{\overline{ON}}$ = 2.5V, $V_{GATE}$ = 9V | ● | 5 | 40 | 80 | µA |
| **Input Pins** | | | | | | | |
| $I_{SENSE(IN)}$ | SENSE Input Current | $V_{SENSE}$ = 5V | | | 10 | | nA |
| $I_{OUT(IN)}$ | OUT Input Current | $V_{OUT}$ = 5V, $V_{\overline{ON}}$ = 0V<br>$V_{OUT}$ = 5V, $V_{\overline{ON}}$ = 2.5V | ●<br>● | 5 | 10<br>0 | 20<br>±3 | µA<br>µA |
| $V_{\overline{ON}(TH)}$ | $\overline{ON}$ Input Threshold | | ● | 0.4 | | 1.5 | V |
| $I_{\overline{ON}}$ | $\overline{ON}$ Pull-Down Current | $V_{\overline{ON}}$ = 2.5V | ● | 2 | 5 | 10 | µA |
| **Output Pins** | | | | | | | |
| $V_{GATEP(CLP)}$ | IN to GATEP Clamp Voltage | $V_{IN}$ = 8V to 80V | ● | 5 | 5.8 | 7.9 | V |
| $R_{GATEP}$ | GATEP Resistive Pull-Down | $V_{GATEP}$ = 3V | ● | 0.6 | 2 | 3.2 | MΩ |
| $V_{\overline{PWRGD}(OL)}$ | $\overline{PWRGD}$ Output Low Voltage | $V_{IN}$ = 5V, $I_{\overline{PWRGD}}$ = 3mA (C-, I-Grade)<br>(H-Grade) | ●<br>● | | 0.23<br>0.23 | 0.4<br>0.5 | V<br>V |
| $R_{\overline{PWRGD}}$ | $\overline{PWRGD}$ Pull-Up Resistance to OUT | $V_{IN}$ = 6.5V, $V_{\overline{PWRGD}}$ = 1V | ● | 220 | 500 | 800 | kΩ |
| **Delay** | | | | | | | |
| $t_{ON}$ | GATE On Delay | $V_{IN}$ High to $I_{GATE}$ = –5µA | ● | 50 | 130 | 219 | ms |
| $t_{OFF}$ | GATE Off Propagation Delay | $V_{IN}$ = Step 5V to 6.5V to $\overline{PWRGD}$ High<br>$V_{IN} - V_{SENSE}$ = Step 0mV to 100mV | ●<br>● | <br>5 | 0.25<br>10 | 1<br>20 | µs<br>µs |
| $t_{\overline{PWRGD}}$ | $\overline{PWRGD}$ Delay | $V_{IN}$ = Step 5V to 6.5V<br>$V_{GATE}$ > $V_{GATE(TH)}$ to $\overline{PWRGD}$ Low | ●<br>● | <br>25 | 0.25<br>65 | 1<br>105 | µs<br>ms |
| $t_{\overline{ON}(OFF)}$ | $\overline{ON}$ High to GATE Off | $V_{\overline{ON}}$ = Step 0V to 2.5V | ● | | 2 | 5 | µs |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

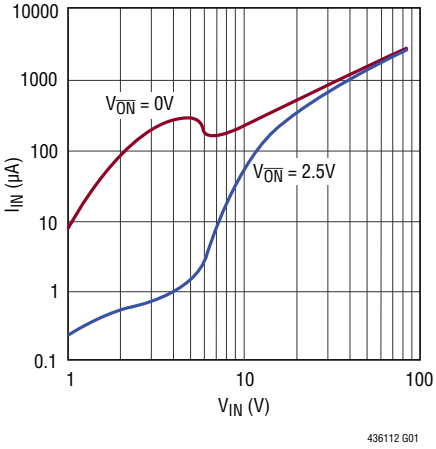
**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

**Note 3:** An internal clamp limits $V_{GATE}$ to a minimum of 4.5V above $V_{OUT}$. Driving this pin to voltages beyond this clamp may damage the device.

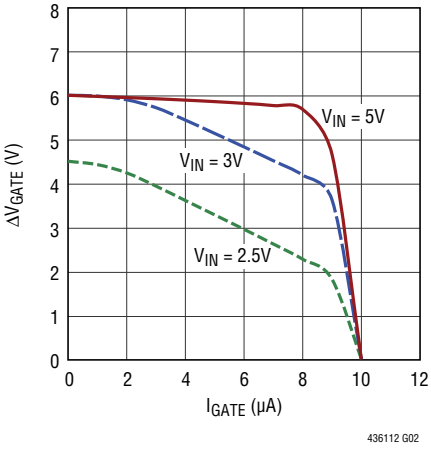
## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, $V_{IN}$ = 5V, $V_{\overline{ON}}$ = 0V, unless otherwise noted.**

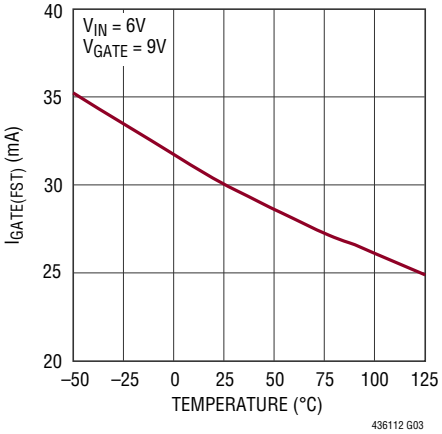
### Input Supply Current vs Input Voltage



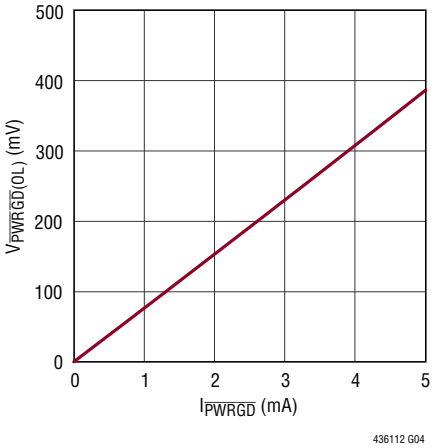

### GATE Drive vs GATE Current



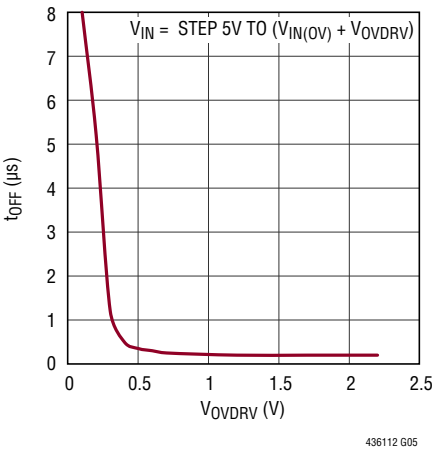

### GATE Fast Pull-Down Current vs Temperature



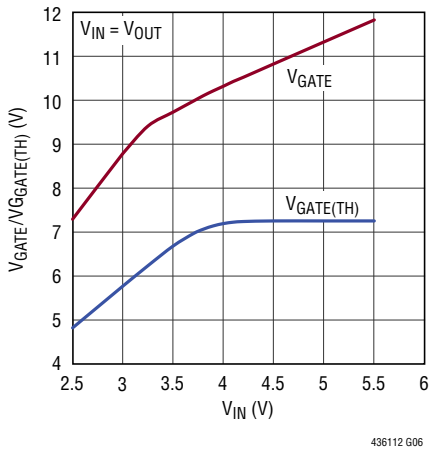

### $\overline{PWRGD}$ Voltage vs $\overline{PWRGD}$ Current




### GATE Off Propagation Delay vs Overdrive




### GATE Voltage and GATE High Threshold (for $\overline{PWRGD}$ Status) vs Input Voltage




### Normal Start-Up Sequence

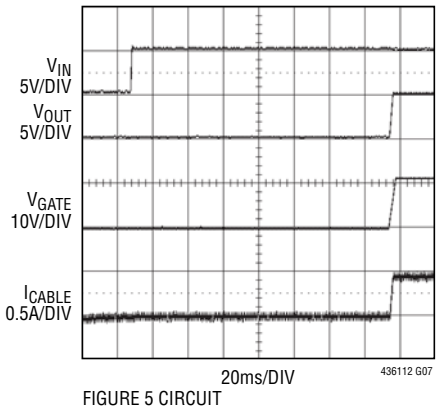



FIGURE 5 CIRCUIT
$R_{IN}$ = 150mΩ, $L_{IN}$ = 0.7µH
$R_{SENSE}$ = 25mΩ
LOAD = 10Ω, $C_{OUT}$ = 10µF

### GATE Slow Ramp-Up

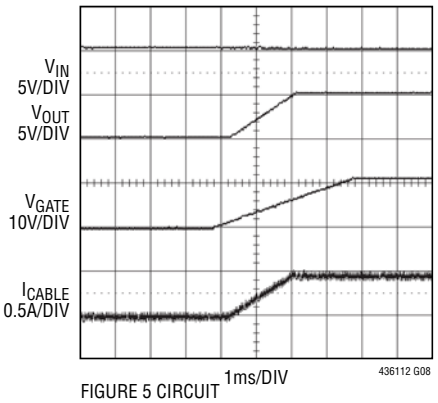



FIGURE 5 CIRCUIT
$R_{IN}$ = 150mΩ, $L_{IN}$ = 0.7µH
$R_{SENSE}$ = 25mΩ
LOAD = 10Ω, $C_{OUT}$ = 10µF

### Entering Sleep Mode

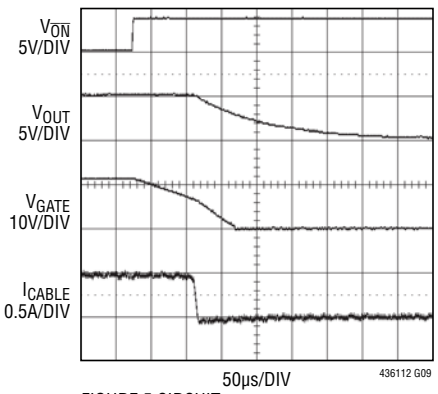



FIGURE 5 CIRCUIT
$R_{IN}$ = 150mΩ, $L_{IN}$ = 0.7µH
$R_{SENSE}$ = 25mΩ
LOAD = 10Ω, $C_{OUT}$ = 10µF

Rev C

## PIN FUNCTIONS

**Exposed Pad (DFN):** Ground. Connection to PCB is optional.

**GATE:** Gate Drive for External N-Channel MOSFET. An internal charge pump provides a 10µA pull-up current to charge the gate of the external N-channel MOSFET. An additional ramp circuit limits the GATE ramp rate when turning on to 3V/ms. For slower ramp rates, connect an external capacitor from GATE to GND. An internal clamp limits GATE to 6V above the OUT pin voltage. An internal GATE high comparator controls the $\overline{\text{PWRGD}}$ pin.

**GATEP:** Gate Drive for External P-Channel MOSFET. GATEP connects to the gate of an optional external P-channel MOSFET to protect against negative voltages at IN. This pin is internally clamped to 5.8V below $V_{IN}$. An internal 2M resistor connects this pin to ground. Connect to IN if not used.

**GND:** Device Ground.

**IN:** Supply Voltage Input. Connect this pin to the input power supply. This pin has an overvoltage threshold of 5.8V. After an overvoltage event, this pin must fall below $V_{IN(OV)} – \Delta V_{OV}$ to release the overvoltage lockout. During lockout, GATE is held low and the $\overline{\text{PWRGD}}$ pull-down releases.

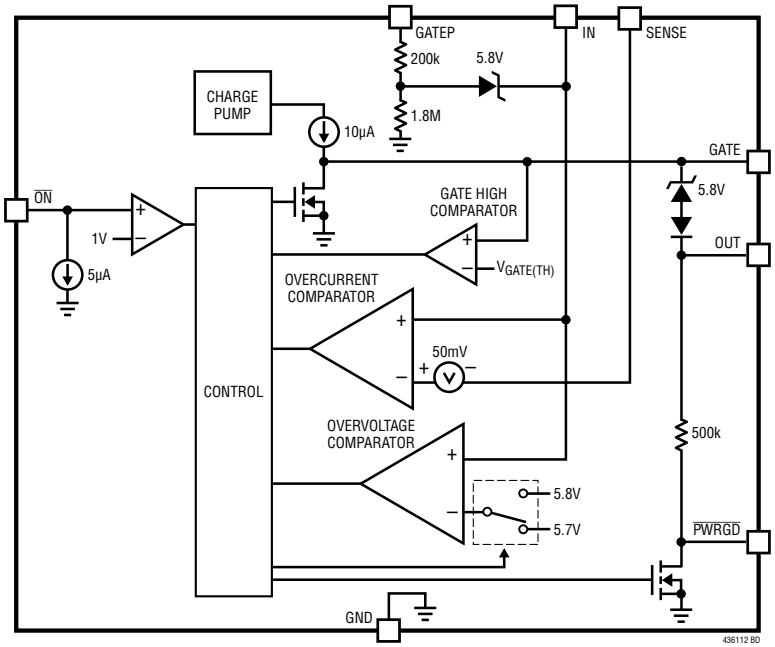
**$\overline{\text{ON}}$:** On Control Input. A logic low at $\overline{\text{ON}}$ enables the LTC4361. A logic high at $\overline{\text{ON}}$ activates a low current pull-down at the GATE pin and causes the LTC4361 to enter a low current sleep mode. An internal 5µA current pulls $\overline{\text{ON}}$ down to ground. Connect to ground or leave open if unused.

**OUT:** Output Voltage Sense Input for GATE Clamp. Connect to the source of the external N-channel MOSFET to sense the output voltage for GATE to OUT clamp.

**$\overline{\text{PWRGD}}$:** Power Good Status. Open-drain output with internal 500k resistive pull-up to OUT. Pulls low 65ms after GATE ramps above $V_{GATE(TH)}$.

**SENSE:** Current Sense Input. Connect a sense resistor between IN and SENSE. An overcurrent protection circuit turns off the N-channel MOSFET when the voltage across the sense resistor exceeds 50mV for more than 10µs.

## BLOCK DIAGRAM




## OPERATION

Mobile devices like cell phones and MP3/MP4 players have highly integrated subsystems fabricated from deep submicron CMOS processes. The small form factor is accompanied by low absolute maximum voltage ratings. The sensitive electronics are susceptible to damage from transient or DC overvoltage conditions from the power supply.

Failures or faults in the power adaptor can cause an overvoltage event. So can hot-plugging an AC adaptor into the power input of the mobile device (see ADI Application Note 88). Today's mobile devices derive their power supply or recharge their internal batteries from multiple alternative inputs like AC wall adaptors, car battery adaptors and USB ports. A user may unknowingly plug in the wrong adaptor, damaging the device with a high or even a negative power supply voltage.

The LTC4361 protects low voltage electronics from these overvoltage conditions by controlling a low cost external N-channel MOSFET configured as a pass transistor. At power-up ($V_{IN}$ > 2.1V), a start-up delay cycle begins. Any overvoltage condition causes the delay cycle to continue until a safe voltage is present. When the delay cycle completes, an internal high side switch driver slowly ramps up the MOSFET gate, powering up the output at a controlled rate and limiting the inrush current to the output capacitor.

If the voltage at the IN pin exceeds 5.8V ($V_{IN(OV)}$), GATE is pulled low quickly to protect the load. The incoming power supply must remain below 5.7V ($V_{IN(OV)} – \Delta V_{OV}$) for the duration of the start-up delay to restart the GATE ramp-up.

A sense resistor placed between IN and SENSE implements an overcurrent protection with a 50mV trip threshold and a 10µs glitch filter. After an overcurrent, the LTC4361-1 latches off while the LTC4361-2 restarts following a 130ms delay.

The LTC4361 has a CMOS compatible $\overline{ON}$ input. When driven low, the part is enabled. When driven high, the external N-channel MOSFET is turned off and the supply current of the LTC4361 drops to 1.5µA. The $\overline{PWRGD}$ pull-down releases during this low current sleep mode, UVLO, overvoltage or overcurrent and the subsequent 130ms start-up delay. After the start-up delay, GATE starts its slow ramp-up and ramps higher than $V_{GATE(TH)}$ to trigger a 65ms delay cycle. When that completes, $\overline{PWRGD}$ pulls low. The LTC4361 has a GATEP pin that drives an optional external P-channel MOSFET to provide protection against negative voltages at IN.

## APPLICATIONS INFORMATION

The typical LTC4361 application protects 2.5V to 5.5V systems in portable devices from power supply overvoltage. The basic application circuit is shown in Figure 1. Device operation and external component selection is discussed in detail in the following sections.

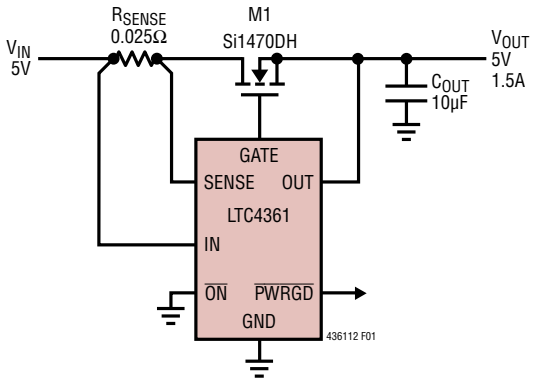



**Figure 1. Protection from Input Overvoltage and Overcurrent**

### Start-Up

When $V_{IN}$ is less than the undervoltage lockout level of 2.1V, the GATE driver is held low and the $\overline{PWRGD}$ pull-down is high impedance. When $V_{IN}$ rises above 2.1V and $\overline{ON}$ is held low, a 130ms delay cycle starts. Any undervoltage or overvoltage event at IN ($V_{IN}$ < 2.1V or $V_{IN}$ > 5.7V) restarts the delay cycle. This delay allows the N-channel MOSFET to isolate the output from any input transients that occur at start-up. When the delay cycle completes, GATE starts its slow ramp-up.

### GATE Control

An internal charge pump provides a gate overdrive greater than 3.5V when 2.5V ≤ $V_{IN}$ < 3V. If $V_{IN}$ ≥ 3V, the gate drive is guaranteed to be greater than 4.5V. This allows the use of logic-level N-channel MOSFETs. An internal 6V clamp between GATE and OUT protects the MOSFET gate.

The GATE ramp rate is limited to 3V/ms. $V_{OUT}$ follows at a similar rate which results in an inrush current into the load capacitor $C_{OUT}$ of:

$$I_{INRUSH} = C_{OUT} \bullet \frac{dV_{GATE}}{dt} = C_{OUT} \bullet 3\ [mA/\mu F]$$

The servo loop is compensated by the parasitic capacitance of the external MOSFET. No further compensation components are normally required. In the case where the parasitic capacitance is less than 100pF, a 100pF compensation capacitor between GATE and ground may be required.

An even slower GATE ramp and lower inrush current can be achieved by connecting an external capacitor, $C_G$, from GATE to ground. The voltage at GATE then ramps up with a slope equal to 10µA/$C_G$ [V/s]. Choose $C_G$ using the formula:

$$C_G = \frac{10\mu A}{I_{INRUSH}} \bullet C_{OUT}$$

### Overvoltage

When power is first applied, $V_{IN}$ must remain below 5.7V ($V_{IN(OV)} - \Delta V_{OV}$) for more than 130ms before GATE is ramped up to turn on the MOSFET. If $V_{IN}$ then rises above 5.8V ($V_{IN(OV)}$), the overvoltage comparator activates the 30mA fast pull-down on GATE within 1µs. After an overvoltage condition, the MOSFET is held off until $V_{IN}$ once again remains below 5.7V for 130ms.

### Overcurrent

The overcurrent comparator protects the MOSFET from excessive current. It trips when the SENSE pin falls more than 50mV below IN for 10µs. When the overcurrent comparator trips, GATE is pulled low quickly and the $\overline{PWRGD}$ pull-down releases. The LTC4361-2 automatically tries

## APPLICATIONS INFORMATION

to apply power again after a 130ms start-up delay. The LTC4361-1 has an internal latch that maintains this off state until it is reset. To reset this latch, cycle IN below 2.1V ($V_{IN(UVL)}$) or $\overline{ON}$ above 1.5V ($V_{\overline{ON}(TH)}$) for more than 500µs. After reset, the LTC4361-1 goes through the start-up cycle.

In applications not requiring the overcurrent protection, tie the SENSE pin to the IN pin. To implement an overcurrent threshold $I_{TRIP}$, choose $R_{SENSE}$ using the formula:

$$R_{SENSE} = \frac{\Delta V_{OC}}{I_{TRIP}}$$

After choosing the $R_{SENSE}$, keep in mind that:

$$I_{TRIP(MAX)} = \frac{\Delta V_{OC(MAX)}}{R_{SENSE(MIN)}}$$

$$I_{TRIP(MIN)} = \frac{\Delta V_{OC(MIN)}}{R_{SENSE(MAX)}}$$

### $\overline{PWRGD}$ Output

$\overline{PWRGD}$ is an active low output with a MOSFET pull-down to ground and a 500k resistive pull-up to OUT. The $\overline{PWRGD}$ pin pull-down releases during the low current sleep mode (invoked by $\overline{ON}$ high), UVLO, overvoltage or overcurrent and the subsequent 130ms start-up delay. After the start-up delay, GATE starts its slow ramp-up and control of the $\overline{PWRGD}$ pull-down passes on to the GATE high comparator. $V_{GATE} > V_{GATE(TH)}$ for more than 65ms asserts the $\overline{PWRGD}$ pull-down and $V_{GATE} < V_{GATE(TH)}$ releases the pull-down. The $\overline{PWRGD}$ pull-down is capable of sinking up to 3mA of current allowing it to drive an optional LED. To interface $\overline{PWRGD}$ to another I/O rail, connect a resistor from $\overline{PWRGD}$ to the I/O rail with a resistance low enough to override the internal 500k pull-up to OUT. Figure 2 details $\overline{PWRGD}$ behavior for a LTC4361-2 with 1k pull-up to 5V at $\overline{PWRGD}$.

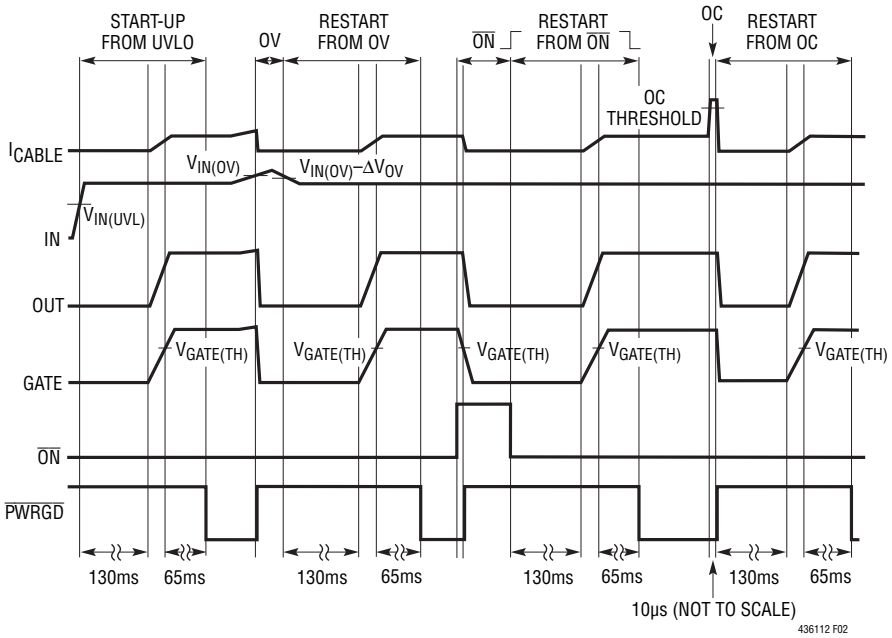



**Figure 2. $\overline{PWRGD}$ Behavior**

## APPLICATIONS INFORMATION

### $\overline{ON}$ Input

$\overline{ON}$ is a CMOS compatible, active low enable input. It has a default 5µA pull-down to ground. Connect this pin to ground or leave open to enable normal device operation. If it is driven high while the external MOSFET is turned on, GATE is pulled low with a weak pull-down current (40µA) to turn off the external MOSFET gradually, minimizing input voltage transients. The LTC4361 then goes into a low current sleep mode, drawing only 1.5µA at IN. When $\overline{ON}$ goes back low, the part restarts with a 130ms delay cycle.

### GATEP Control

GATEP has a 2M resistive pull-down to ground and a 5.8V Zener clamp in series with a 200k resistor to IN. It controls the gate of an optional external P-channel MOSFET to provide negative voltage protection. The 2M resistive pull-down turns on the MOSFET once $V_{IN} – V_{GATEP}$ is more than the MOSFET gate threshold voltage. The IN to GATEP Zener protects the MOSFET from gate overvoltage by clamping its $V_{GS}$ to 5.8V when $V_{IN}$ goes high.

### MOSFET Configurations and Selection

The LTC4361 can be used with various external MOSFET configurations (see Figure 3). The simplest configuration is a single N-channel MOSFET. It has the lowest $R_{DS(ON)}$ and voltage drop and is thus the most power efficient solution. When GATE is pulled to ground, the N-channel MOSFET can isolate OUT from a positive voltage at IN up to the $BV_{DSS}$ of the N-channel MOSFET. However, reverse current can still flow from OUT to IN via the parasitic body diode of the N-channel MOSFET.

For near zero reverse-leakage current protection when GATE is pulled to ground, back-to-back N-channel MOSFETs can be used. Adding an additional P-channel MOSFET controlled by GATEP provides negative input voltage protection down to the $BV_{DSS}$ of the P-channel MOSFET. Another configuration consists of a P-channel MOSFET controlled by GATEP and a N-channel MOSFET controlled by GATE. This provides protection against overvoltage and negative voltage but not reverse current.

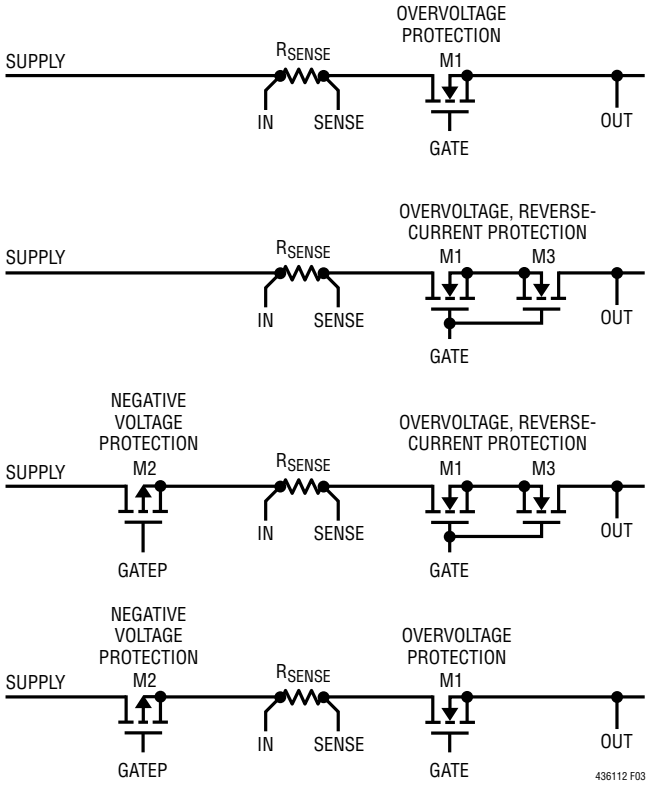
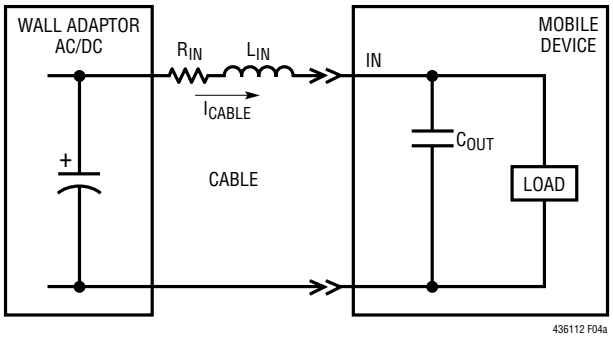
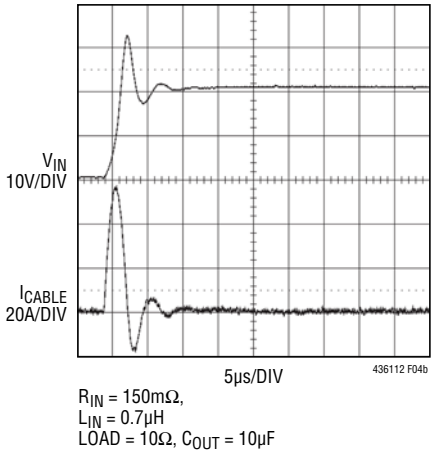



**Figure 3. MOSFET Configurations**

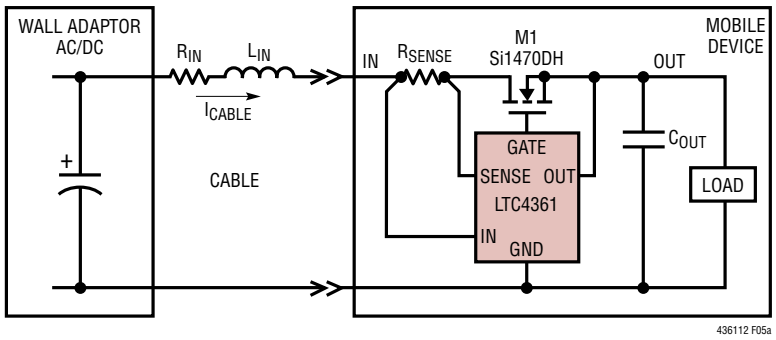
## APPLICATIONS INFORMATION

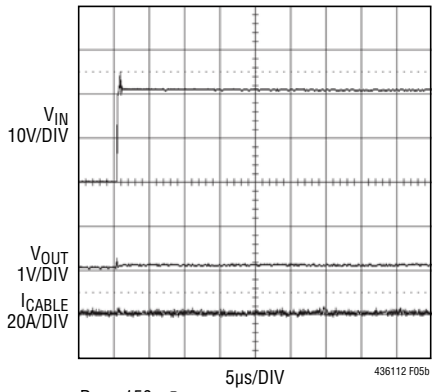



RIN = 150mΩ,
LIN = 0.7µH
LOAD = 10Ω, COUT = 10µF

**Figure 4. 20V Hot-Plug into a 10µF Capacitor**




RIN = 150mΩ,
LIN = 0.7µH, RSENSE = 25mΩ
LOAD = 10Ω, COUT = 10µF

**Figure 5. 20V Hot-Plug into the LTC4361**

### Input Transients

Figure 4 shows a typical setup when an AC wall adaptor charges a mobile device. The inductor $L_{IN}$ represents the lumped equivalent inductance of the cable and the EMI filter found in some wall adaptors. $R_{IN}$ is the lumped equivalent resistance of the cable, adaptor output capacitor ESR and the connector contact resistance.

$L_{IN}$ and $R_{IN}$ form an LC tank circuit with any capacitance at IN. If the wall adaptor is powered up first, plugging the wall adaptor output to IN does the equivalent of applying a voltage step to this LC circuit. The resultant voltage overshoot at IN can rise to twice the DC output voltage of the wall adaptor as shown in Figure 4. Figure 5 shows the 20V adaptor output applied to the LTC4361. Due to the low capacitance at the IN pin, the plug-in transient has been brought down to a manageable level.

## APPLICATIONS INFORMATION

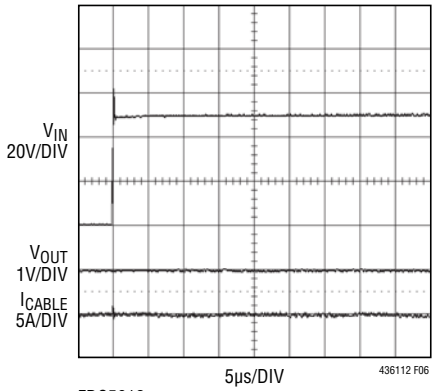
As the IN pin can withstand up to 80V, a high voltage N-channel MOSFET can be used to protect the system against rugged abuse from high transient or DC voltages up to the $BV_{DSS}$ of the MOSFET. Figure 6 shows a 50V input plugged into the LTC4361 controlling a 60V rated MOSFET.

Input transients also occur when the current through the cable inductance changes abruptly. This can happen when the LTC4361 turns off the N-channel MOSFET rapidly in an overvoltage or overcurrent event. Figure 7 shows an input transient after an overcurrent. The current in $L_{IN}$ will cause $V_{IN}$ to overshoot and avalanche the N-channel MOSFET to $C_{OUT}$. Typically, IN will be clamped to a voltage of $V_{OUT}$ + 1.3 • ($BV_{DSS}$ of Si1470DH) = 45V. This is well below the 85V absolute maximum voltage rating of the LTC4361.

The single, nonrepetitive, pulse of energy ($E_{AS}$) absorbed by the MOSFET during this avalanche breakdown with a peak current $I_{AS}$ is approximated by the formula:

$$E_{AS} = 0.5 \bullet L_{IN} \bullet I_{AS}^2$$

For $L_{IN}$ = 0.7µH and $I_{AS}$ = 4A, then $E_{AS}$ = 5.6µJ. This is within the $I_{AS}$ and $E_{AS}$ capabilities of most MOSFET's including the Si1470DH. So in most instances, the LTC4361 can ride through such transients without a bypass capacitor, transient voltage suppressor or other external components at IN. Note that if an IN bypass capacitor is used, the $V_{IN}$ transients will overshoot less but last longer. If $V_{IN}$ dips below $V_{IN(UVL)}$ for more than 10µs, the internal latch-off latch in the LTC4361-1 could be inadvertently reset.




FDC5612
$R_{IN}$ = 150mΩ, $L_{IN}$ = 0.7µH
$R_{SENSE}$ = 25mΩ, LOAD = 10Ω, $C_{OUT}$ = 10µF

**Figure 6. 50V Hot-Plug into the LTC4361**

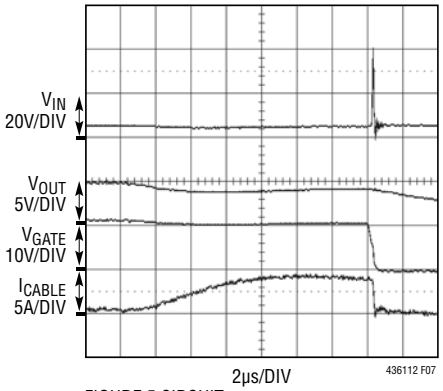



FIGURE 5 CIRCUIT
$R_{IN}$ = 150mΩ, $L_{IN}$ = 0.7µH
$R_{SENSE}$ = 25mΩ, LOAD = 10Ω, $C_{OUT}$ = 10µF

**Figure 7. Overcurrent Turn-Off and Resulting Input Transient**

## APPLICATIONS INFORMATION

Figure 8 shows a particularly severe situation which can occur in a mobile device with dual power inputs. A 20V wall adaptor is mistakenly hot-plugged into the 5V device with the USB input already live. As shown in Figure 9, a large current can build up in $L_{IN}$ to charge up $C_{OUT}$. When the N-channel MOSFET shuts off, the energy stored in $L_{IN}$ is dumped into $C_{OUT}$, causing a large 40V input transient. The LTC4361 limits this to a 1V rise in the output voltage.

If the $\Delta V_{OUT}$ due to the discharge of the energy in $L_{IN}$ into $C_{OUT}$ is not acceptable or the avalanche capability of the MOSFET is exceeded, an additional external clamp such as the SMAJ24A can be placed between IN and GND. $C_{OUT}$ is the decoupling capacitor of the protected circuits and its value will largely be determined by their requirements. Using a larger $C_{OUT}$ will work with $L_{IN}$ to slow down the dV/dt at OUT, allowing time for the LTC4361 to shut off the MOSFET before $V_{OUT}$ overshoots to a dangerous voltage. A larger $C_{OUT}$ also helps to lower the $\Delta V_{OUT}$ due to the discharge of the energy in $L_{IN}$ if the MOSFET $BV_{DSS}$ is used as an input clamp.

### Layout Considerations

Figure 10 shows an example PCB layout for the LTC4361 (TS8 package) with a single N-channel MOSFET (SC70 package) and a 0603 size sense resistor. Keep the traces to the N-channel MOSFET wide and short. The PCB traces associated with the power path through the N-channel MOSFET should have low resistance. Use Kelvin connections to $R_{SENSE}$ for an accurate overcurrent threshold.

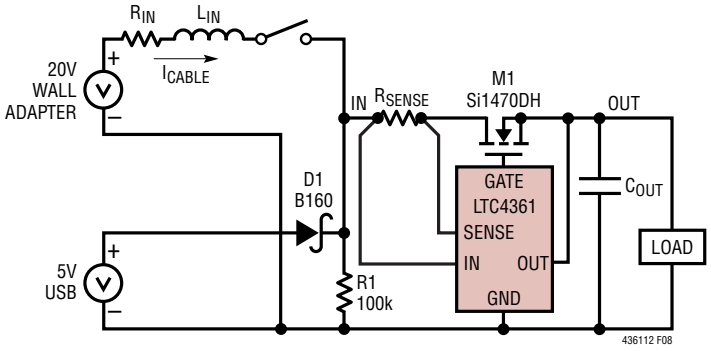



**Figure 8. Setup for Testing 20V Plugged into 5V System**

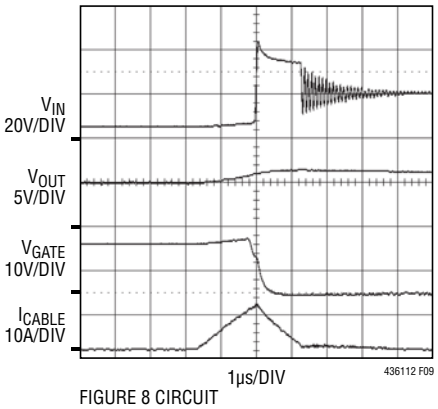



FIGURE 8 CIRCUIT
$R_{IN}$ = 150mΩ
$L_{IN}$ = 2µH, $R_{SENSE}$ = 25mΩ, LOAD = 10Ω
$C_{OUT}$ = 10µF (16V, SIZE 1210)

**Figure 9. Overvoltage Protection Waveforms When 20V Plugged into 5V System**

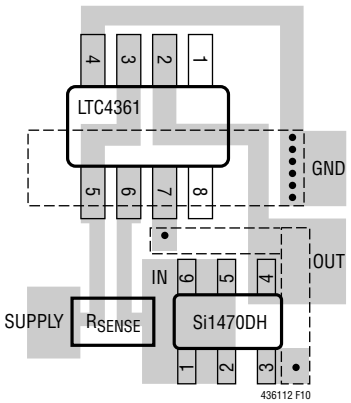
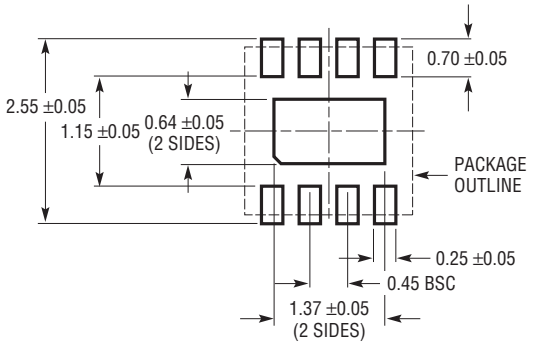


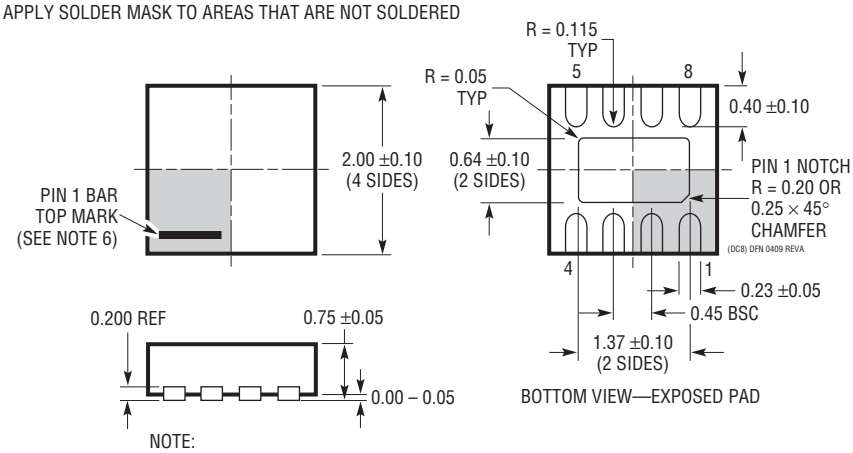

**Figure 10. Layout for N-Channel MOSFET Configuration**

# PACKAGE DESCRIPTION

**DC8 Package**
**8-Lead Plastic DFN (2mm × 2mm)**
(Reference LTC DWG # 05-08-1719 Rev A)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

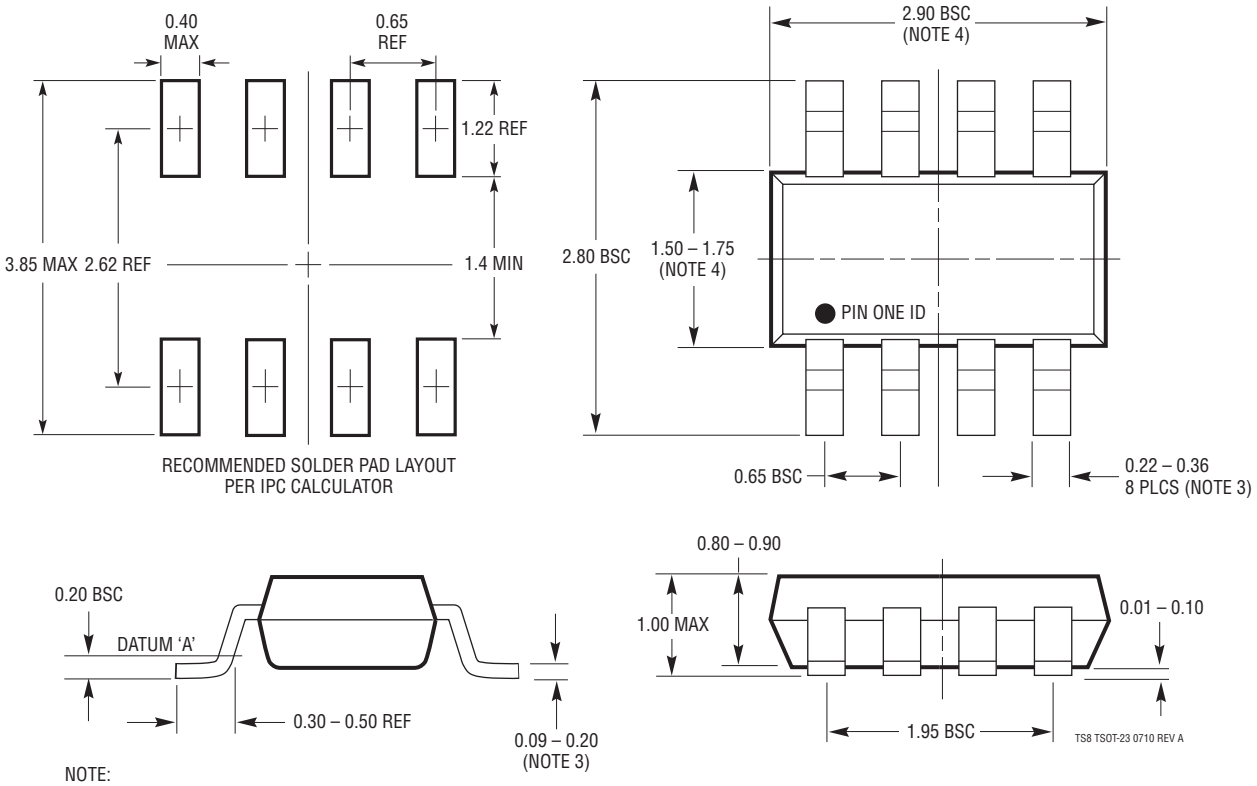



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**TS8 Package**
**8-Lead Plastic TSOT-23**
(Reference LTC DWG # 05-08-1637 Rev A)




NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 01/11 | Revised conditions for $V_{GATE(CLP)}$ and $t_{OFF}$ in Electrical Characteristics section | 3 |
| | | Revised GATE Control in Applications Information section | 7 |
| B | 05/12 | Added H-grade order information | 2 |
| | | Change to Electrical Characteristics Input Undervoltage Lockout | 3 |
| | | Added $V_{IN(OVL)}$ specifications | 3 |
| | | Change to Electrical Characteristics Overvoltage Hysteresis | 3 |
| | | Change to Electrical Characteristics GATE Pull-Up and Pull-Down Current | 3 |
| | | Change to Electrical Characteristics GATE Ramp-Up | 3 |
| | | Added $I_{SENSE(IN)}$ specifications | 3 |
| | | Change to Electrical Characteristics $\overline{ON}$ Pull-Down Current | 3 |
| | | Change to Electrical Characteristics IN to GATEP Clamp Voltage | 3 |
| | | Change to Electrical Characteristics GATEP Resistive Pull-Down | 3 |
| | | Change to Electrical Characteristics $\overline{PWRGD}$ Pull-Up Resistance to OUT | 3 |
| | | Change to Electrical Characteristics GATE On Delay | 3 |
| | | Change to Electrical Characteristics $\overline{PWRGD}$ Delay | 3 |
| | | Replaced GATE Fast Pull-Down Current vs Temperature Curve | 4 |
| | | Added PCB trace to short pin 3 to pin 5 in Figure 10 | 12 |
| | | Added packaging link | 13, 14 |
| C | 06/18 | Changed $\Delta V_{OV}$ maximum limit to 300mV | 3 |