1.2A Overvoltage/Overcurrent Protector

FEATURES

- **2.5V to 5.5V Operation**
- **Overvoltage Protection Up to 28V**
- **Internal 40mΩ N-Channel MOSFET and 31mΩ R_{SENSE}**
- **Avalanche Rated MOSFET Requires No Input Capacitor or TVS for Most Applications**
- **<1µs Overvoltage Turn-Off, Gentle Shutdown**
- 2% Accurate 5.8V Overvoltage Threshold
- 20% Accurate 1.5A Overcurrent Threshold
- Input Withstands Up to ±25kV HBM ESD with ≥1µF C_{OUT}
- Controlled Power-Up dV/dt Limits Inrush Current
- Reverse Voltage Protection Driver
- Low Current Shutdown
- Latchoff (LTC4362-1) or Auto-Retry (LTC4362-2) After Overcurrent
- Available in 8-Lead DFN 2mm × 3mm Package

APPLICATIONS

- USB Protection
- Handheld Computers
- Cell/Smart Phones
- MP3/MP4 Players
- Digital Cameras

DESCRIPTION

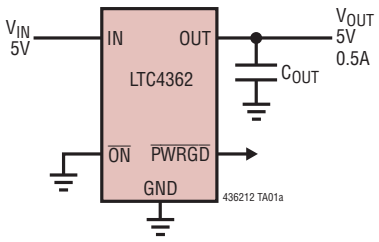
The LTC®4362 monolithic overvoltage/overcurrent protector safeguards 2.5V to 5.5V systems from power supply overvoltage. It is designed for portable devices with multiple power supply options including wall adaptors, car battery adaptors and USB ports.

The LTC4362 controls an internal 40mΩ N-channel MOSFET in series with the input power supply. During overvoltage transients, the LTC4362 turns off the MOSFET within 1µs, isolating downstream components from the input supply. In most applications, the LTC4362 rides through inductive cable transients without requiring transient voltage suppressors or other external components. An internal current sense resistor is used to implement overcurrent protection.

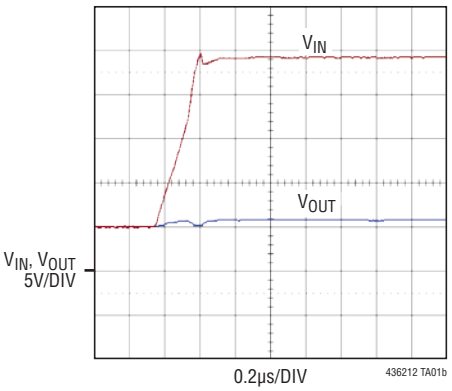
The LTC4362 has a delayed start-up at plug-in and controlled dV/dt ramp-up for inrush current limiting. A $\overline{PWRGD}$ pin provides power good monitoring for V_{IN}. The LTC4362 features a soft-shutdown controlled by the $\overline{ON}$ pin and drives an optional external P-channel MOSFET for negative voltage protection. Following an overvoltage condition, the LTC4362 automatically restarts with a 130ms delay. After an overcurrent fault, the LTC4362-1 remains off while the LTC4362-2 automatically restarts after a 130ms delay.

TYPICAL APPLICATION

Protection from Overvoltage and Overcurrent



Output Protected from Overvoltage at Input



C_{OUT} = 10µF

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Bias Supply Voltage
- IN to OUT (Note 3) ..... –0.3V to 28V

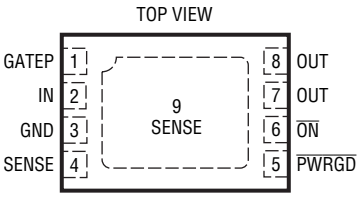
Input Voltages
- SENSE to OUT (Notes 3 and 4) ..... –0.3V to 28V
- $\overline{ON}$ ..... –0.3V to 9V

Output Voltages
- OUT, $\overline{PWRGD}$ ..... –0.3V to 9V
- IN to GATEP ..... –0.3V to 10V

Operating Temperature Range
- LTC4362C ..... 0°C to 70°C
- LTC4362I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DCB PACKAGE
8-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 64°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4362CDCB-1#TRMPBF	LTC4362CDCB-1#TRPBF	LFNC	8-Lead Plastic DFN	0°C to 70°C
LTC4362CDCB-2#TRMPBF	LTC4362CDCB-2#TRPBF	LFJN	8-Lead Plastic DFN	0°C to 70°C
LTC4362IDCB-1#TRMPBF	LTC4362IDCB-1#TRPBF	LFNC	8-Lead Plastic DFN	–40°C to 85°C
LTC4362IDCB-2#TRMPBF	LTC4362IDCB-2#TRPBF	LFJN	8-Lead Plastic DFN	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Contact the factory for parts specified with wider operating temperature ranges.
Contact the factory for information on lead based finish parts.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{ON}}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{IN}	Input Voltage Range		●	2.5		28	V
$V_{IN(UVL)}$	Input Undervoltage Lockout	V_{IN} Rising	●	1.8	2.1	2.45	V
I_{IN}	Input Supply Current	$V_{\overline{ON}}$ = 0V $V_{\overline{ON}}$ = 2.5V	● ●		220 1.5	400 10	µA µA
Thresholds							
$V_{IN(OV)}$	IN Pin Overvoltage Threshold	V_{IN} Rising	●	5.684	5.8	5.916	V
$V_{IN(OVL)}$	IN Pin Overvoltage Recovery Threshold	V_{IN} Falling	●	5.51	5.7	5.85	V
ΔV_{OV}	Overvoltage Hysteresis		●	25	100	300	mV
Input Pins							
$V_{\overline{ON}(TH)}$	$\overline{ON}$ Input Threshold		●	0.4		1.5	V
$I_{\overline{ON}}$	$\overline{ON}$ Pull-Down Current	$V_{\overline{ON}}$ = 2.5V	●	2.5	5	10	µA
Output Pins							
$V_{OUT(UP)}$	OUT Turn-On Ramp-Rate	V_{OUT} = 0.5V to 4V	●	1.5	3	4.5	V/ms
I_{OUT}	OUT Leakage Current	$V_{\overline{ON}}$ = 2.5V, V_{OUT} = 5V	●		0	±3	µA
$V_{GATEP(CLP)}$	IN to GATEP Clamp Voltage	V_{IN} = 8V to 28V	●	5	5.8	7.5	V
R_{GATEP}	GATEP Pull-Down Resistance	V_{GATEP} = 3V	●	0.8	2	3.2	MΩ
$V_{\overline{PWRGD}(OL)}$	$\overline{PWRGD}$ Output Low Voltage	V_{IN} = 5V, $I_{\overline{PWRGD}}$ = 3mA	●		0.23	0.4	V
$R_{\overline{PWRGD}}$	$\overline{PWRGD}$ Pull-Up Resistance to OUT	V_{IN} = 6.5V, $V_{\overline{PWRGD}}$ = 1V	●	250	500	800	kΩ
Internal N-Channel MOSFET							
R_{ON}	On Resistance	I_{OUT} = 0.5A	●		40	70	mΩ
I_{TRIP}	Overcurrent Threshold		●	1.2	1.5	1.8	A
I_{AS}	Peak Avalanche Current	L = 0.1mH (Note 5)			10		A
E_{AS}	Single Pulse Avalanche Energy	I_{AS} = 10A, L = 0.1mH (Note 5)			10		mJ
Delay							
t_{ON}	Turn-On Delay	V_{IN} High to V_{OUT} = 0.5V, R_{OUT} = 1kΩ	●	50	130	200	ms
$t_{OFF(OV)}$	Turn-Off Delay for Overvoltage	V_{IN} = 5V ⌋ 6.5V to V_{OUT} = 4.5V, R_{OUT} = 1kΩ	●		0.45	1	µs
$t_{OFF(OC)}$	Turn-Off Delay for Overcurrent	I_{OUT} = 0.5A ⌋ 3A to V_{OUT} = 4.5V	●	5	10	20	µs
$t_{\overline{PWRGD}(LH)}$	$\overline{PWRGD}$ Rising Delay	V_{IN} = 5V ⌋ 6.5V to $\overline{PWRGD}$ High	●		0.3	1	µs
$t_{\overline{PWRGD}(HL)}$	$\overline{PWRGD}$ Falling Delay	V_{IN} = 0V ⌋ 5V, V_{OUT} = 0.5V to $\overline{PWRGD}$ Low, R_{OUT} = 1kΩ	●	25	65	100	ms
$t_{\overline{ON}(OFF)}$	$\overline{ON}$ High to N-channel MOSFET Off	$V_{\overline{ON}}$ = 0V ⌋ 2.5V	●		40	100	µs
ESD Protection							
	ESD Protection for IN to GND	C_{OUT} = 1µF, Human Body Model			±25		kV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: The minimum drain-source breakdown voltage of the internal MOSFET is 28V. Driving the IN and SENSE pins more than 28V above OUT may damage the device if the E_{AS} capability of the MOSFET is exceeded.

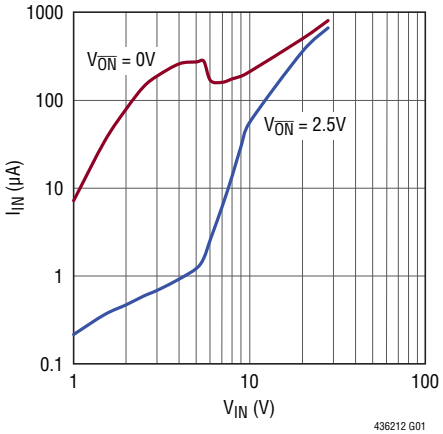
Note 4: An internal current sense resistor ties IN and SENSE. Driving SENSE relative to IN may damage the resistor.

Note 5: The I_{AS} and E_{AS} typical values are based on characterization and are not production tested.

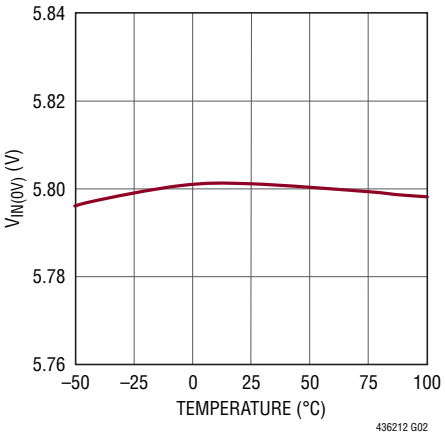
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{IN} = 5V, $V_{\overline{ON}}$ = 0V unless otherwise noted.

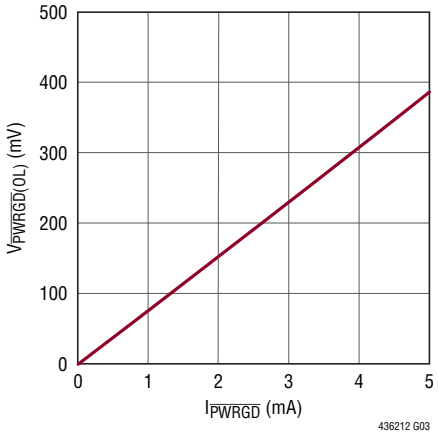
Input Supply Current vs Input Voltage



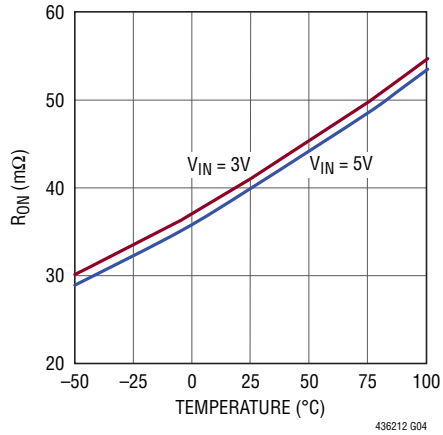
Overvoltage Threshold vs Temperature



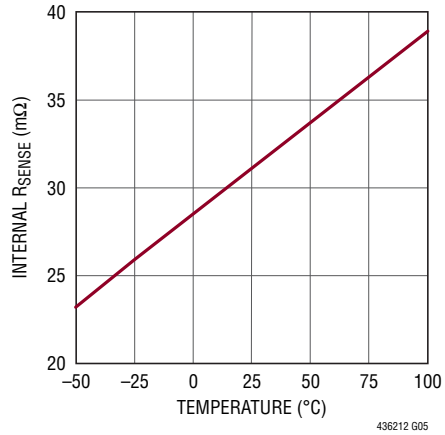
$\overline{PWRGD}$ Voltage vs $\overline{PWRGD}$ Current



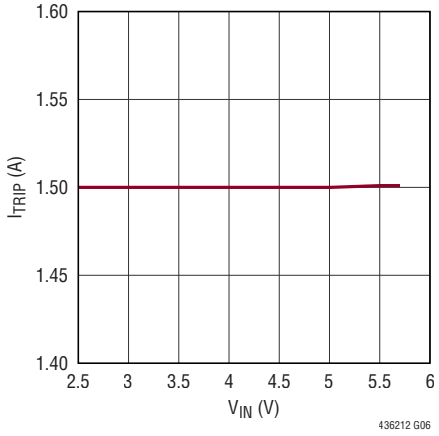
Internal MOSFET On Resistance vs Temperature



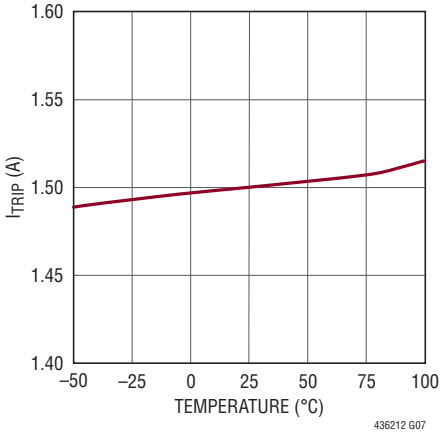
Internal R_{SENSE} vs Temperature



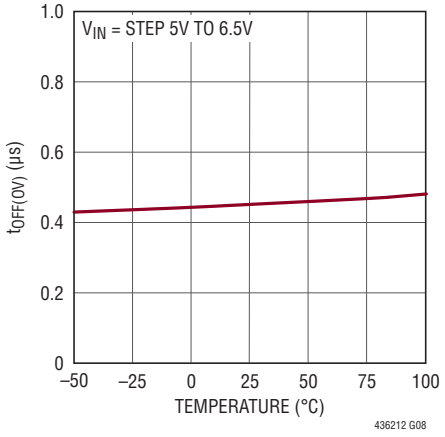
Overcurrent Threshold vs Input Voltage



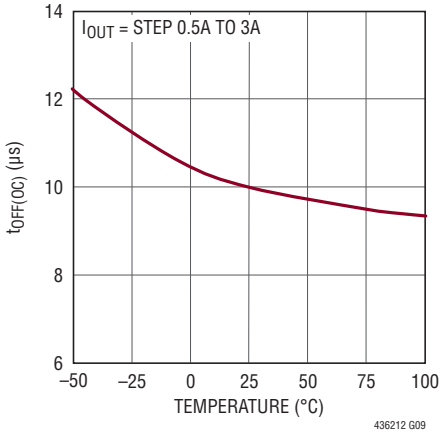
Overcurrent Threshold vs Temperature



Overvoltage Turn-Off Delay vs Temperature



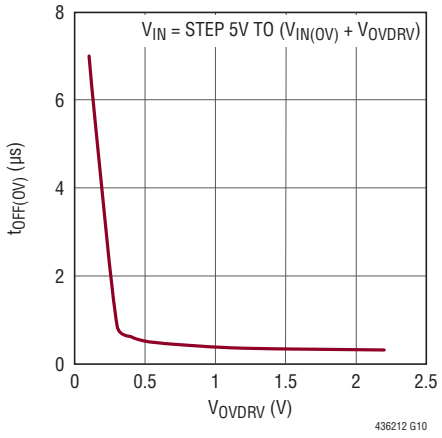
Overcurrent Turn-Off Delay vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{IN} = 5V, $V_{\overline{ON}}$ = 0V unless otherwise noted.

Overvoltage Turn-Off Delay vs Overdrive (V_{OVDRV})



Normal Start-Up Sequence

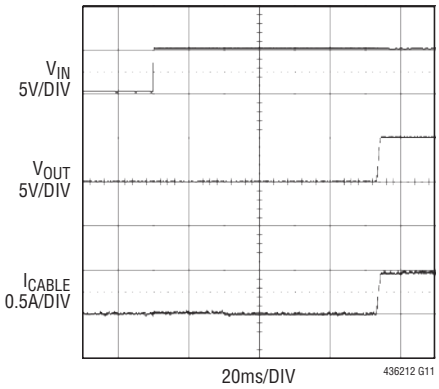


FIGURE 4 CIRCUIT
R_{IN} = 150mΩ, L_{IN} = 0.7µH
LOAD = 10Ω, C_{OUT} = 10µF

Turn-On Ramp-Up

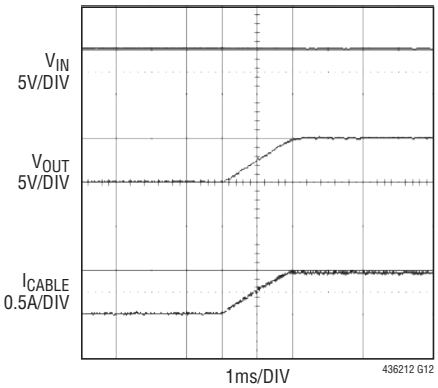


FIGURE 4 CIRCUIT
R_{IN} = 150mΩ, L_{IN} = 0.7µH
LOAD = 10Ω, C_{OUT} = 10µF

PIN FUNCTIONS

GATEP: Gate Drive for External P-channel MOSFET. GATEP connects to the gate of an optional external P-channel MOSFET to protect against negative voltages at IN. Internally clamped to 5.8V below V_{IN}. An internal 2M resistor connects this pin to ground. Connect to IN if unused.

GND: Device Ground.

IN: Supply Voltage Input. Connect this pin to the input power supply. This pin has an overvoltage threshold of 5.8V. After an overvoltage event, this pin must fall below $V_{IN(OV)} – \Delta V_{OV}$ to release the overvoltage lockout. During lockout, the internal N-channel MOSFET remains off and the $\overline{PWRGD}$ pull-down releases.

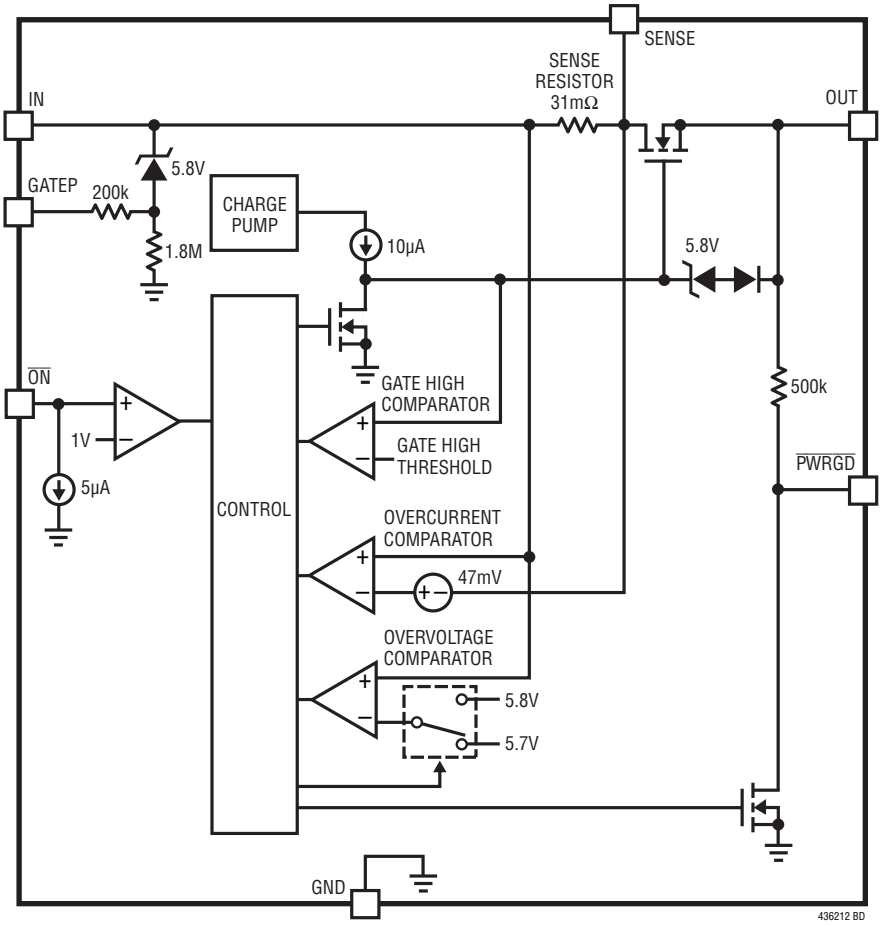
$\overline{ON}$: On Control Input. A logic low at $\overline{ON}$ enables the LTC4362. A logic high at $\overline{ON}$ activates a low current pull-down on the gate of the internal N-channel MOSFET and causes the LTC4362 to enter a low current sleep mode. An internal 5µA current pulls $\overline{ON}$ down to ground. Connect to ground or leave open if unused.

$\overline{OUT}$: Source of Internal N-channel MOSFET. Connect to load.

$\overline{PWRGD}$: Power Good Status. Open-drain output with internal 500k resistive pull-up to OUT. Pulls low 65ms after the MOSFET gate ramps above its internal gate high threshold.

SENSE, Exposed Pad: Current Sense Node and Internal N-channel MOSFET Drain. An internal sense resistor between IN and SENSE is used to implement the 1.5A overcurrent threshold. The exposed pad is connected to SENSE and must be soldered to an electrically isolated printed circuit board trace to properly transfer the heat out of the package. To disable the overcurrent function, connect SENSE and the exposed pad to IN.

BLOCK DIAGRAM



OPERATION

Mobile devices like cell phones and MP3/MP4 players have highly integrated subsystems fabricated from deep submicron CMOS processes. The small form factor is accompanied by low absolute maximum voltage ratings. The sensitive electronics are susceptible to damage from transient or DC overvoltage conditions from the power supply.

Failures or faults in the power adaptor can cause an overvoltage event. So can hot-plugging an AC adaptor into the power input of the mobile device (see Application Note 88). Today's mobile devices derive their power supply or recharge their internal batteries from multiple alternative inputs like AC wall adaptors, car battery adaptors and USB ports. A user might unknowingly plug in the wrong adaptor, damaging the device with a high or even a negative power supply voltage.

The LTC4362 protects low voltage electronics from these overvoltage conditions by controlling an internal N-channel MOSFET configured as a pass transistor. At power-up (V_{IN} > 2.1V), a start-up delay cycle begins. Any overvoltage condition causes the delay cycle to continue until a safe voltage is present. When the delay cycle completes, an internal high-side switch driver slowly ramps up the MOSFET gate, powering up the output at a controlled rate and limiting the inrush current to the output capacitor.

OPERATION

If the voltage at the IN pin exceeds 5.8V ($V_{IN(OV)}$), the internal N-channel MOSFET is turned off quickly to protect the load. The incoming power supply must remain below 5.7V ($V_{OUT(OV)} – \Delta V_{OV}$) for the duration of the start-up delay to restart the OUT ramp-up.

An internal sense resistor is used to implement an overcurrent protection with a 1.5A current trip threshold and a 10µs glitch filter. After an overcurrent, the LTC4362-1 latches off while the LTC4362-2 restarts following a 130ms delay.

The LTC4362 has a CMOS compatible $\overline{ON}$ input. When driven low, the part is enabled. When driven high, the internal N-channel MOSFET is turned off and the supply current of the LTC4362 drops to 1.5µA. The $\overline{PWRGD}$ pull-down releases during this low current sleep mode, UVLO, overvoltage, overcurrent or thermal shutdown and the subsequent 130ms start-up delay. After the start-up delay, the internal MOSFET gate starts its 3V/ms ramp-up. It trips an internal gate high threshold to trigger a 65ms delay. When that completes, $\overline{PWRGD}$ pulls low. The output pull-down device is capable of sinking up to 3mA allowing it to drive an optional LED. The LTC4362 has a GATEP pin that drives an optional external P-channel MOSFET to provide protection against negative voltages at IN.

APPLICATIONS INFORMATION

The typical LTC4362 application protects 2.5V to 5.5V systems in portable devices from power supply overvoltage. The basic application circuit is shown in Figure 1. Device operation and external component selection is discussed in detail in the following sections.

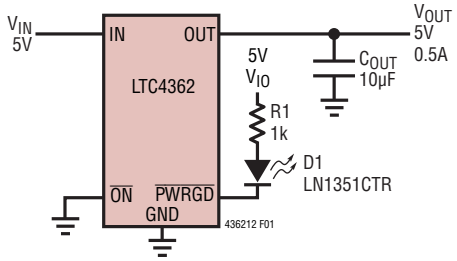


Figure 1. Protection from Overvoltage and Overcurrent

Start-Up

When V_{IN} is less than the undervoltage lockout level of 2.1V, the internal N-channel MOSFET is held off and the $\overline{PWRGD}$ pull-down is high impedance. When V_{IN} rises above 2.1V and $\overline{ON}$ is held low, a 130ms delay cycle starts. Any undervoltage or overvoltage event at IN (V_{IN} < 2.1V or V_{IN} > 5.7V) restarts the delay cycle. This delay allows the MOSFET to isolate the output from any input transients that occur at start-up. When the delay cycle completes, the MOSFET is turned on and OUT starts its slow ramp-up.

OUT Control

An internal charge pump enhances the internal N-channel MOSFET with the OUT ramp-rate limited to 3V/ms. This results in an inrush current into the load capacitor C_{OUT} of:

$$I_{INRUSH} = C_{OUT} \bullet \frac{dV_{OUT}}{dt} = C_{OUT} \bullet 3[mA/\mu F]$$

Overvoltage

When power is first applied, V_{IN} must remain below 5.7V ($V_{IN(OV)} – \Delta V_{OV}$) for more than 130ms before the output is turned on. If V_{IN} then rises above 5.8V ($V_{IN(OV)}$), the overvoltage comparator turns off the internal MOSFET within 1µs. After an overvoltage condition, the MOSFET is held off until V_{IN} once again remains below 5.7V for 130ms.

Overcurrent

The overcurrent comparator protects the internal MOSFET from excessive current. It trips when I_{OUT} > 1.5A for 10µs. When the overcurrent comparator trips, the internal MOSFET is turned off quickly and the $\overline{PWRGD}$ pull-down releases. The LTC4362-2 automatically tries to apply power again after a 130ms start-up delay. The LTC4362-1 has an internal latch that maintains this off state until it is reset. To reset this latch, cycle IN below 2.1V ($V_{IN(UVL)}$)

APPLICATIONS INFORMATION

or $\overline{ON}$ above 1.5V ($V_{\overline{ON}(TH)}$) for more than 500µs. After reset, the LTC4362-1 goes through the start-up cycle. In applications not requiring the overcurrent protection, tie SENSE and the exposed pad to the IN pin.

$\overline{PWRGD}$ Output

$\overline{PWRGD}$ is an active low output with a MOSFET pull-down to ground and a 500k resistive pull-up to OUT. The $\overline{PWRGD}$ pin pull-down releases during the low current sleep mode (invoked by $\overline{ON}$ high), UVLO, overvoltage, overcurrent or thermal shutdown and the subsequent 130ms start-up delay. After the start-up delay, the internal MOSFET gate starts its 3V/ms ramp-up and control of the $\overline{PWRGD}$ pull-down passes on to the internal gate high comparator. When the internal gate is higher than the gate high threshold for more than 65ms, $\overline{PWRGD}$ asserts low. When the internal gate goes lower than the gate high threshold, the $\overline{PWRGD}$ pull-down releases. The $\overline{PWRGD}$ pull-down device is capable of sinking up to 3mA of current allowing it to drive an optional LED. To interface $\overline{PWRGD}$ to another I/O rail, connect a resistor from $\overline{PWRGD}$ to that I/O rail with a resistance low enough to override the internal 500k pull-up to OUT. Figure 2 details $\overline{PWRGD}$ behavior for a LTC4362-2 with 1k pull-up to 5V at $\overline{PWRGD}$.

$\overline{ON}$ Input

$\overline{ON}$ is a CMOS compatible, active low enable input. It has a default 5µA pull-down to ground. Connect this pin to ground or leave open to enable normal device operation. If it is driven high while the MOSFET is turned on, the MOSFET is turned off gradually with an internal 40µA gate pull-down, minimizing input voltage transients. The LTC4362 then goes into a low current sleep mode, drawing only 1.5µA at IN. When $\overline{ON}$ goes back low, the part restarts with a 130ms delay cycle.

GATEP Control

GATEP has a 2M resistive pull-down to ground and a 5.8V Zener clamp in series with a 200k resistor to IN. It controls the gate of an optional external P-channel MOSFET to provide negative voltage protection. The 2M pull-down turns on the external P-channel MOSFET once V_{IN} is more than the P-channel MOSFET gate threshold voltage. The IN to GATEP Zener protects the external P-channel MOSFET from gate overvoltage by clamping its V_{GS} to 5.8V when V_{IN} goes high.

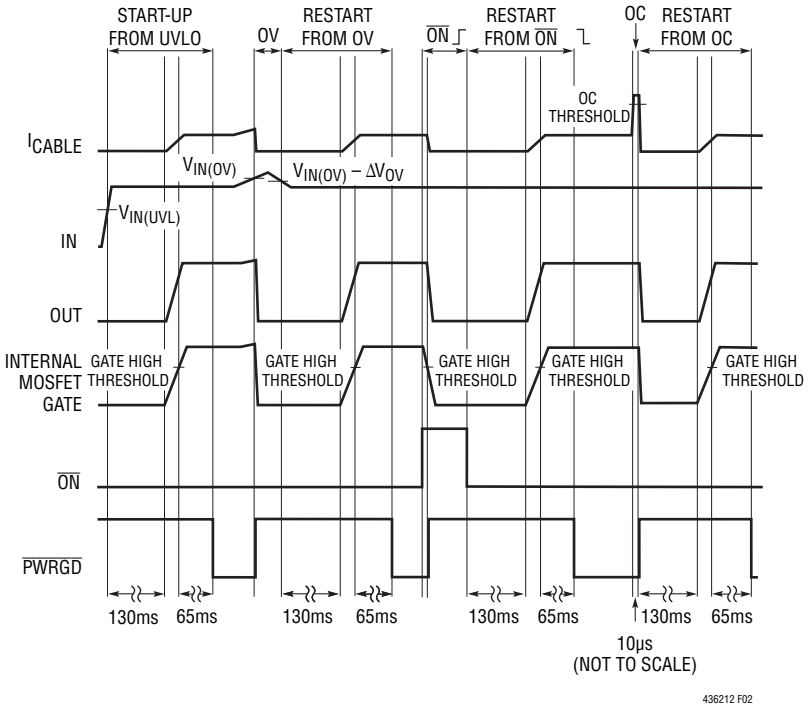


Figure 2. $\overline{PWRGD}$ Behavior

APPLICATIONS INFORMATION

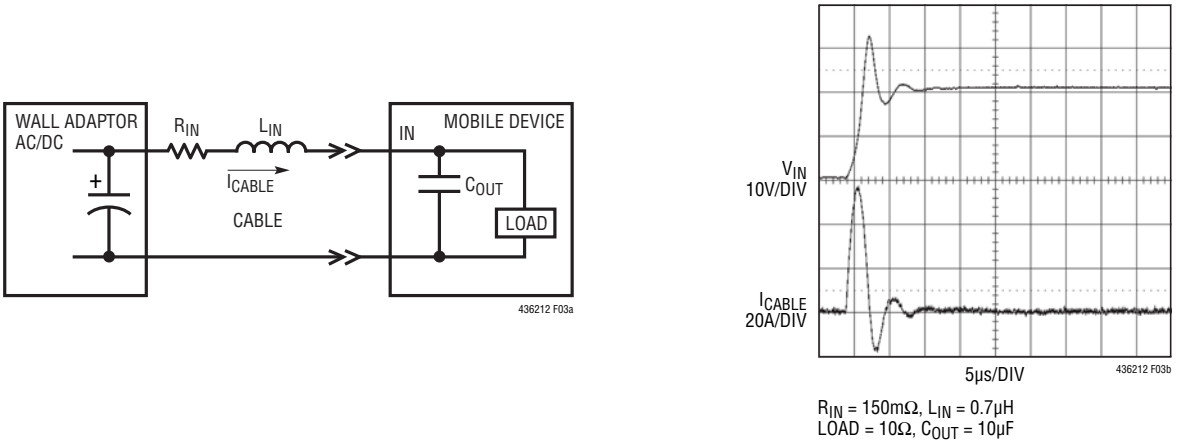


Figure 3. 20V Hot-Plug Into a 10µF Capacitor

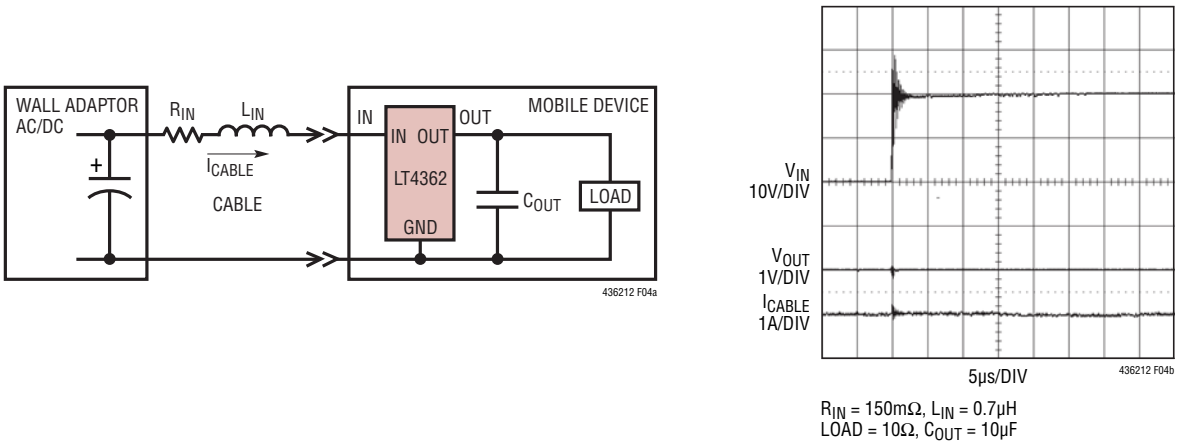


Figure 4. 20V Hot-Plug Into the LTC4362

Thermal Shutdown

The internal N-channel MOSFET is protected by a thermal shutdown circuit. If its temperature reaches 150°C, it will shut off immediately and the $\overline{\text{PWRGD}}$ pull-down releases. It will turn on again after its temperature drops below 140°C.

Input Transients

Figure 3 shows a typical setup when an AC wall adaptor charges a mobile device. The inductor L_{IN} represents the lumped equivalent inductance of the cable and the EMI filter found in some wall adaptors. R_{IN} is the lumped equivalent resistance of the cable, adaptor output capacitor ESR and the connector contact resistance.

L_{IN} and R_{IN} form an LC tank circuit with any capacitance at IN. If the wall adaptor is powered-up first, plugging the wall adaptor output to IN does the equivalent of applying a voltage step to this LC circuit. The resultant voltage overshoot at IN can rise to twice the DC output voltage of the wall adaptor (or more if ceramic capacitors with large voltage coefficients are used) as shown in Figure 3. Figure 4 shows the 20V adaptor output applied to the LTC4362. Due to the low capacitance at the IN pin, the plug-in transient has been brought down to a manageable level.

Input transients also occur when the current through the cable inductance changes abruptly. This can happen when the LTC4362 turns off its internal N-channel MOSFET quickly in an overvoltage or overcurrent event.

APPLICATIONS INFORMATION

Figure 5 shows an input transient after an overcurrent. The current in L_{IN} will cause V_{IN} to overshoot and avalanche the internal N-channel MOSFET to C_{OUT}.

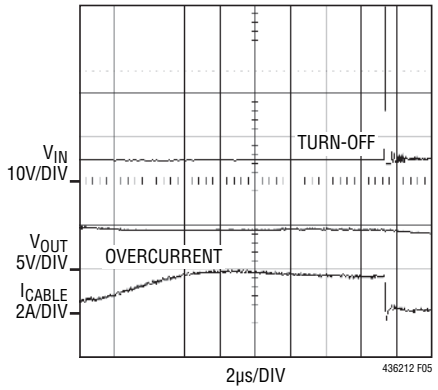


FIGURE 4 CIRCUIT
R_{IN} = 150mΩ, L_{IN} = 0.7µH
LOAD = 10Ω, C_{OUT} = 10µF

Figure 5. Input Transient After Overcurrent

Typically, IN will be clamped to a voltage of V_{OUT} + 1.3•(30V BV_{DSS} of Internal MOSFET) = 45V. The single, nonrepetitive, pulse of energy (E_{AS}) absorbed by the MOSFET during this avalanche breakdown with a peak current I_{AS} is approximated by the formula:

$$E_{AS} = \frac{1}{2} \bullet L_{IN} \bullet I_{AS}^{2}$$

For L_{IN} = 0.7µH and I_{AS} = 3A, then E_{AS} = 3.15µJ. This is within the I_{AS} and E_{AS} capabilities of the internal MOSFET. So in most instances, the LTC4362 can ride through such transients without a bypass capacitor, transient voltage suppressor or other external components at IN.

Figure 6 shows a particularly bad situation which can occur in a mobile device with dual power inputs. A 20V

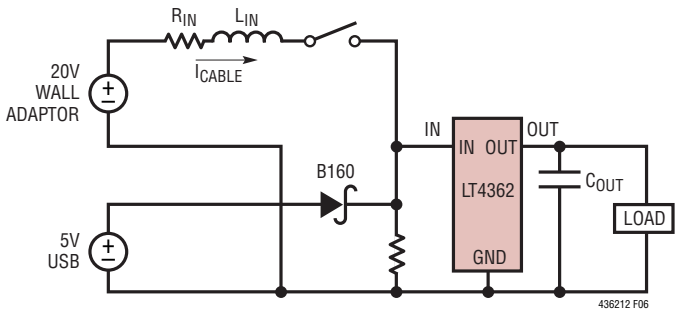
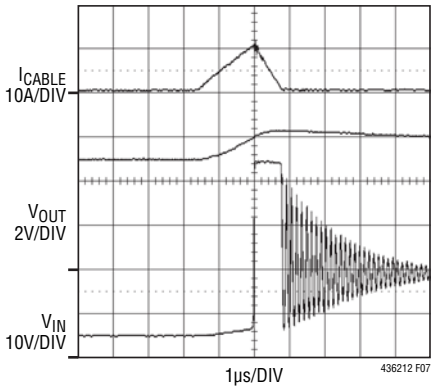


Figure 6. Setup for Testing 20V Plugged into 5V System

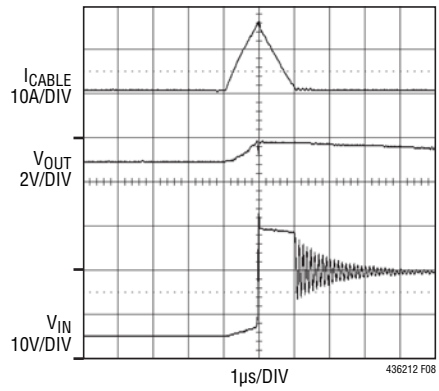
wall adaptor is mistakenly hot-plugged into the 5V device with the USB input already live. As shown in Figure 7, a large current can build up in L_{IN} to charge up C_{OUT}. When the internal MOSFET shuts off, this current is dumped into C_{OUT}, causing a large 40V transient. The LTC4362 limits this to a 1V rise in the output voltage.



R_{IN} = 150mΩ, L_{IN} = 2µH
LOAD = 10Ω
C_{OUT} = 10µF (16V, SIZE 1210)

Figure 7. Overvoltage Protection Waveforms When 20V Plugged into 5V System

If the voltage rise at V_{OUT} due to the discharge of the energy in L_{IN} into C_{OUT} is not acceptable or the avalanche capability of the MOSFET is exceeded, an additional external clamp Z1 such as the SMAJ24A can be placed between IN and GND. Figure 8 shows the resulting waveform.



R_{IN} = 150mΩ, L_{IN} = 0.7µH
LOAD = 10Ω
C_{OUT} = 10µF (16V, SIZE 1210)

Figure 8. Overvoltage Protection Waveforms When 20V Plugged into 5V System with External IN Clamp

APPLICATIONS INFORMATION

C_{OUT} is the decoupling capacitor of the protected circuit and its value is largely determined by the circuit requirements. Using a larger C_{OUT} works with L_{IN} to slow down the dV/dt at OUT, allowing time for the LTC4362 to shut off its MOSFET before V_{OUT} overshoots to a dangerous voltage. A larger C_{OUT} also helps to lower the ΔV_{OUT} due to the discharge of energy in L_{IN} if the MOSFET BV_{DSS} is used as an input clamp.

Layout Considerations

Figure 9 shows an example PCB layout for the LTC4362 with an external P-channel MOSFET for negative voltage protection. Keep the traces to the internal N-channel MOSFET wide and short. The PCB traces associated with the power path through the internal N-channel MOSFET should have low resistance.

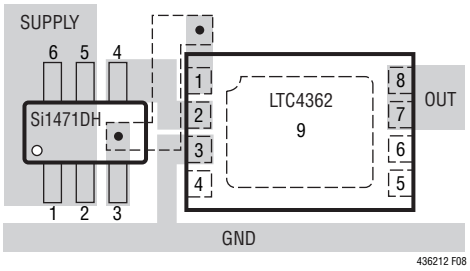


Figure 9. Layout for External P-Channel MOSFET Configuration

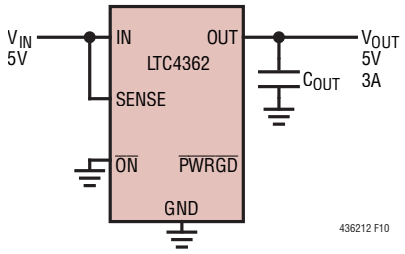
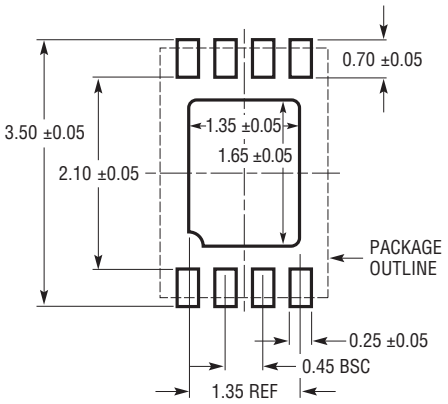


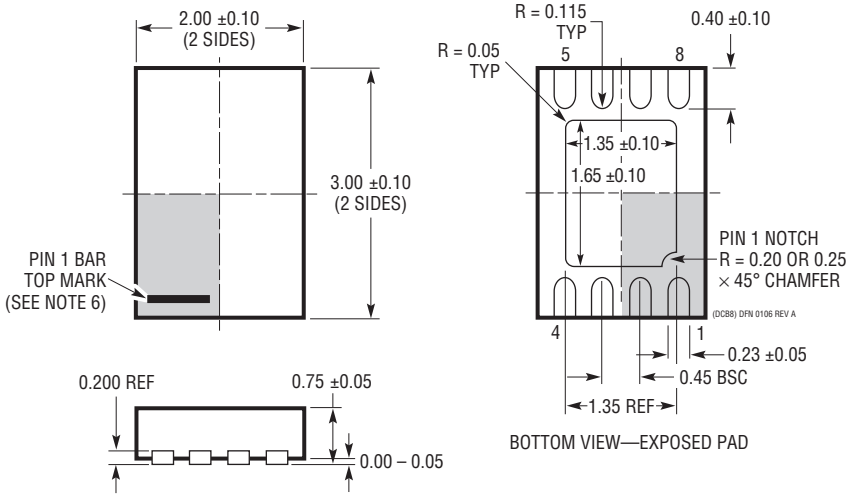
Figure 10. 5V Overvoltage Protection with Overcurrent Disabled

PACKAGE DESCRIPTION

DCB Package
8-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1718 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/11	Revised the Features section.	1
		Revised conditions for $V_{GATEP(CLP)}$, $t_{PWRGD(LH)}$ and $t_{PWRGD(HL)}$ in the Electrical Characteristics section.	3
		Revised Overcurrent in the Applications Information section.	7
B	12/18	Added $V_{IN(OVL)}$ specification, changed ΔV_{OV} maximum limit.	3
		Updated Typical Performance Characteristics.	5
		Added Figure 10.	11