100V Overvoltage, Undervoltage and Reverse Supply Protection Controller

FEATURES

- **Wide Operating Voltage Range: 2.5V to 60V**
- **Overvoltage Protection to 100V**
- **Reverse Supply Protection to –40V**
- **LTC4367: Blocks 50Hz and 60Hz AC Power**
- **LTC4367: 32ms Recovery from Fault**
- **LTC4367-1: Fast 500µs Recovery from Fault**
- **No Input Capacitor or TVS Required for Most Applications**
- Adjustable Undervoltage and Overvoltage Thresholds
- Controls Back-to-Back N-Channel MOSFETs
- Low Operating Current: 70µA
- Low Shutdown Current: 5µA
- 8-Pin MSOP and 3mm × 3mm DFN Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Portable Instrumentation
- Industrial Automation
- Automotive Surge (Load Dump) Protection
- Network Equipment

DESCRIPTION

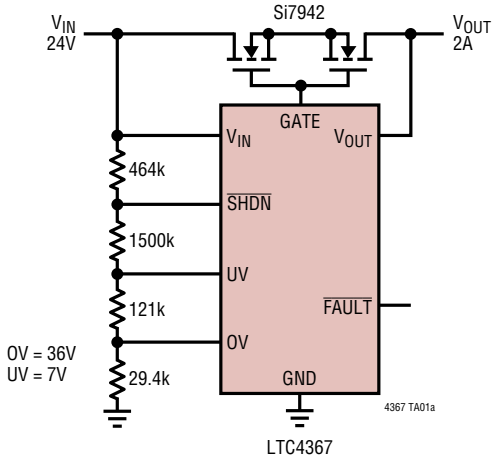
The LTC®4367 protects applications where power supply input voltages may be too high, too low or even negative. It does this by controlling the gate voltages of a pair of external N-channel MOSFETs to ensure that the output stays within a safe operating range.The LTC4367 withstands voltages between –40V and 100V and has an operating range of 2.5V to 60V, while consuming only 70µA in normal operation.

Two comparator inputs allow configuration of the overvoltage (OV) and undervoltage (UV) set points using an external resistive divider. A shutdown pin provides external control for enabling and disabling the MOSFETs as well as placing the device in a low current shutdown state. A fault output indicates that the GATE pin is pulling low when the part is in shutdown or the input voltage is outside the UV and OV set points.

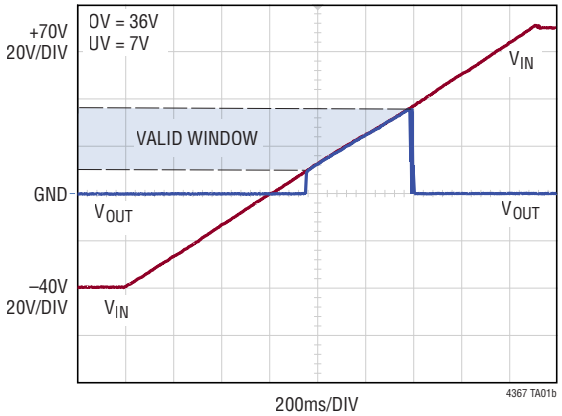
The LTC4367 has a 32ms turn-on delay that debounces live connections and blocks 50Hz to 60Hz AC power. For fast recovery after faults, the LTC4367-1 has a reduced turn-on delay of 500µs.

TYPICAL APPLICATION

24V Automotive Application with +100V, –40V Protection



Load Protected from Reverse and Overvoltage at V_{IN}



Rev. C

ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2)

Supply Voltage
- V_{IN} ..... –40V to 100V

Input Voltages (Note 3)
- UV, $\overline{SHDN}$ ..... –0.3V to 80V
- OV ..... –0.3V to 5V
- V_{OUT} ..... –0.3V to 80V

Output Voltages
- $\overline{FAULT}$ ..... –0.3V to 80V
- GATE (Note 4) ..... –40V to 75V

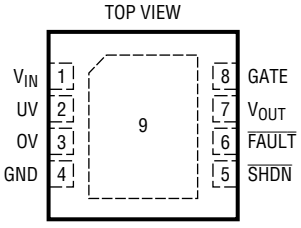
Input Currents
- $\overline{SHDN}$, UV ..... –1mA
- OV ..... –1mA

Operating Ambient Temperature Range
- LTC4367C ..... 0°C to 70°C
- LTC4367I ..... –40°C to 85°C
- LTC4367H ..... –40°C to 125°C

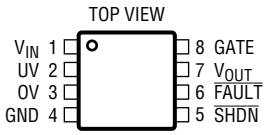
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10sec)
- for MSOP Only ..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
EXPOSED PAD (PIN 9) PCB GROUND CONNECTION OPTIONAL
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 160°C/W

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4367CDD#PBF	LTC4367CDD#TRPBF	LGTF	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4367CDD-1#PBF	LTC4367CDD-1#TRPBF	LGVW	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4367IDD#PBF	LTC4367IDD#TRPBF	LGTF	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4367IDD-1#PBF	LTC4367IDD-1#TRPBF	LGVW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4367HDD#PBF	LTC4367HDD#TRPBF	LGTF	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4367HDD-1#PBF	LTC4367HDD-1#TRPBF	LGVW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4367CMS8#PBF	LTC4367CMS8#TRPBF	LTGTD	8-Lead Plastic MSOP	0°C to 70°C
LTC4367CMS8-1#PBF	LTC4367CMS8-1#TRPBF	LTGVX	8-Lead Plastic MSOP	0°C to 70°C
LTC4367IMS8#PBF	LTC4367IMS8#TRPBF	LTGTD	8-Lead Plastic MSOP	–40°C to 85°C
LTC4367IMS8-1#PBF	LTC4367IMS8-1#TRPBF	LTGVX	8-Lead Plastic MSOP	–40°C to 85°C
LTC4367HMS8#PBF	LTC4367HMS8#TRPBF	LTGTD	8-Lead Plastic MSOP	–40°C to 125°C
LTC4367HMS8-1#PBF	LTC4367HMS8-1#TRPBF	LTGVX	8-Lead Plastic MSOP	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC4367IDD#WPBF	LTC4367IDD#WTRPBF	LGTF	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4367IDD-1#WPBF	LTC4367IDD-1#WTRPBF	LGVW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4367HDD#WPBF	LTC4367HDD#WTRPBF	LGTF	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4367HDD-1#WPBF	LTC4367HDD-1#WTRPBF	LGVW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4367IMS8#WPBF	LTC4367IMS8#WTRPBF	LTGTD	8-Lead Plastic MSOP	–40°C to 85°C
LTC4367IMS8-1#WPBF	LTC4367IMS8-1#WTRPBF	LTGVX	8-Lead Plastic MSOP	–40°C to 85°C
LTC4367HMS8#WPBF	LTC4367HMS8#WTRPBF	LTGTD	8-Lead Plastic MSOP	–40°C to 125°C
LTC4367HMS8-1#WPBF	LTC4367HMS8-1#WTRPBF	LTGVX	8-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.5V to 60V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}, V_{OUT}							
V_{IN}	Input Voltage: Operating Range Protection Range		● ●	2.5 –40		60 100	V V
$V_{IN(UVLO)}$	Input Supply Undervoltage Lockout	V_{IN} Rising	●	1.8	2.2	2.4	V
I_{VIN}	Input Supply Current: On Off	$\overline{SHDN}$ = 2.5V $\overline{SHDN}$ = 0V, V_{IN} = V_{OUT}	● ●		30 5	90 20	µA µA
$I_{VIN(R)}$	Reverse Input Supply Current	V_{IN} = –40V, V_{OUT} = 0V	●		–1.5	–2.5	mA
I_{VOUT}	V_{OUT} Input Current: On Off Reverse	$\overline{SHDN}$ = 2.5V, V_{IN} = V_{OUT} $\overline{SHDN}$ = 0V, V_{IN} = V_{OUT} V_{IN} = –40V, V_{OUT} = 0V	● ● ●		40 3 20	110 15 50	µA µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.5V to 60V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GATE							
ΔV_{GATE}	Gate Drive (GATE – V_{OUT})	V_{IN} = V_{OUT} = 5.0V, I_{GATE} = 0µA, –1µA V_{IN} = V_{OUT} = 12V to 60V, I_{GATE} = 0µA, –1µA	● ●	7.2 10	8.7 11	10.8 13.1	V V
$I_{GATE(UP)}$	Gate Pull Up Current	GATE = 15V, V_{IN} = V_{OUT} = 12V	●	–20	–35	–60	µA
$I_{GATE(SLOW)}$	Gate Slow Pull Down Current	GATE = 20V, V_{IN} = V_{OUT} = 12V	●	50	90	160	µA
$I_{GATE(FAST)}$	Gate Fast Pull Down Current	GATE = 20V, V_{IN} = V_{OUT} = 12V	●	30	60	90	mA
$t_{GATE(SLOW)}$	Slow Turn Off Delay	C_{GATE} = 2.2nF, $\overline{SHDN}$ Falling, V_{IN} = V_{OUT} = 12V	●	150	250	575	µs
$t_{GATE(FAST)}$	Gate Fast Turn Off Delay	C_{GATE} = 2.2nF, UV or OV Fault	●		2	6	µs
$t_{D(ON)}$	GATE Turn-On Delay Time	V_{IN} = 12V, Power Good to ΔV_{GATE} > 0V, C_{GATE} = 2.2nF LTC4367 LTC4367-1	 ● ●	 22 0.2	 32 0.5	 45 1.2	 ms ms
UV, OV							
V_{UV}	UV Input Threshold Voltage	UV Falling	●	492.5	500	507.5	mV
V_{OV}	OV Input Threshold Voltage	OV Rising	●	492.5	500	507.5	mV
V_{UVHYST}	UV Input Hysteresis	V_{IN} = V_{OUT} = 12V	●	20	25	32	mV
V_{OVHYST}	OV Input Hysteresis	V_{IN} = V_{OUT} = 12V	●	20	25	32	mV
I_{LEAK}	UV, OV Leakage Current	V = 0.5V, V_{IN} = 60V	●			±10	nA
t_{FAULT}	UV, OV Fault Propagation Delay	Overdrive = 50mV V_{IN} = V_{OUT} = 12V	●		1	2	µs
$\overline{SHDN}$							
V_{SHDN}	$\overline{SHDN}$ Input Threshold	$\overline{SHDN}$ Falling	●	0.4	0.75	1.2	V
I_{SHDN}	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 10V, V_{IN} = 60V	●			±15	nA
t_{START}	Delay Coming Out of Shutdown Mode	$\overline{SHDN}$ Rising to $\overline{FAULT}$ Released, V_{IN} = V_{OUT} = 12V LTC4367 LTC4367-1	●	 400 125	 800 250	 1400 500	 µs µs
$t_{SHDN(F)}$	$\overline{SHDN}$ to $\overline{FAULT}$ Asserted	V_{IN} = V_{OUT} = 12V	●		1.5	3	µs
t_{LOWPWR}	Delay from Turn Off to Low Power Operation	V_{IN} = V_{OUT} = 12V LTC4367 LTC4367-1	 ● ●	 20 0.125	 32 0.3	 48 0.6	 ms ms
$\overline{FAULT}$							
V_{OL}	$\overline{FAULT}$ Output Voltage Low	I_{FAULT} = 500µA, V_{IN} = 12V	●		0.15	0.4	V
I_{FAULT}	$\overline{FAULT}$ Leakage Current	$\overline{FAULT}$ = 5V, V_{IN} = 60V	●			±200	nA

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

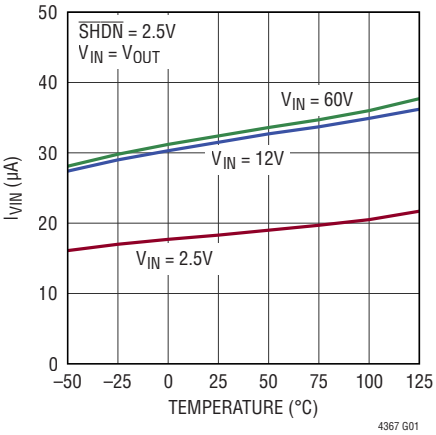
Note 2. All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3. These pins have a diode to GND. They may go below –0.3V if the current magnitude is limited to less than 1mA.

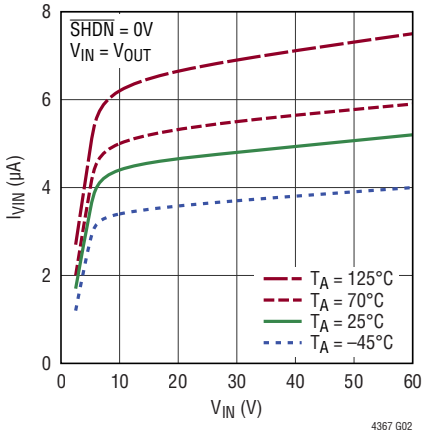
Note 4. The GATE pin is referenced to V_{OUT} and does not exceed 73V for the entire operating range.

TYPICAL PERFORMANCE CHARACTERISTICS

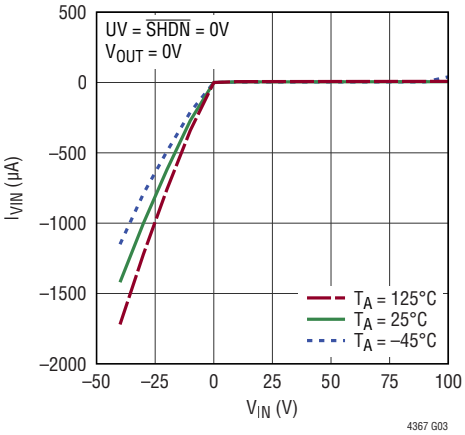
V_{IN} Operating Current vs Temperature



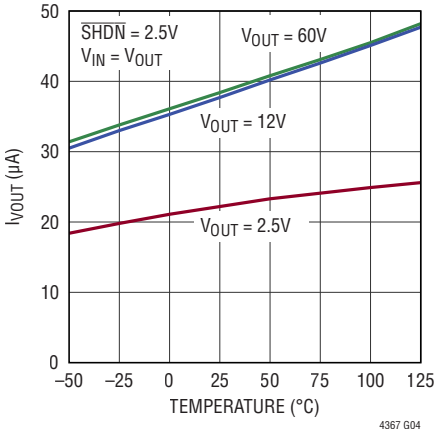
V_{IN} Shutdown Current vs Voltage



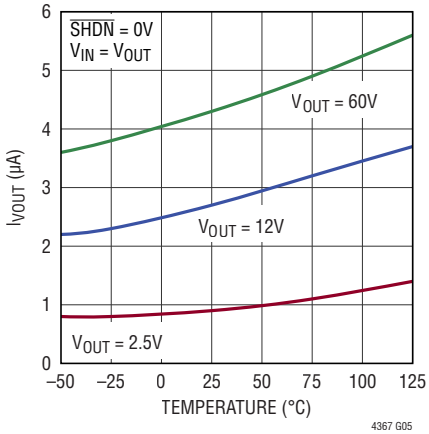
V_{IN} Supply Current vs Voltage (–40V to 100V)



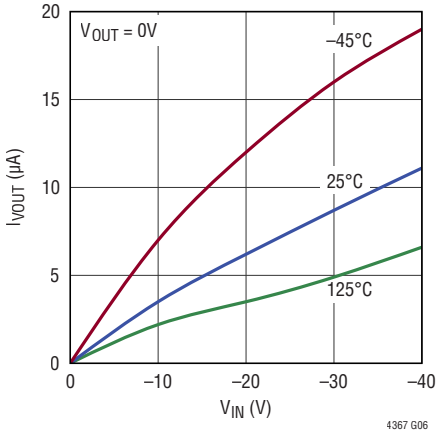
V_{OUT} Operating Current vs Temperature



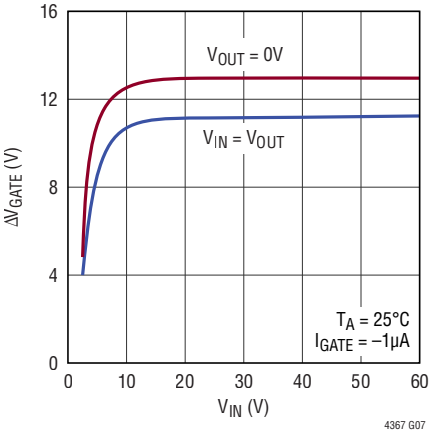
V_{OUT} Shutdown Current vs Temperature



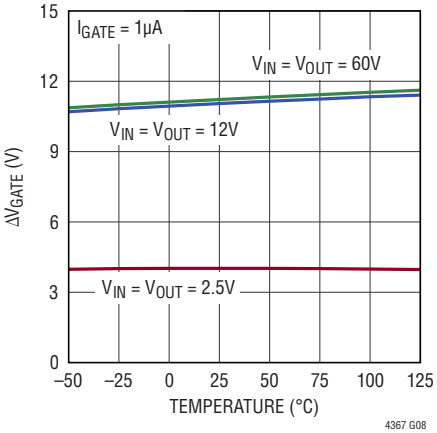
V_{OUT} Current vs Reverse V_{IN}



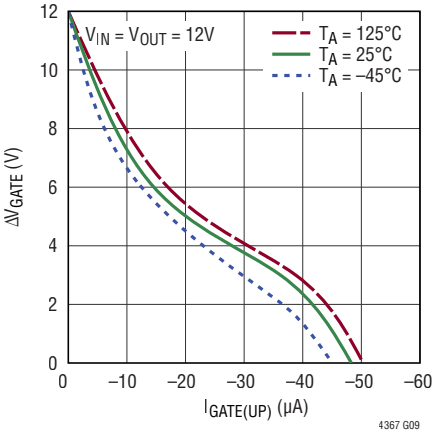
GATE Drive vs V_{IN} Supply Voltage



GATE Drive vs Temperature

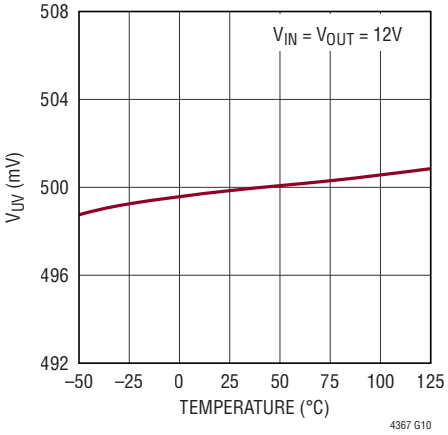


GATE Drive vs GATE Current

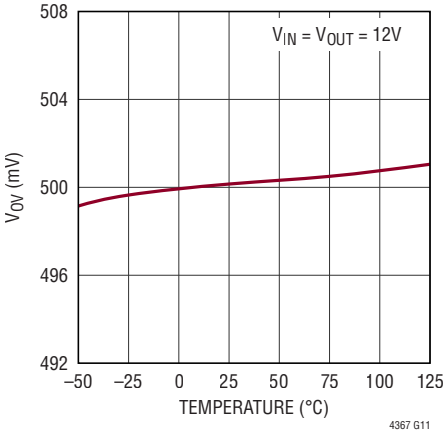


TYPICAL PERFORMANCE CHARACTERISTICS

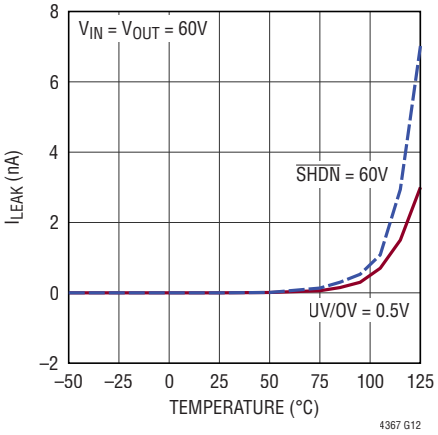
UV Threshold vs Temperature



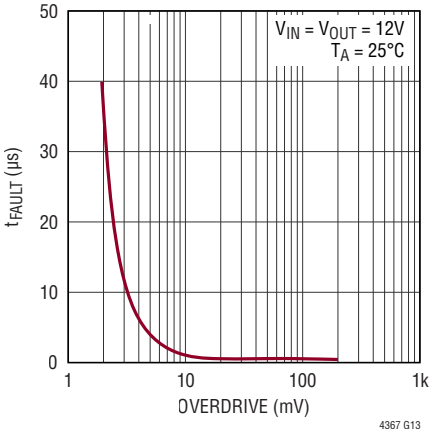
OV Threshold vs Temperature



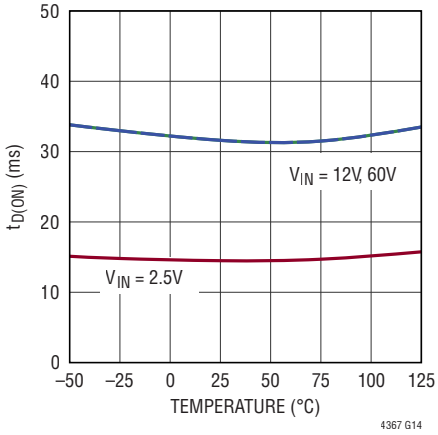
UV/OV/$\overline{SHDN}$ Leakage vs Temperature



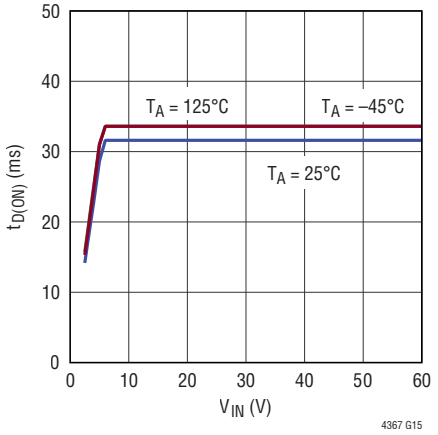
UV/OV Propagation Delay vs Overdrive



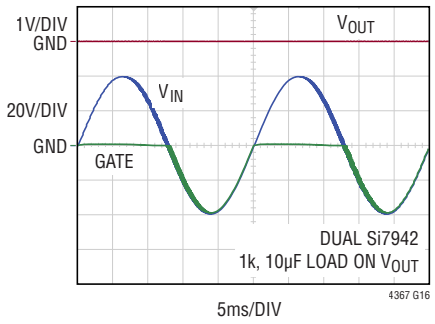
LTC4367 GATE Turn-On Delay Time vs Temperature



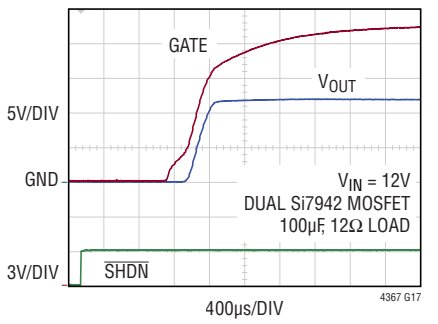
LTC4367 GATE Turn-On Delay Time vs V_{IN}



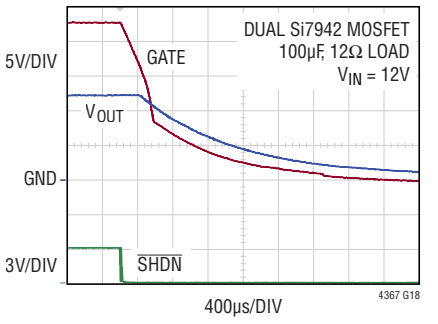
LTC4367 AC Blocking



Turn-On Timing



Turn-Off Timing



PIN FUNCTIONS

Exposed Pad: The exposed pad may be left open or connected to device ground.

$\overline{\text{FAULT}}$: Fault Indication Output. This high voltage open drain output is pulled low if UV is below its monitor threshold, if OV is above its monitor threshold, if $\overline{\text{SHDN}}$ is low, or if V_{IN} has not risen above $V_{IN(UVLO)}$.

GATE: Gate Drive Output for External N-channel MOSFETs. An internal charge pump provides 35µA of pull-up current and up to 13.1V of enhancement to the gate of an external N-channel MOSFET. When turned off, GATE is pulled just below the lower of V_{IN} or V_{OUT}. When V_{IN} goes negative, GATE is automatically connected to V_{IN}.

GND: Device Ground.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider to set the desired V_{IN} overvoltage fault threshold. This input connects to an accurate, fast (1µs) comparator with a 0.5V rising threshold and 25mV of hysteresis. When OV rises above its threshold, a 60mA current sink pulls down on the GATE output. When OV falls back below 0.475V, and after a 32ms GATE turn-on delay waiting period (500µs for LTC4367-1), the GATE charge pump is enabled. The low leakage current of the OV input allows the use of large valued resistors for the external resistive divider. Connect to GND if unused. If the voltage at the OV pin can rise above 5V, place a low leakage Zener clamp on the OV pin.

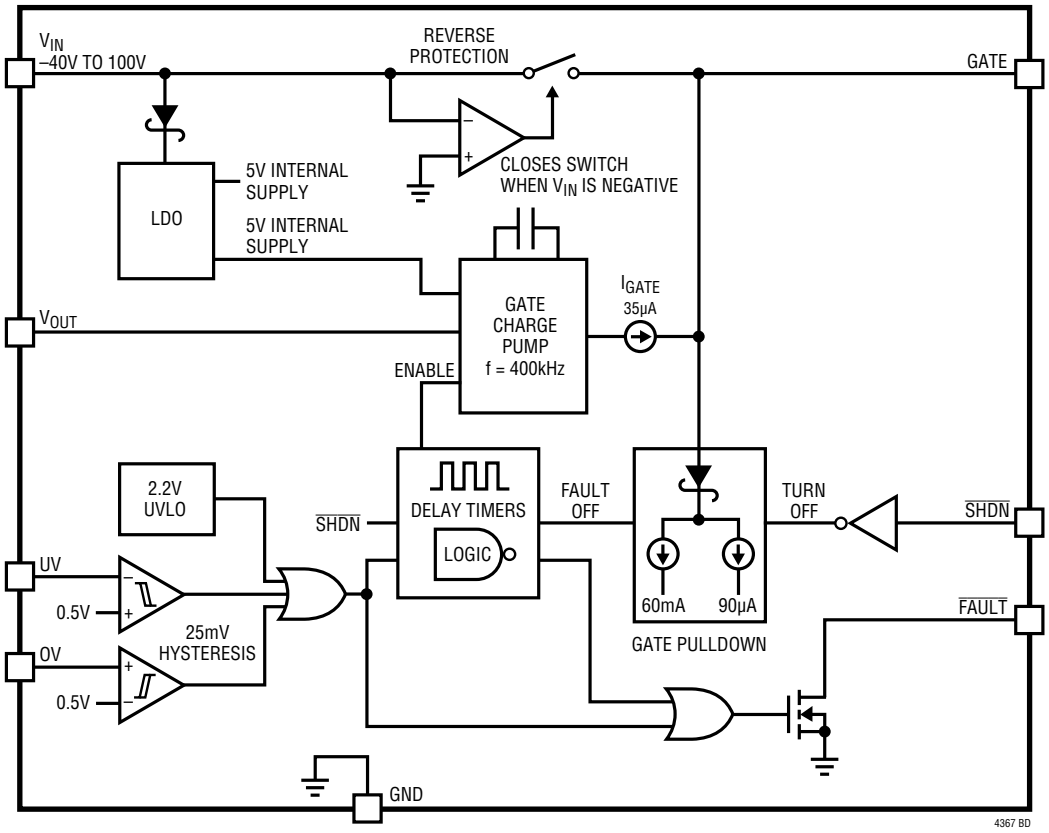
$\overline{\text{SHDN}}$: Shutdown Control Input. $\overline{\text{SHDN}}$ high enables the GATE charge pump which in turn enhances the gate of an external N-channel MOSFET. A low on $\overline{\text{SHDN}}$ generates a pull down on the GATE output with a 90µA current sink and places the LTC4367 in low current mode (5µA). If unused, connect to V_{IN} with a 510k resistor. If V_{IN} goes above 80V, the $\overline{\text{SHDN}}$ pin voltage must be kept below 80V (see Applications Information).

UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider to set the desired V_{IN} undervoltage fault threshold. This input connects to an accurate, fast (1µs) comparator with a 0.5V falling threshold and 25mV of hysteresis. When UV falls below its threshold, a 60mA current sink pulls down on the GATE output. When UV rises back above 0.525V, and after a 32ms GATE turn-on delay waiting period (500µs for LTC4367-1), the GATE charge pump is enabled. The low leakage current of the UV input allows the use of large valued resistors for the external resistive divider. If unused and V_{IN} is less than 80V, connect to V_{IN} with a 510k resistor.

V_{IN}: Power Supply Input. Maximum protection range: –40V to 100V. Operating range: 2.5V to 60V.

V_{OUT}: Output Voltage Sense Input. This pin senses the voltage at the output side of the external N-channel MOSFET. The GATE charge pump voltage is referenced to V_{OUT}. It is used as the charge pump input when V_{OUT} is greater than approximately 5V.

BLOCK DIAGRAM



OPERATION

Many of today's electronic systems get their power from external sources such as AC or wall adaptors, batteries and custom power supplies. Figure 1 shows a supply arrangement using a DC barrel connector. Power is supplied by an AC adaptor or, if the plug is withdrawn, by a removable battery. Note that the polarity of the AC adaptor and barrel connector varies by manufacturer. Trouble arises when any of the following occurs:

- The battery is installed backwards
- An AC adaptor of opposite polarity is attached
- An AC adaptor of excessive voltage is attached
- The battery is discharged below a safe level

This can lead to supply voltages that are too high, too low, or even negative. If these power sources are applied directly to the electronic systems, the systems could be subject to damage. The LTC4367 is an input voltage fault protection N-channel MOSFET controller. The part isolates an input supply from its load to protect the load from unexpected supply voltage conditions, while providing a low loss path for qualified power.

In the past, to protect electronic systems from improperly connected power supplies, system designers often added discrete diodes, transistors and high voltage comparators. The high voltage comparators enable system power only if the input supply falls within a desired voltage window. A Schottky diode or P-channel MOSFET typically added in series with the supply protects against reverse supply connections.

The LTC4367 provides accurate overvoltage and undervoltage comparators to ensure that power is applied to the system only if the input supply meets the user selectable voltage window. Reverse supply protection circuits automatically isolate the load from negative input voltages. During normal operation, a high voltage charge pump enhances the gate of external N-channel power MOSFETs. Power consumption is 5µA during shutdown and 70µA while operating. The LTC4367 integrates all these functions in 8-lead MSOP and 3mm × 3mm DFN packages.

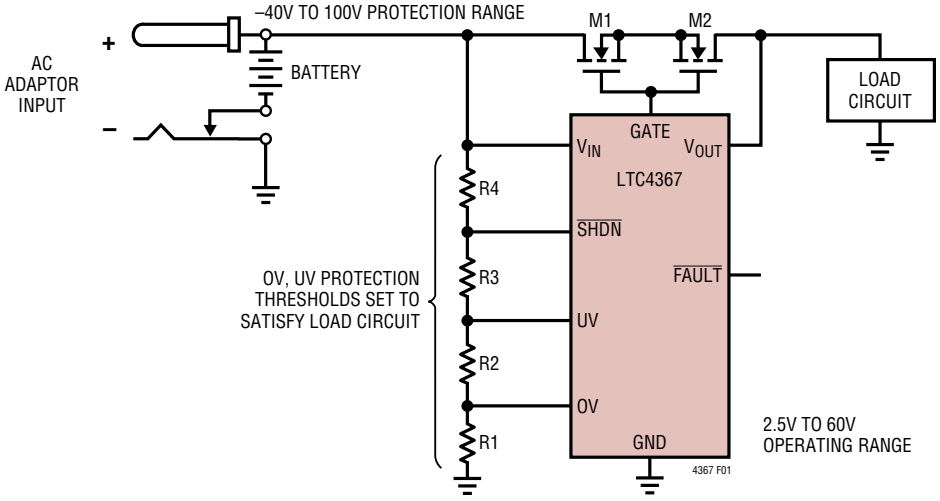


Figure 1. Polarity Protection for DC Barrel Connectors

APPLICATIONS INFORMATION

The LTC4367 is an N-channel MOSFET controller that protects a load from faulty supply connections. A basic application circuit using the LTC4367 is shown in Figure 2 The circuit provides a low loss connection from V_{IN} to V_{OUT} as long as the voltage at V_{IN} is between 3.5V and 18V. Voltages at V_{IN} outside of the 3.5V to 18V range are prevented from getting to the load and can be as high as 100V and as low as –40V. The circuit of Figure 2 protects against negative voltages at V_{IN} as shown. No other external components are needed.

During normal operation, the LTC4367 provides up to 13.1V of gate enhancement to the external back-to-back N-channel MOSFETs. This turns on the MOSFETs, thus connecting the load at V_{OUT} to the supply at V_{IN}.

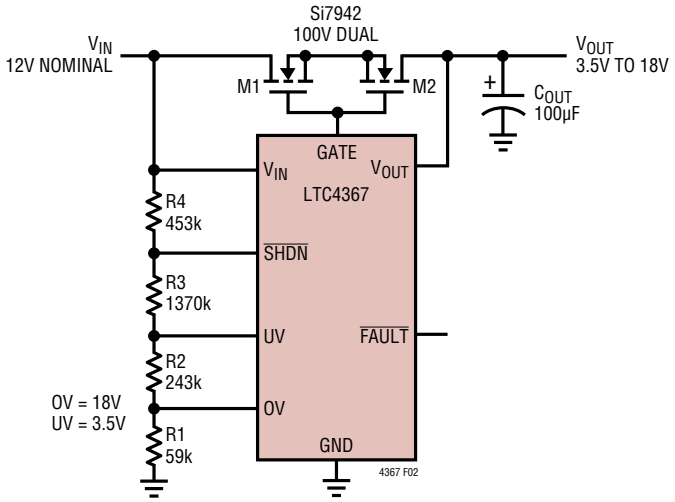


Figure 2. LTC4367 Protects Load from –40V to 100V V_{IN} Faults

GATE Drive

The LTC4367 turns on the external N-channel MOSFETs by driving the GATE pin above V_{OUT}. The voltage difference between the GATE and V_{OUT} pins (gate drive) is a function of V_{IN} and V_{OUT}.

Figure 3 highlights the dependence of the gate drive on V_{IN} and V_{OUT}. When system power is first turned on ($\overline{SHDN}$ low to high, V_{OUT} = 0V), gate drive is at a maximum for all values of V_{IN}. This helps prevent start-up problems into heavy loads by ensuring that there is enough gate drive to support the load.

As V_{OUT} ramps up from 0V, the absolute value of the GATE voltage remains fixed until V_{OUT} is greater than the lower of (V_{IN} – 1V) or 5V. Once V_{OUT} crosses this threshold, gate drive begins to increase up to a maximum of 13.1V (for $V_{IN} \geq$ 12V). The curves of Figure 3 were taken with a GATE load of –1µA. If there were no load on GATE, the gate drive for each V_{IN} would be slightly higher.

Note that when V_{IN} is at the lower end of the operating range, the external N-channel MOSFET must be selected with a corresponding lower threshold voltage.

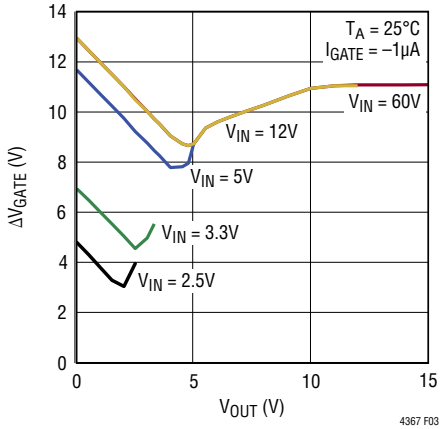


Figure 3. Gate Drive (GATE – V_{OUT}) vs V_{OUT}

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Table 1 lists some external MOSFETs compatible with different V_{IN} supply voltages.

Table 1. Dual MOSFETs for Various Supply Ranges

V_{IN}	MOSFET	$V_{TH(MAX)}$	$V_{GS(MAX)}$	$V_{DS(MAX)}$	$R_{DS(ON)}$ (Ω)
2.5V	SiA920	0.7V	5V	8V	0.027
3.3V	SiA910	1.0V	8V	12V	0.028
3.3V	Si6926	1.0V	8V	20V	0.030
5V	SiA906	1.4V	12V	20V	0.046
5V	Si9926	1.5V	12V	20V	0.018
>12V	SiZ340	2.4V	20V	30V	0.010
>12V	Si4288	2.5V	20V	40V	0.020
>12V	Si7220	3V	20V	60V	0.060
>12V	Si4946	3V	20V	60V	0.040
>12V	FDS3890	4V	20V	80V	0.044
>12V	Si7942	4V	20V	100V	0.049
>12V	FDS3992	4V	20V	100V	0.054
>12V	Si7956	4V	20V	150V	0.105

Overvoltage and Undervoltage Protection

The LTC4367 provides two accurate comparators to monitor for overvoltage (OV) and undervoltage (UV) conditions at V_{IN}. If the input supply rises above the user adjustable OV threshold, the gate of the external MOSFET is quickly turned off, thus disconnecting the load from the input. Similarly, if the input supply falls below the user adjustable UV threshold, the gate of the external MOSFET also is quickly turned off. Figure 4 shows a UV/OV application for an input supply of 12V.

The external resistive divider allows the user to select an input supply range that is compatible with the load at V_{OUT}. Furthermore, the UV and OV inputs have very low leakage currents (typically < 1nA at 100°C), allowing for large values in the external resistive divider. In the application of Figure 4, the load is connected to the supply only if V_{IN} lies between 3.5V and 18V. In the event that V_{IN} goes above 18V or below 3.5V, the gate of the external N-channel MOSFET is immediately discharged with a 60mA current sink, thus isolating the load from the supply.

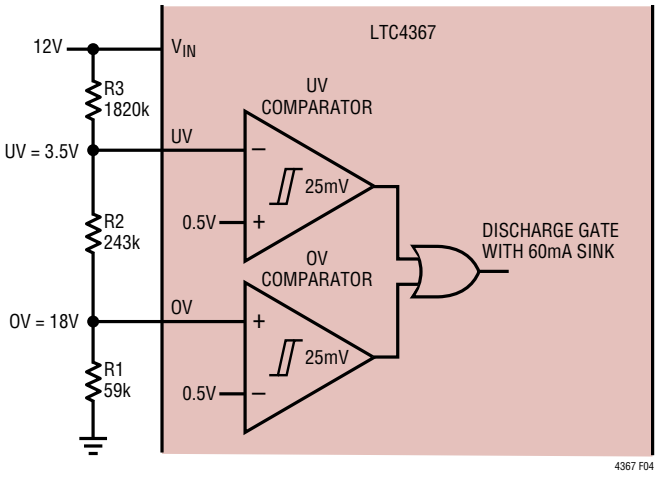

Figure 4. UV, OV Comparators Monitor 12V Supply

APPLICATIONS INFORMATION

Figure 5 shows the timing associated with the UV pin. Once a UV fault propagates through the UV comparator (t_{FAULT}), the $\overline{FAULT}$ output is asserted low and a 60mA current sink discharges the GATE pin. As V_{OUT} falls, the GATE pin tracks V_{OUT}.

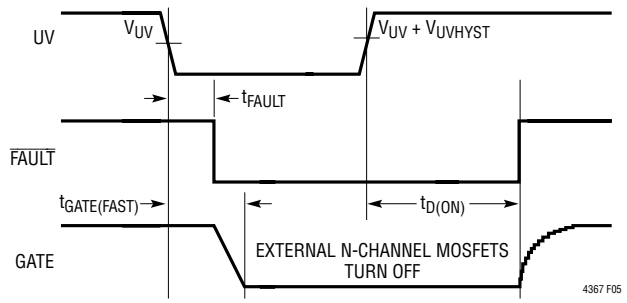

Figure 5. UV Timing (OV < (V_{OV} – V_{OVHYST}), $\overline{SHDN}$ > 1.2V)

Figure 6 shows the timing associated with the OV pin. Once an OV fault propagates through the OV comparator (t_{FAULT}), the $\overline{FAULT}$ output is asserted low and a 60mA current sink discharges the GATE pin. As V_{OUT} falls, the GATE pin tracks V_{OUT}.

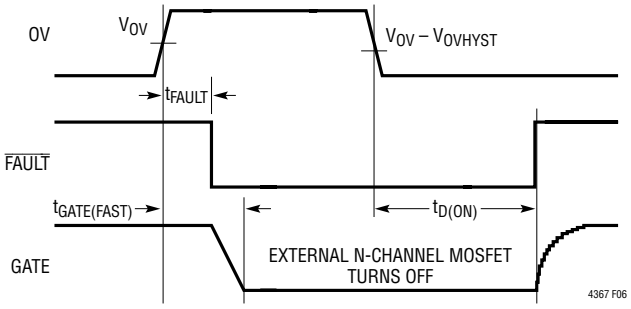

Figure 6. OV Timing (UV > (V_{UV} + V_{UVHYST}), $\overline{SHDN}$ > 1.2V)

When both the UV and OV faults are removed, the external MOSFET is not immediately turned on. The input supply must remain within the user selected power good window for at least 32ms ($t_{D(ON)}$) before the load is again connected to the supply. This GATE turn-on delay period filters noise (including line noise) at the input supply and prevents chattering of power at the load. For applications that require faster turn-on after a fault, the LTC4367-1 provides a 500µs GATE turn-on delay.

Procedure for Selecting UV/OV External Resistor Values

The following 3-step procedure helps select the resistor values for the resistive divider of Figure 4. This procedure minimizes UV and OV offset errors caused by leakage currents at the respective pins.

1. Choose maximum tolerable offset error at the UV pin, $V_{OS(UV)}$. Divide by the worst case leakage current at the UV pin, I_{LEAK} (10nA). Set the sum of R1 + R2 equal to $V_{OS(UV)}$ divided by 10nA. Note that due to the presence of R3, the actual offset at UV will be slightly lower:

$$R1 + R2 = \frac{V_{OS(UV)}}{I_{LEAK}}$$

2. Select the desired V_{IN} UV trip threshold, UV_{TH}. Find the value of R3:

$$R3 = \frac{V_{OS(UV)}}{I_{LEAK}} \bullet \left(\frac{UV_{TH} - 0.5V}{0.5V} \right)$$

3. Select the desired V_{IN} OV trip threshold, OV_{TH}. Find the values of R1 and R2:

$$R1 = \frac{\left(\frac{V_{OS(UV)}}{I_{LEAK}} + R3 \right)}{OV_{TH}} \bullet 0.5V$$

$$R2 = \frac{V_{OS(UV)}}{I_{LEAK}} - R1$$

The example of Figure 4 uses standard 1% resistor values. The following parameters were selected:

$V_{OS(UV)}$ = 3mV

I_{LEAK} = 10nA

UV_{TH} = 3.5V

OV_{TH} = 18V

APPLICATIONS INFORMATION

The resistor values can then be solved:

$$1.\ R1+R2=\frac{3mV}{10nA}=300k$$

$$2.\ R3=\frac{3mV}{10nA}\bullet\frac{(3.5V-0.5V)}{0.5V}=1.8M$$

The closest 1% value: R3 = 1.82M:

$$3.\ R1=\frac{300k+1.82M}{2\bullet 18V}=58.9k$$

The closest 1% value: R1 = 59k:

R2 = 300k – 59k = 241k

The closest 1% value: R2 = 243k

Therefore: OV = 17.93V, UV = 3.51V.

Reverse V_{IN} Protection

The LTC4367's rugged and hot-swappable V_{IN} input helps protect the more sensitive circuits at the output load. If the input supply is plugged in backwards, or a negative supply is inadvertently connected, the LTC4367 prevents this negative voltage from passing to the output load.

The LTC4367 employs a novel, high speed reverse supply voltage monitor. When the negative V_{IN} voltage is detected, an internal switch connects the gates of the external back-to-back N-channel MOSFETs to the negative input supply.

As shown in Figure 7, external back-to-back N-channel MOSFETs are required for reverse supply protection. When V_{IN} goes negative, the reverse V_{IN} comparator closes the internal switch, which in turn connects the gates of the external MOSFETs to the negative V_{IN} voltage. The body diode (D1) of M1 turns on, but the body diode (D2) of M2 remains in reverse blocking mode. This means that the common source connection of M1 and M2 remains about a diode drop higher than V_{IN}. Since the gate voltage of M2 is shorted to V_{IN}, M2 will be turned off and no current can flow from V_{IN} to the load at V_{OUT}. Note that the voltage rating of M2 must withstand the reverse voltage excursion at V_{IN}.

Figure 8 illustrates the waveforms that result when V_{IN} is hot plugged to –20V. V_{IN}, GATE and V_{OUT} start out at ground just before the connection is made. Due to the parasitic inductance of the V_{IN} and GATE connections, the voltage at the V_{IN} and GATE pins ring significantly below –20V. Therefore, a 40V N-channel MOSFET was selected to survive the overshoot.

The speed of the LTC4367 reverse protection circuits is evident by how closely the GATE pin follows V_{IN} during the negative transients. The two waveforms are almost indistinguishable on the scale shown.

The trace at V_{OUT}, on the other hand, does not respond to the negative voltage at V_{IN}, demonstrating the desired reverse supply protection. The waveforms of Figure 8 were captured using a 40V dual N-channel MOSFET, a 10µF ceramic output capacitor and no load current on V_{OUT}.

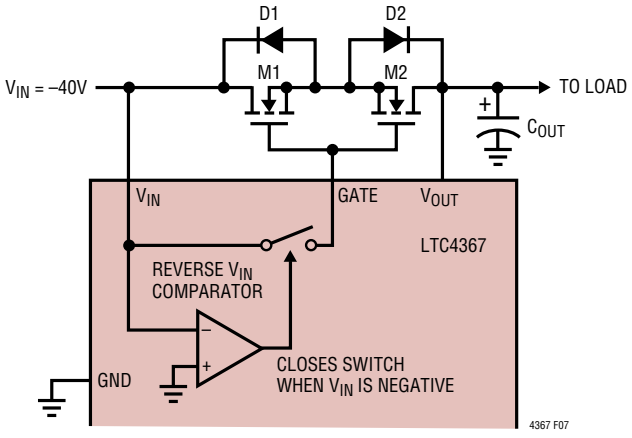

Figure 7. Reverse V_{IN} Protection Circuits

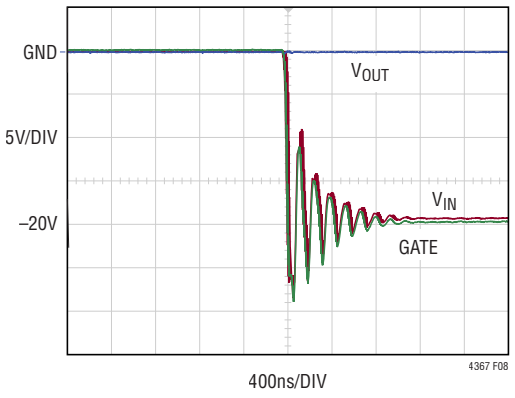

Figure 8. Hot Swapping V_{IN} to –20V

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GATE Turn-On Delay Timer

The LTC4367 has a GATE turn-on delay timer that filters noise at V_{IN} and helps prevent chatter at V_{OUT}. After either an OV or UV fault has occurred, the input supply must return to the desired operating voltage window for at least 32ms ($t_{D(ON)}$) in order to turn the external MOSFET back on as illustrated in Figure 5 and Figure 6. For applications that require faster turn-on after a fault, the LTC4367-1 provides a 500µs GATE turn-on delay.

Going out of and then back into fault in less than $t_{D(ON)}$ will keep the MOSFET off continuously. Similarly, coming out of shutdown ($\overline{SHDN}$ low to high) triggers an 800µs start-up delay timer (see Figure 11).

The GATE turn-on delay timer is also active while the part is powering up. The timer starts once V_{IN} rises above $V_{IN(UVLO)}$ and V_{IN} lies within the user selectable UV/OV power good window. See Figure 9.

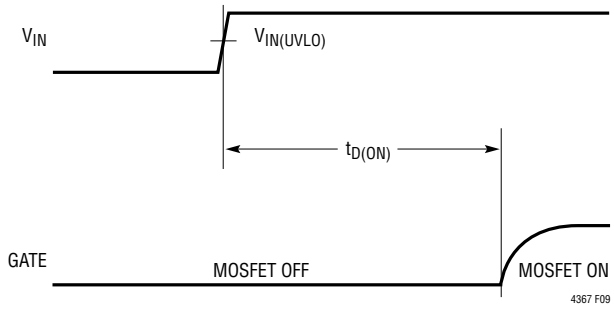


Figure 9. GATE Turn-On Delay Timing During Power-On (OV = GND, UV = $\overline{SHDN}$ = V_{IN})

Shutdown

The $\overline{SHDN}$ input turns off the external MOSFETs in a controlled manner. When $\overline{SHDN}$ is asserted low, a 90µA current sink slowly begins to turn off the external MOSFETs.

Once the voltage at the GATE pin falls below the voltage at the V_{OUT} pin, the current sink is throttled back and a feedback loop takes over. This loop forces the GATE voltage to track V_{OUT}, thus keeping the external MOSFETs off as V_{OUT} decays. Note that when V_{OUT} < 2.2V, the GATE pin is pulled to within 400mV of ground.

Weak gate turn off reduces load current slew rates and mitigates voltage spikes due to parasitic inductances. To further decrease GATE pin slew rate, place a capacitor across the gate and source terminals of the external MOSFETs. The waveforms of Figure 10 were captured using the Si7942 dual N-channel MOSFETs, and a 2A load with 100µF output capacitor.

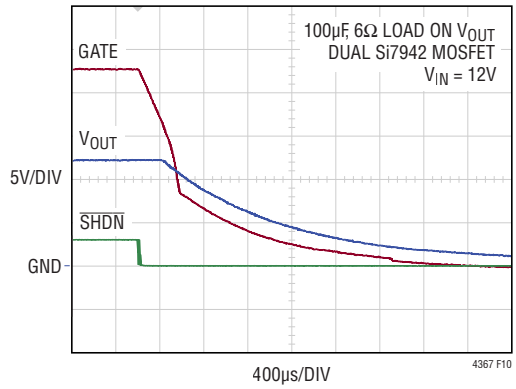


Figure 10. Shutdown: GATE Tracks V_{OUT} as V_{OUT} Decays

FAULT Status

The $\overline{FAULT}$ high voltage open drain output is driven low if $\overline{SHDN}$ is asserted low, if V_{IN} is outside the desired UV/OV voltage window, or if V_{IN} has not risen above $V_{IN(UVLO)}$. Figure 5, Figure 6 and Figure 11 show the $\overline{FAULT}$ output timing.

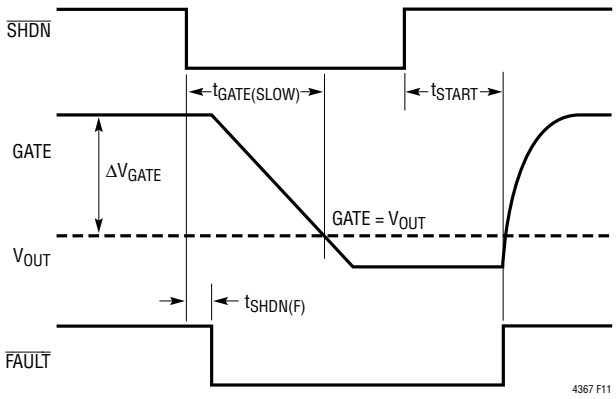


Figure 11. Shutdown Timing

Select Between Two Input Supplies

With the part in shutdown, the V_{IN} and V_{OUT} pins can be driven by separate power supplies. The LTC4367 then automatically drives the GATE pin just below the lower of

APPLICATIONS INFORMATION

the two supplies, thus turning off the external back-to-back MOSFETs. The application of Figure 12 uses two LTC4367s to select between two power supplies. Care should be taken to ensure that only one of the two LTC4367s is enabled at any given time.

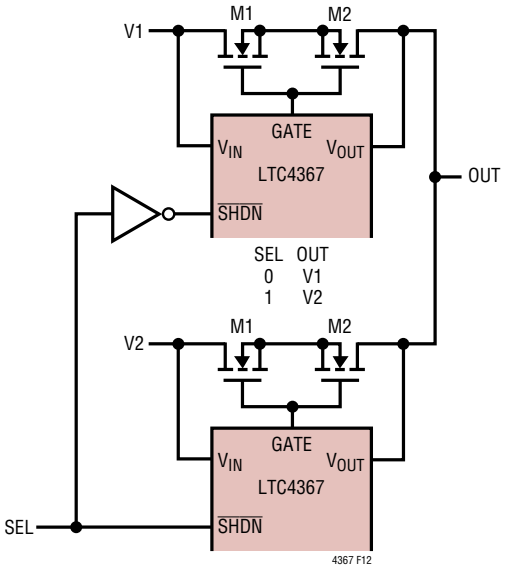


Figure 12. Selecting One of Two Supplies

Single MOSFET Application

When reverse V_{IN} protection is not needed, a single external N-channel MOSFET may be used. The application circuit of Figure 13 connects the load to V_{IN} when V_{IN} is less than 30V, and uses the minimal set of external components.

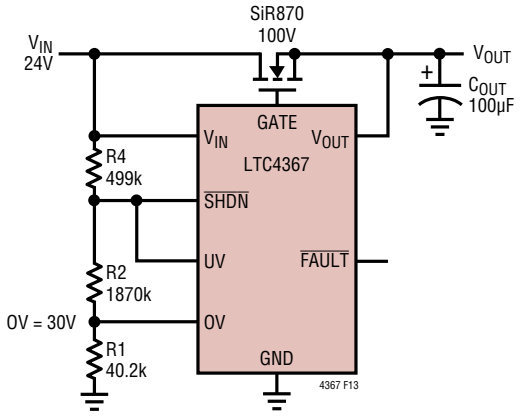


Figure 13. Single MOSFET Application Protects Against 100V

Limiting Inrush Current During Turn-On

The LTC4367 turns on the external N-channel MOSFET with a 35µA current source. The maximum slew rate at the GATE pin can be reduced by adding a capacitor on the GATE pin:

$$\text{Slew Rate} = \frac{35\mu A}{C_{GATE}}$$

Since the MOSFET acts like a source follower, the slew rate at V_{OUT} equals the slew rate at GATE.

Therefore, inrush current is given by:

$$I_{INRUSH} = \frac{C_{OUT}}{C_{GATE}} \bullet 35\mu A$$

For example, a 1A inrush current to a 330µF output capacitance requires a GATE capacitance of:

$$C_{GATE} = \frac{35\mu A \bullet C_{OUT}}{I_{INRUSH}}$$

$$C_{GATE} = \frac{35\mu A \bullet 330\mu F}{1A} = 11.6nF$$

The 12nF C_{GATE} capacitor in the application circuit of Figure 14 limits the inrush current to just under 1A. R_{GATE} makes sure that C_{GATE} does not affect the fast GATE turn off characteristics during UV/OV faults, or during reverse V_{IN} connection. R5A and R5B help prevent high frequency oscillations with the external N-channel MOSFET and related board parasitics.

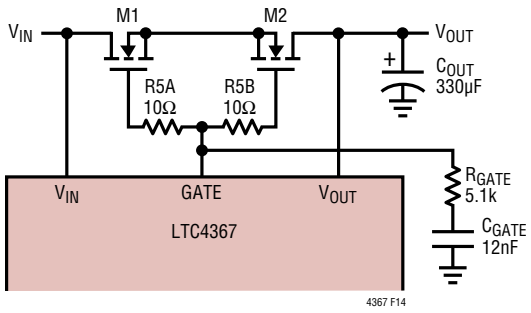


Figure 14. Limiting Inrush Current with C_{GATE}

APPLICATIONS INFORMATION

Transients During OV Fault

The circuit of Figure 15 is used to display transients during an overvoltage condition. The nominal input supply is 48V and it has an overvoltage threshold of 60V. The parasitic inductance is that of a 1 foot wire (roughly 300nH). Figure 16 shows the waveforms during an overvoltage condition at V_{IN}. These transients depend on the parasitic inductance and resistance of the wire along with the capacitance at the V_{IN} node. D1 is an optional power clamp (TVS, TransZorb) recommended for applications where V_{IN} can ring above 100V. No clamp was used to capture the waveforms of Figure 16. In order to maintain reverse supply protection, D1 must be a bidirectional clamp rated for at least 225W peak pulse power dissipation.

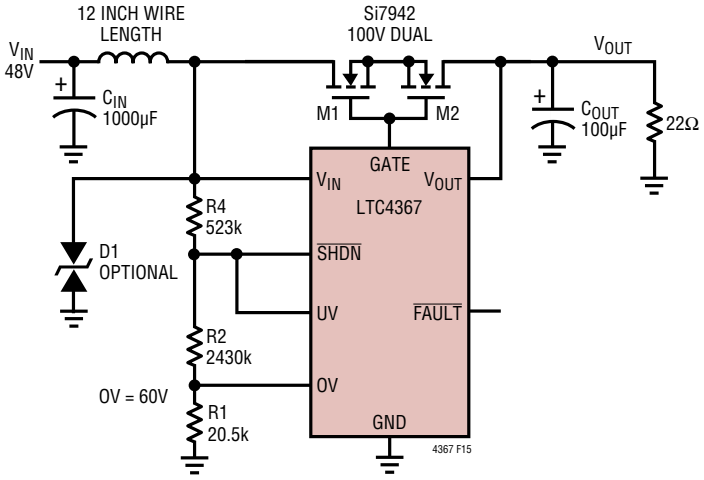


Figure 15. OV Fault with Large V_{IN} Inductance

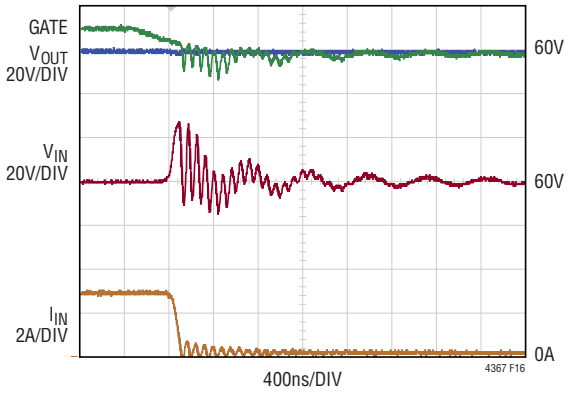


Figure 16. Transients During OV Fault When No TransZorb (TVS) Is Used

APPLICATIONS INFORMATION

REGULATOR APPLICATIONS

Hysteretic Regulator

Built-in hysteresis and the availability of both inverting and noninverting control inputs (OV and UV) facilitate the design of hysteretic regulators. Figure 17 shows how the LTC4367-1 can protect a load from OV transients, while regulating the output voltage at a user-defined level. When the output voltage reaches its OV limit, the LTC4367-1 turns off the external MOSFETs. The load current then discharges the output capacitance until OV falls below the hysteresis voltage. The external MOSFETs are turned back on after a 500µs delay. Figure 18 shows the waveforms for the circuit of Figure 17. The voltage spikes on V_{IN} result from the parasitic inductance of the V_{IN} connector. See Transient During 0V Fault section for more details.

Solar Charger

Figure 19 shows a series regulator for a solar charger. The LTC4367-1 connects the solar charger to the battery when the battery voltage falls below 13.9V (after a 500µs delay). Conversely, when the battery reaches 14.6V, the LTC4367-1 immediately (2µs) opens the charging path.

Regulation of the battery voltage is achieved by connecting a resistive divider from the battery to the accurate OV comparator input (with 5% hysteresis). The fast rising response of the OV comparator prevents the battery voltage from rising above the user-selected threshold.

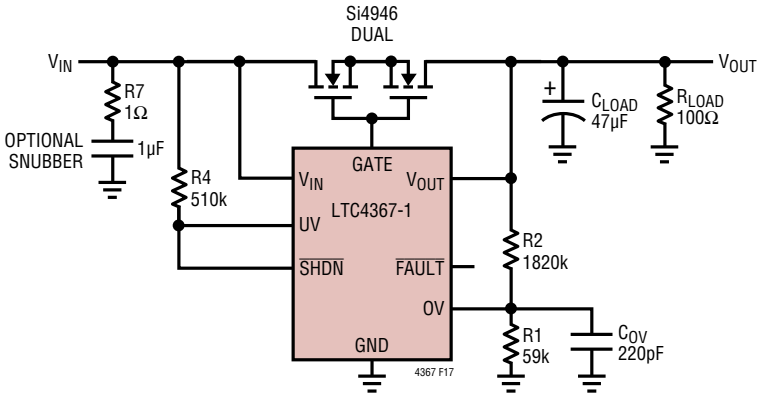


Figure 17. Hysteretic Regulation of V_{OUT} During OV Transients

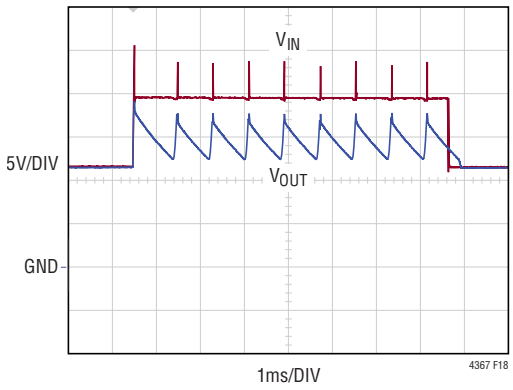


Figure 18. V_{OUT} Regulates at 16V When V_{IN} Rises Above Desired Level

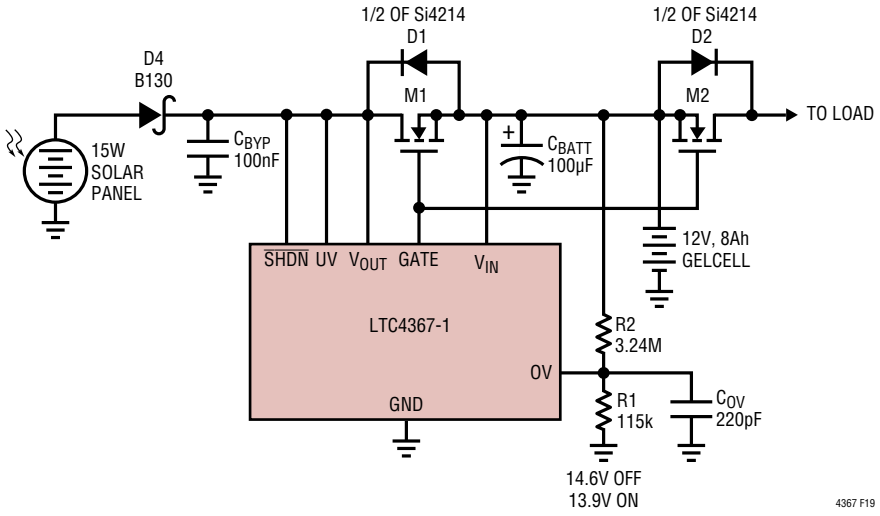


Figure 19. Series Hysteretic Solar Charger with Reverse-Battery and Solar Panel Protection

APPLICATIONS INFORMATION

Note that during initial start-up, the LTC4367-1 will not turn on the external MOSFETs until a battery is first connected to the V_{IN} pin. To begin operation, V_{IN} must initially rise above the 2.2V UVLO lockout voltage. Connecting the battery ensures that the LTC4367-1 comes out of UVLO.

12V Application with 150V Transient Protection

Figure 20 shows a 12V application that withstands input supply transients up to 150V. When the input voltage exceeds 17.9V, the OV resistive divider turns off the external MOSFETs. As V_{IN} rises to 150V, the gate of transistor M1 remains in the Off condition, thus preventing conduction from V_{IN} to V_{OUT}. Note that M1 must have an operating range above 150V.

Resistor R6 and diode D3 clamp the LTC4367 supply voltage to 50V. To prevent R6 from interfering with reverse operation, the recommended value is 1k or less. Note that the power handling capability of R6 must be considered in order to avoid overheating during transients. D3 is shown as a bidirectional clamp in order to achieve reverse-polarity protection at V_{IN}. M2 is also required in order to protect V_{OUT} from negative voltages at V_{IN} and should have an operating range beyond the breakdown of D3. If reverse protection is not desired remove M2 and connect the source of M1 directly to V_{OUT}.

MOSFET Selection

To protect against a negative voltage at V_{IN}, the external N-channel MOSFETs must be configured in a back-to-back arrangement. Dual N-channel packages are thus the best choice. The MOSFET is selected based on its power handling capability, drain and gate breakdown voltages, and threshold voltage.

The drain to source breakdown voltage must be higher than the maximum voltage expected between V_{IN} and V_{OUT}. Note that if an application generates high energy transients during normal operation or during hot swap, the external MOSFET must be able to withstand this transient voltage.

Due to the high impedance nature of the charge pump that drives the GATE pin, the total leakage on the GATE pin must be kept low. The gate drive curves of Figure 3 were measured with a 1µA load on the GATE pin. Therefore, the leakage on the GATE pin must be no greater than 1µA in order to match the curves of Figure 3. Higher leakage currents will result in lower gate drive. The dual N-channel MOSFETs shown in Table 1 all have a maximum gate leakage current of 100nA. Additionally, Table 1 lists representative MOSFETs that would work at different values of V_{IN}.

Layout Considerations

The trace length between the V_{IN} pin and the drain of the external MOSFET should be minimized, as well as the trace length between the GATE pin of the LTC4367 and the gates of the external MOSFETs.

Place the bypass capacitors at V_{OUT} as close as possible to the external MOSFET. Use high frequency ceramic capacitors in addition to bulk capacitors to mitigate hot swap ringing. Place the high frequency capacitors closest to the MOSFET. Note that bulk capacitors mitigate ringing by virtue of their ESR. Ceramic capacitors have low ESR and can thus ring near their resonant frequency.

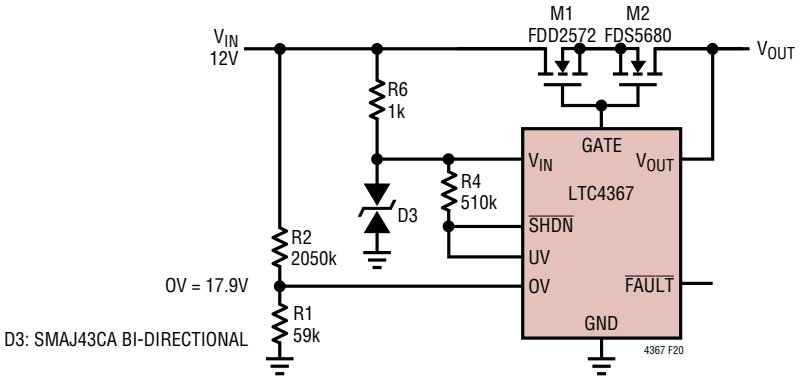
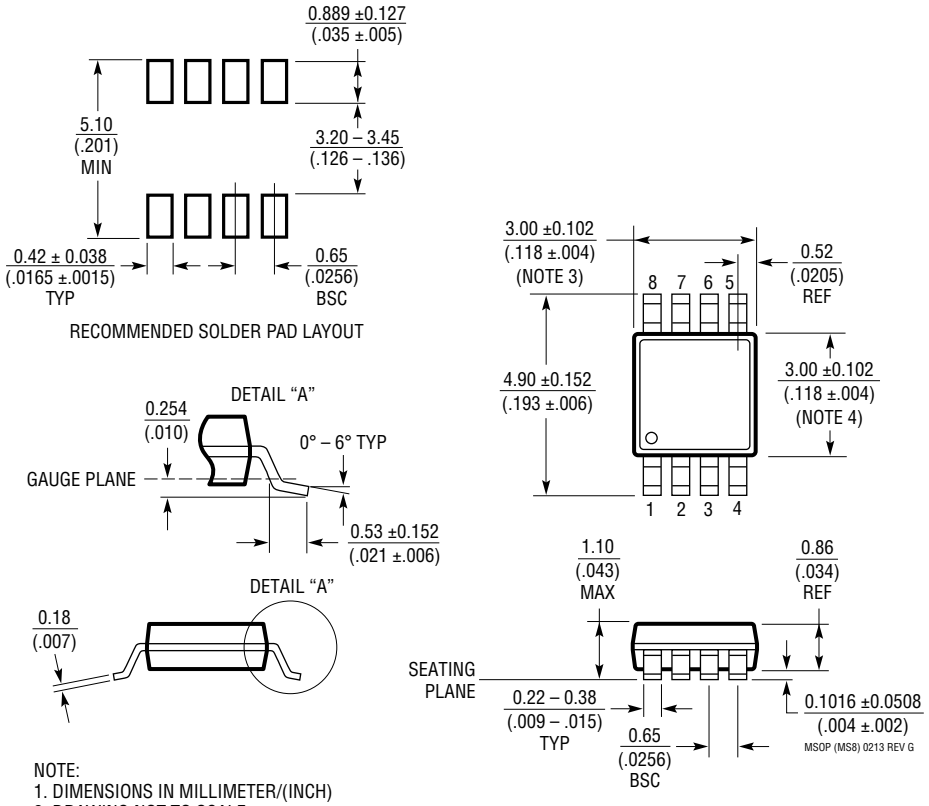


Figure 20. 12V Application Protected from 150V Transients

PACKAGE DESCRIPTION

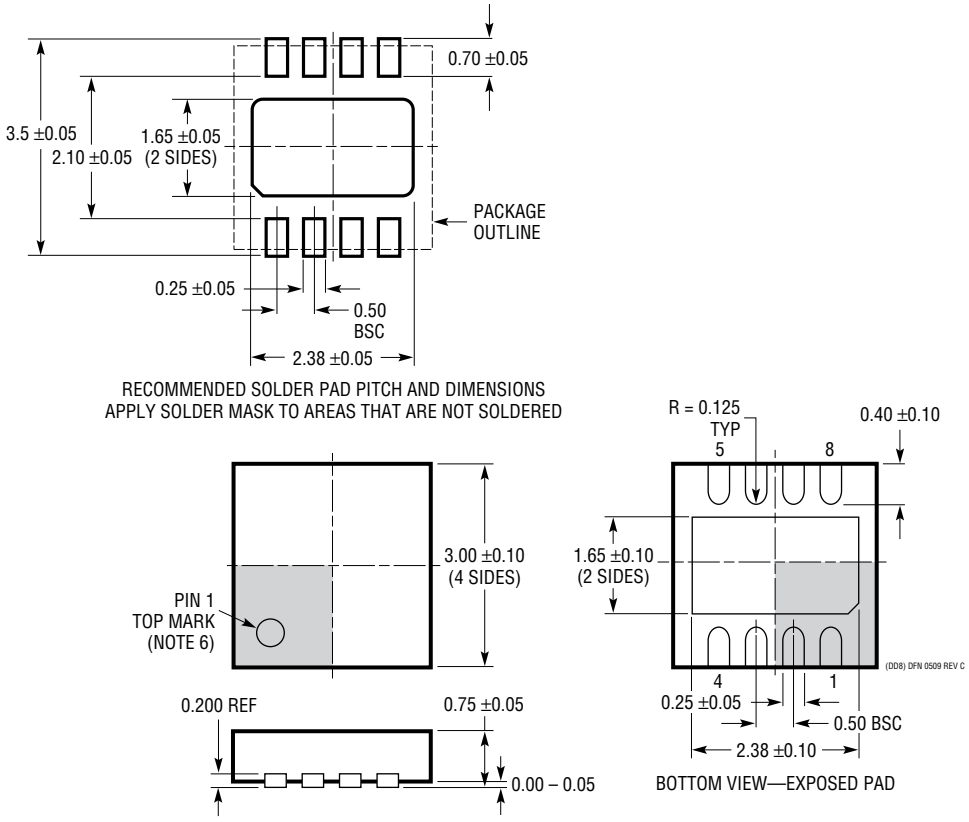
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/16	Updated Typical Application and Figures 1, 2, 13, 15	1, 9, 10, 15, 16
		Updated $\overline{SHDN}$, UV input current rating	2
		Changed I_{SHDN} test condition to 10V from 0.75V	4
		Updated graphs G09 and G12	5, 6
		Updated $\overline{SHDN}$ and UV Pin Functions	7
B	10/17	Increased $t_{GATE(SLOW)}$ max limit to 575µs	3
		Increased $t_{GATE(FAST)}$ max limit to 6µs	3
		Increased t_{START} max limit to 1400µs	4
C	08/20	Added AEC-Q100 qualification and "W" part numbers	1, 3