100V UV/OV and Reverse Protection Controller with Bidirectional Circuit Breaker

FEATURES

- **Wide Operating Voltage Range: 2.5V to 60V**
- **Overvoltage Protection to 100V**
- **Reverse Supply Protection to –40V**
- **Bidirectional Electronic Circuit Breaker:**
  - **+50mV Forward Sense Threshold**
  - **–50mV Reverse (LTC4368-1)**
  - **–3mV Reverse (LTC4368-2)**
- Adjustable ±1.5% Undervoltage and Overvoltage Thresholds
- Low Operating Current: 80µA
- Low Shutdown Current: 5µA
- Controls Back-to-Back N-Channel MOSFETs
- Blocks 50Hz and 60Hz AC Power
- Hot Swappable Supply Input
- Pin-Selectable Overcurrent Auto-Retry Timer or Latchoff
- 10-Pin MSOP and 3mm × 3mm DFN Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Reverse Battery Protection
- Portable Instrumentation
- Automotive and Industrial Surge Protection
- Energy Storage Systems

DESCRIPTION

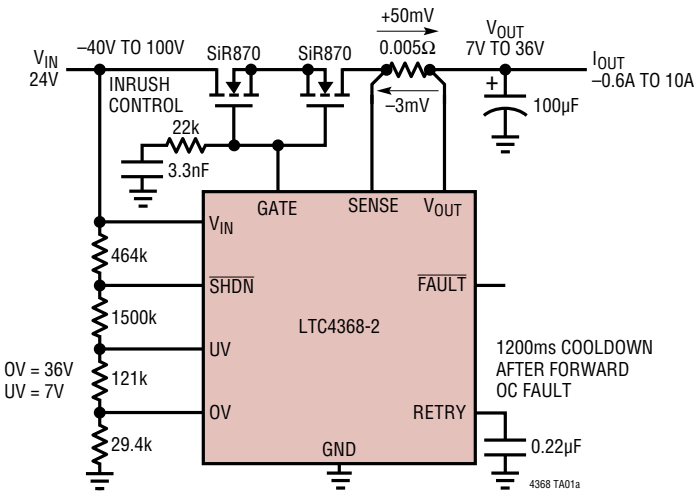
The LTC®4368 protects applications from power supply voltages that may be too high, too low, or even negative and from overcurrent faults in both forward and reverse directions. The LTC4368 controls the gate voltage of a pair of external N-channel MOSFETs to ensure that the load is connected to the input supply only when there are no voltage or current faults.

Two comparator inputs allow configuration of the overvoltage (OV) and undervoltage (UV) set points using an external resistive divider. A current sense resistor sets the forward and reverse circuit breaker current thresholds. After a forward current fault, the LTC4368 will either latch-off power, or retry after a user adjustable delay. After a reverse current fault, the LTC4368 waits for the output to fall 100mV below the input to reconnect power to the load.

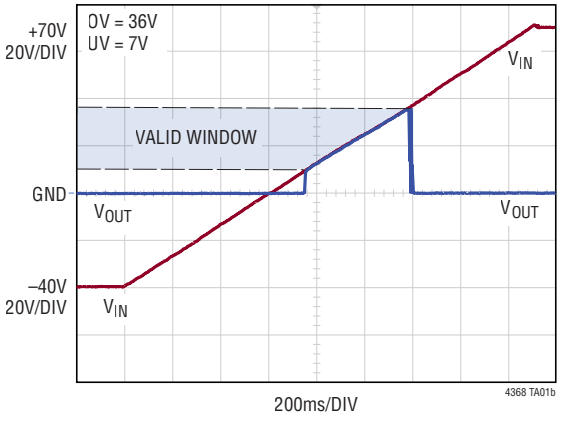
The LTC4368 has a 32ms turn-on delay that debounces live supply input connections and blocks 50Hz and 60Hz AC power. UV/OV faults also trigger the 32ms recovery delay before the external MOSFETs are turned back on.

TYPICAL APPLICATION

24V Application with 10A Circuit Breaker



Load Protected from Reverse and Overvoltage at V_{IN}



ABSOLUTE MAXIMUM RATINGS (Note 1, Note 2)

Supply Voltage
- V_{IN} ..... –40V to 100V

Input Voltages
- UV, $\overline{SHDN}$ (Note 3) ..... –0.3V to 80V
- OV (Note 3) ..... –0.3V to 20V
- RETRY (Note 3) ..... –0.3V to 5V
- V_{OUT}, SENSE ..... –10V to 80V
- V_{OUT} to SENSE ..... –10V to 10V
- V_{IN} to V_{OUT} ..... –60V to 100V

Output Voltages
- $\overline{FAULT}$ (Note 3) ..... –0.3V to 80V
- GATE ..... –40V to V_{IN} + 14V

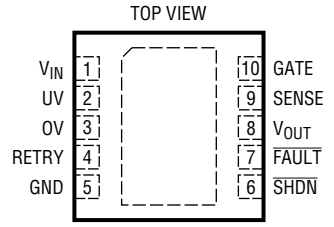
Input Currents
- RETRY, UV, OV ,$\overline{SHDN}$, $\overline{FAULT}$ ..... –1mA

Operating Ambient Temperature Range
- LTC4368C ..... 0°C to 70°C
- LTC4368I ..... –40°C to 85°C
- LTC4368H ..... –40°C to 125°C

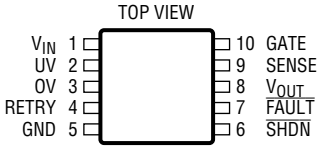
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- MSOP Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) PCB GROUND CONNECTION OPTIONAL



MS10 PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 160°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4368CDD-1#PBF	LTC4368CDD-1#TRPBF	LGTH	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4368CDD-2#PBF	LTC4368CDD-2#TRPBF	LGTK	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4368IDD-1#PBF	LTC4368IDD-1#TRPBF	LGTH	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4368IDD-2#PBF	LTC4368IDD-2#TRPBF	LGTK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4368HDD-1#PBF	LTC4368HDD-1#TRPBF	LGTH	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4368HDD-2#PBF	LTC4368HDD-2#TRPBF	LGTK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4368CMS-1#PBF	LTC4368CMS-1#TRPBF	LTGTG	10-Lead Plastic MSOP	0°C to 70°C
LTC4368CMS-2#PBF	LTC4368CMS-2#TRPBF	LTGTJ	10-Lead Plastic MSOP	0°C to 70°C
LTC4368IMS-1#PBF	LTC4368IMS-1#TRPBF	LTGTG	10-Lead Plastic MSOP	–40°C to 85°C
LTC4368IMS-2#PBF	LTC4368IMS-2#TRPBF	LTGTJ	10-Lead Plastic MSOP	–40°C to 85°C
LTC4368HMS-1#PBF	LTC4368HMS-1#TRPBF	LTGTG	10-Lead Plastic MSOP	–40°C to 125°C
LTC4368HMS-2#PBF	LTC4368HMS-2#TRPBF	LTGTJ	10-Lead Plastic MSOP	–40°C to 125°C

ORDER INFORMATION

AUTOMOTIVE PRODUCTS**				
LTC4368IDD-1#WPBF	LTC4368IDD-1#WTRPBF	LGTH	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4368IDD-2#WPBF	LTC4368IDD-2#WTRPBF	LGTK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4368HDD-1#WPBF	LTC4368HDD-1#WTRPBF	LGTH	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4368HDD-2#WPBF	LTC4368HDD-2#WTRPBF	LGTK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4368IMS-1#WPBF	LTC4368IMS-1#WTRPBF	LTGTG	10-Lead Plastic MSOP	–40°C to 85°C
LTC4368IMS-2#WPBF	LTC4368IMS-2#WTRPBF	LTGTJ	10-Lead Plastic MSOP	–40°C to 85°C
LTC4368HMS-1#WPBF	LTC4368HMS-1#WTRPBF	LTGTG	10-Lead Plastic MSOP	–40°C to 125°C
LTC4368HMS-2#WPBF	LTC4368HMS-2#WTRPBF	LTGTJ	10-Lead Plastic MSOP	–40°C to 125°C

*Temperature grades are identified by a label on the shipping container. Consult ADI Marketing for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.5V to 60V, unless otherwise noted (Note 2). UV = 2.5V, OV = 0V, $\overline{SHDN}$ = 2.5V, SENSE = V_{OUT} = V_{IN} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}, V_{OUT}, SENSE							
V_{IN}	Input Voltage: Operating Range Protection Range		● ●	2.5 –40		60 100	V V
$V_{IN(UVLO)}$	Input Supply Undervoltage Lockout	V_{IN} Rising	●	1.8	2.2	2.4	V
I_{VIN}	Input Supply Current: On Off	$\overline{SHDN}$ = 2.5V, SENSE = V_{OUT} = V_{IN} $\overline{SHDN}$ = 0V, SENSE = V_{OUT} = V_{IN}	● ●		30 5	100 25	µA µA
$I_{VIN(R)}$	Reverse Input Supply Current	V_{IN} = –40V, SENSE = V_{OUT} = 0V	●		–1.5	–2.5	mA
$V_{OUT(UVLO)}$	V_{OUT} Undervoltage Lockout	V_{OUT} Rising, V_{OUT} – SENSE = 100mV, V_{IN} = 12V	●	1.8	2.2	2.4	V
$t_{VOUT(UVLO)}$	V_{OUT} Undervoltage Lockout Delay	V_{IN} = 12V, V_{OUT}:0V→12V, V_{OUT} – SENSE = 100mV	●	40	120	280	µs
I_{VOUT}	V_{OUT} Input Current: On Off Reverse	$\overline{SHDN}$ = 2.5V, SENSE = V_{OUT} = V_{IN} $\overline{SHDN}$ = 0V, SENSE = V_{OUT} = V_{IN} V_{IN} = –40V, SENSE = V_{OUT} = 0V	● ● ●		50 3 20	125 20 50	µA µA µA
Current Sense							
I_{SENSE}	SENSE Input Current: On Off Reverse	$\overline{SHDN}$ = 2.5V, SENSE = V_{OUT} = V_{IN} $\overline{SHDN}$ = 0V, SENSE = V_{OUT} = V_{IN} V_{IN} = –40V, SENSE = V_{OUT} = 0V	● ● ●		1.2 0.1 1	2 2 10	µA µA µA
$\Delta V_{SENSE,F}$	Overcurrent Fault Threshold, Forward (SENSE – V_{OUT})	V_{OUT} = V_{IN} V_{IN} = 12V, V_{OUT} = 0.5V V_{IN} = 12V, V_{OUT} = 0V	● ● ●	40 40 30	50 50 50	60 60 70	mV mV mV
$\Delta V_{SENSE,R}$	Overcurrent Fault Threshold, Reverse (SENSE – V_{OUT})	LTC4368-1 V_{OUT} = V_{IN} LTC4368-2 V_{OUT} = V_{IN}	● ●	–42 –1	–50 –3	–58 –5	mV mV
ΔV_{RR}	Reverse Overcurrent Re-Enable Turn-On Threshold (V_{IN} – V_{OUT})	V_{IN} = SENSE = 6V to 60V V_{IN} = SENSE = 2.5V to <6V	● ●	75 20	100 50	125 125	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.5V to 60V, unless otherwise noted (Note 2). UV = 2.5V, OV = 0V, $\overline{SHDN}$ = 2.5V, SENSE = V_{OUT} = V_{IN} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GATE							
ΔV_{GATE}	Gate Drive (GATE – V_{OUT})	V_{IN} = 2.5V, I_{GATE} = 0µA, –1µA V_{IN} = 5V, I_{GATE} = 0µA, –1µA V_{IN} = 12V to 60V, I_{GATE} = 0µA, –1µA	● ● ●	3 7.2 10	4 8.7 11	5.5 10.8 13.1	V V V
$I_{GATE(UP)}$	Gate Pull Up Current	GATE = 15V, V_{IN} = 12V	●	–20	–35	–60	µA
$I_{GATE(SLOW)}$	Gate Slow Pull Down Current	GATE = 20V, V_{IN} = 12V	●	40	90	160	µA
$I_{GATE(FAST)}$	Gate Fast Pull Down Current	GATE = 20V, SENSE = V_{IN} = 12V	●	30	60	90	mA
$t_{D(FAST)}$	Gate Fast Turn Off Delay	C_{GATE} = 2.2nF: UV, OV Fault	●		2	6	µs
$t_{D(SLOW)}$	Gate Slow Turn Off Delay	C_{GATE} = 2.2nF, $\overline{SHDN}$ Falling, V_{IN} = 12V	●	150	275	575	µs
$t_{D(ON)}$	Gate Turn-On Delay Time	V_{IN} = 12V, Power Good to ΔV_{GATE} > 0V	●	22	32	45	ms
$t_{p(GATE)}$	Overcurrent Fault Propagation Delay	C_{GATE} = 2.2nF, Overcurrent Fault to ΔV_{GATE} = 0V SENSE – V_{OUT}: 0 to +100mV, or SENSE – V_{OUT}: 0 to –100mV (LTC4368-1) SENSE – V_{OUT}: 0 to –10mV (LTC4368-2)	●	3	8	18	µs
UV, OV							
V_{UV}	UV Input Threshold Voltage	UV Falling	●	492.5	500	507.5	mV
V_{OV}	OV Input Threshold Voltage	OV Rising	●	492.5	500	507.5	mV
V_{UVHYST}	UV Input Hysteresis		●	20	25	32	mV
V_{OVHYST}	OV Input Hysteresis		●	20	25	32	mV
I_{LEAK}	UV, OV Leakage Current	V = 0.5V, V_{IN} = 60V	●			±10	nA
t_{FAULT}	UV, OV Fault Propagation Delay	Overdrive = 50mV, V_{IN} = 12V	●		1	2	µs
$\overline{SHDN}$							
V_{SHDN}	$\overline{SHDN}$ Input Threshold	$\overline{SHDN}$ Falling	●	0.4	0.75	1.2	V
I_{SHDN}	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 10V, V_{IN} = 60V	●			±15	nA
t_{START}	Delay Coming Out of Shutdown Mode	$\overline{SHDN}$ Rising to $\overline{FAULT}$, V_{IN} = 12V	●	400	800	1400	µs
$t_{SHDN(F)}$	$\overline{SHDN}$ To $\overline{FAULT}$ Asserted	V_{IN} = 12V	●		1.5	3	µs
t_{LOWPWR}	Delay From Turn Off to Low Power Operation	V_{IN} = 12V	●	20	32	48	ms
$\overline{FAULT}$							
V_{OL}	$\overline{FAULT}$ Output Voltage Low	I_{FAULT} = 500µA, V_{IN} = 12V	●		0.15	0.4	V
I_{FAULT}	$\overline{FAULT}$ Leakage Current	$\overline{FAULT}$ = 5V, V_{IN} = 60V	●			±20	nA
RETRY							
V_{RETRY}	Configuration Threshold for GATE Latch-Off	RETRY Falling to ΔI_{RETRY} > 2µA V_{IN} = 12V	●	0.5	1	1.5	V
I_{RETRY}	Output Current for RETRY Timer	RETRY = 2V, V_{IN} = 12V RETRY = 0V, V_{IN} = 12V	● ●	2.5 –10	3.5 –17	4.5 –25	µA µA
t_{CLEAR}	Minimum $\overline{SHDN}$ Pulse to Clear Forward Overcurrent RETRY Latch	RETRY = 0V, V_{IN} = 12V	●	15			µs
t_{RETRY}	Forward Overcurrent Cool-Down Delay	$\overline{FAULT}$ Asserted to $\overline{FAULT}$ Released, C_{RETRY} = 22nF SENSE = V_{OUT} = V_{IN} = 12V	●	80	120	150	ms

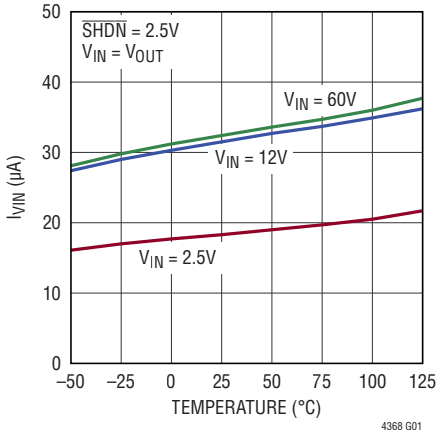
Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

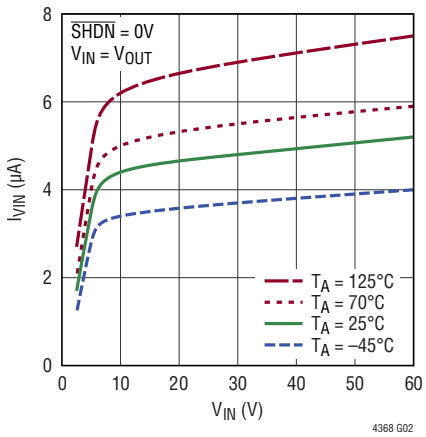
Note 3. These pins can be tied to voltages below –0.3V through a resistor that limits the current below 1mA.

TYPICAL PERFORMANCE CHARACTERISTICS

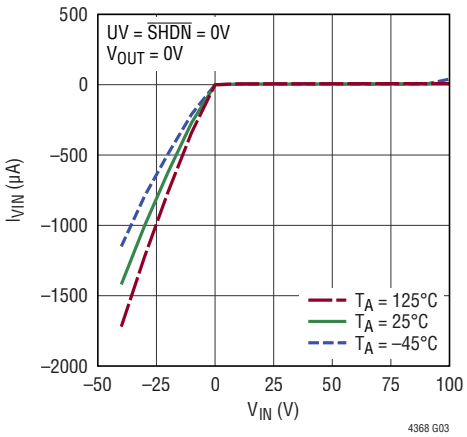
V_{IN} Operating Current vs Temperature



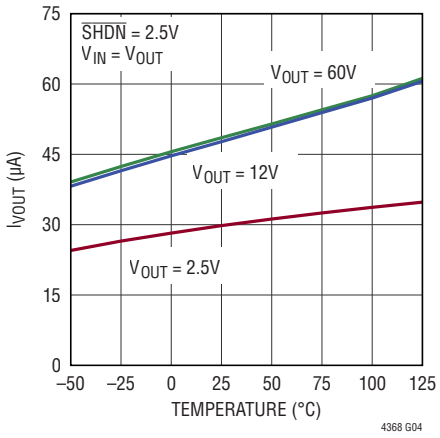
V_{IN} Shutdown Current vs Voltage



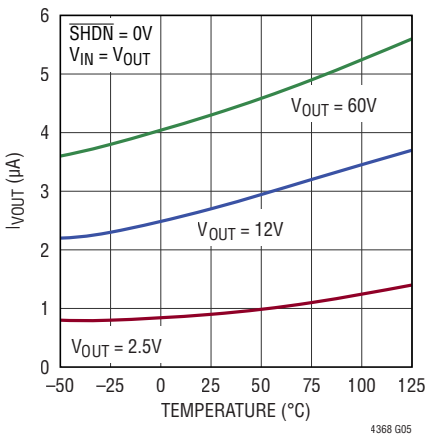
V_{IN} Supply Current vs Voltage (–40V to 100V)



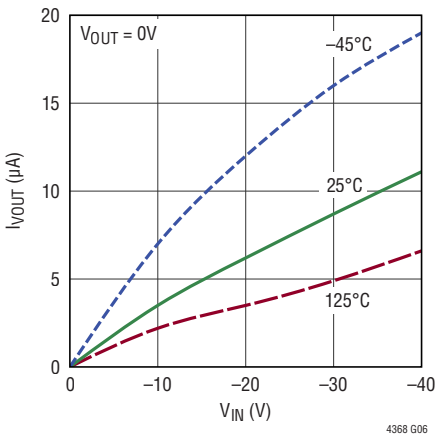
V_{OUT} Operating Current vs Temperature



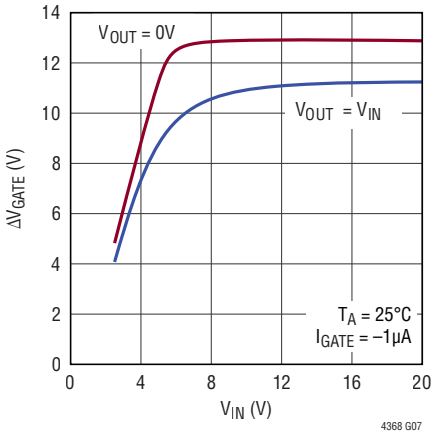
V_{OUT} Shutdown Current vs Temperature



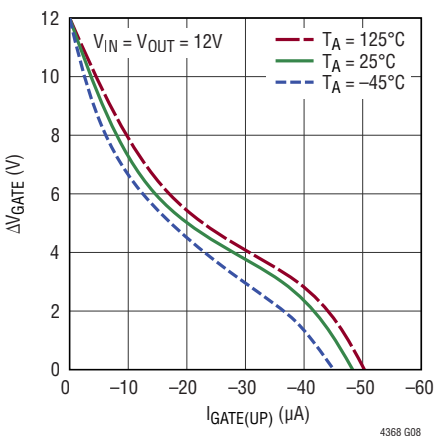
V_{OUT} Current vs Reverse V_{IN}



GATE Drive vs V_{IN} Supply Voltage

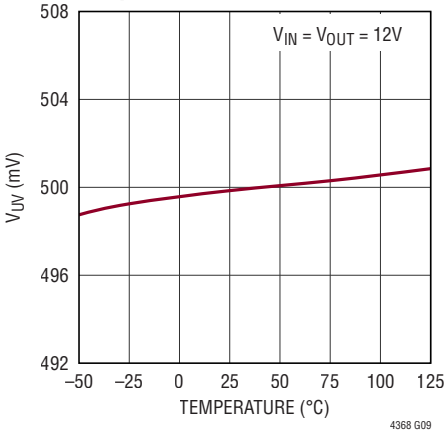


GATE Drive vs GATE Current

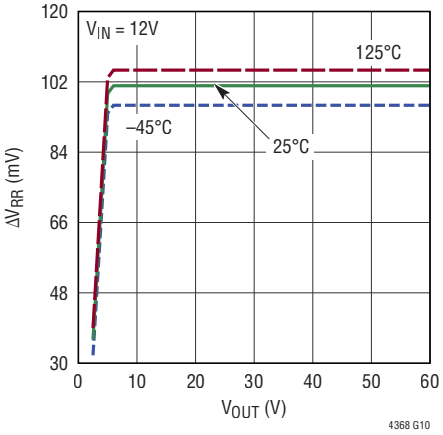


TYPICAL PERFORMANCE CHARACTERISTICS

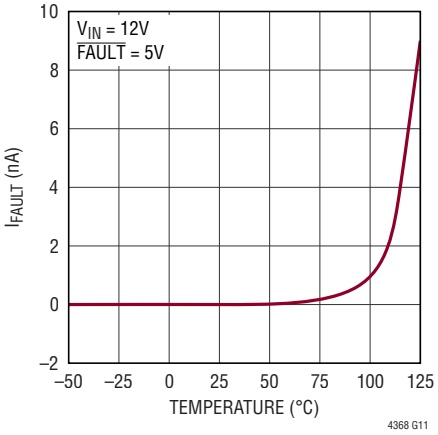
UV, OV Thresholds vs Temperature



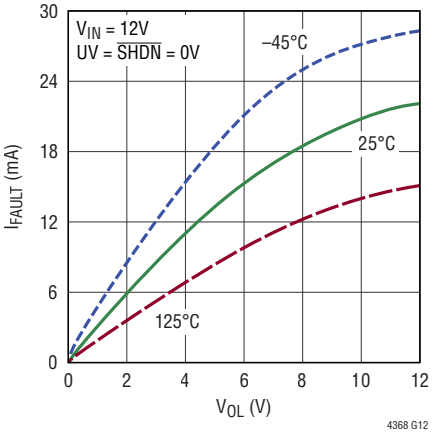
ΔV_{RR} Threshold vs V_{OUT}



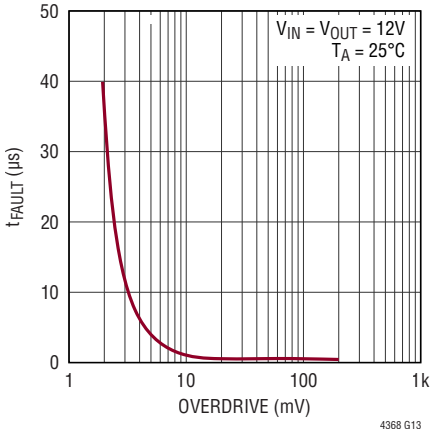
$\overline{FAULT}$ Leakage vs Temperature



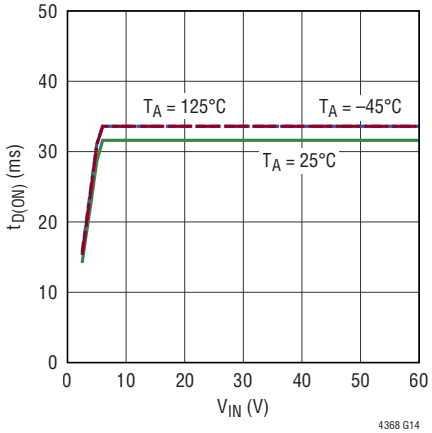
$\overline{FAULT}$ Output Current vs Voltage



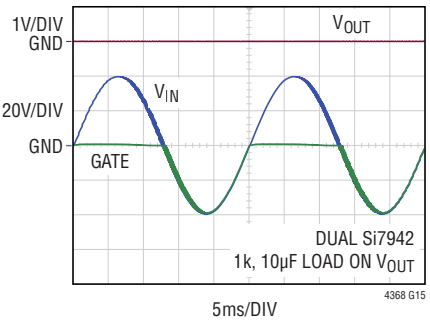
UV/OV Propagation Delay vs Overdrive



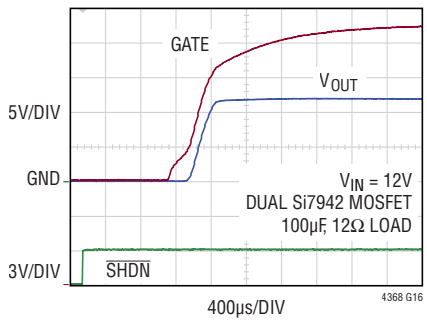
GATE Turn-On Delay Time vs V_{IN}



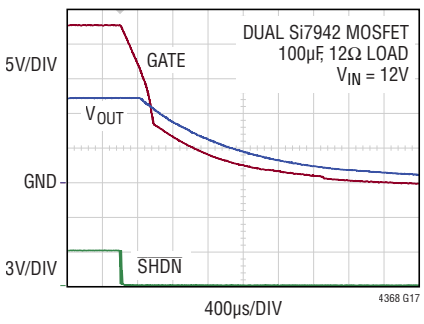
AC Blocking



Turn-On Timing



Turn-Off Timing



PIN FUNCTIONS

Exposed Pad: The exposed pad may be left open or connected to device ground.

$\overline{\text{FAULT}}$: Fault Indication Output. Connect to a pull-up resistor. This high voltage open drain output is pulled low if there is a voltage or current fault, if $\overline{\text{SHDN}}$ is low, or if V_{IN} has not risen above $V_{IN(UVLO)}$. Leave unconnected if unused.

GATE: Gate Drive Output for External N-channel MOSFETs. An internal charge pump provides 35µA of pull-up current and up to 13.1V of enhancement to the gate of an external MOSFET. When turned off, GATE is pulled just below the lower of V_{IN} or V_{OUT}. When V_{IN} goes negative, GATE is automatically connected to V_{IN}.

GND: Device Ground.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider to set the desired V_{IN} overvoltage fault threshold. This input connects an accurate, fast (1µs) comparator with a 0.5V rising threshold and 25mV of hysteresis. When OV rises above its threshold, a 60mA current sink pulls down on the GATE output. When OV falls back below 0.475V, and after a 32ms GATE turn-on delay waiting period, the GATE charge pump is enabled. The low leakage current on this input allows the use of large valued resistors for the external resistive divider. Connect to GND if unused.

RETRY: Retry or Latch-Off Selection Input. Connect to ground to latch off the MOSFETs after a forward overcurrent fault. To turn the external MOSFETs back on, the $\overline{\text{SHDN}}$ pin must be toggled low then high. Connect RETRY to an external capacitor to configure a 5.5ms/nF delay before the MOSFETs automatically turn on again. Leave unconnected if unused.

SENSE: Overcurrent Sense Input. Connect a current sense resistor between SENSE and V_{OUT}. This input detects overcurrent faults in both directions: forward at ΔV_{SENSE} = 50mV, and reverse at ΔV_{SENSE} = –50mV (LTC4368-1 option) or ΔV_{SENSE} = –3mV (LTC4368-2 option). When an overcurrent fault is detected, a 60mA current sink pulls down on the GATE output, thus quickly disconnecting the load from the input. After a reverse current fault, when V_{OUT} falls 100mV below V_{IN}, the LTC4368 automatically turns on the external MOSFETs. A forward overcurrent fault uses the RETRY pin to set the conditions for reconnecting power to the load. Connect to V_{OUT} if unused.

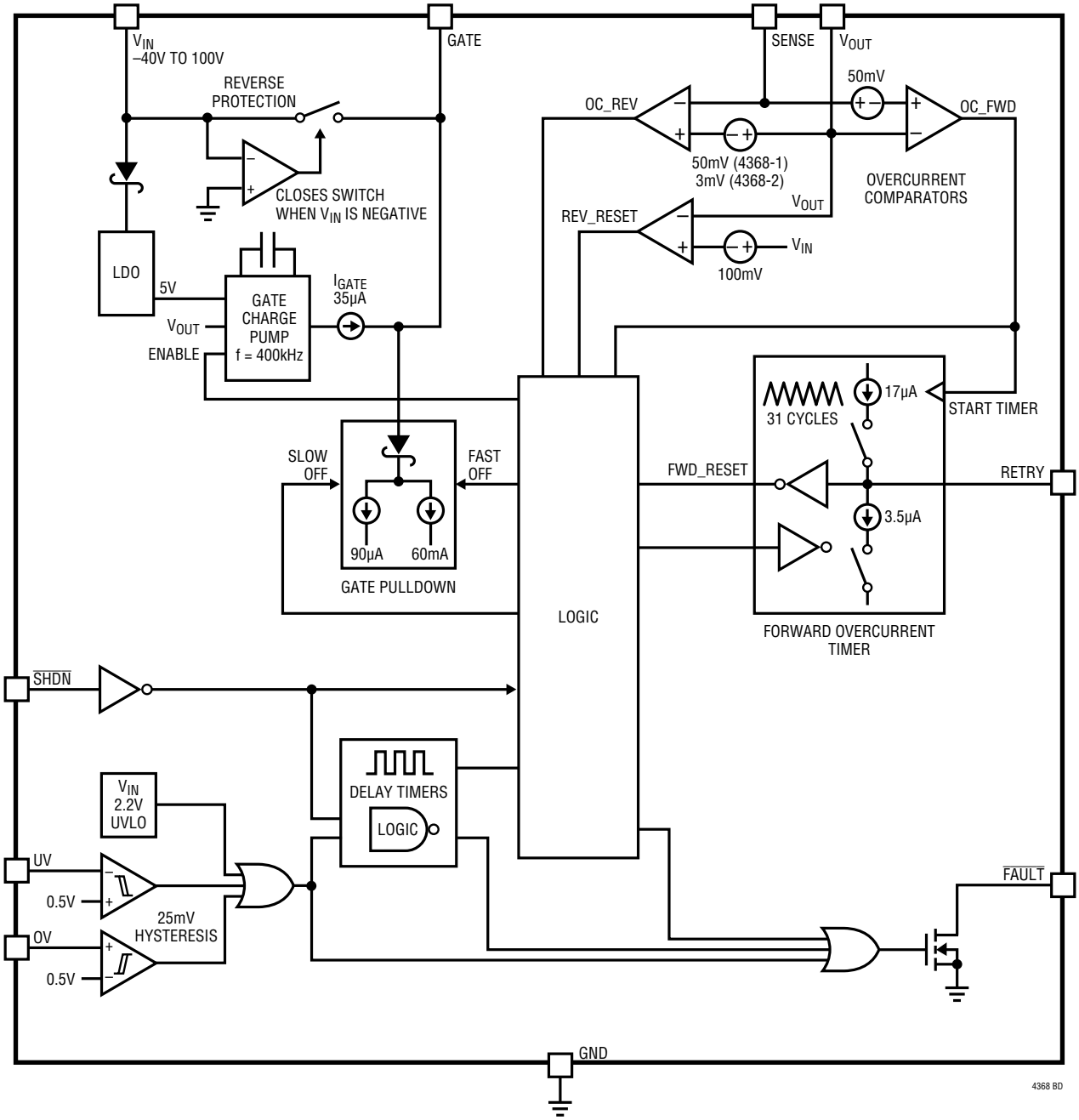
$\overline{\text{SHDN}}$: Shutdown Control Input. Assuming no voltage or current faults, $\overline{\text{SHDN}}$ high enables the GATE charge pump which in turn enhances the gate of the external N-channel MOSFETs. A low on $\overline{\text{SHDN}}$ generates a pull down on the GATE output with a 90µA current sink and places the LTC4368 in low current mode (5µA). If a forward overcurrent condition latches off the external MOSFETs (RETRY grounded), the $\overline{\text{SHDN}}$ pin must be toggled low then high to re-enable the charge pump that enhances the external MOSFETs. If V_{IN} goes above 80V, the $\overline{\text{SHDN}}$ pin voltage must be kept below 80V.

UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider to set the desired V_{IN} undervoltage fault threshold. This input connects to an accurate, fast (1µs) comparator with a 0.5V falling threshold and 25mV of hysteresis. When UV falls below its threshold, a 60mA current sink pulls down on the GATE output. When UV rises back above 0.525V, and after a 32ms GATE turn-on delay waiting period, the GATE charge pump is enabled. The low leakage current on this input allows the use of large valued resistors for the external resistive divider. If unused and V_{IN} is less than 80V, connect to V_{IN} with a 510k resistor.

V_{IN}: Power Supply Input. Maximum protection range: –40V to 100V. Operating range: 2.5V to 60V. This pin can be hot swapped and has a 2.2V UVLO.

V_{OUT}: Output Voltage Sense Input. Connect a current sense resistor between V_{OUT} and SENSE. The GATE charge pump voltage is referenced to V_{OUT}. It is used as the charge pump input when V_{OUT} is greater than approximately 5V. The reverse current fault comparators require that V_{OUT} rise above its 2.2V UVLO. V_{OUT} cannot be hot swapped with supplies above 24V. Place at least 1µF from V_{OUT} to GND.

BLOCK DIAGRAM



OPERATION

Many of today's electronic systems get their power from external sources such as wall adapters, batteries and custom power supplies. Figure 1 shows a supply arrangement using a DC barrel connector. Power is supplied by an AC adapter or, if the plug is withdrawn, by a removable battery. Note that the polarity of the AC adapter and barrel connector varies by manufacturer. Trouble arises when any of the following occurs:

- The battery is installed backwards
- A wall adapter of opposite polarity is attached
- A wall adapter of excessive voltage is attached
- A wall adapter with an AC output is attached
- The battery is discharged below a safe level
- The load or the input is shorted to ground or to another supply
- Excessive current flows from the supply to the load or from the load to the supply

These conditions, if unchecked, can damage electronic systems and their connectors. Damage can take the form of a single catastrophic event, or over time as devices degrade from repeated overstress.

The LTC4368 limits these errant overvoltage and overcurrent conditions and helps extend the life of the electronic systems it protects. When the part detects an overcurrent or overvoltage fault, it isolates the input supply from the load by turning off the external back-to-back MOSFETs.

The LTC4368 provides accurate overvoltage and undervoltage comparators to ensure that power is applied to the load only if the input supply meets the user selectable voltage window. Additionally, two accurate overcurrent comparators disconnect the load from the supply when excessive current flows in either the forward (+50mV/R_{SENSE}) or reverse (–50mV or –3mV/R_{SENSE}) direction. Reverse supply voltage protection circuits automatically isolate the load from negative input voltages. During normal operation, a high voltage charge pump enhances the gate of dual external N-channel power MOSFETs, thus providing a low loss path for qualified power. Power consumption is 5µA during shutdown and 80µA while operating. The LTC4368 integrates all these functions in small 10-lead 3mm × 3mm DFN and MSOP packages.

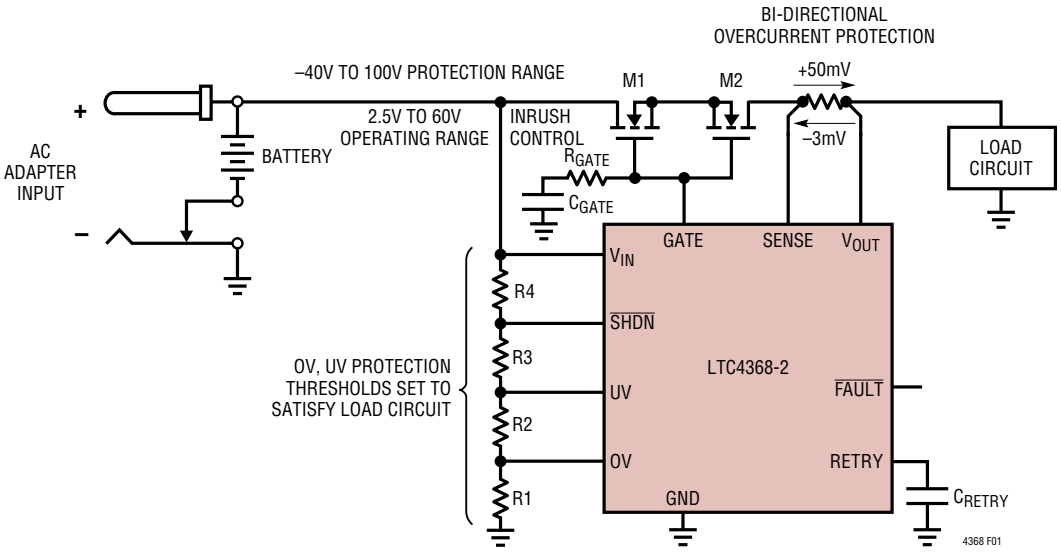


Figure 1. Polarity Protection for DC Barrel Connectors

APPLICATIONS INFORMATION

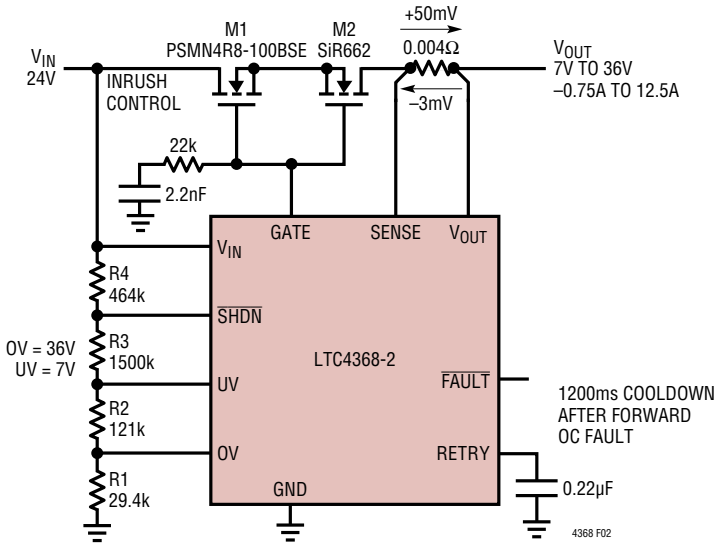


Figure 2. LTC4368-2 Protects Load from Voltage (–40V to 100V) and Current (–0.75A to 12.5A) Faults

The LTC4368 is an N-channel MOSFET controller that protects a load from overvoltage faults (both positive and negative) and from overcurrent faults (both forward and reverse). A typical application circuit using the LTC4368-2 is shown in Figure 2. The circuit provides a low loss connection from V_{IN} to V_{OUT} as long as there are no voltage or current faults.

Voltages at V_{IN} outside of the 7V to 36V range are prevented from getting to the load and can be as high as 100V and as negative as –40V. Load currents (including inrush currents) above 12.5A (forward from V_{IN} to V_{OUT}) and below –0.75A (reverse from V_{OUT} to V_{IN}) will cause the load to be disconnected from V_{IN}. The circuit of Figure 2 protects against negative voltages at V_{IN} as shown. Note that the SOA and voltage requirements are not the same for the two external MOSFETs. During power-up, the input MOSFET (M1) will stand off more voltage (up to V_{IN}) than the output MOSFET (M2). The body diode of M2 will limit its drain to source voltage. This allows the use of smaller MOSFETs at the output.

During normal operation, the LTC4368 provides up to 13.1V of gate enhancement to the external back-to-back N-channel MOSFETs. This turns on the MOSFETs, thus connecting the load at V_{OUT} to the supply at V_{IN}.

GATE Drive

The LTC4368 turns on the external N-channel MOSFETs by driving the GATE pin above V_{OUT}. The voltage difference between the GATE and V_{OUT} pins (gate drive) is a function of V_{IN} and V_{OUT}.

Figure 3 highlights the dependence of the gate drive on V_{IN} and V_{OUT}. When system power is first turned on ($\overline{SHDN}$ low to high, SENSE = V_{OUT} = 0V), gate drive is at a maximum for all values of V_{IN}. This helps prevent startup problems into heavy loads by ensuring that there is enough gate drive to support the load.

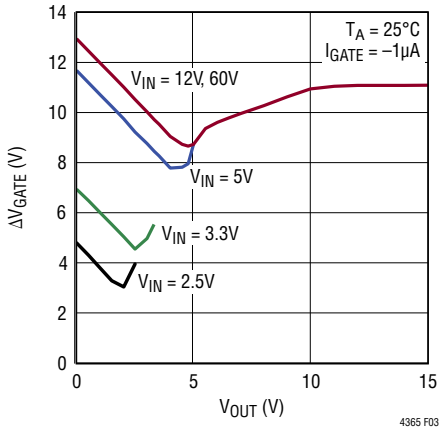


Figure 3. Gate Drive (GATE – V_{OUT}) vs V_{OUT}

APPLICATIONS INFORMATION

As V_{OUT} ramps up from 0V, the absolute value of the GATE voltage remains fixed until V_{OUT} is greater than the lower of (V_{IN} – 1V) or 5V. Once V_{OUT} crosses this threshold, gate drive begins to increase up to a maximum of 13.1V. The curves of Figure 3 were taken with a GATE load of –1µA. If there were no DC load on GATE, the gate drive for each V_{IN} would be slightly higher.

Note that when V_{IN} is at the lower end of the operating range, the external N-channel MOSFET must be selected with a correspondingly lower threshold voltage.

Overvoltage and Undervoltage Protection

The LTC4368 provides two accurate comparators to monitor for overvoltage (OV) and undervoltage (UV) conditions at V_{IN}. If the input supply rises above the user adjustable OV threshold, the gates of the external MOSFETs are quickly turned off, thus disconnecting the load from the input. Similarly, if the input supply falls below the user adjustable UV threshold, the gates of the external MOSFETs are quickly turned off. Figure 4 shows a UV/OV application for an input supply of 12V.

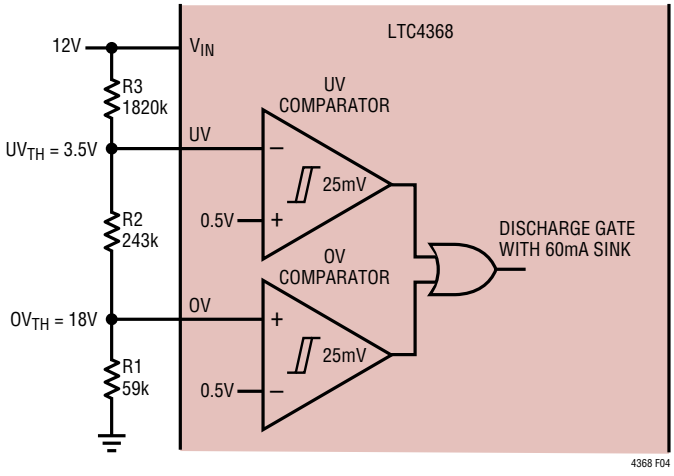


Figure 4. UV, OV Comparators Monitor 12V Supply

The external resistive divider allows the user to select an input supply range that is compatible with the load at V_{OUT}. Furthermore, the UV and OV inputs have very low leakage currents (typically < 1nA at 100°C), allowing for large values in the external resistive divider. In the application of Figure 4, the load is connected to the supply only if V_{IN} lies between 3.5V and 18V. In the event that V_{IN} goes above 18V or below 3.5V, the gate of the external N-channel MOSFET is immediately discharged with a 60mA current sink, thus isolating the load from the supply.

Figure 5 shows the timing associated with the UV pin. Once a UV fault propagates through the UV comparator (t_{FAULT}), the $\overline{FAULT}$ output is asserted low and a 60mA current sink discharges the GATE pin. As V_{OUT} falls, the GATE pin tracks V_{OUT}.

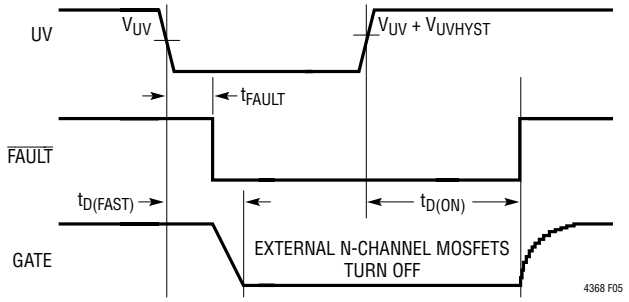


Figure 5. UV Timing (OV < (V_{OV} – V_{OVHYST}), $\overline{SHDN}$ > 1.2V)

Figure 6 shows the timing associated with the OV pin. Once an OV fault propagates through the OV comparator (t_{FAULT}), the $\overline{FAULT}$ output is asserted low and a 60mA current sink discharges the GATE pin. As V_{OUT} falls, the GATE pin tracks V_{OUT}.

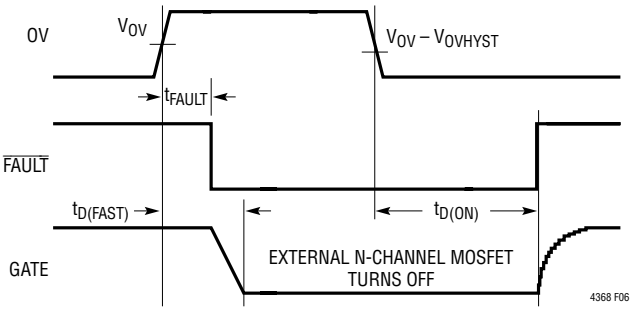


Figure 6. OV Timing (UV > (V_{UV} + V_{UVHYST}), $\overline{SHDN}$ > 1.2V)

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When both the UV and OV faults are removed, the external MOSFETs are not immediately turned on. The input supply must remain within the user selected power good window for typically 32ms ($t_{D(ON)}$) before the load is again connected to the supply. This recovery timeout period filters noise (including line noise) at the input supply and prevents chattering of power at the load.

Procedure for Selecting UV/OV External Resistor Values

The following 3-step procedure helps select the resistor values for the resistive divider of Figure 4. This procedure minimizes UV and OV offset errors caused by leakage currents at the respective pins.

1. Choose maximum tolerable offset at the UV pin, $V_{OS(UV)}$. Divide by the worst case leakage current at the UV pin, I_{UV} (10nA). Set the sum of R1 + R2 equal to $V_{OS(UV)}$ divided by 10nA. Note that due to the presence of R3, the actual offset at UV will be slightly lower.

$$R1 + R2 = \frac{V_{OS(UV)}}{I_{UV}}$$

2. Select the desired V_{IN} UV trip threshold, UV_{TH}. Find the value of R3:

$$R3 = \frac{V_{OS(UV)}}{I_{UV}} \bullet \left(\frac{UV_{TH} - 0.5V}{0.5V} \right)$$

3. Select the desired V_{IN} OV trip threshold, OV_{TH}. Find the values of R1 and R2:

$$R1 = \frac{\left(\frac{V_{OS(UV)}}{I_{UV}} \right) + R3}{OV_{TH}} \bullet 0.5V$$

$$R2 = \frac{V_{OS(UV)}}{I_{UV}} - R1$$

The example of Figure 4 uses standard 1% resistor values. The following parameters were selected:

$V_{OS(UV)}$ = 3mV

I_{UV} = 10nA

UV_{TH} = 3.5V

OV_{TH} = 18V

The resistor values can then be solved:

$$1.\ R1 + R2 = \frac{3mV}{10nA} = 300k$$

$$2.\ R3 = 2 \bullet \frac{3mV}{10nA} \bullet (3.5V - 0.5V) = 1.8M$$

The closest 1% value: R3 = 1.82M

$$3.\ R1 = \frac{300k + 1.82M}{2 \bullet 18V} = 58.9k$$

The closest 1% value: R1 = 59K

R2 = 300K – 59K = 241K

The closest 1% value: R2 = 243K

Therefore: OV = 17.93V, UV = 3.51V.

Limiting Inrush Current During Turn On

Charging large capacitors on V_{OUT} can lead to excessive inrush currents when LTC4368 turns on the external N-channel MOSFET. The maximum slew rate at the GATE pin can be reduced by adding a capacitor on the GATE pin:

$$\text{Slew Rate} = \frac{I_{GATE(UP)}}{C_{GATE}}$$

APPLICATIONS INFORMATION

Since the MOSFET acts like a source follower, the slew rate at V_{OUT} equals the slew rate at GATE. Therefore, the inrush current due to the capacitance on V_{OUT} is given by:

$$I_{INRUSH} = \frac{C_{OUT}}{C_{GATE}} \bullet I_{GATE(UP)}$$

For example, a 1A inrush current into a 100µF output capacitance requires a GATE capacitance of (using $I_{GATE(UP)}$ = 35µA):

$$C_{GATE} = \frac{35\mu A \bullet C_{OUT}}{I_{INRUSH}}$$

$$C_{GATE} = \frac{35\mu A \bullet 100\mu F}{1A} = 3.5nF$$

The 3.3nF C_{GATE} capacitor in the application circuit of Figure 7 limits the inrush current to just over 1A. R_{GATE} prevents C_{GATE} from slowing down the reverse polarity protection circuits. It also stabilizes the fast pull-down circuits and prevents chatter during fault conditions. Set R_{GATE} to 22k for most applications.

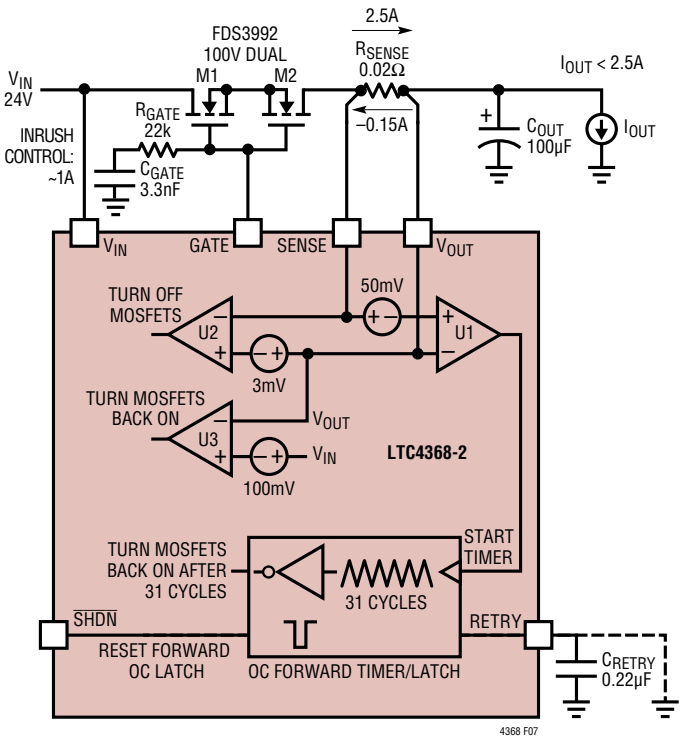

Figure 7. Overcurrent Comparators Monitor 2.5A/–0.15A Current Faults

Forward Overcurrent Fault

Forward overcurrent protection prevents large currents from flowing from V_{IN} to V_{OUT}. This threshold current is determined by the external sense resistor (R_{SENSE}) and an internal comparator (Figure 7, U1) with a 50mV threshold:

$$I_{OC,FWD} = \frac{50mV}{R_{SENSE}}$$

For the example of Figure 7, if 2.5A flows to the output across the 20mΩ sense resistor, the external MOSFETs (M1, M2) are immediately (8µs) turned off. This disconnects the load from the input supply.

Note that during initial startup, the output capacitance (C_{OUT}) charges from ground to V_{IN}. To prevent this capacitive inrush current (I_{INRUSH}) from falsely triggering the forward overcurrent comparator, place an inrush limiting capacitor (C_{GATE}) on the GATE pin (see Limiting Inrush Current During Turn On). This inrush current plus the output current must be less than the desired forward overcurrent threshold:

$$I_{OC,FWD} > I_{INRUSH} + I_{OUT}$$

For the example of Figure 7, the 3.3nF GATE capacitor and the 100µF output capacitor limit the inrush current (I_{INRUSH}) to approximately 1A. This means that the output current (I_{OUT}) must be less than 1.5A during turn on in order to avoid a forward overcurrent fault during turn on. Once V_{OUT} has ramped to its final value, the output current is limited to 2.5A.

Once a forward overcurrent fault is triggered, there are two application choices for turning the external MOSFETs back on:

1. Automatically restart by placing an external capacitor on the RETRY pin. An internal cool-down timer will charge/discharge this capacitor 31 times with a 5.5ms/nF total delay. At the end of this delay, the external MOSFETs are turned back on, thus reconnecting the load to the input supply. The 0.22µF capacitor (C_{RETRY}) in the application of Figure 7 yields a 1200ms cool-down timer delay. Note that the adjustable cool-down period provides the user with a means of keeping the external MOSFETs within the rated SOA (safe operating area). See Figure 8 timing diagram.

APPLICATIONS INFORMATION

2. Latch off the MOSFETs by grounding the RETRY pin (no external RETRY capacitor needed). This latches the forward overcurrent fault. The external MOSFETs are kept in the off condition until the $\overline{SHDN}$ input pin is toggled low then high (t_{CLEAR} pulse width < t_{LOWPWR}). See Figure 9 timing diagram.

Reverse Overcurrent Protection

Reverse overcurrent protection prevents large currents from flowing from V_{OUT} to V_{IN}. There are two options for reverse overcurrent protection thresholds. The LTC4368-1 (–50mV) bidirectional circuit breaker allows load current to flow in either direction: from V_{IN} to V_{OUT} or from V_{OUT} to V_{IN}. The LTC4368-2 provides diode-like behavior by making the reverse overcurrent threshold (–3mV) significantly smaller than the forward overcurrent threshold (+50mV). The reverse overcurrent fault threshold is determined by the external sense resistor (R_{SENSE}) and an internal comparator (Figure 7, U2). For the LTC4368-2 application of Figure 7:

$$I_{OC,REV} = \frac{-3mV}{R_{SENSE}} = \frac{-3mV}{20m\Omega} = -0.15A$$

If –0.15A flows from the output across the 20mΩ sense resistor, the external MOSFETs (M1,M2) are immediately (8µs) turned off.

To turn the MOSFETs back on, an internal comparator (Figure 7, U3) detects when V_{OUT} drops 100mV below V_{IN}:

$$V_{OUT} < V_{IN} - 100mV$$

Once this condition is met, the gates of the external MOSFETs are turned on again to reconnect the input supply to the load. See timing diagrams of Figure 10. Note that if the LTC4368-1 option is used, the reverse current threshold becomes:

$$I_{OC,REV} = \frac{-50mV}{R_{SENSE}}$$

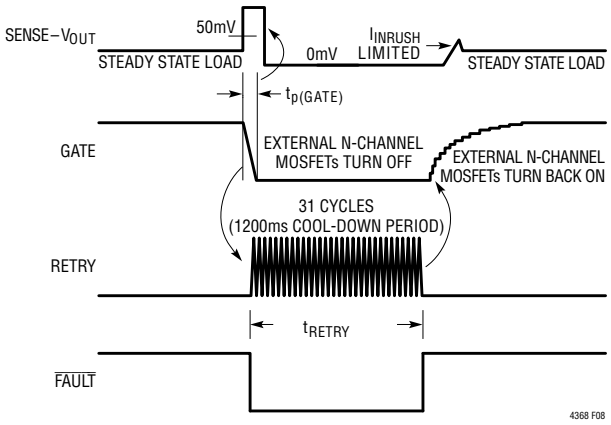

Figure 8. Forward Overcurrent Fault with 0.22µF RETRY Capacitor

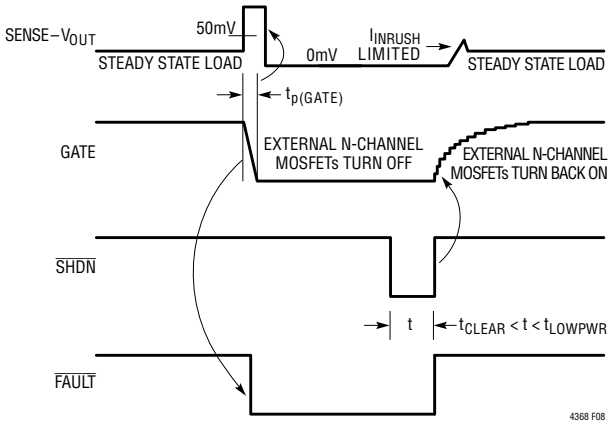

Figure 9. Forward Overcurrent Fault with RETRY Pin Grounded

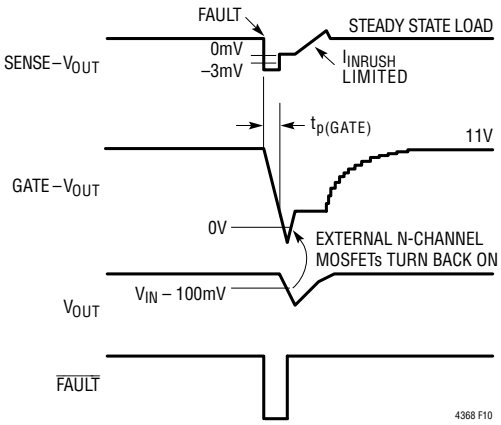

Figure 10. Reverse Overcurrent Fault: SENSE – V_{OUT} < –3mV (LTC4368-2)

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Reverse V_{IN} Protection

The LTC4368's rugged and hot swappable V_{IN} helps protect the more sensitive circuits at the output load. If the input supply is plugged in backwards, or a negative supply is inadvertently connected, the LTC4368 prevents this negative voltage from passing to the output load.

As shown in Figure 11, external back-to-back N-channel MOSFETs are required for reverse supply protection. When V_{IN} goes negative, the reverse V_{IN} comparator closes the internal switch, which in turn connects the gates of the external MOSFETs to the negative V_{IN} voltage. The body diode (D1) of M1 turns on, but the body diode (D2) of M2 remains in reverse blocking mode. This means that the common source connection of M1 and M2 remains about a diode drop higher than V_{IN}. Since the gate voltage of M2 is shorted to V_{IN}, M2 will be turned off and no current can flow from V_{OUT} to V_{IN}. Note that the voltage rating of M2 must withstand the reverse voltage excursion at V_{IN}.

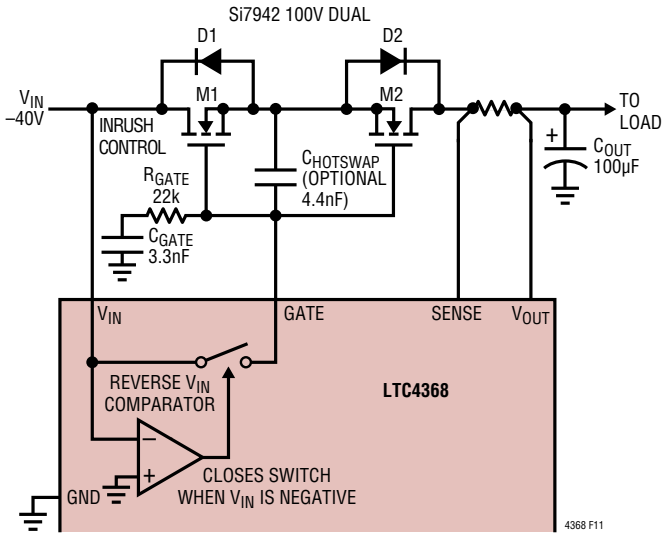


Figure 11. Reverse V_{IN} Protection Circuits

To avoid large currents when the reverse voltage is hot plugged, set R_{GATE} to 22k. To further improve reverse hot swap performance, place the optional $C_{HOTSWAP} \geq$ 4.4nF capacitor across the gate and source terminals of the external MOSFETs.

Figure 12 illustrates the waveforms that result when V_{IN} is hot plugged to –20V. V_{IN}, GATE and V_{OUT} start out at ground just before the connection is made. Due to the parasitic inductance of the V_{IN} and GATE connections, the voltage at the V_{IN} and GATE pins ring significantly below –20V. Therefore, hot swapping a negative input voltage more negative than –20V should not be performed without additional overshoot mitigation techniques in place. The front page application was used to generate the waveforms of Figure 12.

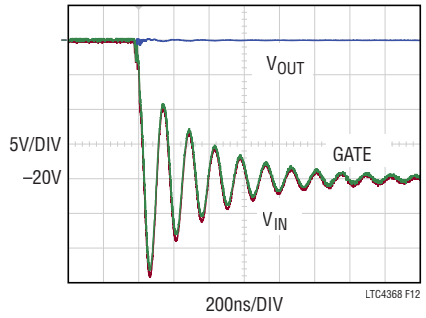


Figure 12. Hot Swapping V_{IN} to –20V

The speed of the LTC4368 reverse protection circuits is evident by how closely the GATE pin follows V_{IN} during the negative transients. The two waveforms are almost indistinguishable on the scale shown.

The trace at V_{OUT}, on the other hand, does not respond to the negative voltage at V_{IN}, demonstrating the desired reverse supply protection. The waveforms of Figure 12 were captured using a 40V dual N-channel MOSFET, a 10µF ceramic output capacitor and no load current on V_{OUT}.

Hot Swap V_{IN} Protection

The V_{IN} input of the LTC4368 can be live inserted or hot swapped into a backplane with minor disturbance to the V_{IN} supply. The idea is to keep the parasitic capacitances of the external MOSFETs (C_{GD}) from coupling onto the GATE pin and enhancing the MOSFETs. To improve positive V_{IN} hot swap capability (without jeopardizing reverse polarity protection), place $C_{HOTSWAP}$ across the gate and source terminals of the back-to-back MOSFETs. Figure 13 illustrates the waveforms that result when the V_{IN} of the front page application is hot plugged to +48V. The top trace is V_{IN}. The bottom two traces are the MOSFETs gate and source terminals. Note that the bottom two traces ring together and thus keep the MOSFETs off

APPLICATIONS INFORMATION

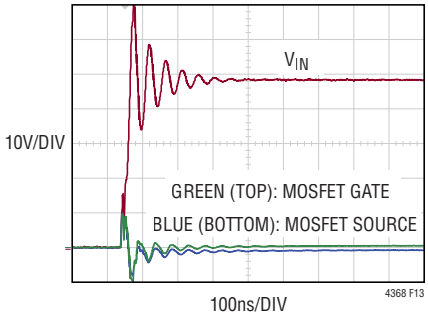


Figure 13. Hot Swapping V_{IN} to +48V

during the fast transients. To further improve positive hot swap, place the optional $C_{HOTSWAP}$ = 6.8nF capacitor across the gate/source of the external MOSFETs. For even more hot swap protection, add a diode (MBR0540) across R_{GATE} (connect cathode to C_{GATE}). Make sure this diode has a reverse breakdown of at least 40V.

Recovery Delay Timer

The LTC4368 has a recovery delay timer that filters noise at V_{IN} and helps prevent chatter at V_{OUT}. After either an OV or UV fault has occurred, the input supply must return to the desired operating voltage window for typically 32ms ($t_{D(ON)}$) in order to turn the external MOSFET back on, as illustrated in Figure 5 and Figure 6. Going out of and then back into fault in fewer than 32ms will keep the MOSFET off continuously. Similarly, coming out of shutdown ($\overline{SHDN}$ low to high) triggers an 800µs startup delay timer (t_{START}, see Figure 16).

The recovery delay timer is also active while the LTC4368 is powering up. The 32ms timer starts once V_{IN} rises above $V_{IN(UVLO)}$ and V_{IN} lies within the user selectable UV/OV power good window. See Figure 14.

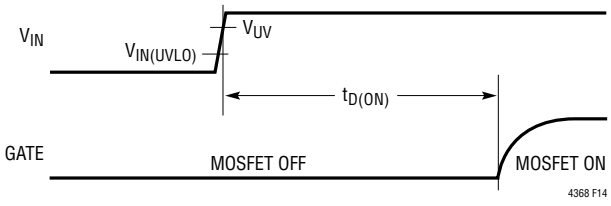


Figure 14. Recovery Timing During Power-On
OV = GND, UV = $\overline{SHDN}$ = V_{IN}

Slow Shutdown

The $\overline{SHDN}$ input turns off the external MOSFETs in a slow, controlled manner. When $\overline{SHDN}$ is asserted low, a 90µA current sink slowly begins to turn off the external MOSFETs.

Once the voltage at the GATE pin falls below the voltage at the V_{OUT} pin, the current sink is throttled back and a feedback loop takes over. This loop forces the GATE voltage to track V_{OUT}, thus keeping the external MOSFETs off as V_{OUT} decays. Note that when V_{OUT} < 2.5V, the GATE pin is pulled all the way to ground.

Slow gate turn off reduces load current slew rates and mitigates voltage spikes due to parasitic inductances. To further decrease GATE pin slew rate, place a capacitor ($C_{HOTSWAP}$, see Figure 11) across the gate and source terminals of the external MOSFETs. The waveforms of Figure 15 were captured using the Si7942 Dual N-channel MOSFETs, and a 2A load with 100µF output capacitor.

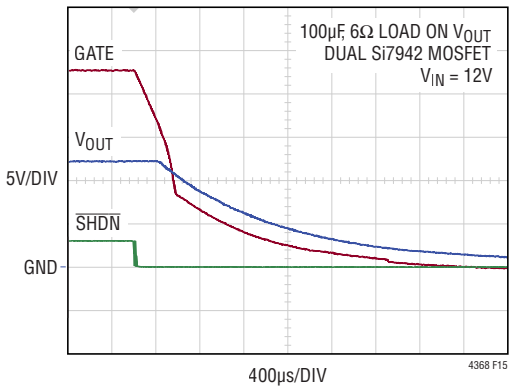


Figure 15. Slow Shutdown: GATE Tracks V_{OUT} as V_{OUT} Decays

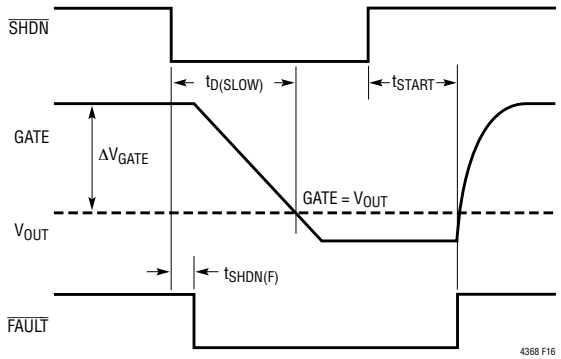


Figure 16. Slow Shutdown Timing

APPLICATIONS INFORMATION

$\overline{\text{FAULT}}$ Status

The $\overline{\text{FAULT}}$ high voltage open drain output is driven low if $\overline{\text{SHDN}}$ is asserted low, if V_{IN} is outside the desired UV/OV voltage window, if there is an overcurrent fault, or if V_{IN} has not risen above $V_{IN(UVLO)}$. Figures 5, 6, 8, 9, 10 and 16 show the $\overline{\text{FAULT}}$ output timing.

Ideal Diode Alternative

Figure 17 shows two LTC4368-2 connected in parallel. With both devices turned on, the output will be the higher of V1 or V2. Unlike ideal diode controllers, the LTC4368 always fully enhances the MOSFETs, even at light loads. Note, however, that if the voltage difference between V1 and V2 is less than 3mV, the reverse overcurrent comparators will not detect a fault and up to 150mA can flow from the higher to the lower supply. Similarly, disconnecting the higher supply may not generate sufficient reverse current to turn off the MOSFETs. A subsequent reconnection may result in an inrush current that temporarily trips the circuit breakers.

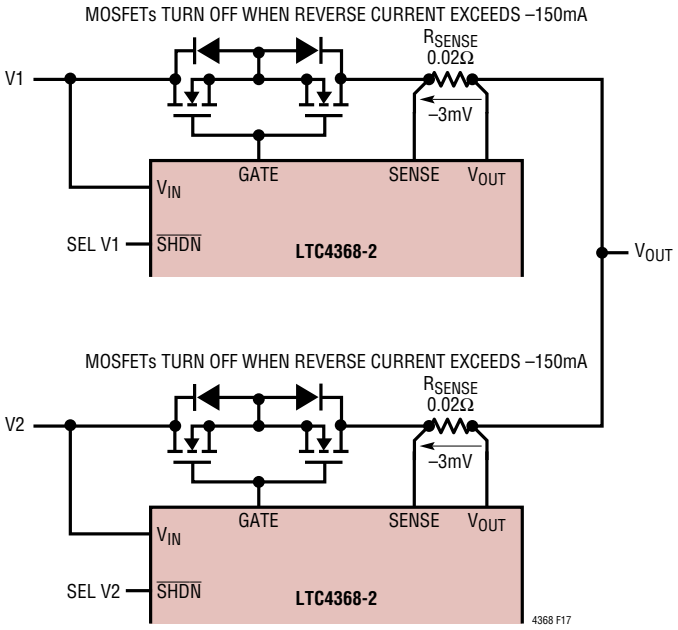


Figure 17. Alternative to Ideal Diode

By driving the $\overline{\text{SHDN}}$ pins separately, this potential backflow can be avoided. V_{OUT} can then be selected from either V1 or V2, irrespective of which supply voltage is higher or lower. While in shutdown, the LTC4368-2 drives the GATE pin just below the lower of V_{IN} and V_{OUT}, thus allowing V_{OUT} to be larger than V_{IN} while in the off condition.

Single MOSFET Higher Power Application

When reverse V_{IN} protection is not needed, only a single external N-channel MOSFET is necessary. This provides the user with a larger selection of MOSFETs (not just dual packages), especially for higher power applications. Note that care must be taken to stay within the SOA of the external MOSFET. The RETRY pin of the LTC4368 can be used to help keep the MOSFET within its SOA. The user can ground the RETRY pin to latch off the MOSFET after a forward current fault. For automatic retry after a forward current fault, C_{RETRY} must be large enough to maintain a low on duty cycle for the MOSFET. See Figure 18.

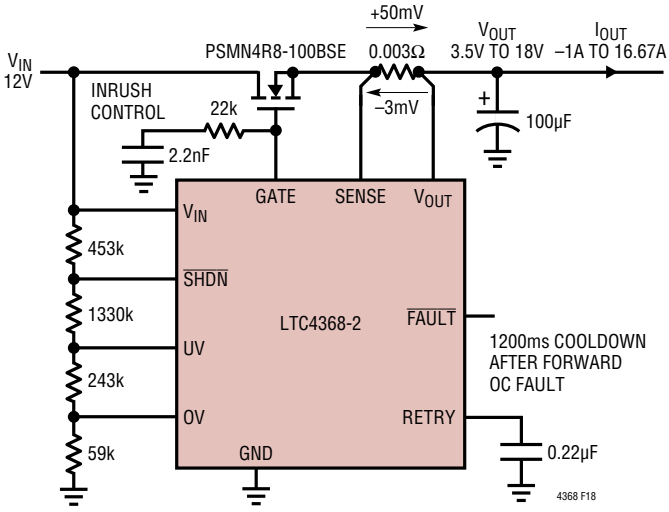


Figure 18. Single MOSFET High Power Application

APPLICATIONS INFORMATION

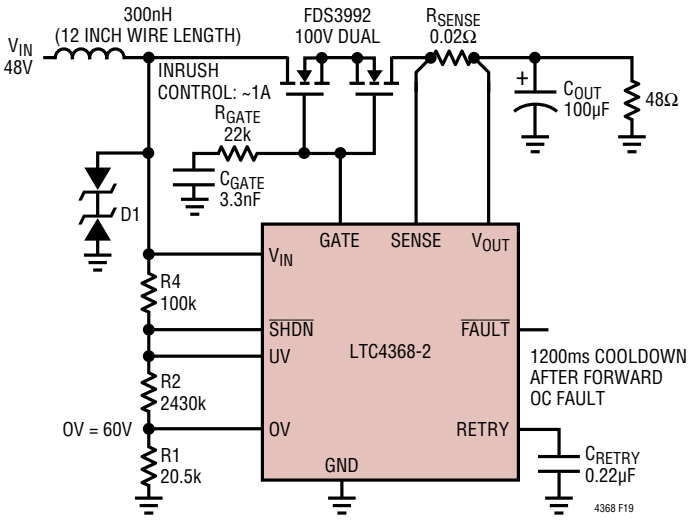


Figure 19. OV Fault with Large V_{IN} Inductance

Transients During OV Fault

The circuit of Figure 19 is used to illustrate transients commonly encountered during an overvoltage condition. The nominal input supply is 48V and it has an overvoltage threshold of 60V. The parasitic inductance is that of a 1 foot wire (roughly 300nH). Figure 20 shows the waveforms during on overvoltage condition at V_{IN}. These transients depend on the parasitic inductance and resistance of the wire along with the capacitance at the V_{IN} node. D1 is an optional power clamp (TVS, TransZorb) recommended for applications where the DC input voltage can exceed 24V and with large V_{IN} parasitic inductance. No clamp was used to capture the waveforms of Figure 20. In order to maintain reverse supply protection, D1 must be a bidirectional clamp with appropriate voltage and power ratings.

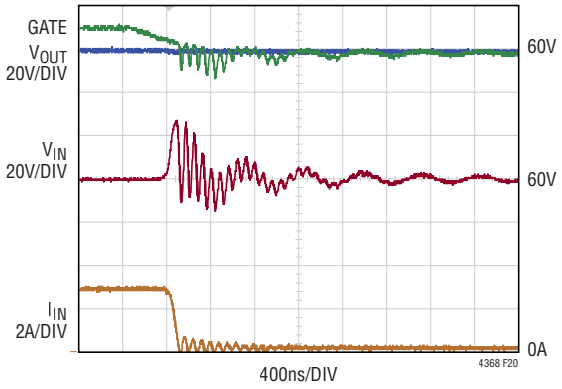


Figure 20. Transients During OV Fault when No TransZorb (TVS) Is Used

Layout Considerations

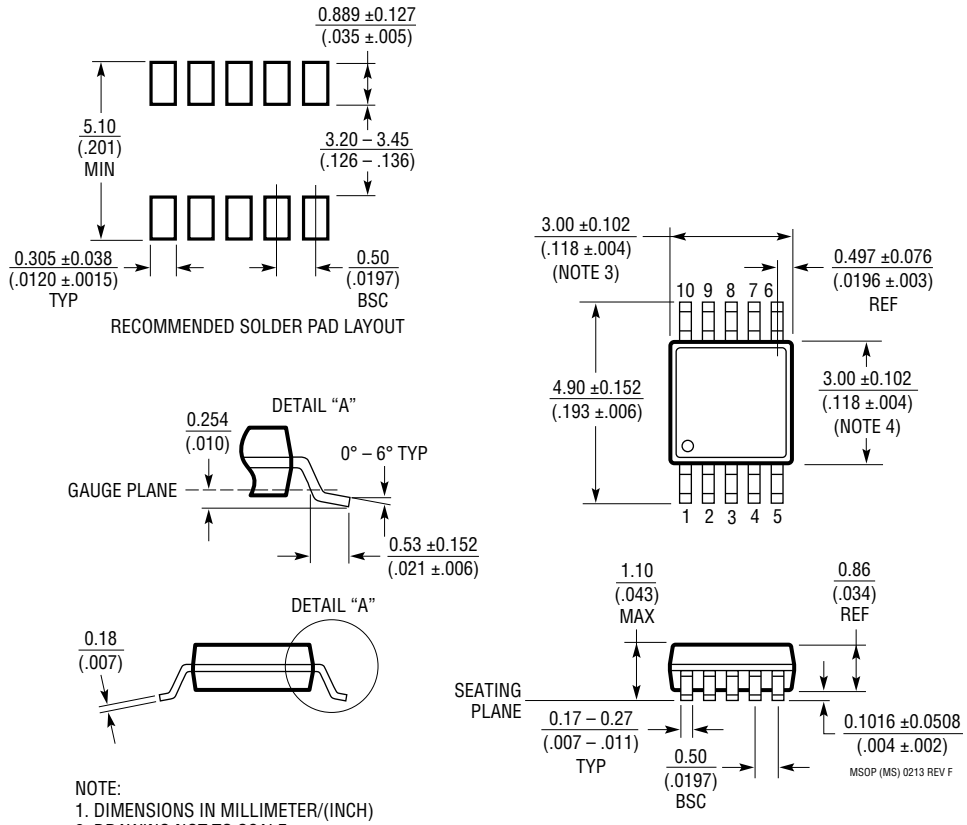
The trace length between the V_{IN} pin and the drain of the external MOSFET should be minimized, as well as the trace length between the GATE pin of the LTC4368 and the gates of the external MOSFETs. The SENSE and V_{OUT} pins must be connected with traces that tie directly and solely to the sense resistor.

Place the bypass capacitors at V_{OUT} as close as possible to the external MOSFET. Use high frequency ceramic capacitors in addition to bulk capacitors to mitigate hot swap ringing. Place the high frequency capacitors closest to the MOSFET. Note that bulk capacitors mitigate ringing by virtue of their ESR. Ceramic capacitors have low ESR and can thus ring near their resonant frequency. The trace length of the GATE pin should be kept as small as possible, and the number of components connected to the GATE pin should also be minimized.

The SOA of the external MOSFET might require the board to have a minimum total area as well as a minimum amount of trace volume connected to the drain and source pins.

PACKAGE DESCRIPTION

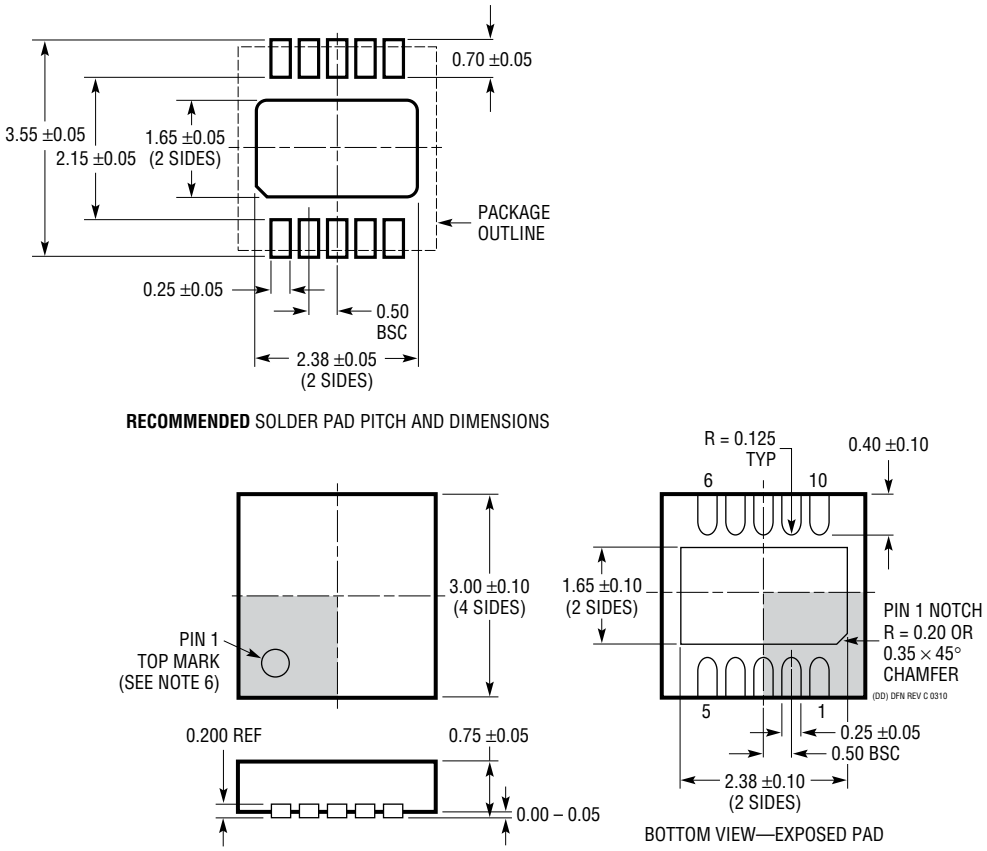
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/18	Attached Note 3 to OV and $\overline{\text{FAULT}}$ Absolute Maximum Ratings.	2
B	06/19	Added AEC-Q100 qualification and W part numbers.	1,3
C	04/21	Added automotive W part numbers for DFN package.	3