7A Ideal Diode with Reverse Input Protection

FEATURES

- **Reduces Power Dissipation by Replacing a Power Schottky Diode**
- **Wide Operating Voltage Range: 4V to 40V**
- **Internal 15mΩ N-Channel MOSFET**
- **Reverse Input Protection to –40V**
- **Low 9µA Shutdown Current**
- Low 150µA Operating Current
- Smooth Switchover without Oscillation
- Available in 16-Pin 5mm × 4mm DFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive Battery Protection
- Redundant Power Supplies
- Portable Battery Devices
- Computer Systems/Servers

DESCRIPTION

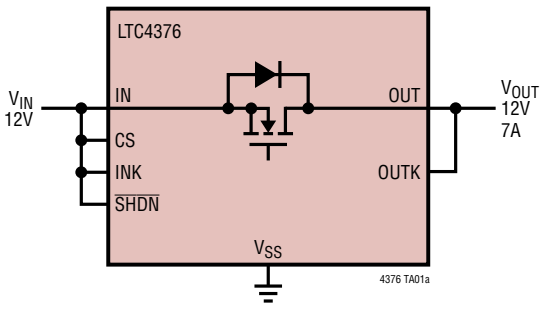
The LTC®4376 is a 7A ideal diode that uses an internal 15mΩ N-channel MOSFET to replace a Schottky diode when used in diode-OR and high current diode applications. The LTC4376 reduces power consumption, heat dissipation and PC board area.

The LTC4376 controls the forward voltage drop across the internal MOSFET to ensure smooth current delivery without oscillation even at light loads. If a power source fails or is shorted, a fast turn-off minimizes reverse current transients. The LTC4376 also easily ORs power sources to increase total system reliability.

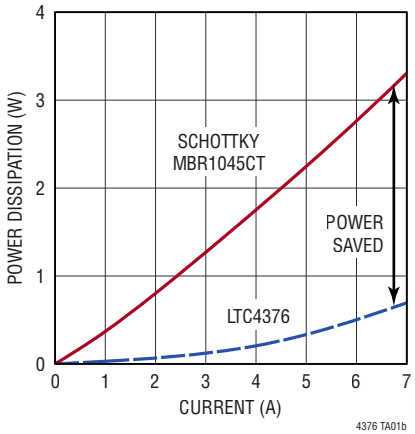
With its low operating voltage, small solution size and the ability to withstand reverse input voltage, the LTC4376 excels in portable battery applications. A shutdown mode is available to reduce the quiescent current to 9µA. The $\overline{SHDN}$ pin can also control the forward current path when an external MOSFET is used in series with the internal MOSFET in a back-to-back configuration.

TYPICAL APPLICATION

12V, 7A Ideal Diode



Power Dissipation vs Load Current

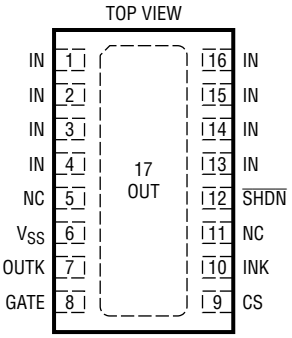


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

IN, INK, CS, $\overline{SHDN}$ ..... –40V to 80V
OUT, OUTK..... –0.3V to 80V
INK–OUTK..... –45V to 100V
INK–CS .....–1V to 80V
IN–OUT (Note 3)..... –45V to 0.3V
GATE (Note 4) ..... V_{CS} – 0.3V to V_{CS} + 10V
Operating Junction Temperature Range
LTC4376C ..... 0°C to 70°C
LTC4376I .....–40°C to 85°C
LTC4376H..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DHD PACKAGE
16-LEAD (5mm × 4mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
MSL RATING 3

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4376CDHD#PBF	LTC4376CDHD#TRPBF	4376	16-Lead (5mm x 4mm) Plastic DFN	0°C to 70°C
LTC4376IDHD#PBF	LTC4376IDHD#TRPBF	4376	16-Lead (5mm x 4mm) Plastic DFN	–40°C to 85°C
LTC4376HDHD#PBF	LTC4376HDHD#TRPBF	4376	16-Lead (5mm x 4mm) Plastic DFN	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC4376IDHD#WPBF	LTC4376IDHD#WTRPBF	4376	16-Lead (5mm x 4mm) Plastic DFN	–40°C to 85°C
LTC4376HDHD#WPBF	LTC4376HDHD#WTRPBF	4376	16-Lead (5mm x 4mm) Plastic DFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{INK} = 4V to 40V, V_{IN} = V_{INK}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{INK}	Operating Supply Range		●	4		40	V
I_{INK}	INK Pin Current	INK = 12V	●		150	250	µA
		INK = OUTK = 12V, $\overline{SHDN}$ = 0V	●		9	30	µA
		INK = OUTK = 24V, $\overline{SHDN}$ = 0V	●		15	40	µA
		INK = –40V	●	0	–15	–40	µA
I_{OUTK}	OUTK Pin Current	INK = 12V, In Regulation	●	3	5	7.5	µA
		INK = 12V, ΔVSD = –1V	●		120	220	µA
		INK = OUTK = 12V, $\overline{SHDN}$ = 0V	●		0.8	3	µA
		INK = OUTK = 24V, $\overline{SHDN}$ = 0V	●		0.8	3	µA
		OUTK = 12V, INK = $\overline{SHDN}$ = 0V	●		6	15	µA
I_{CS}	CS Pin Current	INK = 12V, ΔV_{SD} = –1V	●		150	200	µA
		INK = CS = 12V, $\overline{SHDN}$ = 0V	●	1	4	15	µA
		CS = –40V	●	–0.4	–0.8	–1.5	mA
I_{OUT}	OUT Reverse Leakage Current	IN = GATE = 0V, OUT = 40V	●			150	µA
ΔV_{GATE}	Gate Drive (V_{GATE} – V_{CS})	INK = 4V, I_{GATE} = 0, –1µA	●	4.5	5.5	18	V
		INK = 8V to 40V, I_{GATE} = 0, –1µA	●	10	12	18	V
$\Delta V_{SD(REG)}$	Source-Drain Regulation Voltage (V_{INK} – V_{OUTK})	1mA < I_{IN} < 100mA	●	20	30	45	mV
$\Delta V_{SD(FWD)}$	Body Diode Forward Voltage Drop (V_{IN} – V_{OUT})	I_{IN} = 7A, MOSFET Off	●	0.55	0.77	1	V
$R_{DS(ON)}$	Internal N-Channel MOSFET On Resistance	I_{IN} = 7A	●		15	30	mΩ
I_{AS}	Peak Avalanche Current	L = 0.1mH (Note 5)			40		A
$I_{GATE(UP)}$	Gate Pull-Up Current	GATE = INK, ΔV_{SD} = 0.1V	●	–6	–10	–17	µA
$I_{GATE(DOWN)}$	Gate Pull-Down Current	Fault Condition, ΔV_{GATE} = 5V, ΔV_{SD} = –1V	●	70	130	180	mA
		Shutdown Mode, ΔV_{GATE} = 5V, ΔV_{SD} = 0.7V	●	0.6			mA
t_{OFF}	Gate Turn-Off Delay Time	ΔV_{SD} = 0.1V to –1V, ΔV_{GATE} < 2V	●		0.3	0.5	µs
$V_{\overline{SHDN}(TH)}$	$\overline{SHDN}$ Pin Input Threshold	INK = 4V to 40V	●	0.6	1.2	2	V
$V_{\overline{SHDN}(FLT)}$	$\overline{SHDN}$ Pin Float Voltage	INK = 4V to 40V	●	0.6	1.75	2.5	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ = 0.5V	●	–0.5	–3	–5	µA
		$\overline{SHDN}$ = –40V	●	–0.4	–0.8	–1.5	mA
I_{LEAK}	$\overline{SHDN}$ Leakage Current	$\overline{SHDN}$ = 2.6V	●			1	µA
$V_{CS(TH)}$	Reverse CS Threshold for GATE Off	GATE = 0V, $I_{GATE(DOWN)}$ = 1mA	●	–0.9	–1.8	–2.7	V

Note 1: Stresses beyond those listed underAbsolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to V_{SS} unless otherwise specified.

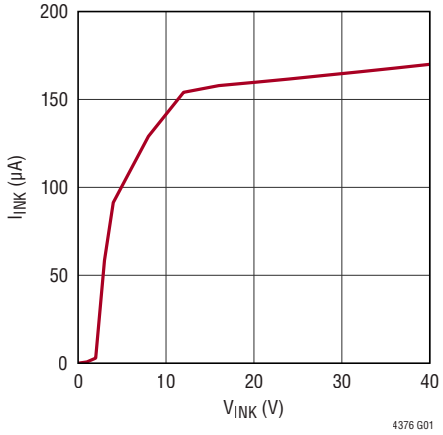
Note 3: This voltage is set by the MOSFET's body diode and will safely exceed 0.3V during start-up for a limited time determined by the body diode thermal dissipation.

Note 4: An internal clamp limits the GATE pin to a minimum of 10V above CS or 90V above V_{SS}. Driving this pin to voltages beyond the clamp may damage the device.

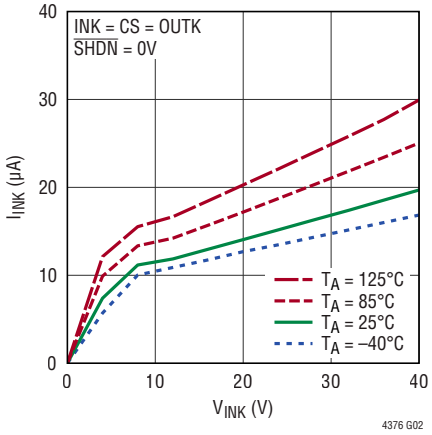
Note 5: The I_{AS} typical value is based on characterization and is not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

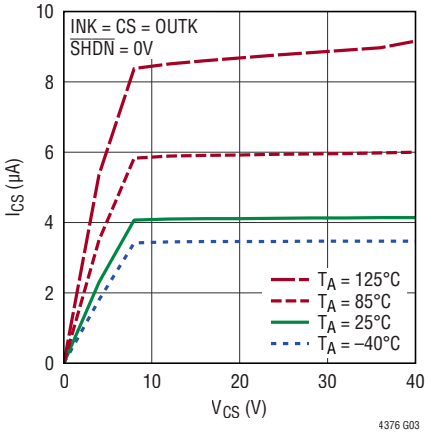
INK Current in Regulation



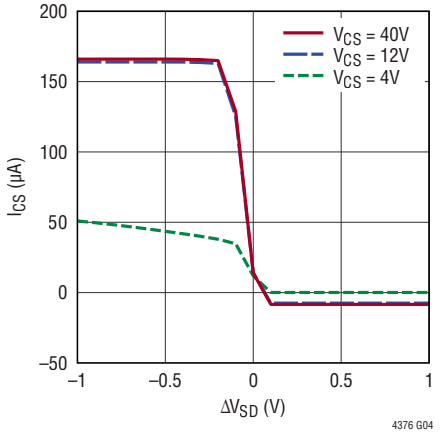
INK Current in Shutdown



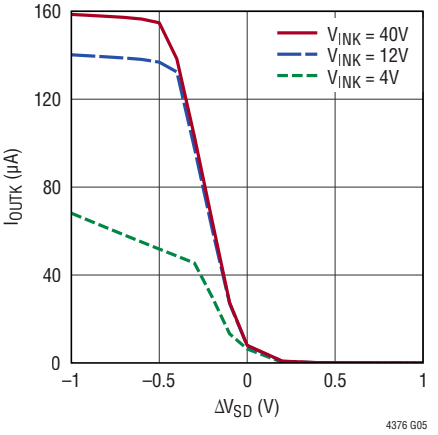
CS Current in Shutdown



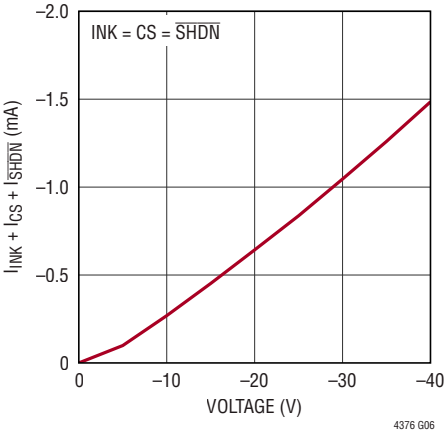
CS Current vs Forward Voltage Drop



OUTK Current vs Forward Voltage Drop

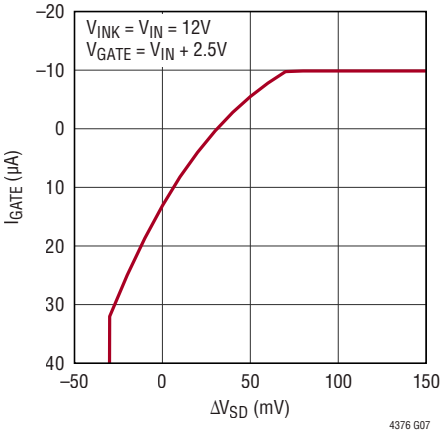


Total Negative Current vs Negative Input Voltage

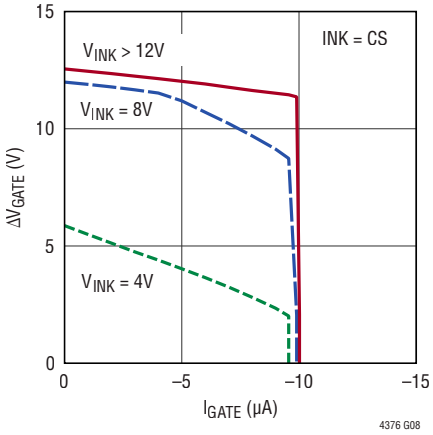


TYPICAL PERFORMANCE CHARACTERISTICS

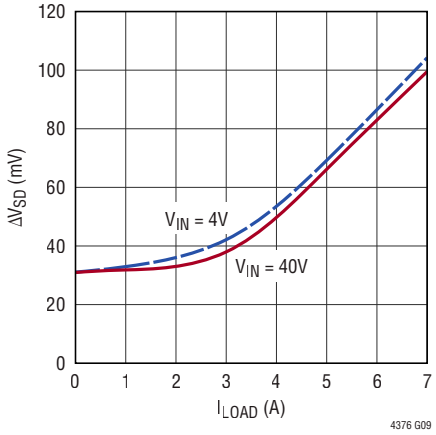
GATE Current vs Forward Voltage Drop



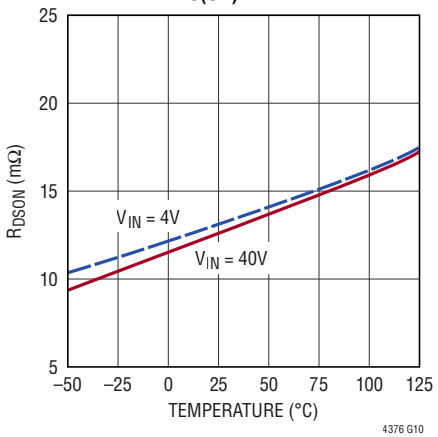
GATE Drive vs GATE Current



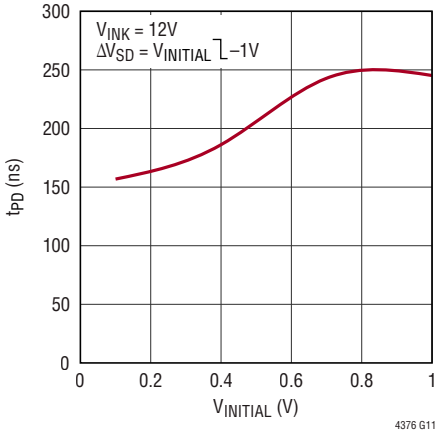
Forward Voltage Drop vs Load Current



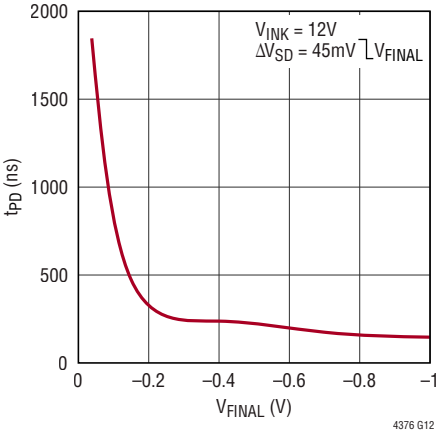
MOSFET $R_{DS(ON)}$ vs Temperature



FET Turn-Off Time vs Initial Overdrive



FET Turn-Off Time vs Final Overdrive



PIN FUNCTIONS

CS: Gate Drive Return. The fast pull-down current is returned through this pin during a reverse current event. This pin can be connected to IN or left open.

GATE: Gate Drive Output. The GATE pin pulls high, enhancing the N-channel MOSFET when the load current creates more than 30mV of voltage drop across the MOSFET. When the load current is small, GATE is actively driven to maintain 30mV across the MOSFET. If reverse current flows, a fast pull-down circuit quickly connects GATE to the CS pin within 300ns, turning off the MOSFET. Connect this pin to the gate of the external MOSFET in a back-to-back configuration, otherwise leave open.

IN: Source of Internal N-Channel MOSFET. IN is the anode of the ideal diode.

INK: Voltage Sense and Supply Voltage. The voltage sensed at this pin is used to control the MOSFET voltage drop. Connect this pin to IN.

NC: No Connection. Not internally connected.

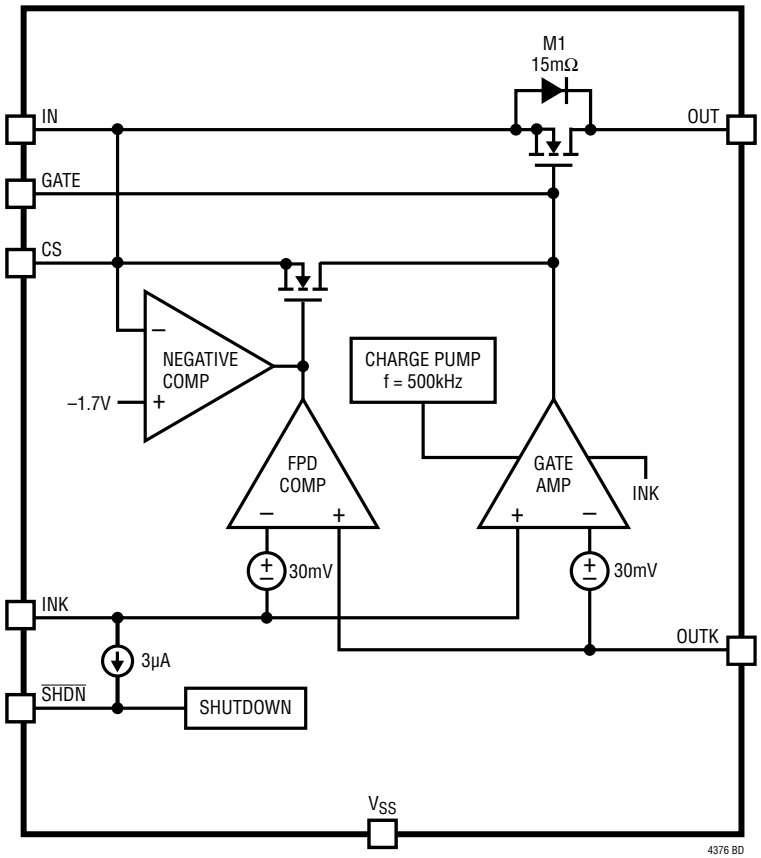
OUT: The exposed pad is the drain of the internal N-channel MOSFET. OUT is the cathode of the ideal diode and the common output when multiple LTC4376s are configured as an ideal diode-OR.

OUTK: Drain Voltage Sense. The voltage sensed at this pin is used to control the MOSFET voltage drop. Connect this pin to OUT.

$\overline{\text{SHDN}}$: Shutdown Control Input. The LTC4376 can be shut down to a low current mode by pulling the $\overline{\text{SHDN}}$ pin below 0.6V. Pulling this pin above 2V turns the part on. The $\overline{\text{SHDN}}$ pin can be pulled up to 40V or below V_{SS} by 40V without damage. If the shutdown feature is not used, connect $\overline{\text{SHDN}}$ to IN.

V_{SS}: Device Ground.

BLOCK DIAGRAM



Rev. A

OPERATION

The LTC4376 is a single positive voltage ideal diode controller that drives an internal N-channel MOSFET as a pass transistor to replace a Schottky diode. The IN and OUT pins form the anode and cathode of the ideal diode, respectively. The input supply is connected to the IN pins, while the OUT pin serves as the output. Both the INK and OUTK pins are connected directly to IN and OUT respectively.

The GATE amplifier (see Block Diagram) senses across INK and OUTK and drives the gate of the internal MOSFET to regulate the forward voltage to 30mV. As the load current increases, GATE is driven higher until a point is reached where the internal MOSFET is fully on. Further increases in load current result in a forward drop of $R_{DS(ON)} \bullet I_{LOAD}$.

If the load current is reduced, the GATE amplifier drives the MOSFET gate lower to maintain a 30mV drop. If the input voltage is reduced to a point where a forward drop of 30mV cannot be supported, the GATE amplifier drives the MOSFET off.

In the event of a rapid drop in input voltage, such as an input short-circuit fault or negative-going voltage spike, reverse current briefly flows through the MOSFET until it shuts off. This current is provided by any load capacitance and by other supplies or batteries that feed the output in diode-OR applications. The FPD COMP (Fast Pull-Down Comparator) quickly responds to this condition by turning the MOSFET off in 300ns, thus minimizing the disturbance to the output bus.

The IN, INK, CS, GATE and $\overline{SHDN}$ pins are protected against reverse inputs of up to –40V. The NEGATIVE COMP detects negative input potentials at the CS pin and quickly pulls GATE to CS, turning off the MOSFET and isolating the load from the negative input.

When pulled low, the $\overline{SHDN}$ pin turns off most of the internal circuitry, reducing the quiescent current to 9µA and holding the MOSFET off. The $\overline{SHDN}$ pin may be either driven high or pulled up with a resistor of 1MΩ or less to enable the LTC4376. In applications where an external MOSFET is used in series with the internal MOSFET, the $\overline{SHDN}$ pin serves as an on/off control for the forward path, as well as enabling the diode function.

APPLICATIONS INFORMATION

Blocking diodes are commonly placed in series with supply inputs for the purpose of ORing redundant power sources and protecting against supply reversal. The LTC4376 replaces diodes in these applications to reduce both the voltage drop and power loss associated with a passive solution.

The LTC4376 has a wide operating range of 4V to 40V which allows operation during cold crank conditions and transient conditions. The LTC4376 also protects against negative inputs to –40V, which can occur when the automotive battery is reversed.

A 12V/7A ideal diode application is shown in Figure 1a. Ideal diodes, like their non-ideal counterparts, exhibit a behavior known as reverse recovery. In combination with parasitic or intentionally introduced inductances, reverse recovery spikes may be generated by an ideal diode during commutation. D1, D2 and R1 protect against these spikes which might otherwise exceed the LTC4376's –40V to 40V survival rating. If reverse input protection is not needed, Figure 1a can be simplified to Figure 1b. D1 and C_{OUT} absorb the reverse recovery energy and protect the LTC4376. Spikes and protection schemes are discussed in detail in the Input Short-Circuit Faults section.

It is important to note that the $\overline{SHDN}$ pin, while disabling the LTC4376 and reducing its current consumption to 9µA, does not disconnect the load from the input since the internal MOSFET's body diode is ever-present. Adding an external MOSFET permits use in load switching applications.

APPLICATIONS INFORMATION

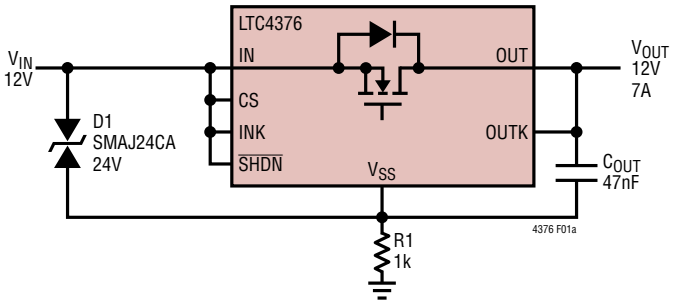


Figure 1a. 12V/7A Ideal Diode with Reverse Input Protection

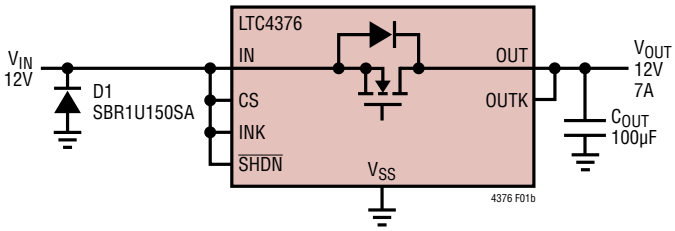


Figure 1b. 12V/7A Ideal Diode without Reverse Input Protection

Shutdown Mode

In shutdown, the LTC4376 pulls GATE low to CS, turning off the internal MOSFET and reducing its current consumption to 9µA. Shutdown does not interrupt forward current flow, a path is still present through the internal MOSFET's body diode. A second external MOSFET is needed to block the forward path; see the section Load Switching and Inrush Control. When enabled, the LTC4376 operates as an ideal diode. If shutdown is not needed, connect $\overline{SHDN}$ to IN. $\overline{SHDN}$ may be driven with a 3.3V or 5V logic signal or pulled up with an external resistor to IN. To enable the part, $\overline{SHDN}$ must be pulled up to at least 2V. Use a resistor value that provides more than the $\overline{SHDN}$ pin leakage current of 1µA at 2.6V. A value of 1MΩ or less is sufficient to turn the part on. To assert $\overline{SHDN}$ low, the pull-down must sink at least 5µA plus the current provided by the external pull-up resistor at 500mV. When a high impedance pull-up resistor is used, $\overline{SHDN}$ is subject to capacitive coupling from nearby clock lines or traces exhibiting high dV/dt. Bypass $\overline{SHDN}$ to V_{SS} with 10nF to eliminate injection. Figure 2 is the simplest way to control the shutdown pin. Since the control signal ground is different from the $\overline{SHDN}$ pin reference, V_{SS}, there could be momentary glitches on $\overline{SHDN}$ during transients. Figure 3 and Figure 4 are alternative solutions that level-shift the control signal and eliminate glitches.

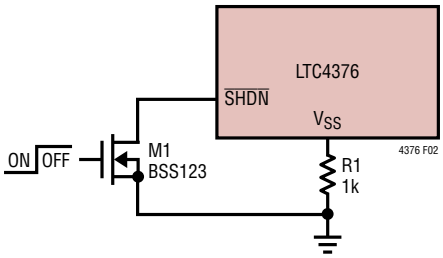


Figure 2. $\overline{SHDN}$ Control

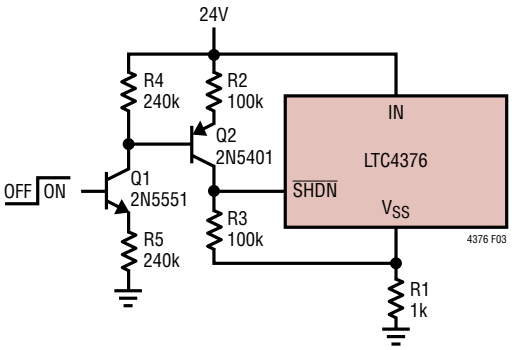


Figure 3. Transistor $\overline{SHDN}$ Control

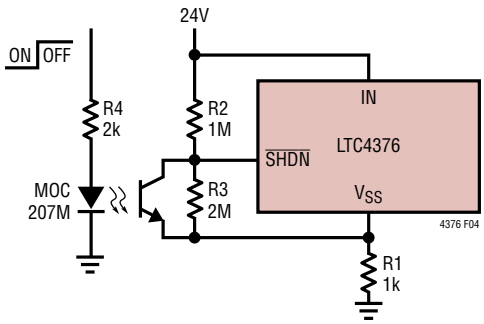


Figure 4. Opto-Isolator $\overline{SHDN}$ Control

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/µs or higher.

APPLICATIONS INFORMATION

High slew rates coupled with parasitic inductances in series with the input and output paths may cause potentially destructive transients to appear at the IN, CS and OUT pins of the LTC4376 during reverse recovery. A zero impedance short-circuit directly across the input and ground is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the internal MOSFET finally turns off to interrupt the reverse current, the LTC4376 IN and CS pins experience a negative voltage spike while the OUT pin spikes in the positive direction.

To prevent damage to the LTC4376 under conditions of input short-circuit, protect the IN, CS and OUT pins as shown in Figure 5. The IN and CS pins are protected by clamping to the V_{SS} pin with a Tranzorb or TVS. For input voltages 24V and greater, D3 is needed to protect the internal MOSFET's gate oxide during input short-circuit conditions. Negative spikes, seen after the MOSFET turns off during an input short, are clamped by D2, a 24V TVS. D2 allows reverse inputs to 24V while keeping the MOSFET off and is not required if reverse input protection is not needed. D1 blocks D2 from conducting during normal operation. When the input short condition disappears, the current stored in the source parasitic inductance, L_S, flows through the body diode of the MOSFET charging up C_{LOAD}. If C_{LOAD} is small or nonexistent, both the IN/CS and OUT pins may rise to a level that can damage the LTC4376. In this case, D1 will need to be a TVS or TransZorb to limit the voltage difference between the IN/CS and V_{SS} pins.

OUT is protected by the MOSFET's avalanche breakdown. Nevertheless, the MOSFET could be damaged by excessive current in applications greater than 24V. If the input is greater than 24V, then a 28V TVS (SMAJ28A) or a snubber can be used to protect the MOSFET and OUT pin. The snubber allows applications up to 40V (see Figure 13). C_{OUT} and R1 preserve the fast turn-off time when output parasitic inductance causes the IN and OUT voltages to drop quickly.

Paralleling Supplies

Multiple LTC4376s can be used to combine the outputs of two or more supplies for redundancy or for droop sharing, as shown in Figure 6. For redundant supplies, the supply with the highest output voltage sources most or all of the load current. If this supply's output is quickly shorted to ground while delivering load current, the flow of current temporarily reverses and flows backwards through the LTC4376's internal MOSFET. The LTC4376 senses this reverse current and activates a fast pull-down to quickly turn off the MOSFET.

If the other, initially lower supply was not delivering any load current at the time of the fault, the output falls until the body diode of its ORing internal MOSFET conducts. Meanwhile, the LTC4376 charges the internal MOSFET gate with 10µA until the forward drop is reduced to 30mV. If this supply was sharing load current at the time of the fault, its associated ORing internal MOSFET was already driven partially on. In this case, the LTC4376 will simply

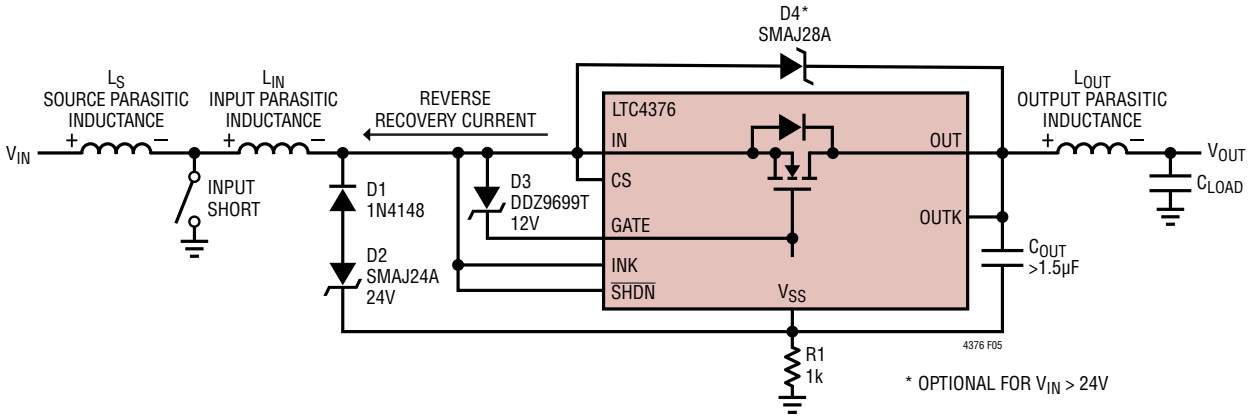


Figure 5. Reverse Recovery Produces Inductive Spikes at the IN, CS and OUT Pins. The Polarity of Step Recovery Is Shown Across Parasitic Inductances

APPLICATIONS INFORMATION

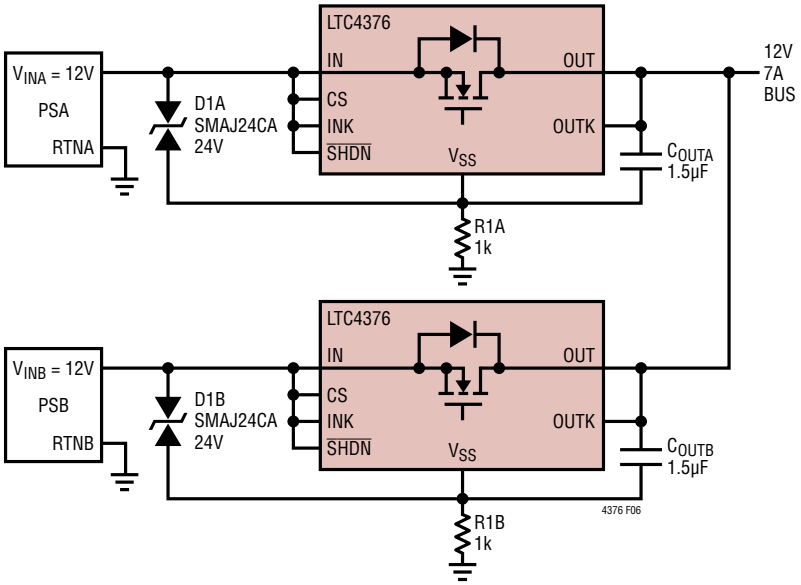


Figure 6. Redundant Power Supplies

drive the internal MOSFET gate harder in an effort to maintain a drop of 30mV.

Droop sharing can be accomplished if both power supply output voltages and output impedances are nearly equal. The 30mV regulation technique ensures smooth load sharing between outputs without oscillation. The degree of sharing is a function of internal MOSFET $R_{DS(ON)}$, the output impedance of the supplies and their initial output voltages.

Load Switching and Inrush Control

By adding an external MOSFET as shown in Figure 7, the LTC4376 can be used to control power flow in the forward direction while retaining ideal diode behavior in the reverse direction. The body diodes of both the external and internal MOSFETs prohibit current flow when the MOSFETs are off. The internal MOSFET serves as the ideal diode, while the external MOSFET, M1, acts as a switch to control forward power flow. On/Off control is provided by the $\overline{SHDN}$ pin, and C1 and R3 may be added if inrush control is desired.

When $\overline{SHDN}$ is driven high and provided $V_{IN} > V_{OUT} + 30mV$, GATE sources 10µA and gradually charges C1, pulling up both MOSFET gates. The external MOSFET operates as source follower and

$$I_{INRUSH} = \frac{10\mu A \bullet C_{LOAD}}{C1}$$

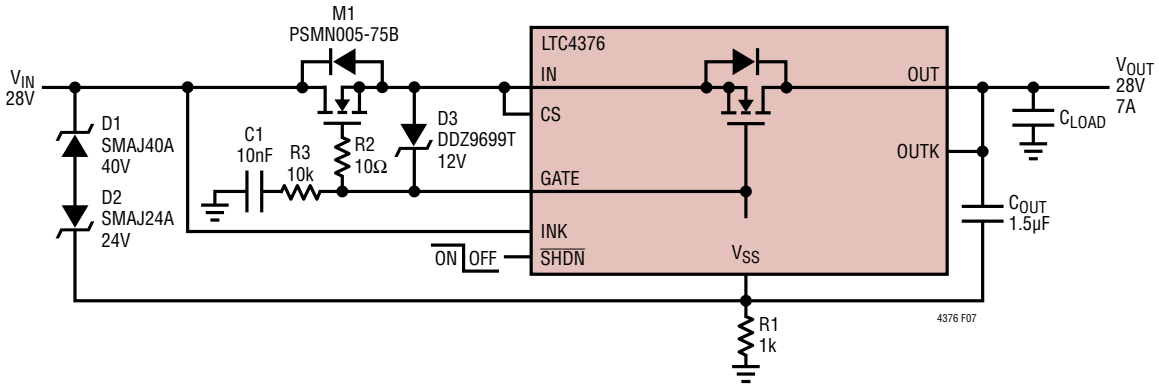


Figure 7. 28V Load Switch and Ideal Diode with Reverse Input Protection

APPLICATIONS INFORMATION

If $V_{IN} < V_{OUT}$ + 30mV, the LTC4376 will be activated but holds both the MOSFETs off until the input exceeds the output by 30mV. In this way, normal diode behavior of the circuit is preserved, but with soft starting when the diode turns on.

When $\overline{SHDN}$ is pulled low, GATE pulls both the MOSFET gates down quickly to CS turning off both forward and reverse paths, and the input current is reduced to 9µA.

While C1 and R3 may be omitted if soft starting is not needed, R2 is necessary to prevent MOSFET parasitic oscillations and must be placed close to the external MOSFET, M1.

Layout Considerations

The following advice should be considered when laying out a printed circuit board for the LTC4376: The INK and OUTK pins should be connected as close as possible to the IN and OUT pins respectively for good accuracy. The PCB traces associated with the power path through the MOSFET should have low resistance. Keep the traces to the IN and OUT wide and short to minimize resistive losses. To ensure a low resistance contact, solder the device's OUT pin to the board using a reflow process. The wide OUT trace also acts as a heat sink to remove the heat from the device at high current load. Place C_{OUT}, surge suppressors and necessary transient protection components close to the LTC4376 using short lead lengths. See Figure 8 for the recommended layout. The temperature rise of the recommended layout with 7A is 50°C.

Figure 9 through Figure 16 show typical applications of the LTC4376.

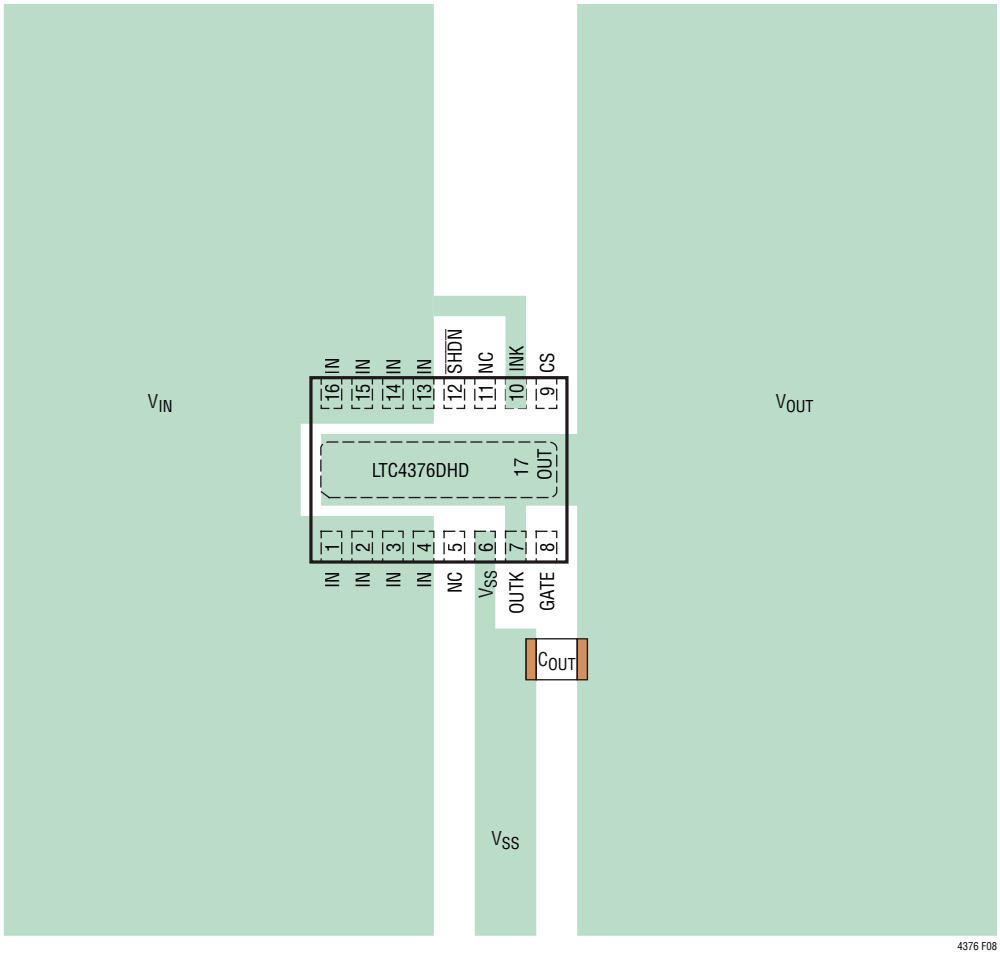


Figure 8. Recommended Layout for DFN Package

APPLICATIONS INFORMATION

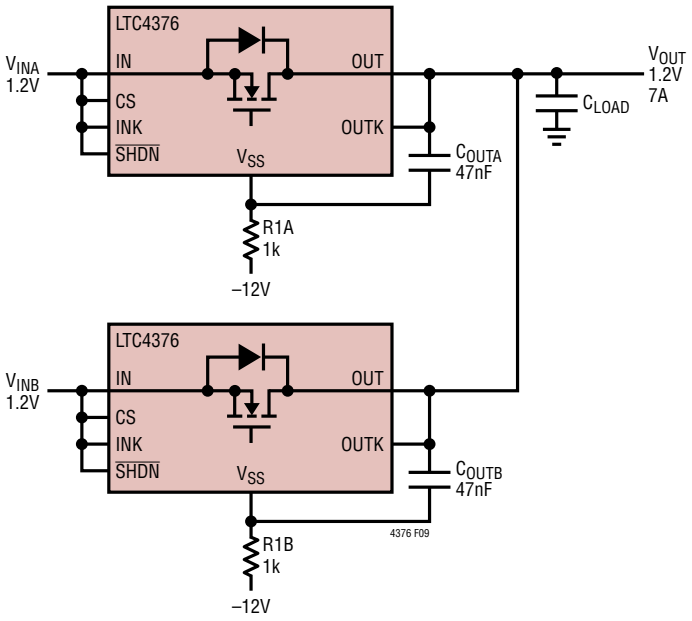


Figure 9. 1.2V Diode-OR

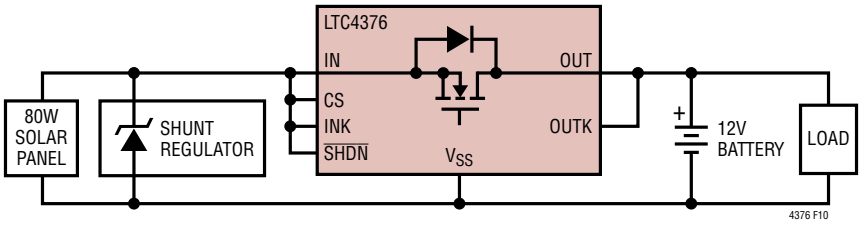


Figure 10. Lossless Solar Panel Isolation

APPLICATIONS INFORMATION

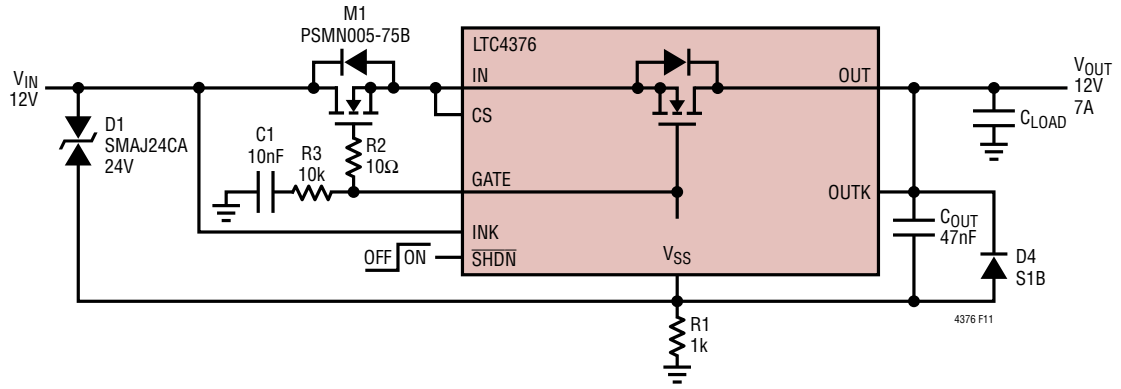


Figure 11. 12V Load Switch and Ideal Diode with Reverse Input Protection

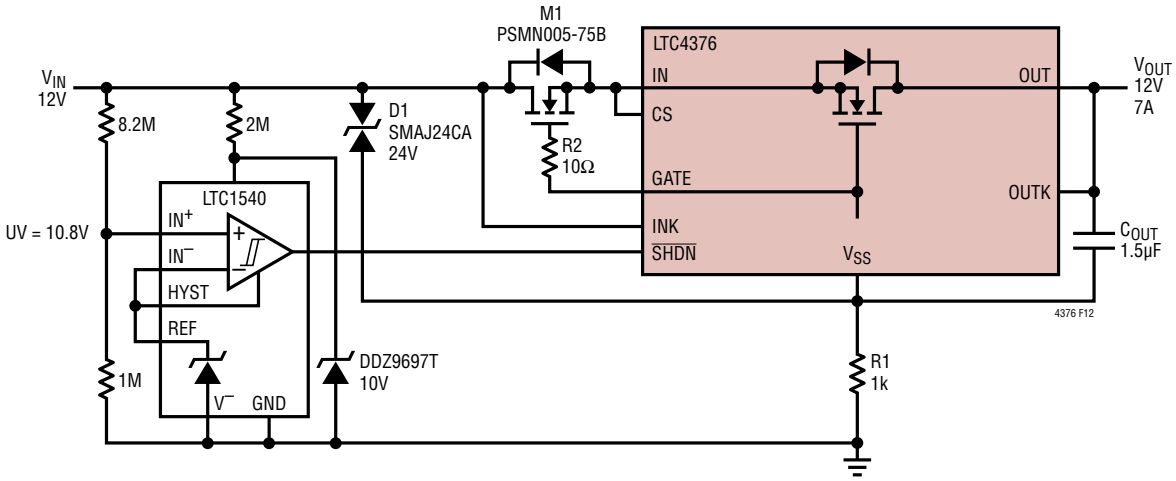


Figure 12. 12V Load Switch and Ideal Diode with Precise Undervoltage Lockout

APPLICATIONS INFORMATION

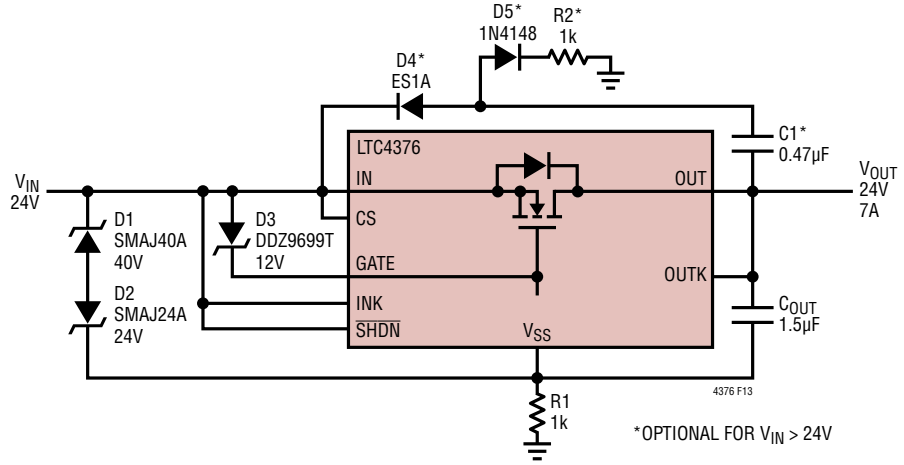


Figure 13. 24V/7A Ideal Diode with Reverse Input Protection to $V_{IN} < V_{OUT} – 40V$

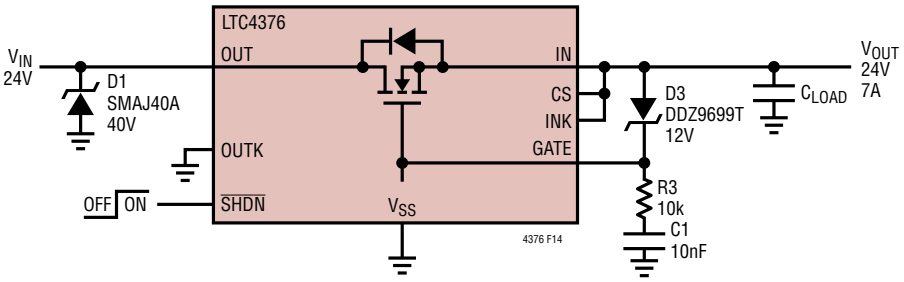


Figure 14. 24V Load Switch without Ideal Diode Function

APPLICATIONS INFORMATION

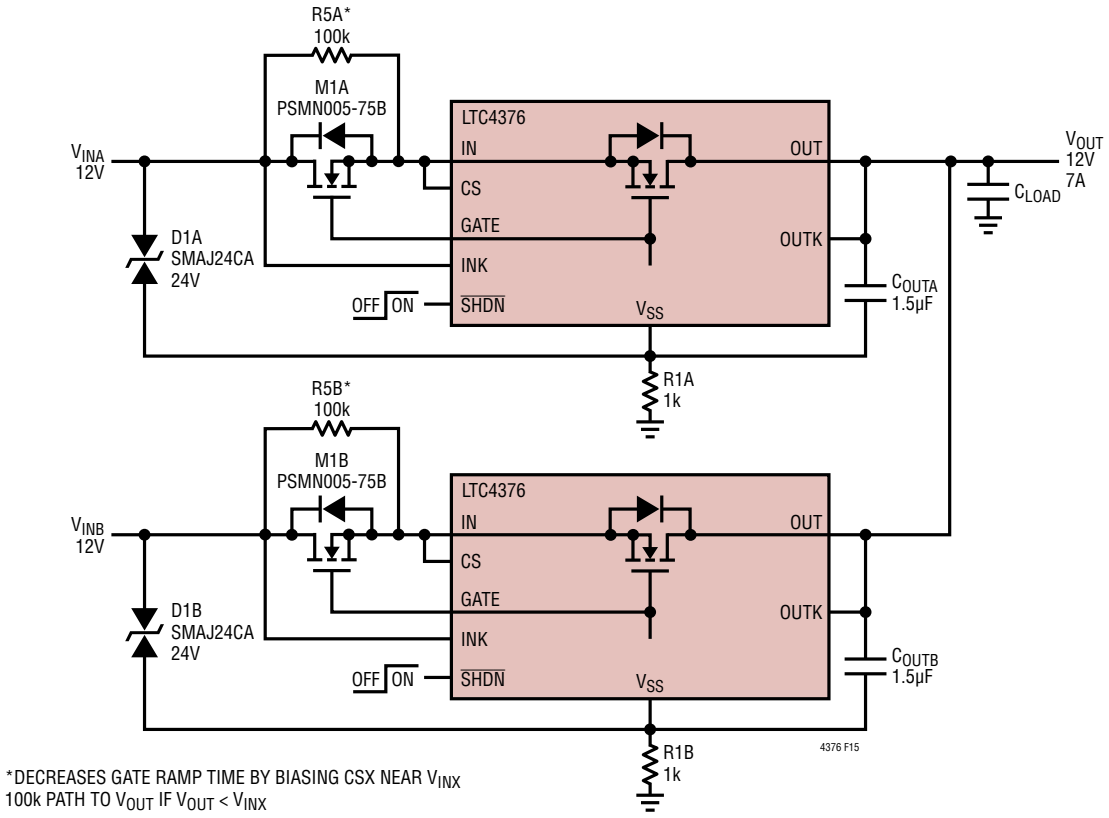


Figure 15. Diode-OR with Selectable Power Supply Feeds and Reverse Input Protection

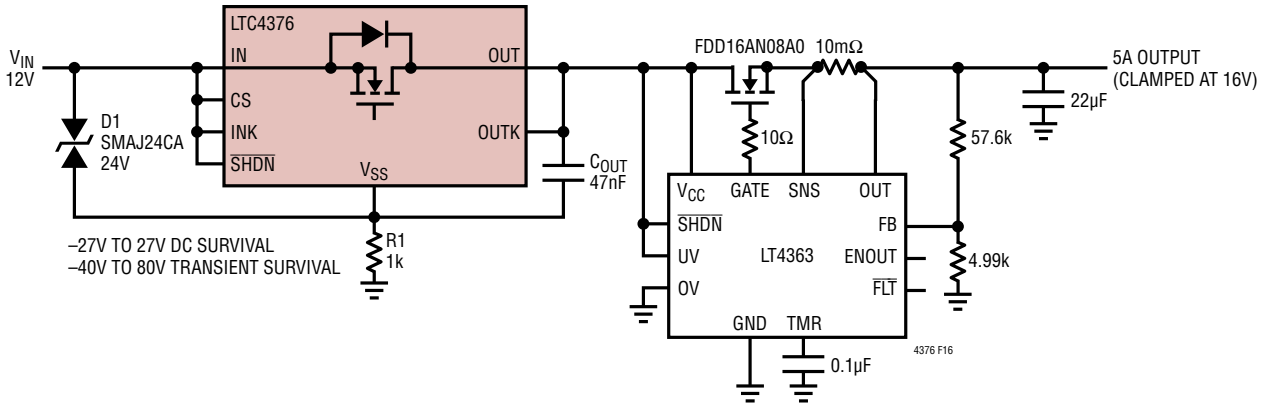
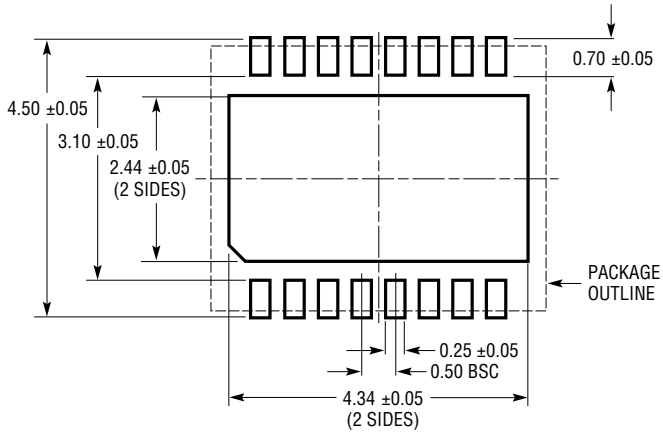


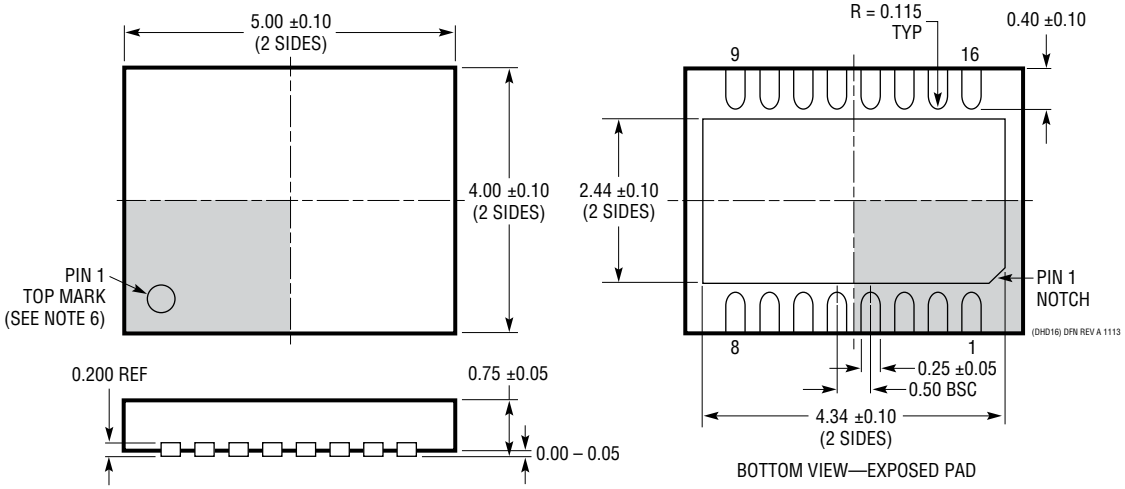
Figure 16. Overvoltage Protector and Ideal Diode Blocks Reverse Input Voltage

PACKAGE DESCRIPTION

DHD Package
16-Lead Plastic DFN (5mm × 4mm)
(Reference LTC DWG # 05-08-1707 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJGD-2) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/19	Added AEC-Q100.	1, 2