Low Quiescent Current eFuse with Surge Protection

FEATURES

- **Withstands Surge Voltages Up to 100V**
- **Internal 9mΩ N-Channel MOSFET**
- **Guaranteed Safe Operating Area: 20ms at 70V, 1A**
- **Low Quiescent Current: 6µA Operating**
- **Operates Through Automobile Cold Crank**
- **Wide Operating Voltage Range: 4V to 72V**
- **No Input TVS needed**
- **Overcurrent Protection**
- **Selectable Internal 28.5V/47V or Adjustable Output Clamp Voltage (Table 1)**
- Reverse Input Protection to –60V
- Adjustable Turn-On Threshold
- Adjustable Fault Timer with MOSFET Stress Acceleration
- Latchoff and Retry Options (Table 1)
- Low Retry Duty Cycle During Faults (Table 1)
- 32-Lead DFN (7mm × 5mm) Package

APPLICATIONS

- Automotive 12V, 24V and 48V System
- Avionic/Industrial Surge Protection
- Hot Swap/Live Insertion
- High Side Switch for Battery Powered Systems
- Automotive Load Dump Protection

DESCRIPTION

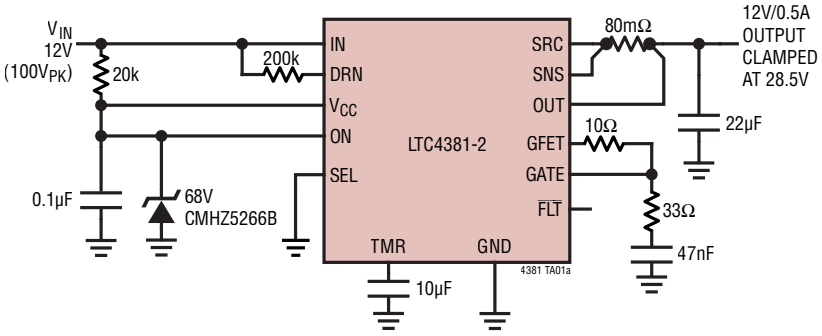
The LTC®4381 is an integrated solution for low quiescent current eFuse with an internal 9mΩ N-Channel MOSFET. Overvoltage protection is provided by clamping the gate voltage of an internal 9mΩ N-channel MOSFET to limit the output voltage to a safe value during overvoltage events such as load dump in automobiles. The MOSFET safe operating area is production tested and guaranteed for the stresses during high voltage transients. Fixed output clamp voltages are selectable for 12V and 24V/28V systems. For systems of any voltage up to 80V, use the adjustable clamp versions.

Overcurrent protection is also provided. An internal multiplier generates a TMR pin current proportional to V_{DS} and I_D, so that operating time in both overcurrent and overvoltage conditions is limited in accordance with MOSFET stress.

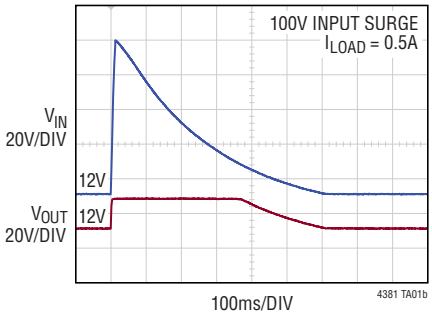
The GATE pin can drive back-to-back MOSFETs for reverse input protection, eliminating the voltage drop and dissipation of a Schottky diode solution. A low 6µA operating current permits use in always-on and battery powered applications.

TYPICAL APPLICATION

12V System with 100V/0.5A/400ms Load Dump Overvoltage Protection



12V, 0.5A with 100V Overvoltage Protection

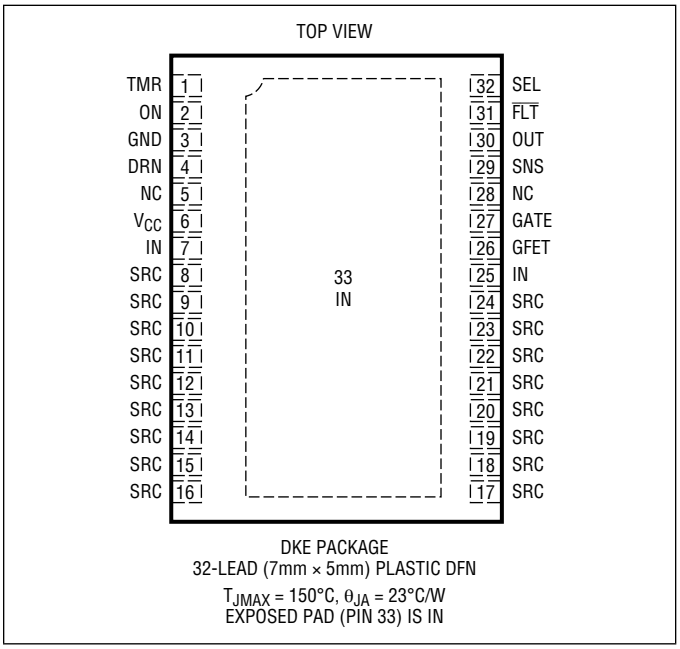


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

IN (Note 5) ..... –0.3V to 100V
V_{CC}, ON, SEL ..... –60V to 80V
DRN (Note 3), SNS, OUT, SRC
  LTC4381-1/LTC4381-2 ..... –0.3V to 53V
  LTC4381-3/LTC4381-4 ..... –0.3V to 80V
SNS to OUT ..... –5V to 5V
GATE, GFET (Note 4)
  LTC4381-1/LTC4381-2 ..... –0.3V to 53V
  LTC4381-3/LTC4381-4 ..... –0.3V to 86V
GATE to OUT, GATE to V_{CC},
  GFET to SRC (Note 4) ..... –0.3V to 10V
TMR ..... –0.3V to 5V
$\overline{FLT}$ ..... –0.3V to 80V
I_{DRN} 2.5mA
Operating Junction Temperature Range
  LTC4381A ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DKE PACKAGE
32-LEAD (7mm × 5mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 23°C/W
EXPOSED PAD (PIN 33) IS IN

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4381ADKE-1#PBF	LTC4381ADKE-1#TRPBF	43811	32-Lead (7mm × 5mm) Plastic DFN	–40°C to 125°C
LTC4381ADKE-2#PBF	LTC4381ADKE-2#TRPBF	43812	32-Lead (7mm × 5mm) Plastic DFN	–40°C to 125°C
LTC4381ADKE-3#PBF	LTC4381ADKE-3#TRPBF	43813	32-Lead (7mm × 5mm) Plastic DFN	–40°C to 125°C
LTC4381ADKE-4#PBF	LTC4381ADKE-4#TRPBF	43814	32-Lead (7mm × 5mm) Plastic DFN	–40°C to 125°C

Contact ADI Sales for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = OUT = SNS = DRN = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
V_{IN}	Input Voltage Range	(Note 7)	●	4		80	V
V_{CC}	Operating Voltage Range	LTC4381-1/LTC4381-2 (Note 7) LTC4381-3/LTC4381-4 (Note 7, 8)	● ●	4 4		80 72	V V
V_{OUT}	Operating Voltage Range	V_{CC} = OUT = SNS = DRN = 12V	●			72	V
I_Q	Total Supply Current, ON (Note 6)	C-Grade and I-Grade H-Grade	● ●		6	12 20	µA µA
		V_{CC} = OUT = SNS = DRN = 4V	●		18	35	µA
I_{CC}	V_{CC} Current, Shutdown	ON = OUT = SNS = 0V	●		5	10	µA
	V_{CC} Current, ON	V_{CC} = OUT = SNS = DRN = 12V	●		4	12	µA
		V_{CC} = OUT = SNS = DRN = 4V	●		16	30	µA
I_{IN}	IN pin Leakage Current	V_{IN} = 24V, V_{GFET} = V_{SRC} = 0V, ON = 0V	●			10	µA
I_R	Reverse Input Current	V_{CC} = –60V, ON Open, SEL = 0V V_{CC} = ON = SEL = –60V	● ●		0 –1	–2 –5	mA mA
R_{ON}	MOSFET On-Resistance	IN = V_{CC} = 8V, 12V, I_{SRC} = –1A, I_{GATE} = –1µA	 ●		9	13 28	mΩ mΩ
SOA	MOSFET Safe Operating Area	V_{IN} – V_{SRC} = 70V, 1A, 10W$\sqrt{s}$		20			ms
I_{AL}	MOSFET Avalanche Current	(Note 9)			82		A
SNS, OUT, SEL, ON, DRN							
I_{SNS}	SNS Current, ON		●		0.5	1.4	µA
$I_{OUT, ON}$	OUT Current, ON		●		1.5	5.5	µA
$I_{OUT, SD}$	OUT Current, Shutdown	C-Grade and I-Grade H-Grade	● ●		6	12 80	µA µA
ΔV_{SNS}	Current Limit Sense Voltage (SNS – OUT)	V_{CC} = 12V, 24V, OUT = 6V, 12V V_{CC} = 12V, 24V, OUT = 0V	● ●	45 40	50 62	55 95	mV mV
I_{SEL}	SEL Input Current	SEL = 0V to 80V	●			±0.1	µA
V_{SEL}	SEL Input Threshold		●	0.4		3	V
I_{ON}	ON Input Current	V_{ON} = 1V	●	–1	–2	–4	µA
V_{ON}	ON Input Threshold	ON Rising	●	0.99	1.05	1.1	V
$V_{ON(HYST)}$	ON Input Hysteresis				45		mV
ΔV_{DRN}	DRN Voltage (DRN – OUT)	I_{DRN} = 0.1mA	●	0.7	2.25	2.6	V
$V_{DS(MAX)}$	Overvoltage V_{DS} Threshold (DRN – OUT)	TMR = 0.8V, I_{DRN} = 2µA	 ●	0.58 0.3	0.7	0.8 1.0	V V
SRC, GATE, FLT, TMR							
V_{SRC}	SRC Voltage Output Clamp	V_{IN} = V_{CC} = 80V, SEL = 0V, I_{OUT} = –10mA, LTC4381-1/LTC4381-2 V_{IN} = V_{CC} = 80V, SEL = V_{CC}, I_{OUT} = –10mA, LTC4381-1/LTC4381-2 V_{IN} = 80V, V_{CC} = 12V, I_{OUT} = –10mA, LTC4381-3/LTC4381-4 V_{IN} = 80V, V_{CC} = 24V, I_{OUT} = –10mA, LTC4381-3/LTC4381-4	● ● ● ●	25.5 43.5 19.0 31.0	28.5 47.0 22.5 34.5	31.5 50.5 26.0 38.0	V V V V
$V_{GFET(TH)}$	MOSFET Threshold	I_{SRC} = –10mA	●	1	3	4.6	V
ΔV_{GATE}	GATE Drive (GATE – OUT)	SEL = SNS = OUT = V_{CC}, 8V ≤ V_{CC} ≤ 30V	●	10	11.1	14	V
ΔV_{CLAMP}	GATE Clamp to V_{CC} (GATE – V_{CC})	SNS = OUT = 20V, I_{GATE} = 0µA	●	12	13.5	15.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = OUT = SNS = DRN = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{GATE}	GATE Clamp to GND	V_{CC} = 30V, SEL = 0V, LTC4381-1/LTC4381-2	●	30	31.5	33	V
		V_{CC} = 60V, SEL = V_{CC}, LTC4381-1/LTC4381-2	●	47.5	50	52.5	V
$I_{GATE(UP)}$	GATE Pull-Up Current	V_{CC} = GATE = OUT = 12V, 24V	●	–8.5	–20	–35	µA
$I_{GATE(DN)}$	GATE Pull-Down Current						
	Overcurrent	ΔV_{SNS} = 200mV, GATE = 12V, OUT = 0V	●	50	100		mA
	Shutdown	ON = 0V, GATE = 20V	●	0.3	5		mA
	Input UV	V_{CC} = 1.5V, GATE = 10V	●	2	5		mA
	Fault Time Out	TMR = 2V, GATE = 10V	●	1.5	3.5		mA
$I_{\overline{FLT}}$	$\overline{FLT}$ Leakage Current	$\overline{FLT}$ = 80V	●			2	µA
$V_{\overline{FLT}(LOW)}$	$\overline{FLT}$ Output Low	I_{SINK} = 0.1mA	●		0.1	0.5	V
		I_{SINK} = 3mA	●		1	4	V
$I_{TMR(DN)}$	TMR Pull-Down Current	TMR = 0.8V	●	1.2	1.6	2.75	µA
$I_{TMR(UP, COOL)}$	TMR Pull-Up Current, Cool Down	TMR = 2V	●	–1	–2	–3	µA
$I_{TMR(OV)}$	TMR Pull-Up Current, Overvoltage	TMR = 0.8V, OUT = 11V, V_{DS} = 1.1V, ΔV_{SNS} = 0mV	●	–0.7	–1.6	–2.4	µA
		OUT = 28V, TMR = 0.8V					
	Small OV, Light Load	I_{DRN} = 0.1mA, ΔV_{SNS} = 10mV	●	–3.5	–6.7	–12	µA
	High OV, Light Load	I_{DRN} = 1mA, ΔV_{SNS} = 10mV	●	–13	–30	–61	µA
	Small OV, Heavy Load	I_{DRN} = 0.1mA, ΔV_{SNS} = 40mV	●	–10	–20	–30	µA
	High OV, Heavy Load	I_{DRN} = 1mA, ΔV_{SNS} = 40mV	●	–60	–120	–180	µA
$I_{TMR(OC)}$	TMR Pull-Up Current, Overcurrent	TMR = 0.8V					
		I_{DRN} = 0mA, OUT = 11V	●	–3	–6	–9	µA
		I_{DRN} = 0mA, OUT = 0V	●	–16	–24	–36	µA
	Small OV, Light Load	I_{DRN} = 0.1mA, OUT = 11V	●	–16	–27	–38	µA
	High OV, Light Load	I_{DRN} = 1mA, OUT = 11V	●	–80	–142	–206	µA
$I_{TMR(SC)}$	Small OV, Heavy Load	I_{DRN} = 0.1mA, OUT = 0V	●	–35	–50	–60	µA
	High OV, Heavy Load	I_{DRN} = 1mA, OUT = 0V	●	–130	–170	–220	µA
V_{TMR}	TMR Gate Off Threshold	TMR Rising	●	1.178	1.215	1.251	V
AC Characteristics							
D	Retry Duty Cycle; Overvoltage, LTC4381-2/LTC4381-4	ΔV_{SNS} = 40mV, I_{DRN} = 5µA, OUT = 28V, V_{CC} = 29V	●		2.8	4.2	%
		ΔV_{SNS} = 40mV, I_{DRN} = 500µA, OUT = 28V, V_{CC} = 80V	●		0.1	0.2	%
	Retry Duty-Cycle; Overcurrent, LTC4381-2/LTC4381-4	I_{DRN} = 500µA					
		OUT = 0V	●		0.1	0.2	%
		OUT = 6V	●		0.35	0.7	%
$t_{ON(ON)}$	Turn-On Propagation Delay	ON Steps from 0V to 1.5V, OUT = SNS = 0V	●		7.5	25	ms
$t_{OFF(ON)}$	Turn-Off Propagation Delay	ON Steps from 1.5V to 0V, OUT = SNS = V_{CC}	●		1	5	µs
$t_{OFF(OC)}$	Overcurrent Turn-Off Propagation Delay	ΔV_{SNS} Steps from 0V to 250mV, OUT = 6V	●		2	4	µs
		ΔV_{SNS} Steps from 0V to 250mV, OUT = 0V	●		2	4	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: Internal clamps limit the DRN pin to a minimum of 10V above the OUT and SNS pins.

Note 4: Internal clamps limit the GATE pin to a minimum of 10V above the OUT pin or V_{CC} pin, or 50V (SEL = V_{CC}) or 31.5V (SEL = GND) above the GND pin (LTC4381-1/LTC4381-2). Driving this pin to voltages beyond the clamp may damage the device.

Note 5: IN ABS MAX is rated at 25°C to 125°C only.

Note 6: Total supply current is the sum of the current into the V_{CC}, OUT, SNS and DRN pins.

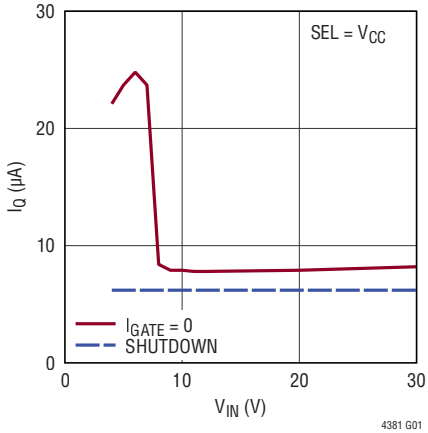
Note 7: The LTC4381 can operate through the cold crank down to 4V in automotive applications, wheres V_{CC} is powered with a 12V supply initially and stays above 8V during the cold crank period.

Note 8: Operating voltage is limited by the maximum GATE voltage of 86V.

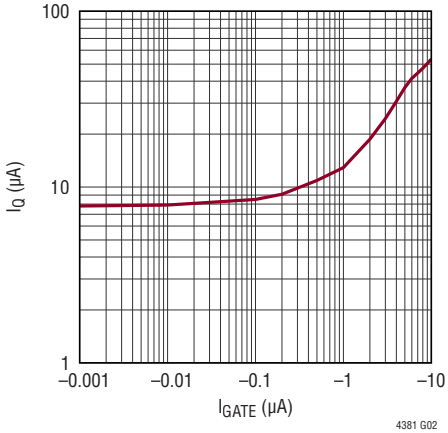
Note 9: Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS V_{CC} = 12V, unless otherwise noted.

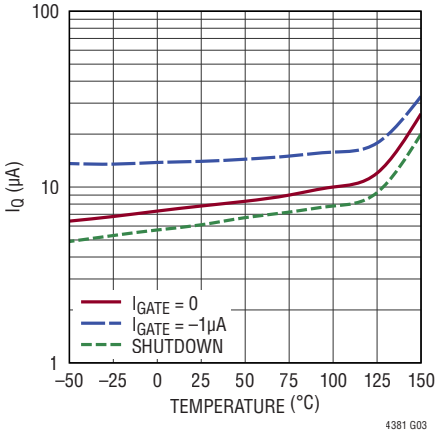
Total Supply Current (I_Q) vs Input Voltage



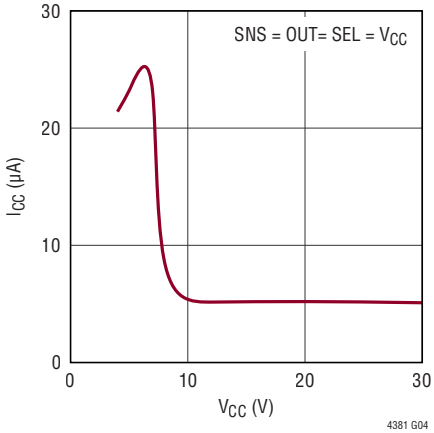
Total Supply Current (I_Q) vs Gate Leakage



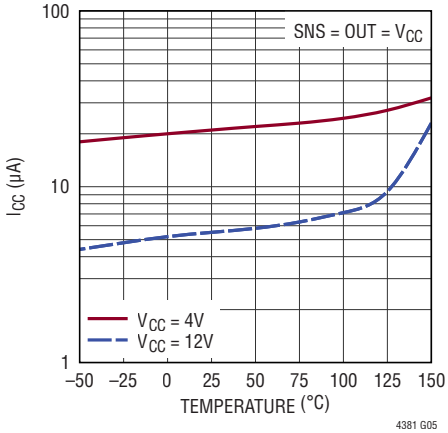
Total Supply Current (I_Q) vs Temperature



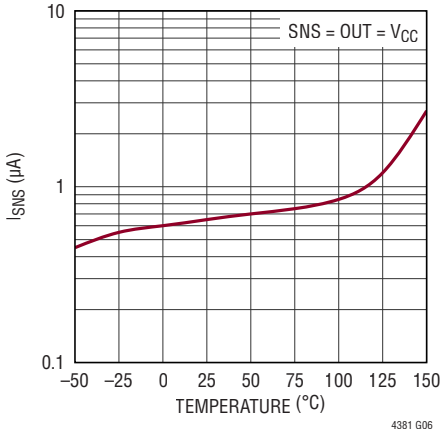
Supply Current (I_{CC}) vs Supply Voltage



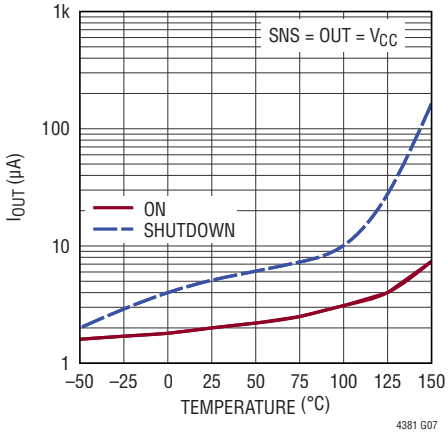
Supply Current (I_{CC}) vs Temperature



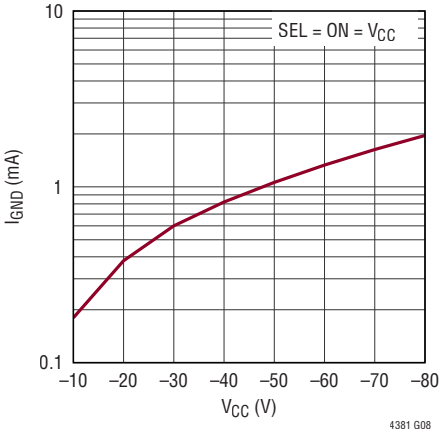
I_{SNS} vs Temperature



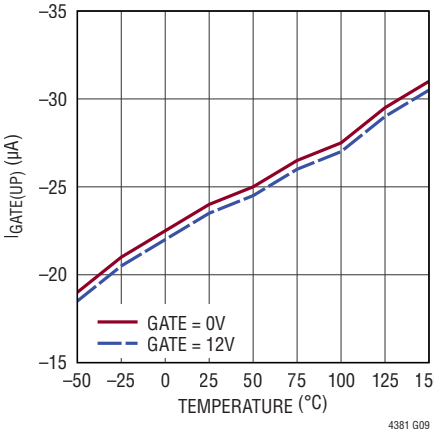
Output Pin Current vs Temperature



Reverse Current vs Reverse Voltage

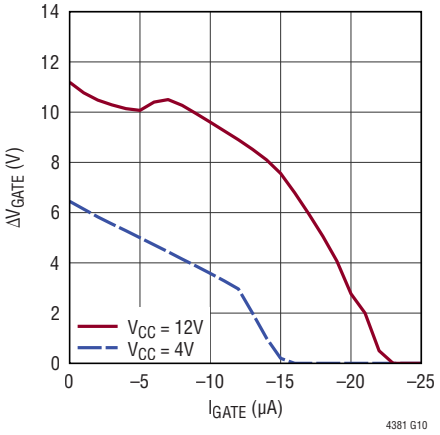


Gate Pull-Up Current vs Temperature

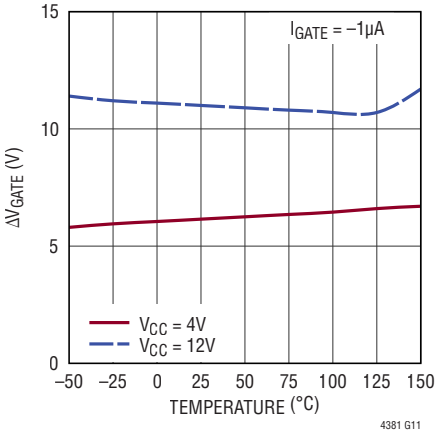


TYPICAL PERFORMANCE CHARACTERISTICS V_{CC} = 12V, unless otherwise noted.

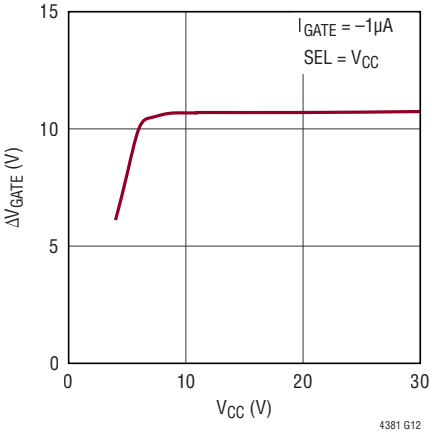
Gate Drive vs Pull-Up Current



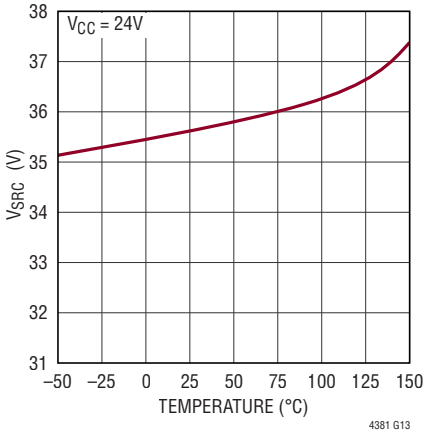
Gate Drive vs Temperature



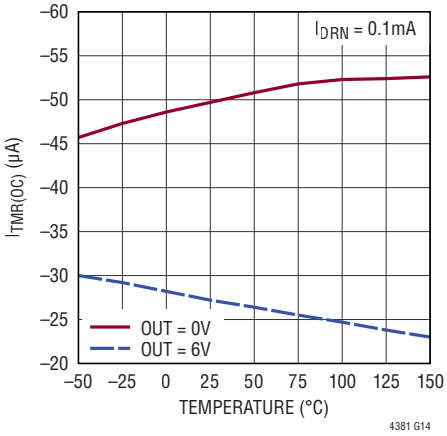
Gate Drive vs Supply Voltage



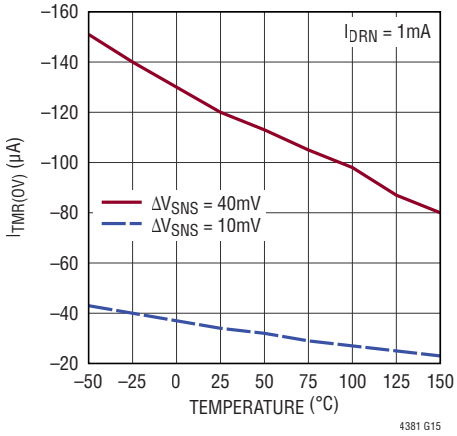
V_{SRC} vs Temperature



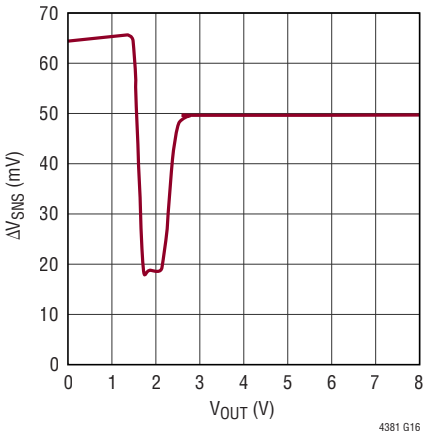
TMR Pin Current vs Temperature, Overcurrent Fault



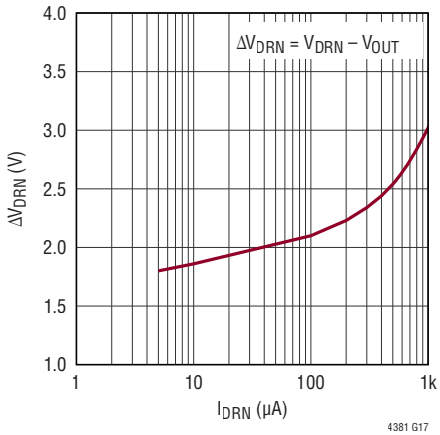
TMR Pin Current vs Temperature, Overvoltage Fault



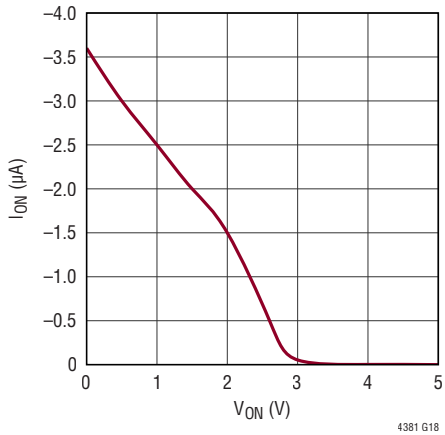
Current Limit vs Output Voltage



DRN Voltage vs Current

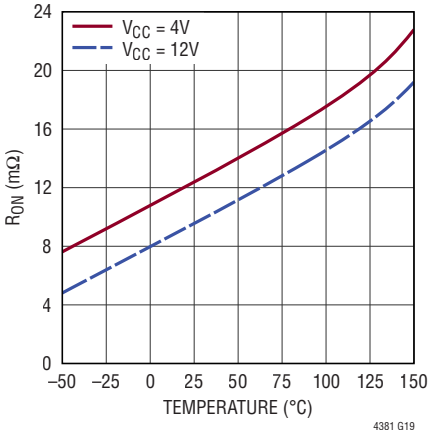


ON Pin Current vs Voltage

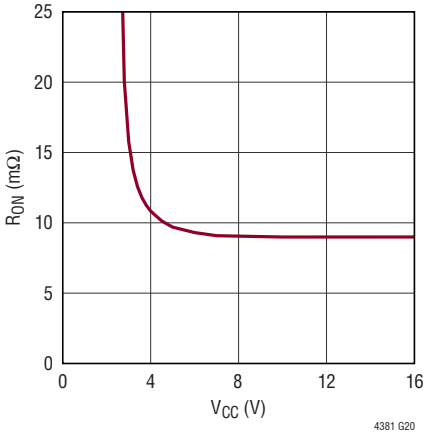


TYPICAL PERFORMANCE CHARACTERISTICS V_{CC} = 12V, unless otherwise noted.

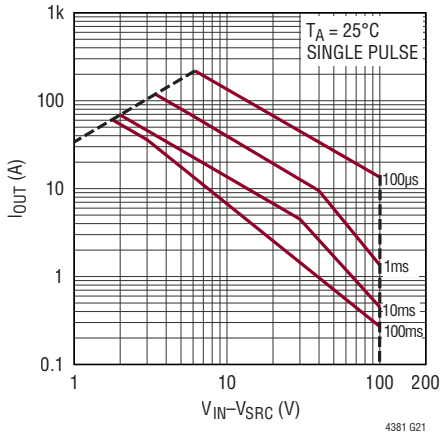
R_{ON} vs Temperature



R_{ON} vs V_{CC}



MOSFET SOA Curve



PIN FUNCTIONS

DRN: MOSFET Drain-Source Sense. The DRN pin voltage tracks the OUT pin. The resulting DRN pin current through external resistor R_{DRN} is proportional to the MOSFET V_{DS}. The DRN pin current and ΔV_{SNS} (SNS – OUT) are multiplied internally to produce a TMR pin current approximately proportional to the MOSFET's power dissipation. This reduces the SOA requirement of the MOSFET by timing out faster during more severe faults. Choose R_{DRN} to limit the current to 1mA at the peak input voltage. Connect to OUT if unused.

$\overline{\text{FLT}}$: Fault Output. This open-drain logic output pin pulls low after the voltage at the TMR pin has reached the fault threshold of 1.215V. It indicates that the MOSFET is off because either the supply voltage has stayed at an elevated level for an extended period of time (voltage fault) or the device is in an overcurrent condition (current fault). The fault output is capable of sinking up to 3mA. Leave open or tie to GND if unused.

GATE: Gate Drive for Internal N-Channel MOSFET. The GATE pin is pulled up by an internal 20µA charge pump that is regulated to 11.5V above the OUT pin. An amplifier controls the GATE pin to limit the current through the MOSFET. A minimum of 47nF of capacitance and 33Ω series resistor at the pin is necessary to compensate the current limit amplifier. To avoid damaging the MOSFET during an output short, GATE is also clamped internally to 17V above OUT.

GFET: Gate of Internal N-Channel MOSFET. Connect this pin to the GATE pin through a 10Ω resistor.

GND: Device Ground.

IN: Input of MOSFET. This is the drain terminal of the internal MOSFET. Connect this pin to the supply input.

ON: Turn-On Control Input. The LTC4381 can be turned on by pulling this pin above 1.05V or by leaving it open to allow an internal 1MΩ resistor to turn the part on. Pulling the pin below the threshold puts the part in shutdown mode and reduces the supply current to 5µA. Limit the ON leakage current to less than 1µA if no external pull-up is used. The ON pin can be pulled up to 80V or below GND by 60V without damage.

OUT: Output Voltage Sense. This pin senses the output voltage at the output terminal of the current sense resistor. An internal clamp limits the voltage in between the GATE and OUT pins to 17V. Bypass the OUT pin with a minimum of 22µF as close to the pin as possible.

SEL: Output Clamp Voltage Select for LTC4381-1 and LTC4381-2. Connect the SEL pin to GND to set the internal output clamp voltage to 28.5V. Connect it to V_{CC} or OUT for a 47V output clamp voltage. The SEL pin can be pulled up to 80V or below GND by 60V without damage. The SEL pin has no effect on the LTC4381-3 and LTC4381-4, it can be tied to GND or V_{CC} or OUT.

SNS: Current Sense Input. Connect to the input terminal of the current sense resistor. The current limit amplifier controls the GATE pin to limit the current sense voltage to 50mV. This voltage increases to 62mV in a severe fault when OUT is below 1.5V. A fixed 6µA is added to the TMR pin current during an overcurrent condition to shorten the turn-off time. In a severe short condition when the output voltage is below 1.5V, the extra current increases to 24µA to reduce the power dissipation in the MOSFET. ΔV_{SNS} (SNS – OUT) must be limited to less than ±5V. Connect to OUT if unused.

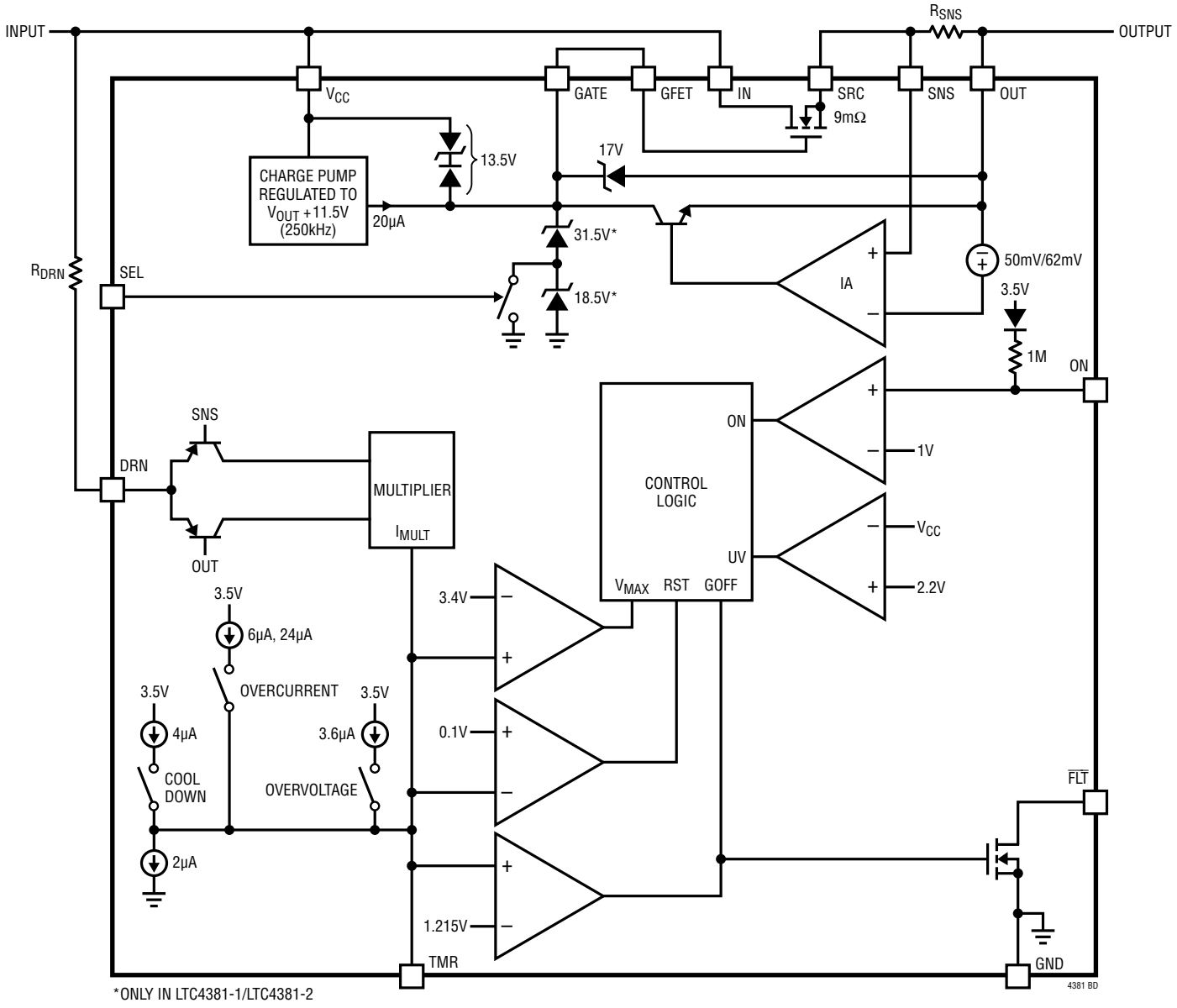
PIN FUNCTIONS

SRC: Output of MOSFET. This is the source terminal of the internal MOSFET, connect this pin to the sense resistor. The SRC pin and output is indirectly clamped through GATE pin during an overvoltage event. The LTC4381-1/ LTC4381-2 SRC pin is clamped at 28.5V above GND with SEL = 0 V, or 47V above GND when SEL = V_{CC}. It is also clamped at 10.5V above V_{CC} if the V_{CC} voltage is low. The LTC4381-3/LTC4381-4 SRC pin does not have the 28.5V/47V clamp to GND, it is only clamped at 10.5V above V_{CC}.

TMR: Fault Timer Input. Connect a capacitor between this pin and ground to set the fault turn-off time and cool down period. The charging current during fault conditions varies depending on the power dissipation of the MOSFET. When TMR reaches 1.215V, the MOSFET turns off and $\overline{FLT}$ pulls low. Upon gate off, the part immediately enters a cool down period with a 2µA current pull up and pull down on the TMR pin. After the cool down period has concluded, the LTC4381-2 and LTC4381-4 immediately restart, while the LTC4381-1and LTC4381-3 remain off until the ON pin is pulled low momentarily for more than 100µs or power is cycled. A 10V rated X7R capacitor is recommended for C_{TMR}.

V_{CC}: Positive Supply Voltage Input. The positive supply input ranges from 4V to 80V. For applications where the input voltage is expected to exceed 80V, the V_{CC} pin may be protected by a Zener diode clamp or, in the case of short duration spikes, by a simple RC filter. Clamping the V_{CC} pin with a Zener diode can also be used as a means of adjusting the output clamp voltage to a value less than the internal 28.5V/47V clamps for the LTC4381-1/LTC4381-2. For the adjustable versions, LTC4381-3/LTC4381-4, which have no internal clamp, a Zener diode at the V_{CC} pin is the only way to limit the voltage at the output. The V_{CC} pin can also be powered separately from the V_{IN} pin.

BLOCK DIAGRAM



OPERATION

The LTC4381 is a low quiescent current eFuse that drives an internal 9mΩ N-channel MOSFET as the pass device. In normal operation, a 20µA charge pump (see Block Diagram) drives MOSFET M1 fully on, providing a low impedance path from input to the load. The MOSFET gate is clamped to ground by a Zener stack. If the input voltage rises to the point where the output approaches the gate clamp, the output is effectively limited to one threshold voltage (typically 3V) below the gate clamp and the input surge is blocked from reaching the load.

For the LTC4381-1 and LTC4381-2 versions, two output clamping voltages to ground are available: 28.5V for use in 12V systems, and 47V for use in 24V and 28V systems. The clamping voltage is selectable using the SEL pin. Besides the output to ground clamp, the output is also limited to 10.5V above the V_{CC} pin.

There is no GATE clamp to ground for the LTC4381-3 and LTC4381-4 versions and the output is only limited to 10.5V above the voltage at the V_{CC} pin. A Zener diode clamp connected from the V_{CC} pin to ground thus clamps the voltages at both the V_{CC} and SRC pins during overvoltage events.

Load current is limited by a current limit amplifier (IA), using a sense resistor in series with the MOSFET source to monitor the current. The current limit threshold is 50mV, rising to 62mV when the output is less than 1.5V.

MOSFET stress is monitored by a timer, whose current is a function of MOSFET's V_{DS} as well as I_D. V_{DS} is monitored by R_{DRN} at the DRN pin, while I_D is monitored by sensing the voltage drop across R_{SNS}. The timer allows the load to continue functioning during short transient events while protecting the MOSFET from being damaged by a sustained overvoltage, such as load dump in vehicles, or an output overload or short circuit.

A multiplier sets the timer period depending on the power dissipation in the MOSFET. Higher power dissipation corresponds to a shorter timer period, helping to keep the MOSFET within its safe operating area (SOA).

The timer responds to stresses at start-up and during voltage and current limiting. TMR pin current is integrated on timing capacitor C_{TMR} and if TMR charges to 1.215V, the MOSFET is turned off. At this point, the LTC4381-1 and LTC4381-3 latch off, and can be reset by cycling power or by pulling the ON pin low for at least 100µs. For the LTC4381-2 and LTC4381-4, the TMR pin enters a cool down phase, allowing time for the MOSFET temperature to equalize with its surroundings before automatically restarting. The TMR pin slowly charges up and down in between 3.4V and 1.215V for 15 times and discharges to ground at the last cycle. When the TMR pin has reached the 100mV threshold, the MOSFET is turned back on. The cool down interval can be curtailed by pulling the ON pin low for at least 10ms/µF of C_{TMR}.

In addition to resetting the timer, the ON pin is used for on/off control and for undervoltage detection. The ON pin threshold is 1.05V.

The open drain $\overline{FLT}$ pin pulls low whenever the timer is faulted off and goes high again when reset by a power cycle, by pulling the ON pin low for at least 100µs or in the case of the LTC4381-2 and LTC4381-4, when the TMR pin discharges to 100mV.

Table 1. LTC4381 Options

PART NUMBER	OUTPUT CLAMP	FAULT BEHAVIOR
LTC4381-1	Internal 28.5V/47V to GND	Latchoff
LTC4381-2	Internal 28.5V/47V to GND	Auto Retry
LTC4381-3	Externally Adjustable	Latchoff
LTC4381-4	Externally Adjustable	Auto Retry

APPLICATIONS INFORMATION

The LTC4381 limits the voltage and current delivered to the load during supply transient or output overload events. The N-channel MOSFET provides a low resistance path from the input to the load during normal operation. In overvoltage conditions it limits the output to a threshold voltage below the clamped gate voltage. The total fault timer period is set to ride through short-duration faults, while longer events cause the output to shut off and protect the MOSFET from damage.

Start-Up

Figure 1 shows a 12V, 1A application which limits the output to approximately 28.5V. When power is first applied with $V_{CC} \geq 4V$ and $ON \geq 1.05V$, there is a delay of about 10ms before the GATE pin begins charging C2 and MOSFET's gate terminal with a fixed 20µA current source. The internal MOSFET operates as a source follower, ramping the output up at a rate of $I_{GATE(UP)}/C2$. Inrush current in the load capacitance C_{OUT} is given by Equation 1.

$$I_{INRUSH} = I_{GATE(UP)} \bullet \frac{C_{OUT}}{C2} \quad (1)$$

where $I_{GATE(UP)}$ is typically 20µA.

Eventually, the GATE pin charges to the point where $V_{IN} \approx V_{OUT}$ and stops only when ΔV_{GATE} ($V_{GATE} - V_{OUT}$) reaches its regulation point of 11.5V, fully enhancing the MOSFET.

Overcurrent Fault Protection

The LTC4381 features an adjustable current limit that protects against short circuits and excessive load current. During an overcurrent event, the GATE pin is regulated to limit the current sense voltage across the SNS and OUT pins (ΔV_{SNS}) to 50mV when OUT is above 3V. In the case of a severe short at the output, where OUT is less than 1.5V, the current sense voltage is 62mV. Output current is thereby limited to $\Delta V_{SNS}/R_{SNS}$. Current limit may control the startup ramp rate in extreme cases, such as if C_{OUT} is unusually large or if current limit is set to an unusually low value, and artificially reduces C_{OUT}'s inrush current below the value previously calculated.

Overvoltage Fault Protection

The LTC4381 limits the voltage at the output during an overvoltage at the input. For the LTC4381-1/LTC4381-2 illustrated in Figure 1, an internal clamp limits the output to either 28.5V or 47V, depending on the state of the SEL pin. With the SEL pin grounded as shown, the output is clamped at 28.5V. Tying the SEL pin high causes the output to clamp at 47V.

The GATE pin may also be limited by the compliance of the internal 20µA current source, to V_{CC} + 13.5V. In the LTC4381-3/LTC4381-4 the GATE pin clamp is entirely disconnected, leaving only the V_{CC} + 13.5V compliance limit. This arrangement allows the output to be effectively clamped at any voltage from 14.5V to 72V, by clamping V_{CC} to between 4V and 61.5V.

V_{CC} Pin

The LTC4381 can withstand an input surge voltage of up to 100V. If the maximum expected surge voltage is less than 80V, the V_{CC} pin can be connected directly to the input supply. If the surge voltage is between 80V to 100V, the V_{CC} pin must be protected by filtering or clamping since its operating range is from 4V to 80V for LTC4381-1/LTC4381-2 and 4V to 72V for LTC4381-3/LTC4381-4. For short duration spikes and transients exceeding 80V, filtering is the most sensible means of protecting the V_{CC} pin. R1 and C1 provide filtering in Figure 1. Owing to the LTC4381's low I_{CC}, values up to 100k may be used for R1 without seriously impairing the lower end of the operating voltage range. For long duration surges such as automotive load dump, C1 becomes prohibitively large and Zener D1 is the most effective means of limiting the V_{CC} voltage. Using a 68V Zener assures that D1 will not override the internal GATE pin clamp in the LTC4381-1 and LTC4381-2 devices. For the LTC4381-3 and LTC4381-4, the V_{CC} operating range extends from 4V to 72V. Since the SRC pin is regulated to V_{CC} + 10.5V, D1 is chosen to achieve the desired output clamping effect while at the same time keeping the V_{CC} pin within its 4V to 72V range. The LTC4381 can operate through the cold crank down to 4V in automotive applications, wheres V_{CC} is powered with a 12V supply initially and stays above 8V during the cold crank period.

APPLICATIONS INFORMATION

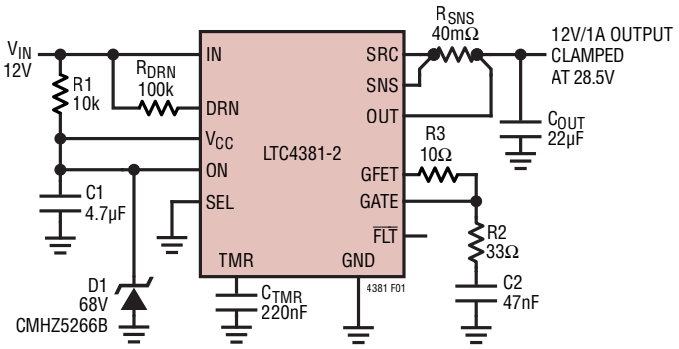


Figure 1. 12V/1A, Output Limited to 28.5V

Fault Timer Overview

Overvoltage and overcurrent conditions, and high V_{DS} conditions in MOSFET are limited in duration by an adjustable fault timer. A capacitor at the TMR pin (C_{TMR}) sets the delay time before a fault condition is reported at the $\overline{FLT}$ pin and MOSFET is turned off. C_{TMR} also sets the cool down time before MOSFET is permitted to turn back on for the LTC4381-2 and LTC4381-4 auto retry versions. The LTC4381-1 and LTC4381-3 versions simply latch off at the end of the timer delay. A 10V or higher rated X7R capacitor is recommended for C_{TMR} to minimize temperature and voltage sensitivity.

Fault timing starts as soon as the input power is applied with the part in the on condition, or when the part turns on after application of power. A 1.5µA current is generated to pull up the TMR pin when the voltage across the MOSFET is higher than 0.7V. The timer speeds up with an additional current that varies with the power dissipated in the MOSFET. The power dissipation is the product of the voltage across the MOSFET (V_{DS}) and the current flowing through it (I_D). V_{DS} is inferred from the voltage drop across the drain pin resistor, R_{DRN}, while ΔV_{SNS} represents I_D.

At initial power-up, the 1.5µA pilot current charges the TMR pin capacitor because the input supply is, at least for a short time, more than 0.7V above the output voltage. When the output rises to within 0.7V of the input supply voltage, the pull-up current disappears and an internal 2µA current source discharges the TMR pin capacitor. The capacitor must be sized to ride through the initial start-up interval for successful power-up.

In the presence of a sustained fault, the timer current charges the TMR pin to 1.215V. At this point, the $\overline{FLT}$ pin pulls low to indicate a fault condition and the GATE pin pulls low, shutting off the MOSFET. After faulting off, the timer enters the cool down phase. At the end of the cool down period, the LTC4381-1/LTC4381-3 remain off until manually reset, while the LTC4381-2/LTC4381-4 automatically restart.

Fault Timer Operation in Overvoltage or Large V_{DS}

During start-up or an overvoltage condition, where the MOSFET's V_{DS} exceeds 0.7V, the TMR pin charges from 0V to 1.215V with a current that varies principally as a function of V_{DS} and I_D. V_{DS} is inferred from the current flowing in the DRN pin resistor, R_{DRN}, while the voltage difference between the SNS and OUT pins (ΔV_{SNS}) represents the MOSFET current, I_D.

The TMR pin current is given by Equation 2.

$$I_{TMR(OV)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet \Delta V_{SNS} \bullet \sqrt{I_{DRN} - 70\mu A}\right) \quad (2)$$

where $0.0917\sqrt{A}/V$ is the gain term of the multiplier. If I_{DRN} is less than 70µA (for example during start-up), use I_{TMR} of 1.5µA.

Substituting for ΔV_{SNS} and I_{DRN} is given by Equation 3.

$$I_{TMR(OV)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet R_{SNS} \bullet \sqrt{\frac{V_{DS}}{R_{DRN}} - 70\mu A}\right) \quad (3)$$

If I_{DRN} is less than 70µA (for example during start-up), use I_{TMR} of 1.5µA.

When TMR reaches 1.215V, the $\overline{FLT}$ pin pulls low and the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of output clamping and turning off is given by Equation 4.

$$t_{TMR} = V_{TMR} \bullet \frac{C_{TMR}}{I_{TMR}} \quad (4)$$

Because I_{TMR} is a function of V_{DS} and I_D, the exact time spent in overvoltage before turning off depends upon the input waveform and the load current.

APPLICATIONS INFORMATION

Fault Timer Operation in Overcurrent

TMR pin behavior in overcurrent is substantially the same as in overvoltage. In the presence of an overcurrent condition when the LTC4381 regulates the output current, the TMR pin charges from 0V to 1.215V with a current that varies principally as a function of the power dissipated in the MOSFET. In addition to the variable current, an additional 24µA hastens timeout in a low impedance short where the output is less than 1.5V. This additional current is reduced to 6µA when V_{OUT} is above 3V.

The TMR pin current with V_{OUT} less than 1.5V is given by Equation 5.

$$I_{TMR(SC)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet R_{SNS} \bullet \sqrt{\frac{V_{DS}}{R_{DRN}} - 70\mu A}\right) \quad (5)$$
$$24\mu A$$

where 24µA is the extra TMR current during V_{OUT} short circuit condition. If I_{DRN} is less than 70µA, use I_{TMR} of 24µA.

And with V_{OUT} above 3V given by Equation 6.

$$I_{TMR(OC)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet R_{SNS} \bullet \sqrt{\frac{V_{DS}}{R_{DRN}} - 70\mu A}\right) \quad (6)$$
$$6\mu A$$

where 6µA is the extra TMR current during overcurrent condition. If I_{DRN} is less than 70µA, use I_{TMR} of 6µA.

When TMR reaches 1.215V, the $\overline{FLT}$ pin pulls low and the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of output clamping and turning off is given by Equation 7.

$$t_{TMR} = V_{TMR} \bullet \frac{C_{TMR}}{I_{TMR}} \quad (7)$$

Because I_{TMR} is a function of V_{DS} and I_D, the exact time spent in overcurrent before turning off depends upon the input waveform, the output voltage and the time required for the output current to come into regulation.

Cool Down Phase

Cool down behavior is the same whether initiated by overvoltage or overcurrent. During the cool down phase, the timer continues to charge from 1.215V to 3.4V with 2µA, and then discharge back down to 1.215V with 2µA. This cycle repeats 14 times and at the 15th cycle the TMR pin is pulled all the way to ground. The total cool down time is given by Equation 8.

$$t_{COOL} = C_{TMR} \bullet \frac{15 \bullet 4.37V + (1.215V - 0.1V)}{2\mu A} = C_{TMR} \bullet 33.3\left[\frac{s}{\mu F}\right] \quad (8)$$

where C_{TMR} is in µF.

Up to this point the operation of the LTC4381-1/LTC4381-3 and LTC4381-2/LTC4381-4 is the same. Behavior at the end of the cool down phase is entirely different.

At the end of the cool down phase, when TMR crosses the 100mV reset threshold, the LTC4381-1/LTC4381-3 remain latched off and $\overline{FLT}$ remains low. They may be restarted by pulling the ON pin low for at least 100µs or by cycling the power supply. The cool down phase may be interrupted at anytime by pulling the ON pin low for at least 10ms/µF of C_{TMR}; the LTC4381-1/LTC4381-3 will restart when ON goes high. The LTC4381-2/LTC4381-4 will automatically retry at the end of the cool down phase without cycling the ON pin and the cool down phase may be interrupted by pulling the ON pin low for at least 10ms/µF of C_{TMR}.

For both versions, the $\overline{FLT}$ pin goes high in shutdown and is cleared high when power is first applied to V_{CC}. If $\overline{FLT}$ is set low, it can be reset during the cool down phase by pulling the ON pin low for at least 10ms/µF of C_{TMR}.

Supply Transient Protection

During a short-circuit condition, the large change in current flowing through power supply traces and associated wiring can cause large inductive voltage transients. If this voltage transient is higher than the junction breakdown voltage of the LTC4381 internal MOSFET, the junction conducts and absorb this avalanche current. No TVS is required at the IN pin. On the other hand, the V_{CC} pin is guaranteed to be safe from damage up to 80V only. The V_{CC} pin cannot be tied directly to the IN pin if Avalanche breakdown is expected. An RC filter at the V_{CC} pin is an effective measure against this voltage spike.

APPLICATIONS INFORMATION

Another way to limit transients to less than 80V at the V_{CC} pin is to use a small Zener diode and a resistor, D1 and R1 in Figure 1. The Zener diode limits the voltage at the pin while the resistor limits the current through the diode to a safe level during the surge. However, D1 can be omitted if the filtered voltage at the V_{CC} pin, due to R1 and C1, stays below 80V. The inclusion of R1 in series with the V_{CC} pin modestly increases the minimum required voltage at V_{IN} due to the extra voltage drop across it from the small V_{CC} current of the LTC4381 and the leakage current of D1.

A total bulk capacitance of at least 22µF low ESR electrolytic or ceramic is required close to the OUT pin.

Transient Stress in the MOSFET

During an overvoltage event, the LTC4381 clamps the gate of the pass MOSFET to limit the output voltage at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. MOSFET dissipation or stress is a function of the input voltage waveform, output voltage and load current.

Most transient event specifications use the prototypical waveshape shown in Figure 2, comprising a linear ramp of rise time t_r, reaching a peak voltage of V_{PK} and exponentially decaying back to V_{IN} with a time constant of τ. A common automotive transient specification has constants of t_r = 10µs, V_{PK} = 80V and τ = 1ms. A surge condition known as load dump commonly has constants of t_r = 5ms, V_{PK} = 60V and τ = 200ms.

MOSFET stress is the result of power dissipated within the device. For long duration surges of 100ms or more, stress is increasingly dominated by heat transfer out of the package; this is a matter of device packaging and mounting and heat sink thermal mass. This is best analyzed by simulation using the MOSFET thermal model.

For short duration transients of less than 100ms, MOSFET survival is a matter of safe operating area (SOA), an intrinsic property of the MOSFET. SOA quantifies the time required at any given condition of V_{DS} and I_D to raise the junction temperature of the MOSFET to its rated maximum. MOSFET SOA can be expressed in units of watt-root-seconds ($P\sqrt{t}$), which is essentially constant for intervals of less than 100ms for any given device type and rises to infinity under DC operating conditions. Destruction mechanisms other than bulk die temperature distort the lines of an accurately drawn SOA graph so that $P\sqrt{t}$ is not the same for all combinations of I_D and V_{DS}. In particular $P\sqrt{t}$ tends to degrade as V_{DS} approaches the maximum rating, rendering some devices useless for absorbing energy above a certain voltage. The LTC4381 internal MOSFET has a guaranteed SOA of 20ms at 70V and 1A, which gives a $P\sqrt{t}$ of $10W\sqrt{s}$. To survive a longer overvoltage transient, reduce the load current according to this $P\sqrt{t}$ spec.

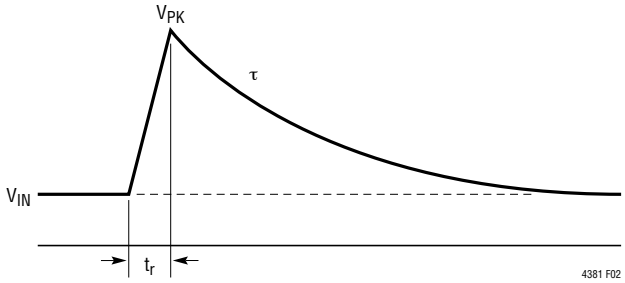


Figure 2. Prototypical Transient Waveform

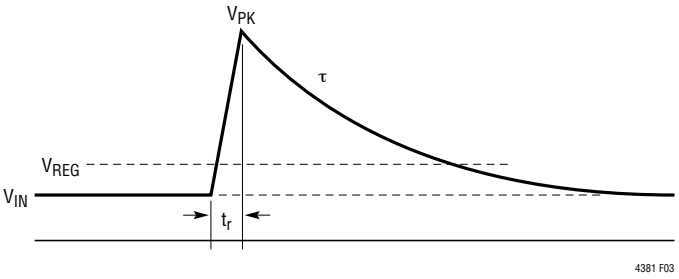


Figure 3. Safe Operating Area Required to Survive Prototypical Transient Waveform

Calculating Transient Stress

$P\sqrt{t}$ for a prototypical transient waveform is calculated using Equation 9 and Figure 3.

Let

$a = V_{REG} - V_{IN}$

$b = V_{PK} - V_{IN}$

(V_{IN} = Nominal Input Voltage)

APPLICATIONS INFORMATION

Then

$$P\sqrt{t} = I_{LOAD} \bullet \sqrt{\left[\frac{1}{3}t_r\frac{(b-a)^3}{b} + \frac{1}{2}\tau\left(2a^2\ln\frac{b}{a} + 3a^2 + b^2 - 4ab\right)\right]} \quad (9)$$

For the transient conditions of V_{PK} = 100V, V_{IN} = 12V, V_{REG} = 28.5V, t_r = 10µs, τ = 1ms, and a load current of 1A, $P\sqrt{t}$ is 1.4W$\sqrt{s}$ which can be handled by the MOSFET. The $P\sqrt{t}$ of other transient waveshapes is evaluated by integrating the MOSFET power over root of time. LTspice® can be used to simulate timer behavior for more complex transients and cases where overvoltage and overcurrent faults coexist, as well as the peak temperature rise of the MOSFET.

Calculating Short-Circuit Stress

SOA stress must also be calculated for a short-circuit condition. Short-circuit $P\sqrt{t}$ is given by Equation 10.

$$P\sqrt{t} = \left(\Delta V_{DS} \bullet \frac{\Delta V_{SNS}}{R_{SNS}}\right) \bullet \sqrt{t_{TMR}} \quad (10)$$

where ΔV_{DS} is the voltage across the MOSFET, ΔV_{SNS} is the current limit threshold and t_{TMR} is the overcurrent timer interval, given by Equation 5 and Equation 6.

For V_{IN} = 15V, ΔV_{DS} = 12V (V_{OUT} = 3V), ΔV_{SNS} = 50mV, R_{SNS} = 12mΩ, R_{DRN} = 100kΩ and C_{TMR} = 68nF, $P\sqrt{t}$ is 2.32W$\sqrt{s}$ – somewhat higher than the transient SOA calculated in the previous example.

$$I_{TMR(OC)} = \left[0.0917 \bullet (50mV) \bullet \sqrt{\frac{12V}{100k} - 70 \bullet 10^{-6}}\right] + 6 \bullet 10^{-6} \quad (10a)$$

$$I_{TMR(OC)} = 38.4\mu A$$

$$t_{TMR} = \frac{(68nF \bullet 1.215V)}{38.4\mu A} \quad (10b)$$

$$t_{TMR} = 2.15ms$$

$$P\sqrt{t} = (15V - 3V) \bullet \frac{50mV}{12m} \bullet \sqrt{2.15ms} = 2.32W\sqrt{s} \quad (10c)$$

Limiting Inrush Current and GATE Pin Compensation

The LTC4381 limits the inrush current to any load capacitance by controlling the GATE pin voltage slew rate. Connect an external capacitor, C2, from GATE to ground to reduce the inrush current at the expense of slower turn-off time. The gate capacitor is set using Equation 11.

$$C2 = I_{GATE(UP)} \bullet \frac{C_{OUT}}{I_{INRUSH}} \quad (11)$$

The LTC4381 needs a minimum of 47nF capacitance (C2) and a 33Ω (R2) resistor in series at the GATE pin to stabilize the current limit amplifier during an overcurrent event. C2 also limits self enhancement of the MOSFET. A 10Ω resistor, R3, is connected to the gate of the MOSFET to suppress parasitic oscillations.

Automobile Cold Crank Ride Through

During cold crank, the battery potential drops from the 12V nominal to as low as 3V for up to 40ms. The LTC4381 needs at least 8V at the V_{CC} pin to function normally. The part can operate at 4V if the load current is low. At V_{CC} = 4V, the R_{ON} of the internal MOSFET is high and this may heat up the MOSFET at high load current. The low quiescent current requirement of the part allows an RC filter with reasonable values to be placed at the V_{CC} pin to ride through cold crank as shown in Figure 4.

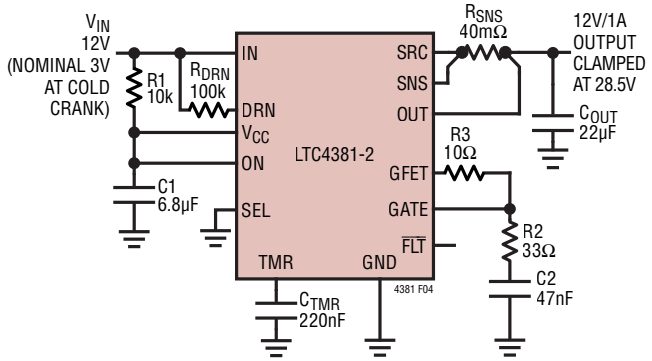


Figure 4. Automotive Cold Crank Ride Through

Ignoring the supply current (I_{CC}), the V_{CC} potential at the end of cold crank is given by Equation 12.

$$V_{CC} = (V_{IN(NOM)} - V_{IN(LOW)}) \bullet e^{\frac{-t}{R1 \bullet C1}} + V_{IN(LOW)} \quad (12)$$

APPLICATIONS INFORMATION

where $V_{IN(NOM)}$ is the input voltage before the cold crank starts, $V_{IN(LOW)}$ is the lowest input voltage during cold crank, and t is the duration of the cold crank.

With the combination of R1 (10kΩ) and C1 (6.8µF), V_{CC} drops to 8V after the input voltage drops from 12V to 3V for 40ms. During this time GATE stays high, keeping the MOSFET on to continue providing current to the output.

Shutdown

The LTC4381 can be shut down to a lower current mode by pulling the ON pin below the shutdown threshold of 1.05V. The quiescent current drops down to 5µA. An external Zener diode from the input supply to the ON pin can be used to implement undervoltage lockout, as illustrated in Figure 7. The UV threshold is the Zener voltage plus 1.05V.

The ON pin can be pulled up to 80V or below GND by up to 60V without damage. Leaving the pin open allows an internal resistor to pull it up and turn on the part. The leakage current at the pin should be limited to no more than 1µA if no pull-up device is used to help turn on the part.

Layout Considerations

To achieve accurate current sensing, use Kelvin connections to the current sense resistor (R_{SNS} in Figure 5). The minimum trace width for 1oz copper foil is 0.02" per amp to ensure the trace stays at a reasonable temperature. 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/square. Small resistances can cause large errors in high current applications. During an overvoltage event, the LTC4381 clamps the gate of the pass MOSFET to limit the output voltage at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. The power dissipated in the MOSFET could be as high as 140W. To remove this heat, solder the IN exposed pad to a copper trace that contains vias underneath the pad. The SRC pins also conduct substantial heat from the MOSFET. Connect all the SRC pins to a plane of 1oz or 2oz copper.

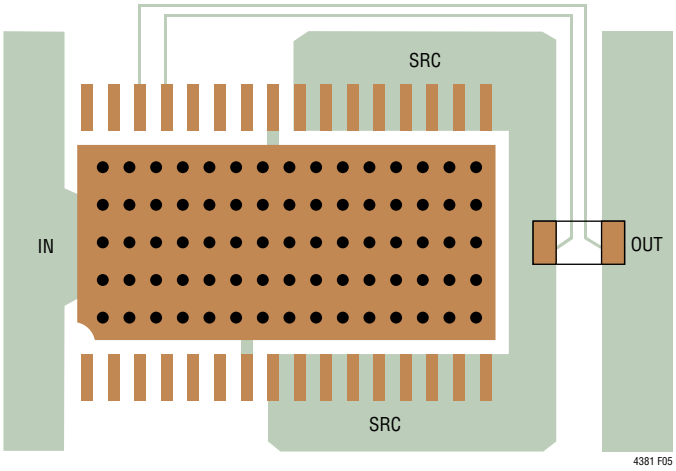


Figure 5. Recommended PCB Layout

Design Example 1

As a design example, take an application with the following specifications: V_{IN} = 10V to 14VDC with a transient of 100V and duration of 2ms, $V_{OUT} \leq$ 20V and cold crank to 3V for 40ms. Maximum load of 1A.

To clamp V_{OUT} to less than 20V, the required V_{CC} clamp is given by Equation 13.

$$V_{CC}\ (\text{Clamp}) = V_{OUT} - 10.5V = 20V - 10.5V = 9.5V \quad (13)$$

The selection of a 8.2V Zener diode for D1 limits the voltage at the V_{OUT} to less than 20V during a 100V surge. The minimum required voltage at the V_{CC} pin is 8V when V_{IN} is at 10V; the V_{CC} pin input current is less than 30µA. The maximum value for R1 to ensure proper operation is given by Equation 14.

$$R1 = \frac{\text{Min } V_{IN} - \text{Min } V_{CC}}{\text{Supply Current}} = \frac{10V - 8V}{30\mu A} = 66.7k \quad (14)$$

We used R1 of 68.1k.

The maximum current through R1 into D1 during transients is then calculated using Equation 15.

$$I_{D1} = \frac{100V - 8.2V}{68.1k\Omega} = 1.35mA \quad (15)$$

APPLICATIONS INFORMATION

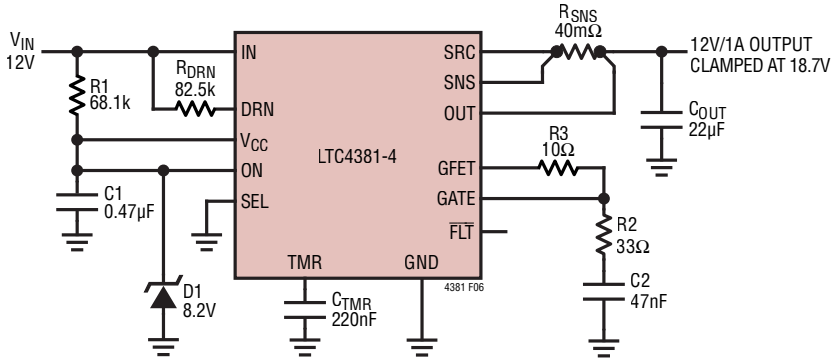


Figure 6. Design Example 1: 12V/1A Application Survives 100V, 2ms OV Transient

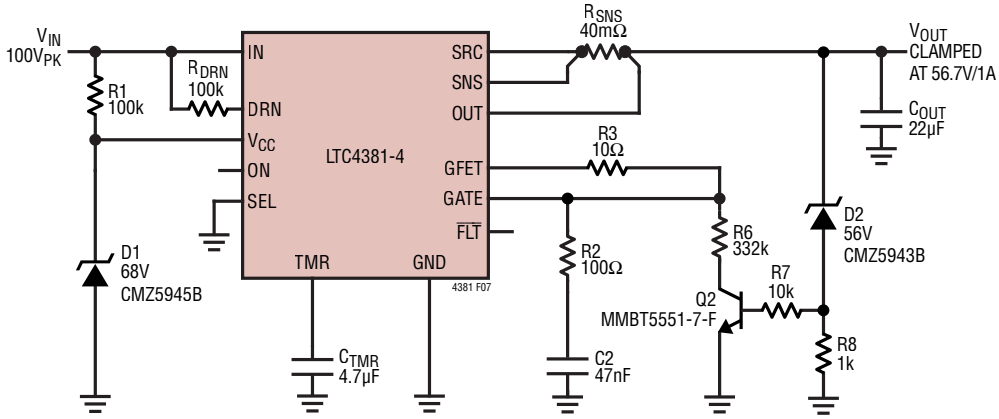


Figure 7. Surge Stopper with Output Clamped Below 60V with 100V/1A/400ms Overvoltage Protection

CMHZ5237B can handle 500mW indefinitely and 1W for 1 second. Maintaining a V_{CC} of 8V during cold crank will require a very large C1 since D1 clamps voltage across C1 at 8.2V when V_{CC}=12V. We therefore use V_{CC} of > 4V during cold crank to calculate C1. The load current should remain low during cold crank to avoid heating up the internal MOSFET. The V_{CC} pin needs at least 4V to operate through cold crank from 12V down to 3V for 40ms. The value of C1 can be calculated by Equation 16.

$$V_{CC} = \left[V_{IN(NOM)} - V_{IN(LOW)}\right] \bullet e^{\frac{-t}{R1 \bullet C1}} + V_{IN(LOW)}$$

$$4V = \left[8.2V - 3V\right] \bullet e^{\frac{-40ms}{68.1k \bullet C1}} + 3V \qquad (16)$$

$$C1 = -40ms/\left(68.1k \bullet \ln\left[\frac{(4V - 3V)}{(8.2V - 3V)}\right]\right) = 0.357\mu F$$

0.47µF is chosen to accommodate for the supply current of the part and other conditions. With C1 = 0.47µF and R1 = 68.1kΩ, high voltage transients up to 100V with a pulse width of less than 2ms are filtered out at the V_{CC} pin. Longer surges are suppressed by D1.

R_{DRN} is chosen to produce a current into the DRN pin of 1mA, during the maximum overvoltage transient event (Equation 17). V_{OUT} is clamped to 8.2V + 10.5V or 18.7V.

$$R_{DRN} = \frac{100V - 18.7V}{1mA} = 81.3k\Omega \qquad (17)$$

82.5kΩ is chosen as the next bigger value. The GATE pin pull-up current is 20µA typically, it takes a while to pull the GATE pin high during input transient. So the MOSFET sees a larger V_{DS} initially and the worst case $P\sqrt{t}$ occur when V_{IN} is minimum and load current is at its maximum when the input transient occur (Equation 18).

APPLICATIONS INFORMATION

$$P\sqrt{t} = I_{LOAD} \bullet V_{DS} \bullet \sqrt{t}$$
$$P\sqrt{t} = (1A) \bullet (100V - 10V) \bullet \sqrt{2ms} \quad (18)$$
$$P\sqrt{t} = 4.02W\sqrt{s}$$

Next calculate the sense resistor (R_{SNS}) value with a current limit of greater than 1A with 10% tolerance (Equation 19).

$$R_{SNS} = \frac{45mV}{1.1 \bullet 1A} = 40.9m\Omega \quad (19)$$

We will use 40mΩ, which gives a current limit of 1.25A. Next we select C_{TMR} to shut off the MOSFET if the 100V transient is longer than 2ms at maximum load of 1A (Equation 20).

$$I_{TMR(OV)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet R_{SNS} \bullet \sqrt{\frac{V_{DS}}{R_{DRN}} - 70[\mu A]}\right)$$
$$I_{TMR(OV)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet 1A \bullet 0.04\Omega \bullet \sqrt{\frac{100V - 10V}{82.5k} - 70[\mu A]}\right) \quad (20)$$
$$= 117.2\mu A$$

Next the value is calculated using Equation 21 to achieve a fault time of greater than 2ms:

$$C_{TMR} = I_{TMR(OV)} \bullet \frac{t_{TMR}}{V_{TMR}} \quad (21)$$
$$C_{TMR} = 0.193\mu F$$

So we choose a C_{TMR} = of 0.22µF. Next, we need to make sure that the chosen C_{TMR} allow enough time to power up the output (Equation 22).

$$C_{TMR} = \frac{I_{TMR(UP)} \bullet t_{INRUSH}}{V_{TMR}} \quad (22)$$

where (Equation 23).

$$t_{INRUSH} = \frac{V_{IN} \bullet C_{OUT}}{I_{INRUSH}} = \frac{V_{IN} \bullet C_2}{I_{GATE(UP)}} = \frac{14V \bullet 47nF}{20\mu A} = 32.9ms \quad (23)$$

$I_{TMR(UP)} \approx 1.5\mu A$ at power up:

$$V_{TMR} = 1.5\mu A \bullet \frac{32.9ms}{0.22\mu F} \approx 0.224V,$$

which is much lower than the 1.215V trip off threshold.

Next, we need to check to make sure that in the case of a severe output short where V_{OUT} = 0V, the power dissipation in the MOSFET is also within the safe operating area (Equation 24a & 24b).

$$I_{TMR(SC)} = \left[0.0917 \bullet (62mV) \bullet \sqrt{\frac{14V}{82.5k} - 70 \bullet 10^{-6}}\right] + 24 \bullet 10^{-6} \quad (24a)$$
$$I_{TMR(SC)} = 80.8\mu A$$

$$t_{TMR} = 0.22\mu F \bullet \frac{1.215V}{80.8\mu A} = 3.31ms \quad (24b)$$

The power dissipation in the MOSFET is given by Equation 25.

$$P = 14V \bullet \frac{62mV}{40m\Omega} = 21.7W$$
$$P\sqrt{t} = 1.248W\sqrt{s} \quad (25)$$

During an output overload or soft short, the voltage at the OUT pin could stay at 3V or higher. The total overcurrent fault time when V_{OUT} = 3V is given by Equation 26a & 26b.

$$I_{TMR(OC)} = \left[0.0917 \bullet (50mV) \bullet \sqrt{\frac{11V}{82.5k} - 70 \bullet 10^{-6}}\right] + 6 \bullet 10^{-6} \quad (26a)$$
$$I_{TMR(OC)} = 42.5\mu A$$

$$t_{TMR} = 0.22\mu F \bullet \frac{1.215V}{42.5\mu A} = 6.29ms \quad (26b)$$

The power dissipation in the MOSFET is given by Equation 27.

$$P = (14V - 3V) \bullet \frac{50mV}{40m\Omega} = 13.75W$$
$$P\sqrt{t} = 1.09W\sqrt{s} \quad (27)$$

These conditions are within the 10W√s safe operating area of the MOSFET.

APPLICATIONS INFORMATION

Design Example 2

A second design example has the following specifications: V_{IN} = 24V_{DC} with a transient of 100V peak and a duration of 400ms like a load dump waveform, $V_{OUT} \leq$ 60V, load of 1A.

There are a few methods to clamp V_{OUT} to less than 60V, we can use the LTC4381-2 by connecting SEL pin to IN to clamp V_{OUT} to 47V. Or we can use a LTC4381-4 and clamp V_{CC} to <50V. A third method is to regulate V_{OUT} directly using a 56V Zener and NPN as shown in Figure 7. This method gives a slightly tighter V_{OUT} clamp at an expense of more external components.

Since IN can go as high as 100V, a clamp at V_{CC} pin is needed to limit it to <80V. Use Zener CMZ5945B as D1 which limits V_{CC} to <68V.

The maximum current through R1 into D1 during transients is then calculated by Equation 28.

$$I_{D1} = \frac{100V - 68V}{100k\Omega} = 0.32mA \quad (28)$$

Power dissipated in D1 is 22mW.

R_{DRN} is chosen to produce a current into the DRN pin of less than 1mA, during the maximum overvoltage transient event (Equation 29).

$$R_{DRN} = \frac{100V - 24V}{1mA} = 76k\Omega \quad (29)$$

100kΩ is chosen to give enough margin.

The MOSFET stress can be calculated using the prototypical transient waveform shown in Figure 3 using t_r = 5ms, V_{PK} = 100V and τ = 200ms (Equation 30).

$$a = V_{REG} - V_{IN} = 56.7V - 24V = 32.7V$$

$$b = V_{PK} - V_{IN} = 100V - 24V = 76V$$

$$P\sqrt{t} = I_{LOAD}\left[\frac{1}{3}t_r\frac{(b-a)^3}{b} + \frac{1}{2}\tau\left(2a^2\ln\frac{b}{a} + 3a^2 + b^2 - 4ab\right)\right]^{1/2} \quad (30)$$

$$P\sqrt{t} = 9.3W\sqrt{s}$$

This is within the LTC4381 SOA limit of 10W$\sqrt{s}$.

Next calculate the sense resistor (R_{SNS}) value with a current limit of greater than 1A with 20% tolerance (Equation 31).

$$R_{SNS} = \frac{50mV}{I_{LIM}} = \frac{50mV}{1.2A} = 41.67m\Omega \quad (31)$$

We will use 40mΩ, which gives a current limit of 1.25A.

The load dump waveform can be represented as an exponentially decaying waveform with a time constant of 0.2sec (Equation 32).

$$V_{IN} = 100Ve^{-t/0.2s} \quad (32)$$

The LTC4381 clamps the V_{OUT} at 56.7V, (56V from D2 and 0.7V from V_{BE} of Q2) which means that V_{DS} and ITMR drops to zero when V_{IN} drops to 56.7V. To find the time t when this happen, we use Equation 33.

$$t = -0.2s \bullet \ln\left(\frac{56.7V}{100V}\right) = 0.113s \quad (33)$$

V_{DS} can be approximated as a triangular waveform with a peak of 100V – 56.7V or 43.3V and a time base of 0.113sec. We take half of the peak, 21.65V to calculate the ITMR (Equation 34).

$$I_{TMR(OV)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet I_D \bullet R_{SNS} \bullet \sqrt{\frac{V_{DS}}{R_{DRN}} - 70\mu A}\right)$$

$$I_{TMR(OV)} = \left(0.0917\left[\frac{\sqrt{A}}{V}\right] \bullet 1A \bullet 0.04\Omega \bullet \sqrt{\frac{21.65V}{100k} - 70\mu A}\right) \quad (34)$$

$$I_{TMR(OV)} = 44\mu A$$

$$C_{TMR} = \frac{t \bullet I_{TMR}}{V_{TMR}}$$

$$C_{TMR} = \frac{0.113s \bullet 44\mu A}{1.215V}$$

$$C_{TMR} = 4.1\mu F$$

APPLICATIONS INFORMATION

We shall use a 4.7µF capacitor for more margin. Next, we need to make sure that the chosen CTMR allow enough time to power up the output (Equation 35).

$$C_{TMR} = \frac{I_{TMR(UP)} \bullet t_{INRUSH}}{V_{TMR}}$$

$$t_{INRUSH} = \frac{V_{IN} \bullet C_{OUT}}{I_{INRUSH}} = \frac{V_{IN} \bullet C_2}{I_{GATE(UP)}} = \frac{24V \bullet 47nF}{20\mu A} = 56.4ms \quad (35)$$

$I_{TMR(UP)} \approx 1.5\mu A$ at power up:

$$V_{TMR} = \frac{1.5\mu A \bullet 56.4ms}{4.7\mu F} \approx 18mV$$

Next, we need to check to makes sure that in the case of a severe output short where V_{OUT} = 0V, the power dissipation in the MOSFET is also within the safe operating area (Equation 36a & 36b).

$$I_{TMR(SC)} = \left[0.0917 \bullet (62mV) \bullet \sqrt{\frac{24V}{100k} - 70 \bullet 10^{-6}}\right] + 24 \bullet 10^{-6} \quad (36a)$$

$I_{TMR(SC)} = 98.1\mu A$

$$V_{TMR} = \frac{4.7\mu F \bullet 1.215V}{98.1\mu A} = 58.2ms \quad (36b)$$

The power dissipation in MOSFET is given by Equation 37.

$$P = 24V \bullet \frac{62mV}{40m\Omega} = 37.2W$$
$$P\sqrt{t} = 8.97W\sqrt{s} \quad (37)$$

During an output overload or soft short, the voltage at the OUT pin could stay at 3V or higher. The total overcurrent fault time when V_{OUT} = 3V is given by Equation 38a & 38b.

$$I_{TMR(OC)} = \left[0.0917 \bullet (50mV) \bullet \sqrt{\frac{21V}{100k} - 70 \bullet 10^{-6}}\right] + 6 \bullet 10^{-6} \quad (38a)$$

$I_{TMR(OC)} = 60.3\mu A$

$$t_{TMR} = 4.7\mu F \bullet \frac{1.215V}{60.3\mu A} = 94.7ms \quad (38b)$$

The power dissipation in MOSFET is given by Equation 39.

$$P = (24V - 3) \bullet \frac{50mV}{40m\Omega} = 26.25W$$
$$P\sqrt{t} = 8.08W\sqrt{s} \quad (39)$$

These conditions are within the safe operating area of the MOSFET.

TYPICAL APPLICATION

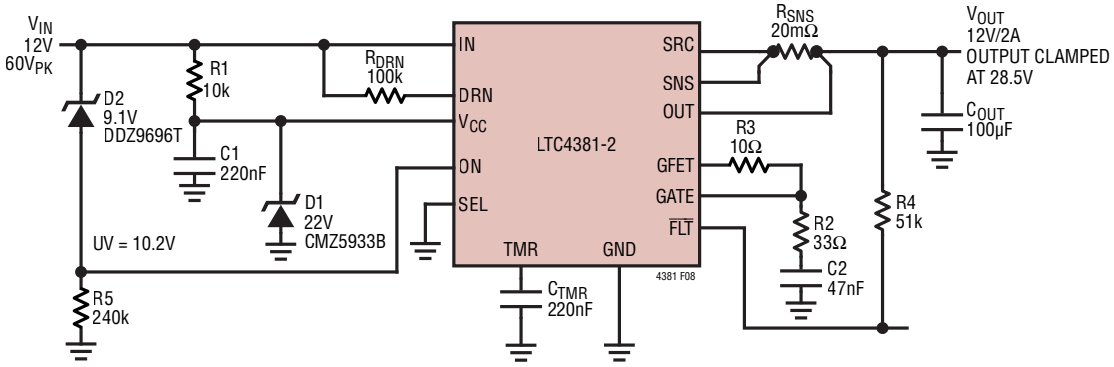


Figure 8. 12V Hot Swap Controller with Input UV Detection with 60V/2A/3.5ms Overvoltage Protection

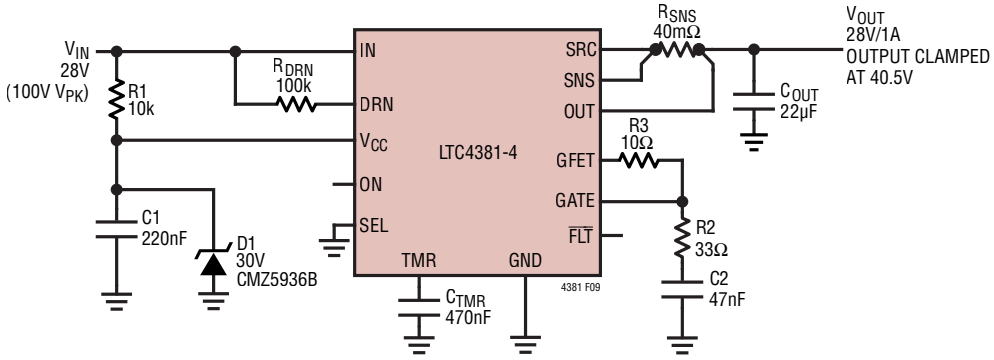


Figure 9. 28V Surge Stopper with Output Clamped to Below 40V with 100V/1A/6ms Overvoltage Protection

TYPICAL APPLICATION

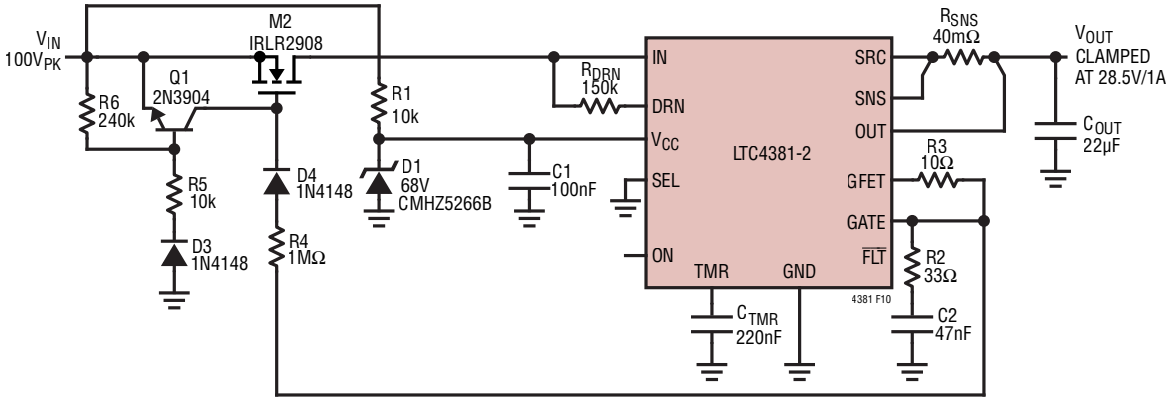


Figure 10. –60V Reverse Battery Protection with 100V/1A/3ms Overvoltage Protection

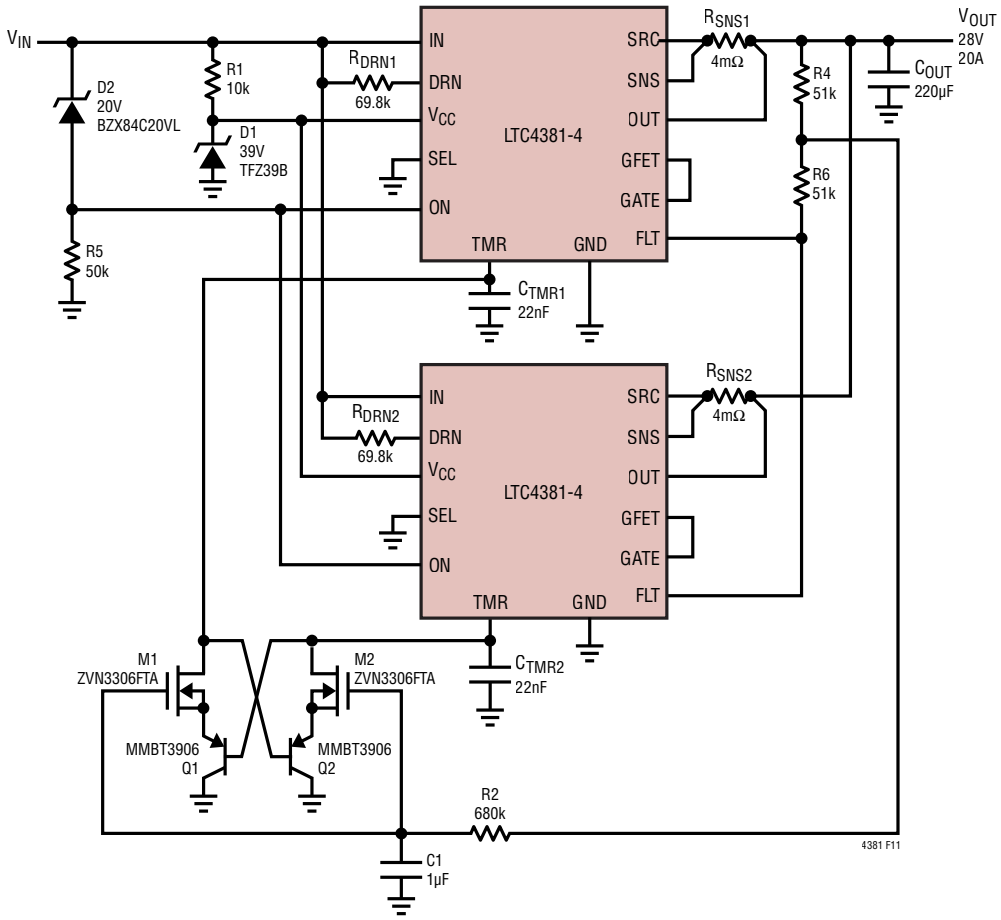
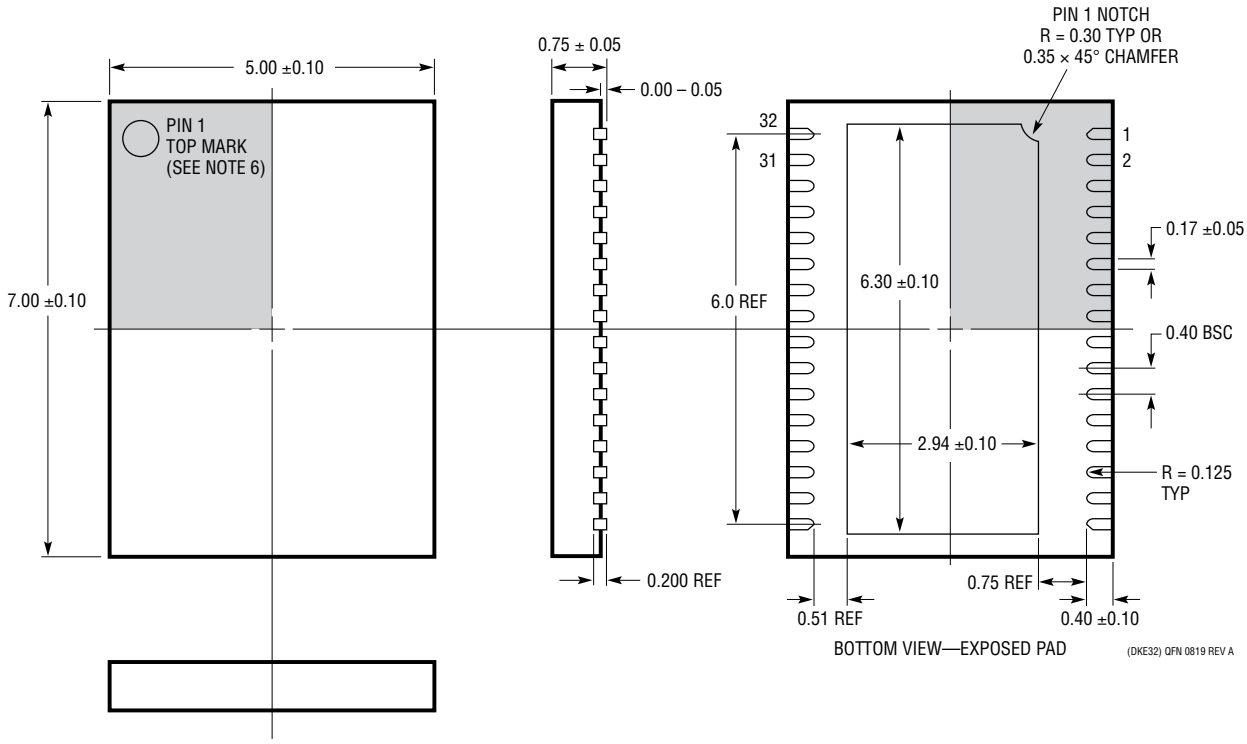


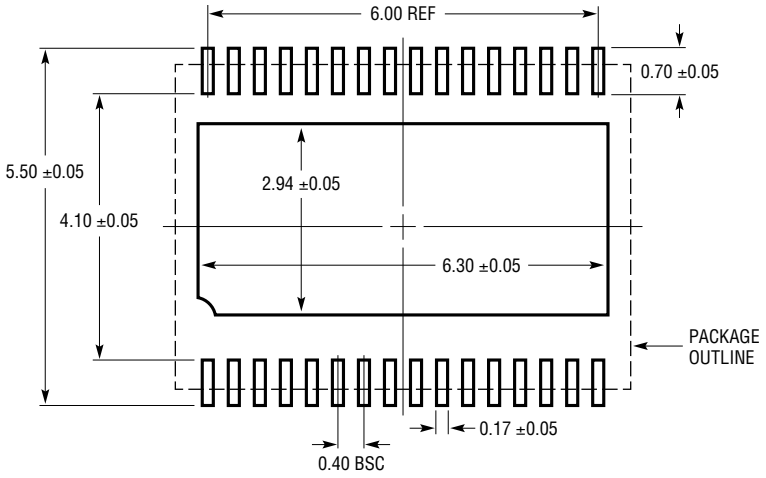
Figure 11. 28V, 20A eFuse

PACKAGE DESCRIPTION

DKE Package
32-Lead Plastic DFN (7mm × 5mm)
(Reference LTC DWG # 05-08-1789 Rev A)



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/22	Changed Part Description.	1
		Added a new MOSFET Avalanche Current spec in EC Table.	3
		Changed labels of Timer pin current Spec.	4
		Replaced Current Limit vs Output Voltage curve.	6
		Changed labels in Timer pin current Equations.	13-14, 16-21
		Changed text in Supply Transient Protection section.	14
		Changed Equation 14 and 15.	17
		Added Timer pin current Equations.	19-21
		Added Figure 11: 28V. 20A eFuse.	23
		Changed Figure 12's R_{DRN} and CTMR value.	26