

FEATURES

- Wide Operating V_{IN} Range: Up to 80V
- Rugged Architecture Tolerant of 100V V_{IN} Transients
- Powerful 1.5 Ω Driver Pull-Down
- Powerful 2.4A Peak Current Driver Pull-Up
- 7ns Fall Time Driving 1000pF Load
- 10ns Rise Time Driving 1000pF Load
- Drives Standard Threshold MOSFETs
- TTL/CMOS Compatible Inputs with Hysteresis
- Input Thresholds are Independent of Supply
- Undervoltage Lockout
- Low Profile (1mm) SOT-23 (ThinSOT)[™] and Thermally Enhanced 8-Pin MSOP Packages

APPLICATIONS

- Telecommunications Power Systems
- Distributed Power Architectures
- Server Power Supplies
- High Density Power Modules

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DESCRIPTION

The LTC[®]4440 is a high frequency high side N-channel MOSFET gate driver that is designed to operate in applications with V_{IN} voltages up to 80V. The LTC4440 can also withstand and continue to function during 100V V_{IN} transients. The powerful driver capability reduces switching losses in MOSFETs with high gate capacitances. The LTC4440's pull-up has a peak output current of 2.4A and its pull-down has an output impedance of 1.5 Ω .

The LTC4440 features supply independent TTL/CMOS compatible input thresholds with 350mV of hysteresis. The input logic signal is internally level-shifted to the bootstrapped supply, which may function at up to 115V above ground.

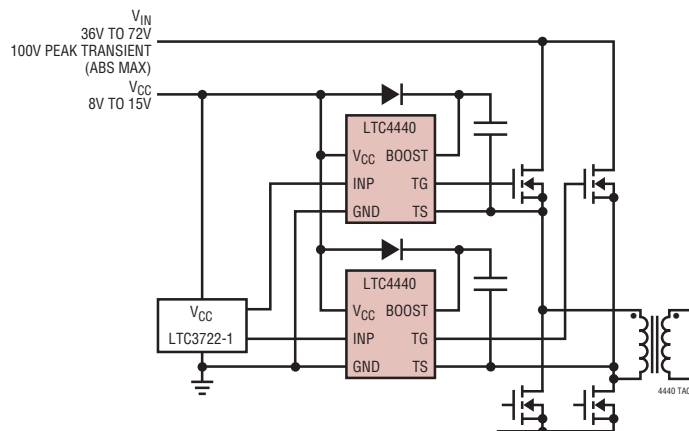
The LTC4440 contains both high side and low side undervoltage lockout circuits that disable the external MOSFET when activated.

The LTC4440 is available in the low profile (1mm) SOT-23 and thermally enhanced 8-lead MSOP packages.

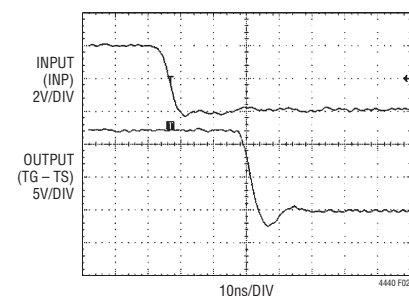
PARAMETER	LTC4440	LTC4440-5	LTC4440A-5
Max Operating TS	80V	60V	80V
Absolute Max TS	100V	80V	100V
MOSFET Gate Drive	8V to 15V	4V to 15V	4V to 15V
V_{CC} UV ⁺	6.3V	3.2V	3.2V
V_{CC} UV ⁻	6.0V	3.04V	3.04V

TYPICAL APPLICATION

Synchronous Phase-Modulated Full-Bridge Converter



LTC4440 Driving a 1000pF Capacitive Load

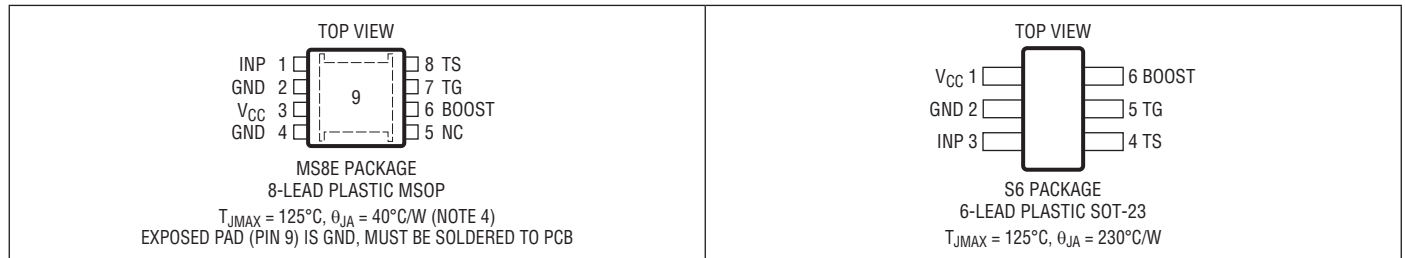


LTC4440

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage		Peak Output Current < 1 μ s (TG).....	4A
V_{CC}	-0.3V to 15V	Driver Output TG (with Respect to TS).....	-0.3V to 15V
BOOST – TS.....	-0.3V to 15V	Operating Temperature Range (Note 2)	
INP Voltage	-0.3V to 15V	LTC4440E	-40°C to 85°C
BOOST Voltage (Continuous)	-0.3V to 95V	LTC4440I	-40°C to 125°C
BOOST Voltage (100ms)	-0.3V to 115V	Junction Temperature (Note 3)	125°C
TS Voltage (Continuous)	-5V to 80V	Storage Temperature Range	-65°C to 150°C
TS Voltage (100ms)	-5V to 100V	Lead Temperature (Soldering, 10 sec).....	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4440EMS8E#PBF	LTC4440EMS8E#TRPBF	LTF9	8-Lead Plastic MSOP	-40°C to 85°C
LTC4440IMS8E#PBF	LTC4440IMS8E#TRPBF	LTF9	8-Lead Plastic MSOP	-40°C to 125°C
LTC4440ES6#PBF	LTC4440ES6#TRPBF	LTZY	6-Lead Plastic SOT-23	-40°C to 85°C
LTC4440IS6#PBF	LTC4440IS6#TRPBF	LTZY	6-Lead Plastic SOT-23	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = V_{BOOST} = 12\text{V}$, $V_{TS} = \text{GND} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Main Supply (V_{CC})							
I_{VCC}	DC Supply Current Normal Operation UVLO	INP = 0V $V_{CC} < \text{UVLO Threshold (Falling)} - 0.1\text{V}$		250 25	400 80	μA μA	
UVLO	Undervoltage Lockout Threshold	V_{CC} Rising V_{CC} Falling Hysteresis	● ●	5.7 5.4	6.5 6.2 300	V V mV	
Bootstrapped Supply (BOOST – TS)							
I_{BOOST}	DC Supply Current Normal Operation UVLO	INP = 0V $V_{BOOST} - V_{TS} < \text{UVLO}_{\text{HS(FALLING)}} - 0.1\text{V}$, $V_{CC} = \text{INP} = 5\text{V}$		110 86	180 170	μA μA	
UVLO _{HS}	Undervoltage Lockout Threshold	$V_{BOOST} - V_{TS}$ Rising $V_{BOOST} - V_{TS}$ Falling Hysteresis	● ●	6.75 6.25	7.4 6.9 500	V V mV	
Input Signal (INP)							
V_{IH}	High Input Threshold	INP Ramping High	●	1.3	1.6	2	V
V_{IL}	Low Input Threshold	INP Ramping Low	●	0.85	1.25	1.6	V
$V_{IH} - V_{IL}$	Input Voltage Hysteresis			0.350			V
I_{INP}	Input Pin Bias Current			± 0.01	± 2		μA
Output Gate Driver (TG)							
V_{OH}	High Output Voltage	$I_{TG} = -10\text{mA}$, $V_{OH} = V_{BOOST} - V_{TG}$			0.7		V
V_{OL}	Low Output Voltage	$I_{TG} = 100\text{mA}$: $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	● ●	150 150	220 300	mV mV	
I_{PU}	Peak Pull-Up Current	$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	● ●	1.7 1.5	2.4 2.4	A A	
R_{DS}	Output Pull-Down Resistance	$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	● ●	1.5 1.5	2.2 3	Ω Ω	
Switching Timing							
t_r	Output Rise Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		10 100		ns ns	
t_f	Output Fall Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		7 70		ns ns	
t_{PLH}	Output Low-High Propagation Delay	$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	● ●	30 30	65 75	ns ns	
t_{PHL}	Output High-Low Propagation Delay	$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	● ●	28 28	65 75	ns ns	

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC4440E is guaranteed to meet performance specifications from 0°C to 70°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4440I is guaranteed and tested over the -40°C to 125°C operating temperature range.

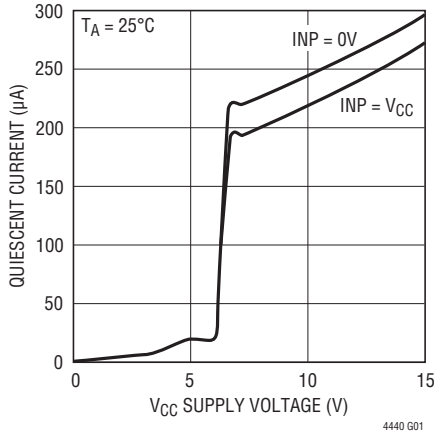
Note 3: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula:

$$T_J = T_A + (\text{PD} \cdot \theta_{JA})^\circ\text{C/W}$$

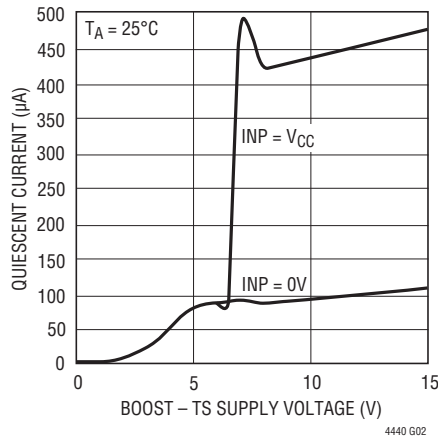
Note 4: Failure to solder the exposed back side of the MS8E package to the PC board will result in a thermal resistance much higher than 40°C/W .

TYPICAL PERFORMANCE CHARACTERISTICS

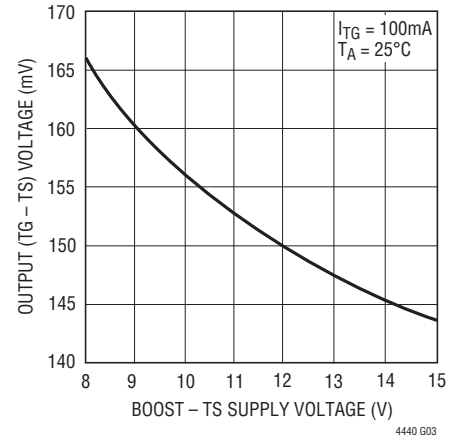
V_{CC} Supply Quiescent Current vs Voltage



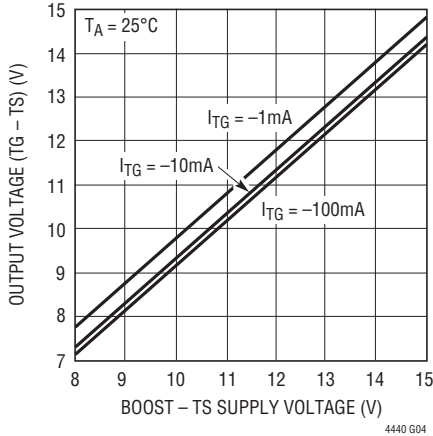
BOOST – TS Supply Quiescent Current vs Voltage



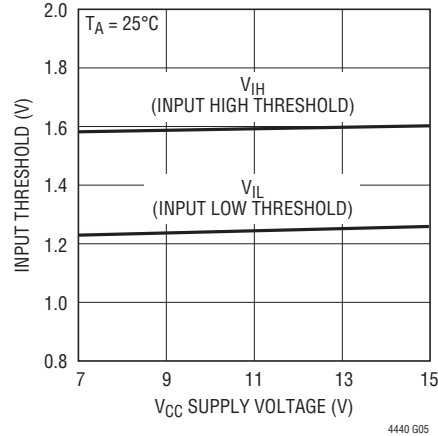
Output Low Voltage (V_{OL}) vs Supply Voltage



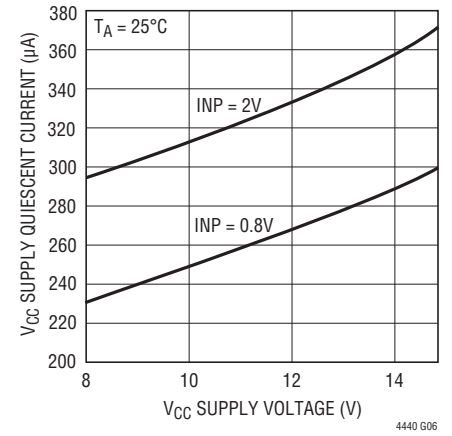
Output High Voltage (V_{OH}) vs Supply Voltage



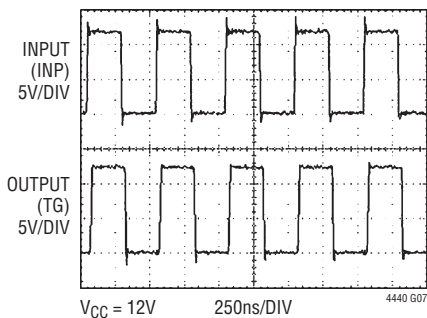
Input Thresholds (INP) vs Supply Voltage



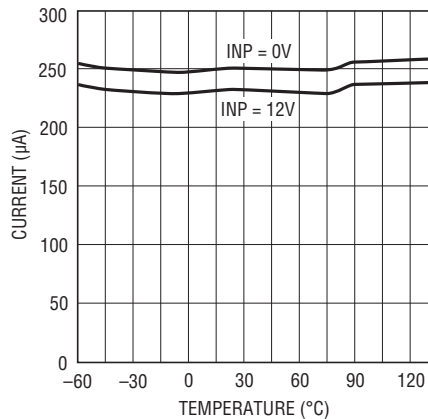
V_{CC} Supply Current at TTL Input Levels



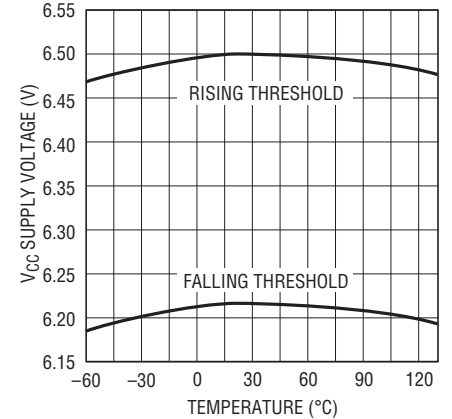
2MHz Operation



V_{CC} Supply Current (V_{CC} = 12V) vs Temperature

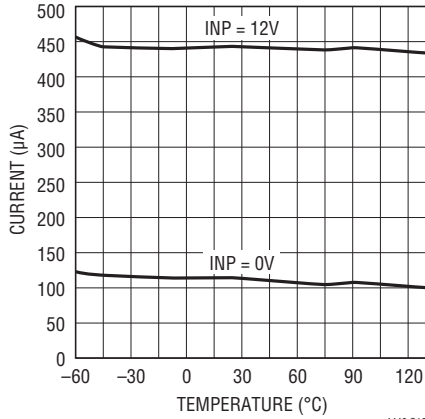


V_{CC} Undervoltage Lockout Thresholds vs Temperature

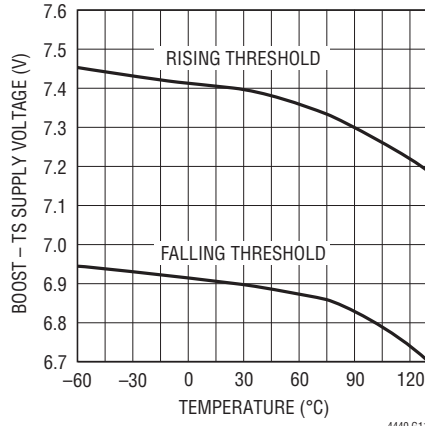


TYPICAL PERFORMANCE CHARACTERISTICS

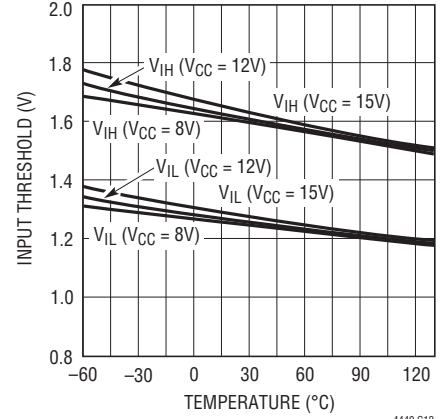
Boost Supply Current vs Temperature



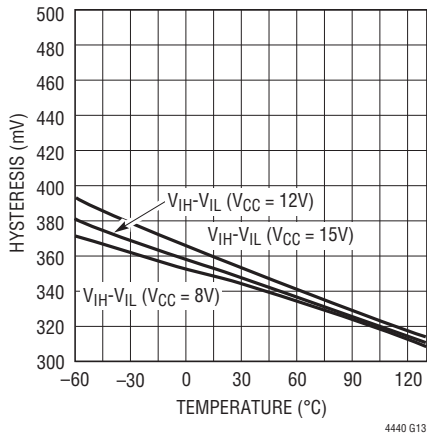
Boost Supply (BOOST – TS) Undervoltage Lockout Thresholds vs Temperature



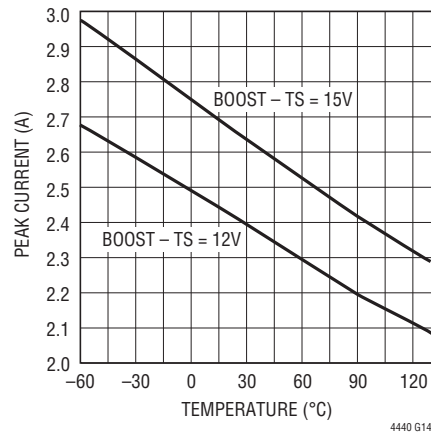
Input Threshold vs Temperature



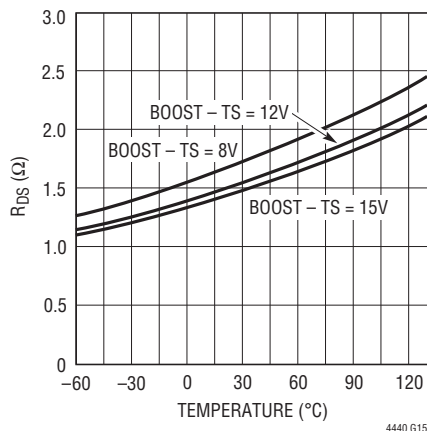
Input Threshold Hysteresis vs Temperature



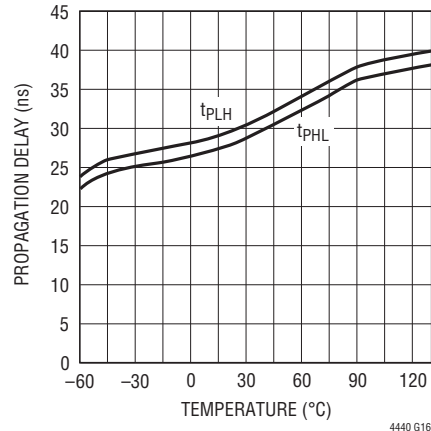
Peak Driver (TG) Pull-Up Current vs Temperature



Output Driver Pull-Down Resistance vs Temperature



Propagation Delay vs Temperature (V_{CC} = BOOST = 12V)



PIN FUNCTIONS

SOT-23 Package

V_{CC} (Pin 1): Chip Supply. This pin powers the internal low side circuitry. A low ESR ceramic bypass capacitor should be tied between this pin and the GND pin (Pin 2).

GND (Pin 2): Chip Ground.

INP (Pin 3): Input Signal. TTL/CMOS compatible input referenced to GND (Pin 2).

TS (Pin 4): Top (High Side) Source Connection.

TG (Pin 5): High Current Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

BOOST (Pin 6): High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 4). Normally, a bootstrap diode is connected between V_{CC} (Pin 1) and this pin. Voltage swing at this pin is from V_{CC} - V_D to V_{IN} + V_{CC} - V_D, where V_D is the forward voltage drop of the bootstrap diode.

Exposed Pad MS8E Package

INP (Pin 1): Input Signal. TTL/CMOS compatible input referenced to GND (Pin 2).

GND (Pins 2, 4): Chip Ground.

V_{CC} (Pin 3): Chip Supply. This pin powers the internal low side circuitry. A low ESR ceramic bypass capacitor should be tied between this pin and the GND pin (Pin 2).

NC (Pin 5): No Connect. No connection required. For convenience, this pin may be tied to Pin 6 (BOOST) on the application board.

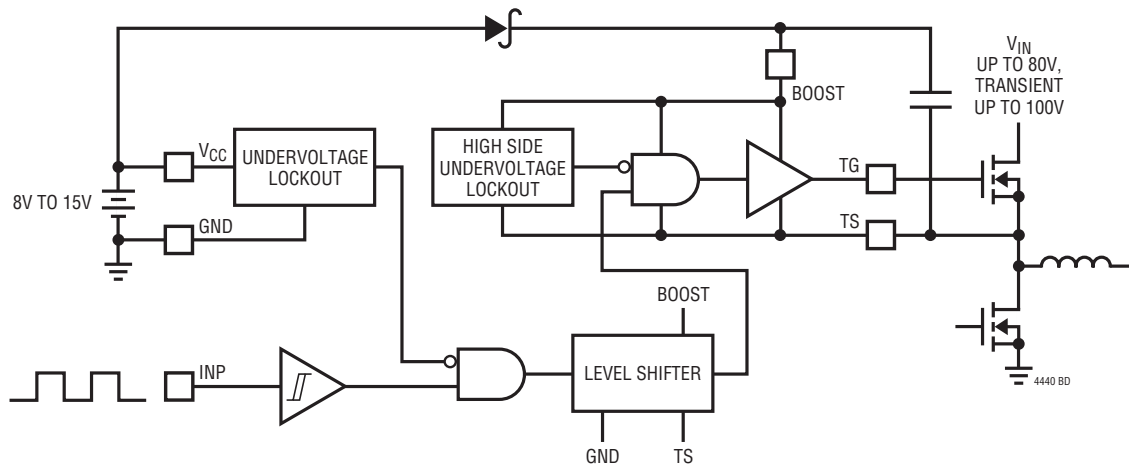
BOOST (Pin 6): High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 8). Normally, a bootstrap diode is connected between V_{CC} (Pin 3) and this pin. Voltage swing at this pin is from V_{CC} - V_D to V_{IN} + V_{CC} - V_D, where V_D is the forward voltage drop of the bootstrap diode.

TG (Pin 7): High Current Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

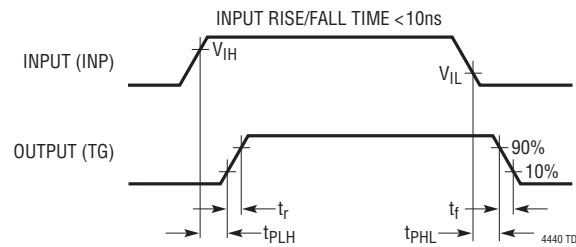
TS (Pin 8): Top (High Side) Source Connection.

Exposed Pad (Pin 9): Ground. Must be electrically connected to Pins 2 and 4 and soldered to PCB ground for optimum thermal performance.

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Overview

The LTC4440 receives a ground-referenced, low voltage digital input signal to drive a high side N-channel power MOSFET whose drain can float up to 100V above ground, eliminating the need for a transformer between the low voltage control signal and the high side gate driver. The LTC4440 normally operates in applications with input supply voltages (V_{IN}) up to 80V, but is able to withstand and continue to function during 100V, 100ms transients on the input supply.

The powerful output driver of the LTC4440 reduces the switching losses of the power MOSFET, which increase with transition time. The LTC4440 is capable of driving a 1nF load with 10ns rise and 7ns fall times using a bootstrapped supply voltage $V_{BOOST-TS}$ of 12V.

Input Stage

The LTC4440 employs TTL/CMOS compatible input thresholds that allow a low voltage digital signal to drive standard power MOSFETs. The LTC4440 contains an internal voltage regulator that biases the input buffer, allowing the input thresholds ($V_{IH} = 1.6V$, $V_{IL} = 1.25V$) to be independent of variations in V_{CC} . The 350mV hysteresis between V_{IH} and V_{IL} eliminates false triggering due to noise during switching transitions. However, care should be taken to keep this pin from any noise pickup, especially in high frequency, high voltage applications. The LTC4440 input buffer has a high input impedance and draws negligible input current, simplifying the drive circuitry required for the input.

Output Stage

A simplified version of the LTC4440's output stage is shown in Figure 3. The pull-down device is an N-channel MOSFET (N1) and the pull-up device is an NPN bipolar junction transistor (Q1). The output swings from the lower rail (TS) to within an NPN V_{BE} ($\sim 0.7V$) of the positive rail (BOOST). This large voltage swing is important in driving external power MOSFETs, whose $R_{DS(ON)}$ is inversely proportional to its gate overdrive voltage ($V_{GS} - V_{TH}$).

The LTC4440's peak pull-up (Q1) current is 2.4A while the pull-down (N1) resistance is 1.5Ω . The low impedance of N1 is required to discharge the power MOSFET's gate capacitance during high-to-low signal transitions. When the power MOSFET's gate is pulled low (gate shorted to source through N1) by the LTC4440, its source (TS) is pulled low by its load (e.g., an inductor or resistor). The slew rate of the source/gate voltage causes current to flow back to the MOSFET's gate through the gate-to-drain capacitance (C_{GD}). If the MOSFET driver does not have sufficient sink current capability (low output impedance), the current through the power MOSFET's C_{GD} can momentarily pull the gate high, turning the MOSFET back on.

A similar scenario exists when the LTC4440 is used to drive a low side MOSFET. When the low side power MOSFET's gate is pulled low by the LTC4440, its drain voltage is pulled high by its load (e.g., inductor or resistor). The slew rate of the drain voltage causes current to flow back to the MOSFET's gate through its gate-to-drain capacitance. If

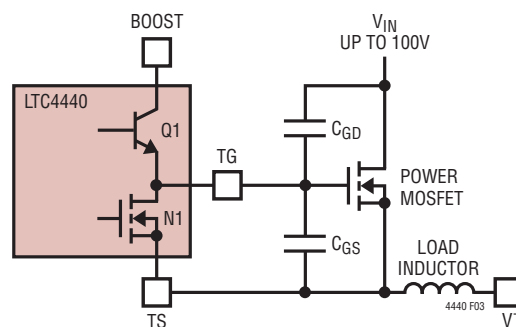


Figure 3. Capacitance Seen by TG During Switching

APPLICATIONS INFORMATION

the MOSFET driver does not have sufficient sink current capability (low output impedance), the current through the power MOSFET's C_{GD} can momentarily pull the gate high, turning the MOSFET back on.

Rise/Fall Time

Since the power MOSFET generally accounts for the majority of the power loss in a converter, it is important to quickly turn it on or off, thereby minimizing the transition time in its linear region. The LTC4440 can drive a 1nF load with a 10ns rise time and 7ns fall time.

The LTC4440's rise and fall times are determined by the peak current capabilities of Q1 and N1. The predriver that drives Q1 and N1 uses a nonoverlapping transition scheme to minimize cross-conduction currents. N1 is fully turned off before Q1 is turned on and vice versa.

Power Dissipation

To ensure proper operation and long-term reliability, the LTC4440 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + PD (\theta_{JA})$$

where:

T_J = Junction Temperature

T_A = Ambient Temperature

PD = Power Dissipation

θ_{JA} = Junction-to-Ambient Thermal Resistance

Power dissipation consists of standby and switching power losses:

$$PD = P_{STDBY} + P_{AC}$$

where:

P_{STDBY} = Standby Power Losses

P_{AC} = AC Switching Losses

The LTC4440 consumes very little current during standby. The DC power loss at $V_{CC} = 12V$ and $V_{BOOST-TS} = 12V$ is only $(250\mu A + 110\mu A)(12V) = 4.32mW$.

AC switching losses are made up of the output capacitive load losses and the transition state losses. The capacitive load losses are primarily due to the large AC currents needed to charge and discharge the load capacitance during switching. Load losses for the output driver driving a pure capacitive load C_{OUT} would be:

$$\text{Load Capacitive Power} = (C_{OUT})(f)(V_{BOOST-TS})^2$$

The power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A power MOSFET's capacitive load power dissipation can be calculated using its gate charge, Q_G . The Q_G value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's Q_G vs V_{GS} curves:

$$\text{Load Capacitive Power (MOS)} = (V_{BOOST-TS})(Q_G)(f)$$

Transition state power losses are due to both AC currents required to charge and discharge the driver's internal nodal capacitances and cross-conduction currents in the internal gates.

APPLICATIONS INFORMATION

Undervoltage Lockout (UVLO)

The LTC4440 contains both low side and high side undervoltage lockout detectors that monitor V_{CC} and the bootstrapped supply $V_{BOOST-TS}$. When V_{CC} falls below 6.2V, the internal buffer is disabled and the output pin OUT is pulled down to TS. When $V_{BOOST-TS}$ falls below 6.9V, OUT is pulled down to TS. When both supplies are undervoltage, OUT is pulled low to TS and the chip enters a low current mode, drawing approximately 25 μ A from V_{CC} and 86 μ A from BOOST.

Bypassing and Grounding

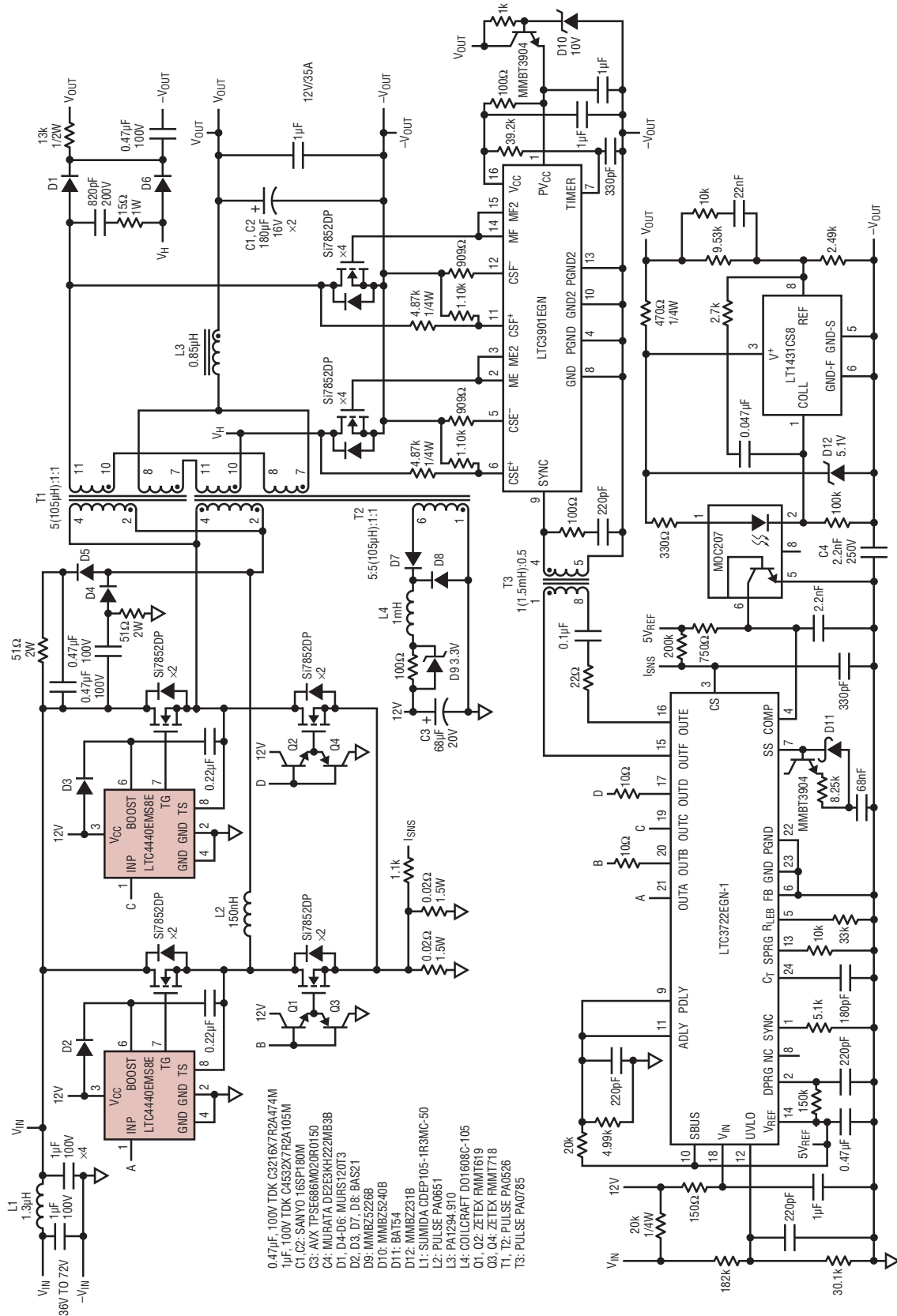
The LTC4440 requires proper bypassing on the V_{CC} and $V_{BOOST-TS}$ supplies due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimum performance from the LTC4440:

- A. Mount the bypass capacitors as close as possible between the V_{CC} and GND pins and the BOOST and TS pins. The leads should be shortened as much as possible to reduce lead inductance.
- B. Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC4440 switches >2A peak currents and any significant ground drop will degrade signal integrity.
- C. Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- D. Keep the copper trace between the driver output pin and the load short and wide.
- E. When using the MS8E package, be sure to solder the exposed pad on the back side of the LTC4440 package to the board. Correctly soldered to a 2500mm² double-sided 1oz copper board, the LTC4440 has a thermal resistance of approximately 40°C/W. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than 40°C/W.

TYPICAL APPLICATIONS

LTC3722/LTC4440 420W 36V-72V_{IN} to 12V/35A Isolated Full-Bridge Supply

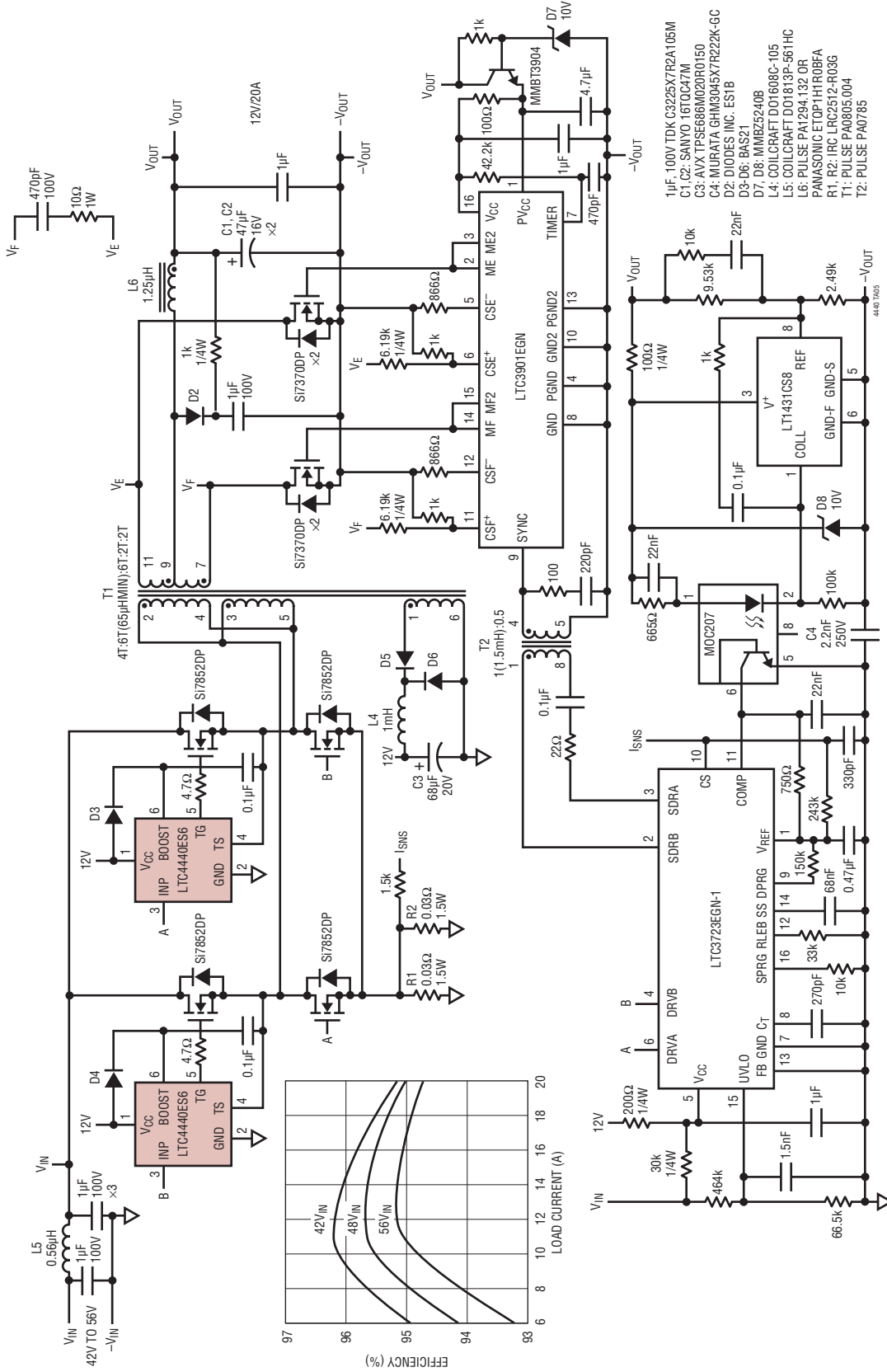


- 0.47µF, 100V TDK C3216X7R2A474M
- 1µF, 100V TDK C4532X7R2A105M
- C1, C2: SANYO 16S160M
- C3: AVX TPSE68M020R0150
- C4: MURATA DEPE3K1222MB3B
- D1: D4-D6: MUR5120T3
- D2, D3, D7, D8: BAS21
- D9: MMBZ5226B
- D10: MMBZ5240B
- D11: BAT54
- D12: MMBZ231B
- L1: SUMIDA CDEP105-1R3MC-50
- L2: PULSE PA0651
- L3: PA1294.910
- L4: COILCRAFT D01608C-105
- O1, O2: ZETEX RMMT619
- O3, O4: ZETEX RMMT718
- T1, T2: PULSE PA0626
- T3: PULSE PA0785

4440 TAB

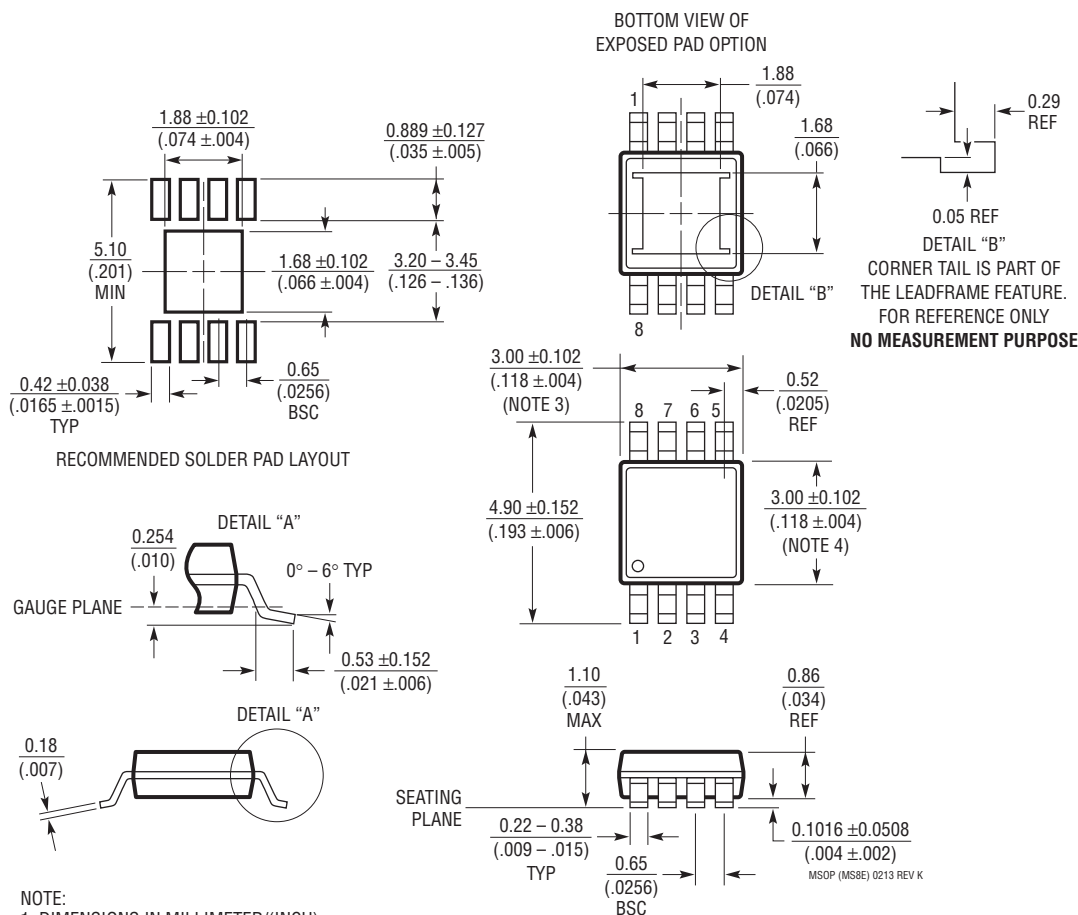
TYPICAL APPLICATIONS

LTC3723-1 240W 42-56V_{IN} to 12V/20A Isolated 1/4Brick (2.3" × 1.45")



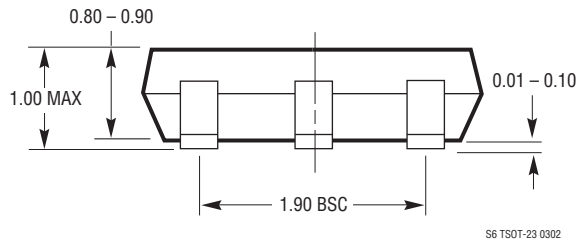
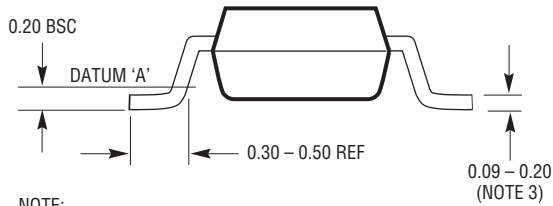
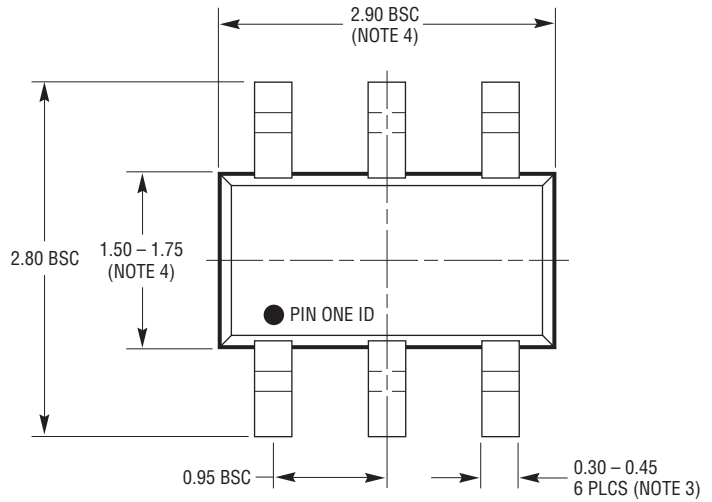
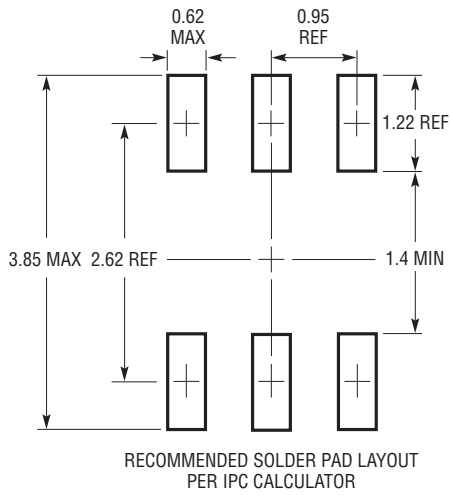
PACKAGE DESCRIPTION

MS8E Package 8-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1662 Rev K)



PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
 (Reference LTC DWG # 05-08-1636)



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DRAWING NOT TO SCALE
 3. DIMENSIONS ARE INCLUSIVE OF PLATING
 4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 5. MOLD FLASH SHALL NOT EXCEED 0.254mm
 6. JEDEC PACKAGE REFERENCE IS MO-193

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1013	Added comparison table	1
B	0215	Released I-Grade Version	2, 3