600MHz to 1.3GHz High Dynamic Range Downconverting Mixer

FEATURES

- **Conversion Gain: 7.9dB at 900MHz**
- **IIP3: 25.9dBm at 900MHz**
- **Noise Figure: 9.9dB at 900MHz**
- **16.2dB NF Under +5dBm Blocking**
- **High Input P1dB**
- **3.3V Supply, 640mW Power Consumption**
- **Shutdown Pin**
- **50Ω Single-Ended RF and LO Inputs**
- **LO Inputs 50Ω Matched when Shutdown**
- **High Isolation LO Switch**
- 0dBm LO Drive Level
- High LO-RF and LO-IF Isolation
- Small Solution Size
- 20-Lead (5mm × 5mm) QFN package

APPLICATIONS

- Wireless Infrastructure Receivers (LTE, GSM, W-CDMA)
- Point-to-Point Microwave links
- High Dynamic Range Downmixer Applications

DESCRIPTION

The LTC®5540 is part of a family of high dynamic range, high gain passive downconverting mixers covering the 600MHz to 4GHz frequency range. **The LTC5540 is optimized for 0.6GHz to 1.3GHz RF applications. The LO frequency must fall within the 0.7GHz to 1.2GHz range for optimum performance.** A typical application is a LTE or GSM receiver with a 700MHz to 915MHz RF input and high-side LO.

The LTC5540 is designed for 3.3V operation, however; the IF amplifier can be powered by 5V for the highest P1dB. An integrated SPDT LO switch with fast switching accepts two active LO signals, while providing high isolation.

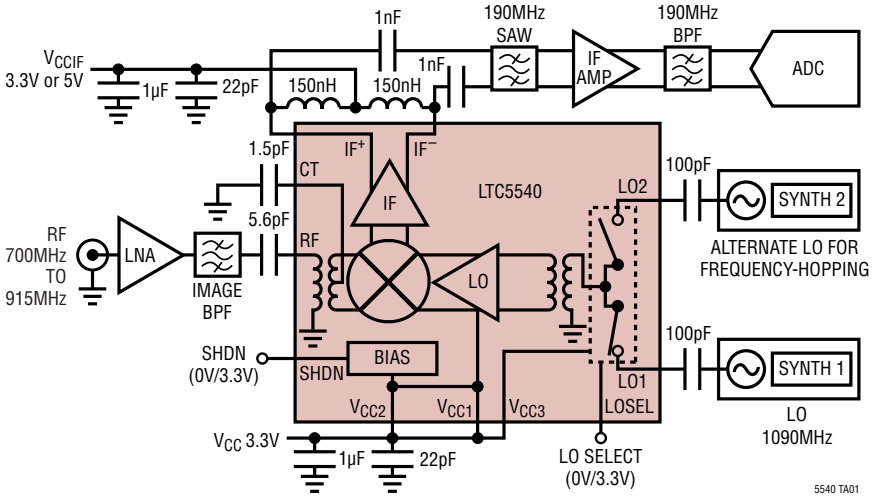
The LTC5540's high conversion gain and high dynamic range enable the use of lossy IF filters in high-selectivity receiver designs, while minimizing the total solution cost, board space and system-level variation.

High Dynamic Range Downconverting Mixer Family

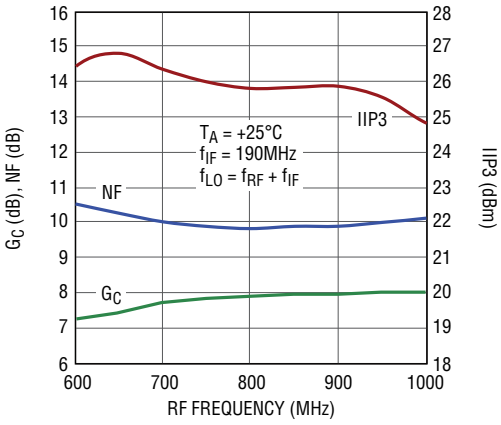
PART#	RF RANGE	LO RANGE
LTC5540	**600MHz –1.3GHz**	**700MHz – 1.2GHz**
LTC5541	1.3GHz – 2.3GHz	1.4GHz – 2.0GHz
LTC5542	1.6GHz – 2.7GHz	1.7GHz – 2.5GHz
LTC5543	2.3GHz – 4GHz	2.4GHz – 3.6GHz

TYPICAL APPLICATION

Wideband Receiver



Wideband Conversion Gain, IIP3 and NF vs RF Input Frequency

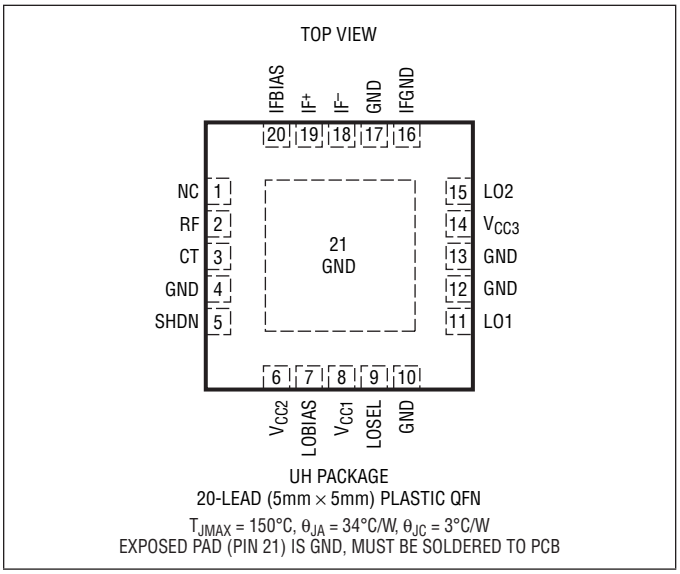


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Mixer Supply Voltage (V_{CC1}, V_{CC2}).....3.8V
LO Switch Supply Voltage (V_{CC3}).....3.8V
IF Supply Voltage (IF^+, IF^-) 5.5V
Shutdown Voltage (SHDN).....–0.3V to V_{CC} +0.3V
LO Select Voltage (LOSEL).....–0.3V to V_{CC} +0.3V
LO1, LO2 Input Power (0.2GHz to 2GHz) 9dBm
LO1, LO2 Input DC Voltage .....±0.5V
RF Input Power (0.2GHz to 2GHz).....15dBm
RF Input DC Voltage..... ±0.1V
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Junction Temperature (T_J) ..... 150°C

PIN CONFIGURATION



UH PACKAGE
20-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5540IUH#PBF	LTC5540IUH#TRPBF	5540	20-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LO Input Frequency Range			700 to 1200		MHz
RF Input Frequency Range	Low-Side LO High-Side LO		800 to 1300 600 to 1100		MHz MHz
IF Output Frequency Range	Requires External Matching		5 to 500		MHz
RF Input Return Loss	Z_O = 50Ω, 600MHz to 1300MHz		>12		dB
LO Input Return Loss	Z_O = 50Ω, 700MHz to 1200MHz		>12		dB
IF Output Return Loss	Requires External Matching		>12		dB
LO Input Power	f_{LO} = 700MHz to 1200MHz	–4	0	6	dBm
LO to RF Leakage	f_{LO} = 700MHz to 1200MHz		<–30		dBm
LO to IF Leakage	f_{LO} = 700MHz to 1200MHz		<–37		dBm
LO Switch Isolation	LO1 Selected, 700MHz < f_{LO} < 1200MHz LO2 Selected, 700MHz < f_{LO} < 1200MHz		>50 >47		dB dB
RF to LO Isolation	f_{RF} = 600MHz to 1300MHz		>55		dB
RF to IF Isolation	f_{RF} = 600MHz to 1300MHz		>37		dB

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (Δf = 2MHz for two-tone IIP3 tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

High-Side LO Downmixer Application: RF = 600MHz to 1100MHz, IF = 190MHz, $f_{LO} = f_{RF}+f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 700MHz RF = 900MHz RF = 1100MHz	 6.3	7.6 7.9 7.9		dB dB dB
Conversion Gain Flatness	RF = 900 ±30MHz, LO = 1090MHz, IF=190 ±30MHz		±0.20		dB
Conversion Gain vs Temperature	T_A = –40°C to +85°C, RF = 900MHz		–0.008		dB/°C
Input 3rd Order Intercept	RF = 700MHz RF = 900MHz RF = 1100MHz	 23.4	26.5 25.9 23.8		dBm dBm dBm
SSB Noise Figure	RF = 700MHz RF = 900MHz RF = 1100MHz		10.0 9.9 10.4	 11.7	dB dB dB
SSB Noise Figure Under Blocking	f_{RF} = 900MHz, f_{LO} = 1090MHz, f_{BLOCK} = 800MHz, P_{BLOCK} = 5dBm		16.2		dB
2LO – 2RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/2$)	f_{RF} = 995MHz at –10dBm, f_{LO} = 1090MHz, f_{IF} = 190MHz		–70		dBc
3LO – 3RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/3$)	f_{RF} = 1026.67MHz at –10dBm, f_{LO} = 1090MHz, f_{IF} = 190MHz		–75		dBc
Input 1dB Compression	RF = 900MHz, V_{CCIF} = 3.3V RF = 900MHz, V_{CCIF} = 5V		11 14.5		dBm dBm

Low-Side LO Downmixer Application: RF = 800MHz-1300MHz, IF = 190MHz, $f_{LO} = f_{RF}–f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 900MHz RF = 1100MHz RF = 1300MHz		7.0 7.8 8.0		dB dB dB
Conversion Gain Flatness	RF = 900MHz ±30MHz, LO = 710MHz, IF = 190 ±30MHz		±0.33		dB
Conversion Gain vs Temperature	T_A = –40°C to 85°C, RF = 900MHz		–0.007		dB/°C
Input 3rd Order Intercept	RF = 900MHz RF = 1100MHz RF = 1300MHz		24.4 24.1 23.6		dBm dBm dBm
SSB Noise Figure	RF = 900MHz RF = 1100MHz RF = 1300MHz		10.6 10.5 10.3		dB dB dB
SSB Noise Figure Under Blocking	f_{RF} = 900MHz, f_{LO} = 710MHz, f_{IF} = 190MHz, f_{BLOCK} = 1000MHz, P_{BLOCK} = 5dBm		16.7		dB
2RF – 2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF/2}$)	f_{RF} = 805MHz at –10dBm, f_{LO} = 710MHz, f_{IF} = 190MHz		–61.5		dBc
3RF – 3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF/3}$)	f_{RF} = 773.33MHz at –10dBm, f_{LO} = 710MHz, f_{IF} = 190MHz		–68		dBc
Input 1dB Compression	RF = 900MHz, V_{CCIF} = 3.3V RF = 900MHz, V_{CCIF} = 5V		11 14		dBm dBm

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Requirements (V_{CC}, V_{CCIF})					
V_{CC} Supply Voltage (Pins 6, 8 and 14)		3.1	3.3	3.5	V
V_{CCIF} Supply Voltage (Pins 18 and 19)		3.1	3.3	5.3	V
V_{CC} Supply Current (Pins 6 + 8 + 14) V_{CCIF} Supply Current (Pins 18 + 19) Total Supply Current (V_{CC} + V_{CCIF})			97 96 193	116 120 236	mA mA mA
Total Supply Current – Shutdown	SHDN = High			500	µA
Shutdown Logic Input (SHDN) Low = On, High = Off					
SHDN Input High Voltage (Off)		3			V
SHDN Input Low Voltage (On)				0.3	V
SHDN Input Current	–0.3V to V_{CC} + 0.3V	–20		30	µA
Turn On Time			1		µs
Turn Off Time			1.5		µs
LO Select Logic Input (LOSEL) Low = LO1 Selected, High = LO2 Selected					
LOSEL Input High Voltage		3			V
LOSEL Input Low Voltage				0.3	V
LOSEL Input Current	–0.3V to V_{CC} + 0.3V	–20		30	µA
LO Switching Time			50		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5540 is guaranteed functional over the operating temperature range from –40°C to 85°C.

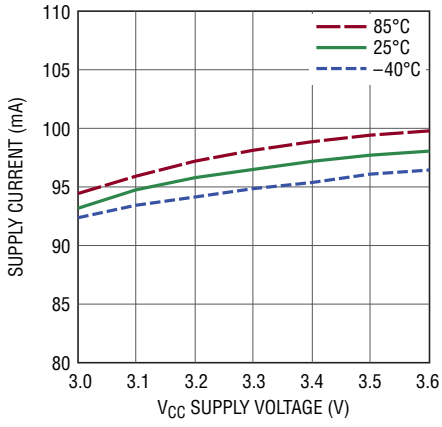
Note 3: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 6dB matching pad on RF input, bandpass filter and 6dB matching pad on the LO input, and no other RF signals applied.

Note 4: LO switch isolation is measured at the IF output port at the IF frequency with f_{LO1} and f_{LO2} offset by 2MHz.

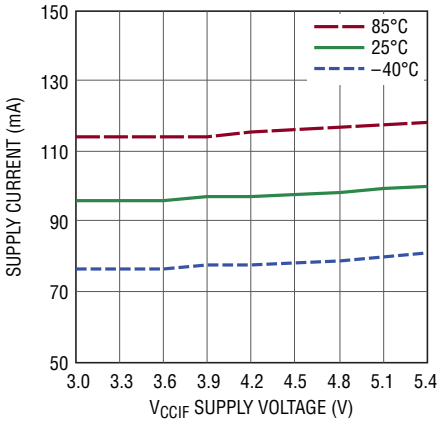
TYPICAL DC PERFORMANCE CHARACTERISTICS

SHDN = Low, Test circuit shown in Figure 1.

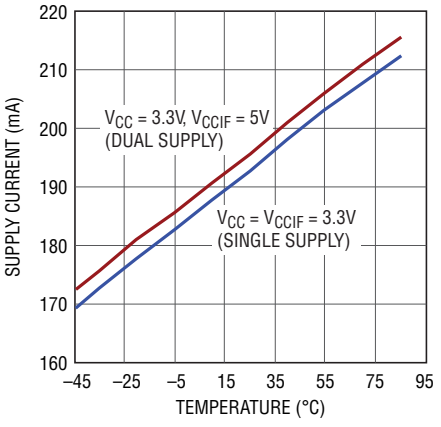
V_{CC} Supply Current vs Supply Voltage (Mixer and LO Switch)



V_{CCIF} Supply Current vs Supply Voltage (IF Amplifier)



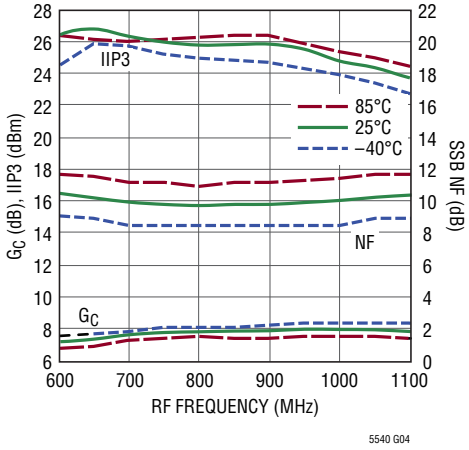
Total Supply Current vs Temperature (V_{CC} + V_{CCIF})



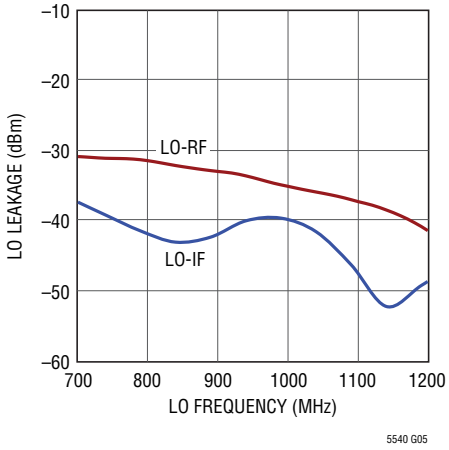
TYPICAL AC PERFORMANCE CHARACTERISTICS High-Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

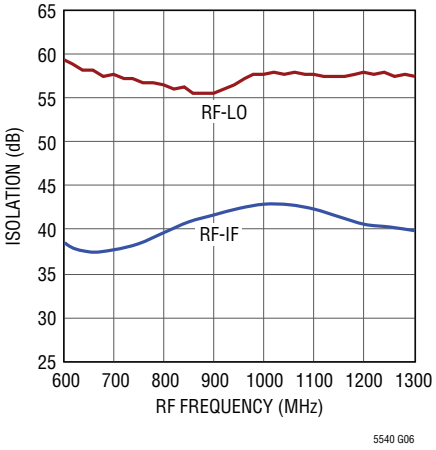
Conversion Gain, IIP3 and NF vs RF Frequency



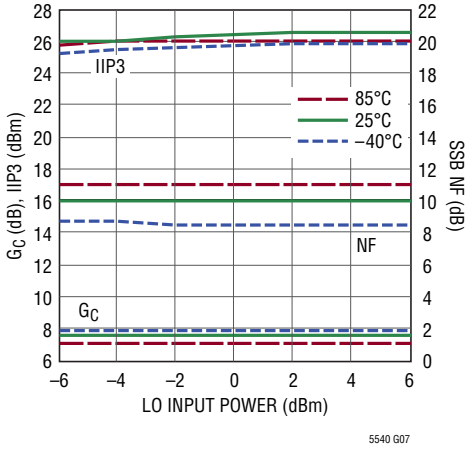
LO Leakage vs LO Frequency



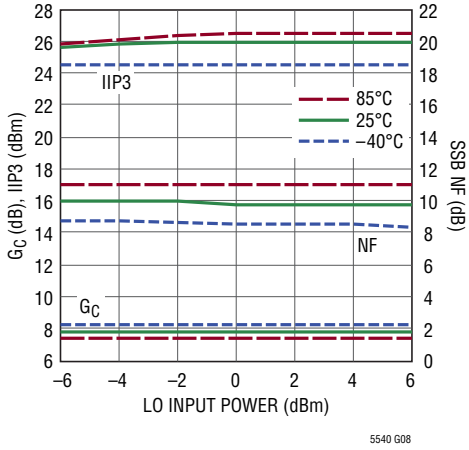
RF Isolation vs RF Frequency



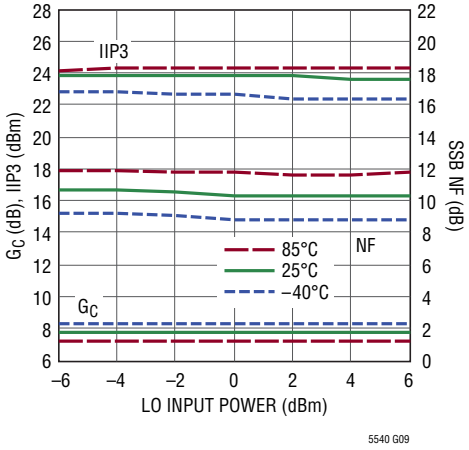
700MHz Conversion Gain, IIP3 and NF vs LO Input Power



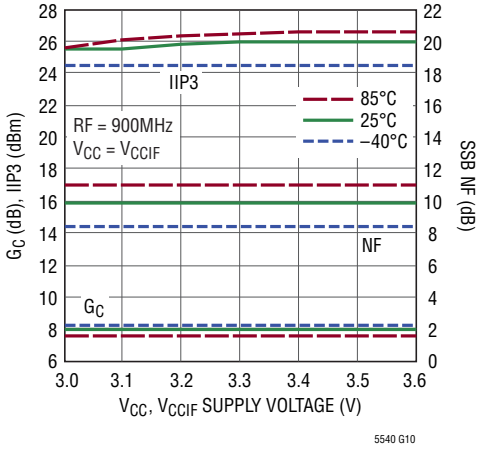
900MHz Conversion Gain, IIP3 and NF vs LO Input Power



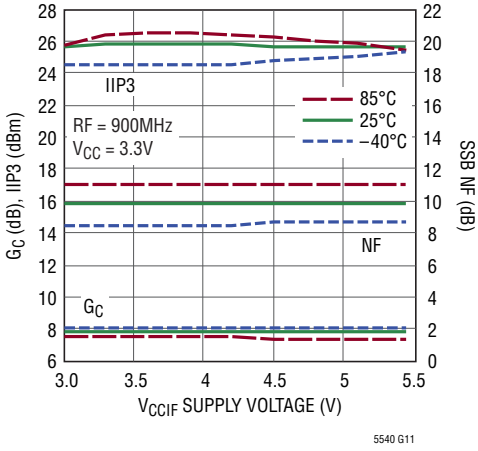
1100MHz Conversion Gain, IIP3 and NF vs LO Input Power



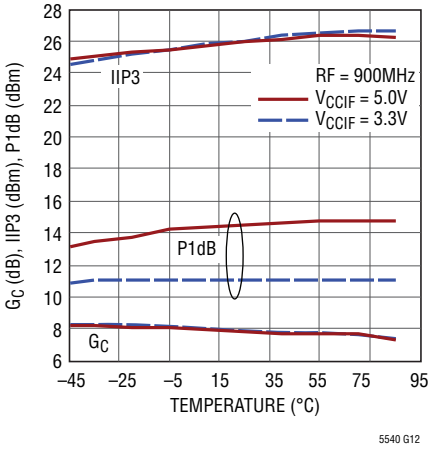
Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)



Conversion Gain, IIP3 and NF vs IF Supply Voltage (Dual Supply)



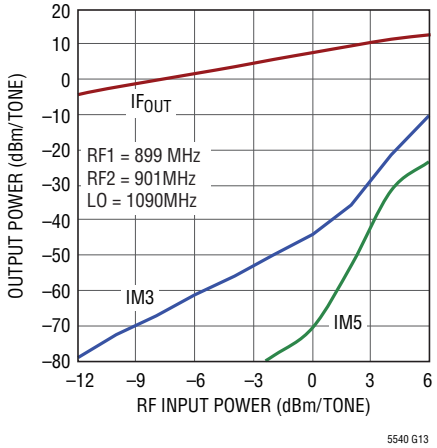
900MHz Conversion Gain, IIP3 and RF Input P1dB vs Temperature



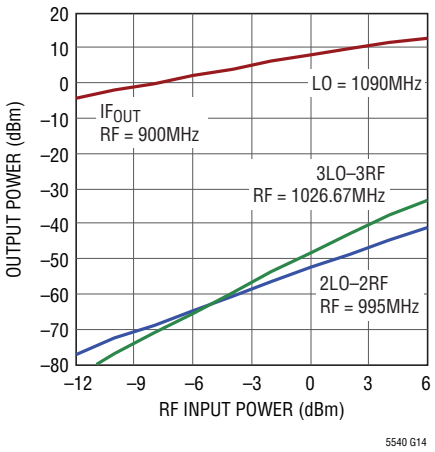
TYPICAL AC PERFORMANCE CHARACTERISTICS High-Side LO (continued)

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

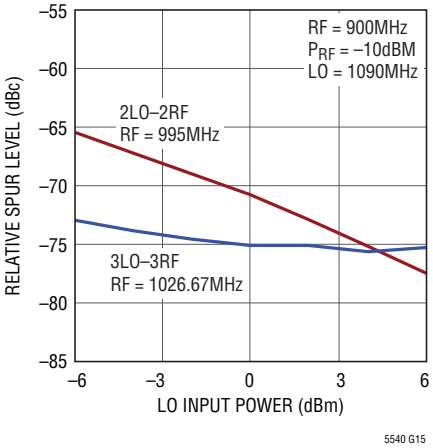
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



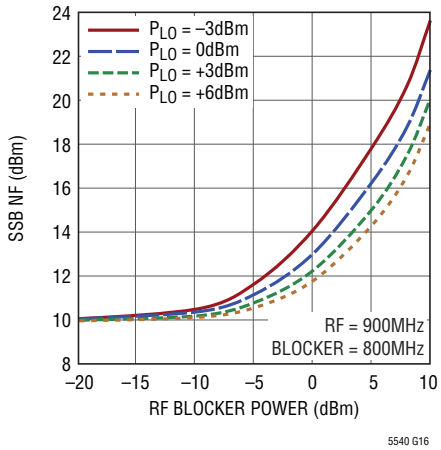
Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



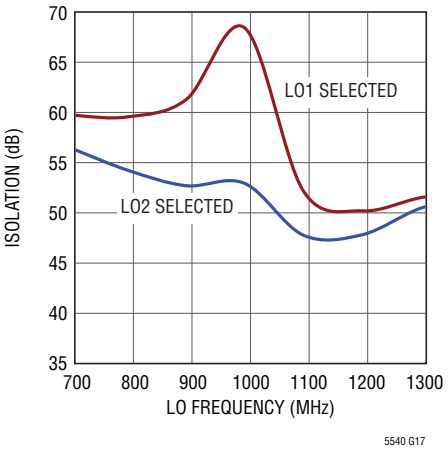
2 × 2 and 3 × 3 Spur Suppression vs LO Power



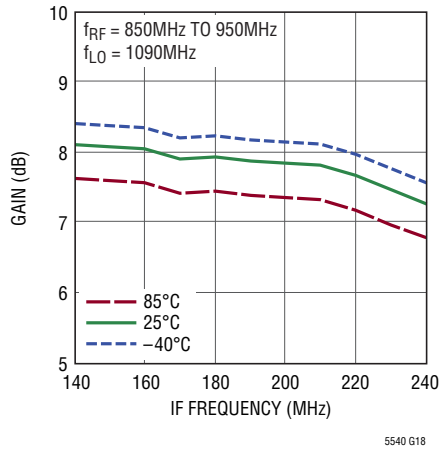
SSB Noise Figure vs RF Blocker Level



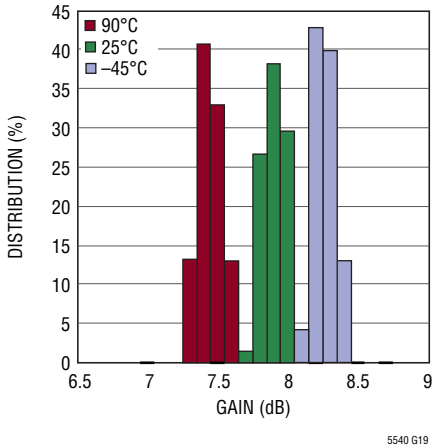
LO Switch Isolation vs LO Frequency



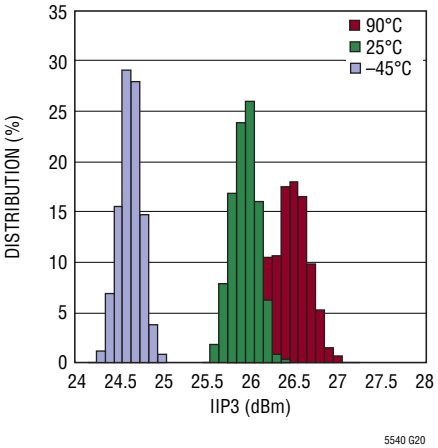
Wideband Conversion Gain vs IF Frequency



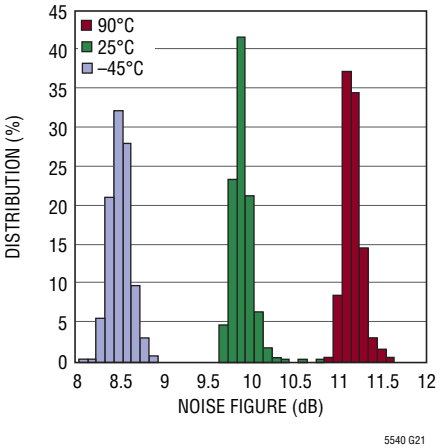
900MHz Conversion Gain Distribution



900MHz IIP3 Distribution



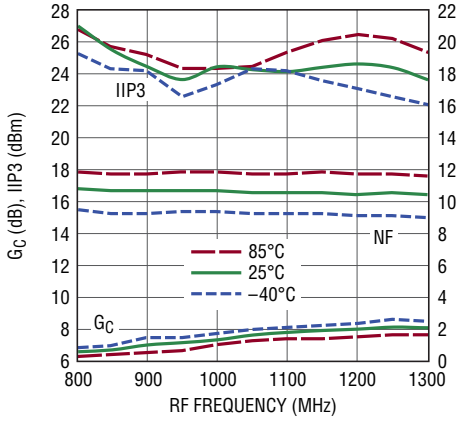
900MHz SSB Noise Figure Distribution



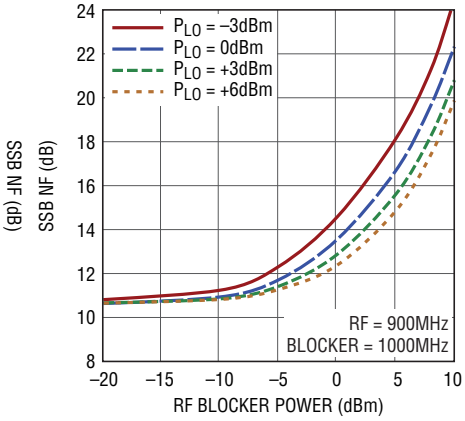
TYPICAL AC PERFORMANCE CHARACTERISTICS Low-Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

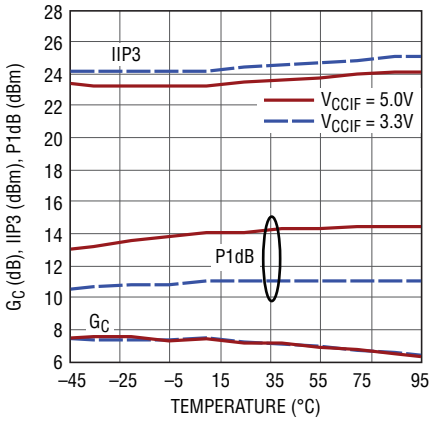
Conversion Gain, IIP3 and NF vs RF Frequency



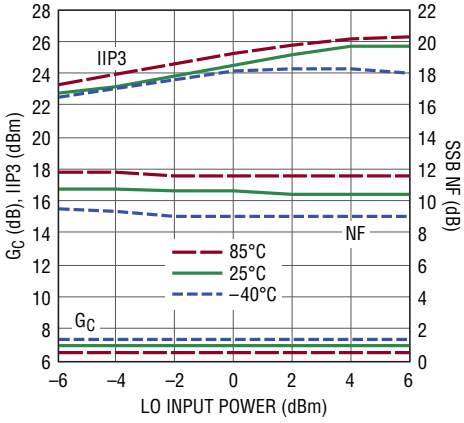
900MHz SSB Noise Figure vs RF Blocker Level



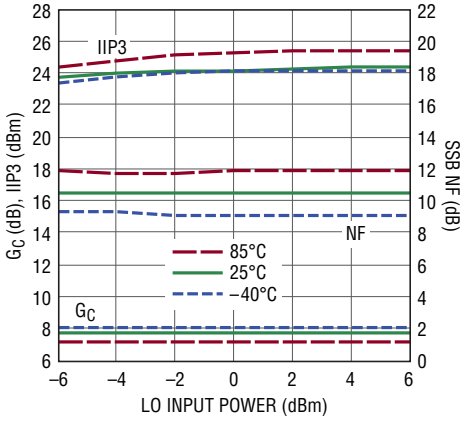
900MHz Conversion Gain, IIP3 and RF Input P1dB vs Temperature



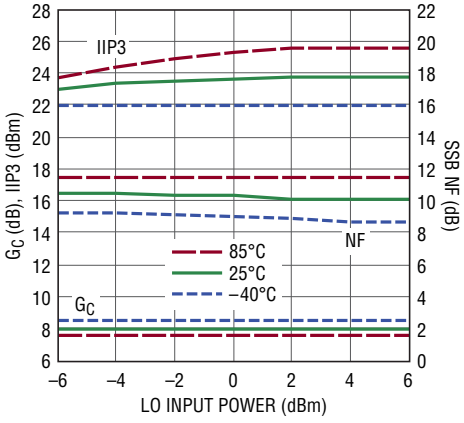
900MHz Conversion Gain, IIP3 and NF vs LO Power



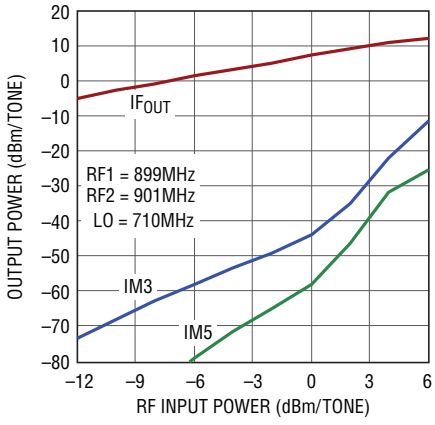
1100MHz Conversion Gain, IIP3 and NF vs LO Power



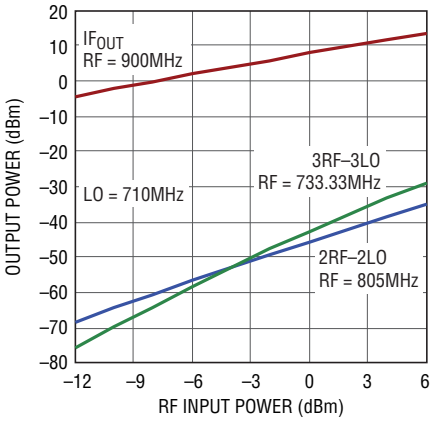
1300MHz Conversion Gain, IIP3 and NF vs LO Power



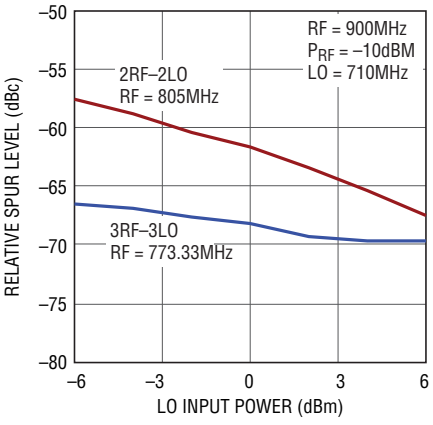
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



2 × 2 and 3 × 3 Spur Suppression vs LO Power



PIN FUNCTIONS

NC (Pin 1): This pin is not connected internally. It can be left floating, connected to ground or to V_{CC}.

RF (Pin 2): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **A series DC-blocking capacitor should be used to avoid damage to the integrated transformer.** The RF input is impedance matched, as long as the selected LO input is driven with a 0dBm ±6dB source between 0.7GHz and 1.2GHz.

CT (Pin 3): RF Transformer Secondary Center-Tap. This pin may require a bypass capacitor to ground. See the Applications Information section. This pin has an internally generated bias voltage of 1.2V. It must be DC-isolated from ground and V_{CC}.

GND (Pins 4, 10, 12, 13, 17, Exposed Pad Pin 21): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

SHDN (Pin 5): Shutdown Pin. When the input voltage is less than 0.3V, the internal circuits supplied through pins 6, 8, 14, 18 and 19 are enabled. When the input voltage is greater than 3V, all circuits are disabled. Typical input current is less than 10µA. This pin must not be allowed to float.

V_{CC2} (Pin 6) and V_{CC1} (Pin 8): Power Supply Pins for the LO Buffer and Bias Circuits. These pins are internally connected and must be externally connected to a regulated 3.3V supply, with bypass capacitors located close to the pin. Typical current consumption is 97mA.

LOBIAS (Pin 7): This Pin Allows Adjustment of the LO Buffer Current. Typical DC voltage is 2.2V.

LOSEL (Pin 9): LO1/LO2 Select Pin. When the input voltage is less than 0.3V, the LO1 port is selected. When the input voltage is greater than 3V, the LO2 port is selected. Typical input current is 11µA for LOSEL = 3.3V. This pin must not be allowed to float.

LO1 (Pin 11) and LO2 (Pin 15): Single-Ended Inputs for the Local Oscillators. These pins are internally biased at 0V and require external DC blocking capacitors. Both inputs are internally matched to 50Ω, even when the chip is disabled (SHDN = high).

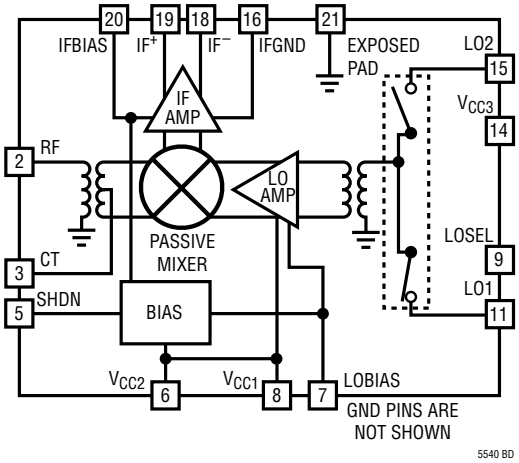
V_{CC3} (Pin 14): Power Supply Pin for the LO Switch. This pin must be connected to a regulated 3.3V supply and bypassed to ground with a capacitor near the pin. Typical DC current consumption is less than 100µA.

IFGND (Pin 16): DC Ground Return for the IF Amplifier. This pin must be connected to ground to complete the IF amplifier's DC current path. Typical DC current is 96mA.

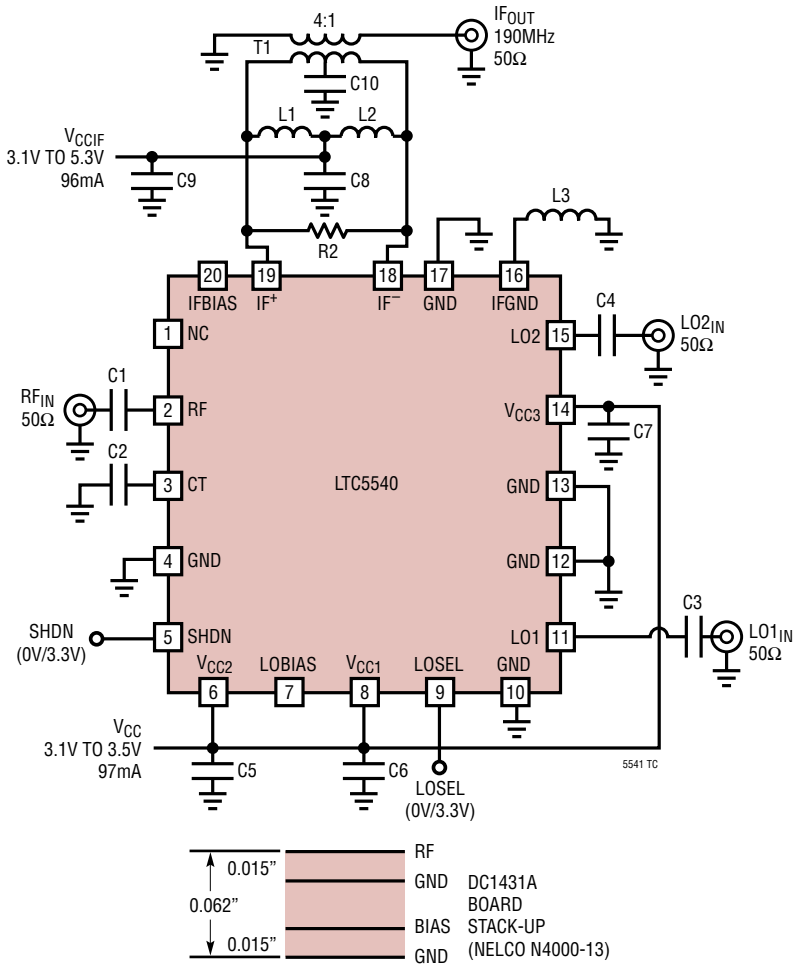
IF^- (Pin 18) and IF^+ (Pin 19): Open-Collector Differential Outputs for the IF Amplifier. These pins must be connected to a DC supply through impedance matching inductors, or a transformer center-tap. Typical DC current consumption is 48mA into each pin.

IFBIAS (Pin 20): This Pin Allows Adjustment of the IF Amp Current. Typical DC voltage is 2.1V.

BLOCK DIAGRAM



TEST CIRCUIT



L1, L2 vs IF Frequencies	
IF (MHz)	**L1, L2 (nH)**
140	270
190	150
240	100
380	33
450	22

REF DES	VALUE	SIZE	COMMENTS
C3, C4	100pF	0402	AVX
C6, C7, C8	22pF	0402	AVX
C5, C9	1µF	0603	AVX
C10	1000pF	0402	AVX
L1, L2	150nH	0603	Coilcraft 0603CS
L3	30nH	0603	Coilcraft 0603CS
R2	2.05k	0402	
T1 (Alternate)	TC4-1W-7ALN+ (WBC4-6TLB)		Mini-Circuits (Coilcraft)
HIGH-SIDE LO			
C1	5.6pF	0402	AVX
C2	1.5pF	0402	AVX
LOW-SIDE LO			
C1, C2	100pF	0402	AVX

Figure 1. Standard Downmixer Test Circuit Schematic (190MHz IF)

APPLICATIONS INFORMATION

Introduction

The LTC5540 consists of a high linearity passive double-balanced mixer core, IF buffer amplifier, high speed single-pole double-throw (SPDT) LO switch, LO buffer amplifier and bias/enable circuits. See Pin Functions section for a description of each pin function. The RF and LO inputs are single-ended. The IF output is differential. Low-side or high-side LO injection can be used. The evaluation circuit, shown in Figure 1, utilizes bandpass IF output matching and an IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

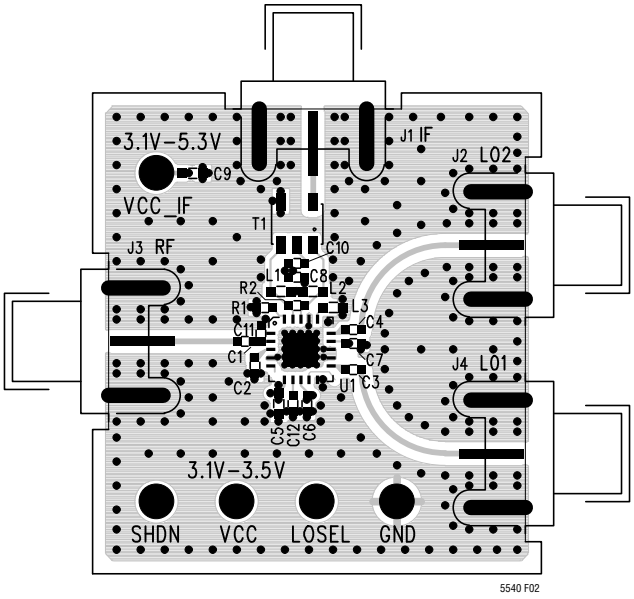


Figure 2. Evaluation Board Layout

RF Input

The mixer's RF input, shown in Figure 3, is connected to the primary winding of an integrated transformer. A 50Ω match is realized when a series capacitor, C1, is connected to the RF input. C1 is also needed for DC blocking if the RF source has DC voltage present, since the primary side of the RF transformer is DC-grounded internally. The DC resistance of the primary is approximately 5Ω.

The secondary winding of the RF transformer is internally connected to the passive mixer. The center-tap of the transformer secondary is connected to pin 3 (CT) to allow the connection of bypass capacitor, C2. The value of C2 is LO frequency-dependent. C2 should be located within 2mm of pin 3 for proper high-frequency decoupling. The nominal DC voltage on the CT pin is 1.2V.

For the RF input to be properly matched, the selected LO input must be driven. The values of C1 and C2 can be chosen to optimize the performance for high-side or low-side LO (see the table in Figure 1). For high-side applications, a broadband input match is realized with C1 = 5.6pF. The measured input return loss is shown in Figure 4 for LO frequencies of 700MHz, 1090MHz and 1200MHz. As shown in Figure 4, the RF input impedance is dependent on LO frequency, although a single value of C1 is adequate to cover a wide RF range.

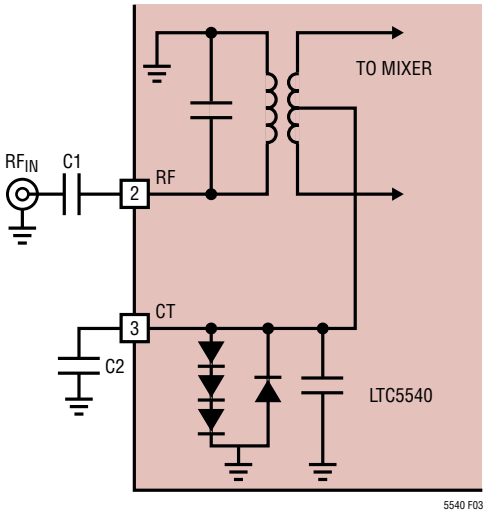


Figure 3. RF Input Schematic

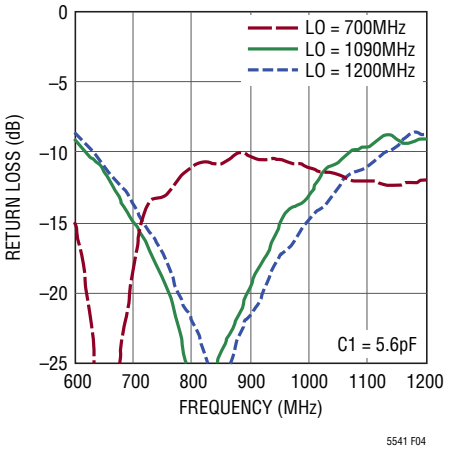


Figure 4. RF Input Return Loss

APPLICATIONS INFORMATION

The RF input impedance and input reflection coefficient, versus RF frequency, is listed in Table 1. The reference plane for this data is pin 2 of the IC, with no external matching, and the LO is driven at 1090MHz.

Table 1. RF Input Impedance and S11 (at Pin 2, No External Matching, LO Input Driven at 1090MHz)

RF (GHz)	RF INPUT IMPEDANCE	S11	
		MAG	ANGLE
0.4	14.7 + j19.7	0.6	133.8
0.5	18.1 + j24.4	0.6	122.9
0.6	23.1 + j27.7	0.5	113.4
0.7	29.9 + j30.6	0.4	102.3
0.8	39.0 + j32.9	0.4	88.2
0.9	52.8 + j31.7	0.3	67.8
1.0	67.3 + j15.4	0.2	34.3
1.1	55.2 – j13.4	0.1	–61.4
1.2	36.2 – j11.2	0.2	–133.5
1.3	31.2 – j4.8	0.2	–162.4
1.4	29.8 – j0.2	0.3	–179.2

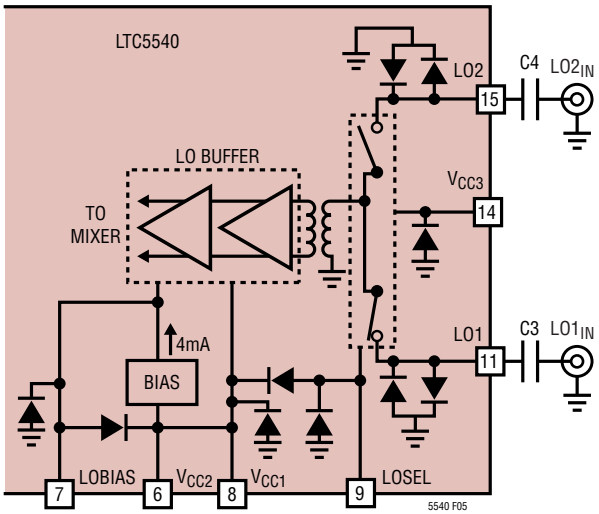


Figure 5. LO Input Schematic

LO Inputs

The mixer's LO input circuit, shown in Figure 5, consists of an integrated SPDT switch, a balun transformer, and a two-stage high-speed limiting differential amplifier to drive the mixer core. The LTC5540's LO amplifiers are optimized for the 0.7GHz to 1.2GHz LO frequency range. LO frequencies above or below this frequency range may be used with degraded performance.

The LO switch is designed for high isolation and fast (<50ns) switching. This allows the use of two active synthesizers in frequency-hopping applications. If only one synthesizer is used, then the unused LO input may be grounded. The LO switch is powered by V_{CC3} (Pin 14) and controlled by the LOSEL logic input (Pin 9). The LO1 and LO2 inputs are always 50Ω-matched when V_{CC} is applied to the chip, even when the chip is shutdown. The DC resistance of the selected LO input is approximately 23Ω and the unselected input is approximately 50Ω. A logic table for the LO switch is shown in Table 2. Measured LO input return loss is shown in Figure 6.

Table 2. LO Switch Logic Table

LOSEL	ACTIVE LO INPUT
Low	LO1
High	LO2

The LO amplifiers are powered by V_{CC1} and V_{CC2} (pin 8 and pin 6). When the chip is enabled (SHDN = low), the internal bias circuit provides a regulated 4mA current to the amplifier's bias input, which in turn causes the amplifiers to draw approximately 80mA of DC current. This 4mA reference is also connected to LOBIAS (Pin 7) to allow modification of the amplifier's DC bias current for special applications. The recommended application circuits require no LO amplifier bias modification, so this pin should be left open-circuited.

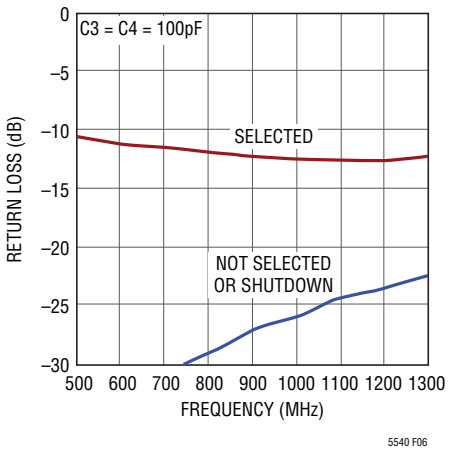


Figure 6. LO Input Return loss

APPLICATIONS INFORMATION

The nominal LO input level is 0dBm although the limiting amplifiers will deliver excellent performance over a ±6dBm input power range. LO input power greater than 6dBm may cause conduction of the internal ESD diodes. Series capacitors C3 and C4 optimize the input match and provide DC blocking.

The LO1 input impedance and input reflection coefficient, versus frequency, is shown in Table 3. The LO2 port is identical due to the symmetric device layout and packaging.

Table 3. LO1 Input Impedance vs Frequency (at Pin 11, No External Matching, LOSEL = Low)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
0.6	48.9 + j30.6	0.3	74.9
0.7	62.8 + j29.4	0.28	51.9
0.8	78.0 + j17.2	0.25	23.9
0.9	80.4 – j4.55	0.24	–6.5
1.0	68.3 – j20.5	0.23	–38.4
1.1	54.6 – j24.1	0.23	–66.3
1.2	44.7 – j22.3	0.24	–90.1
1.3	38.1 – j18.7	0.25	–110.5
1.4	33.8 – j14.9	0.26	–127.3

IF Output

The IF amplifier, shown in Figure 7, has differential open-collector outputs (IF^+ and IF^-), a DC ground return pin (IFGND), and a pin for modifying the internal bias (IFBIAS). The IF outputs must be biased at the supply voltage (V_{CCIF}), which is applied through matching inductors L1 and L2. Alternatively, the IF outputs can be biased through the center tap of a transformer. Each IF output pin draws approximately 48mA of DC supply current (96mA total). Resistor R2 is used to improve the impedance match.

IFGND (pin 16) must be grounded or the amplifier will not draw DC current. Grounding through inductor L3 improves LO-IF and RF-IF leakage performance but is otherwise not necessary. High DC resistance in L3 will reduce the IF amplifier supply current, which will degrade RF performance.

For optimum single-ended performance, the differential IF outputs must be combined through an external IF transformer or discrete IF balun circuit. The evaluation board (see Figures 1 and 2) uses a 4:1 ratio IF transformer for impedance transformation and differential to single-ended transformation. It is also possible to eliminate the IF transformer and drive differential filters or amplifiers directly.

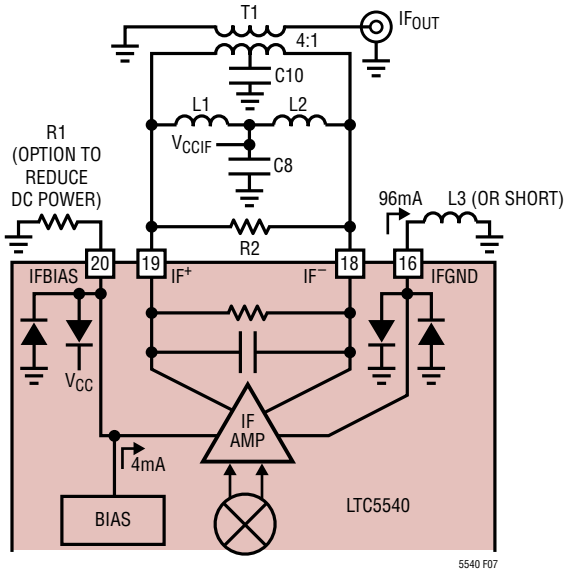


Figure 7. IF Amplifier Schematic with Bandpass Match

The IF output impedance can be modeled as 320Ω in parallel with 2.3pF at IF frequencies. An equivalent small-signal model (including bondwire inductance) is shown in Figure 8. Frequency-dependent differential IF output impedance is listed in Table 4. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics.

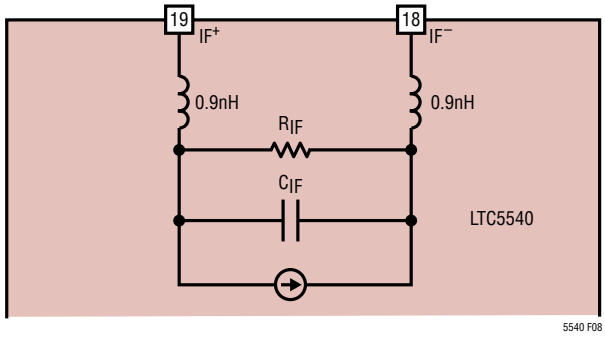


Figure 8. IF Output Small-Signal Model

APPLICATIONS INFORMATION

Bandpass IF Matching

The IF output can be matched for IF frequencies as low as 70MHz or as high as 500MHz using the bandpass IF matching shown in Figure 1 and Figure 7. L1 and L2 resonate with the internal IF output capacitance at the desired IF frequency. The value of L1, L2 is calculated as follows:

$$L1 = L2 = 1/[(2\,\pi\,f_{IF})^2 \bullet 2 \bullet C_{IF}]$$

where C_{IF} is the internal IF capacitance (listed in Table 4).

Values of L1 and L2 are tabulated in Figure 1 for various IF frequencies. For IF frequencies below 70MHz, the values of L1, L2 become unreasonably high and the lowpass topology shown in Figure 9 is preferred. Measured IF output return loss for bandpass IF matching is plotted in Figure 10.

Table 4. IF Output Impedance vs Frequency

FREQUENCY (MHz)	DIFFERENTIAL OUTPUT IMPEDANCE (R_{IF} || X_{IF} (C_{IF}))
70	674 || -j1137 (2pF)
140	628 || -j569 (2pF)
190	606 || -j419 (2pF)
240	584 || -j316 (2.1pF)
300	561 || -j253 (2.1pF)
380	532 || -j182 (2.3pF)
450	511 || -j154 (2.3pF)

Lowpass IF Matching

An alternative IF matching network shown in Figure 9 uses a lowpass topology, which provides excellent RF to IF and LO to IF isolation. V_{CCIF} is supplied through the center tap of the 4:1 transformer. A lowpass impedance transformation is realized by shunt elements R2 and C13 (in parallel with the internal R_{IF} and C_{IF}), and series inductors L1 and L2. Resistor R2 is used to reduce the IF output resistance, or it can be deleted for the highest conversion gain. The final impedance transformation to 50Ω is realized by transformer T1. The matching element values shown in Figure 9 are optimized for a wideband 30MHz-150MHz IF match. The demo board (see Figure 2) has been laid out to accommodate this matching topology with very few modifications.

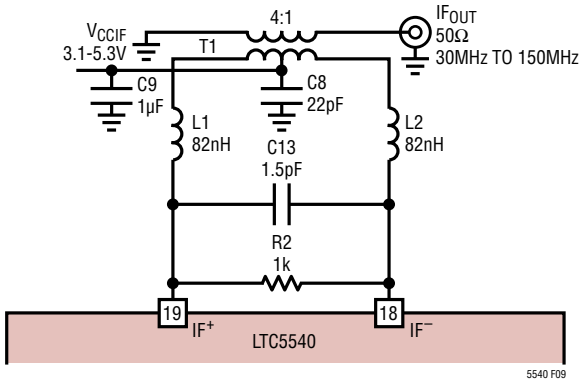


Figure 9. IF Output with Lowpass Matching

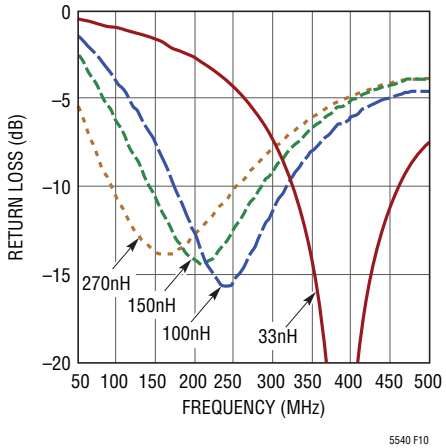


Figure 10. IF Output Return Loss - Bandpass Matching

IF Amplifier Bias

The IF amplifier delivers excellent performance with V_{CCIF} = 3.3V, which allows the V_{CC} and V_{CCIF} supplies to be common. With V_{CCIF} increased to 5V, the RF input P1dB increases by almost 3dB, at the expense of higher power consumption. Mixer performance at 900MHz is shown in Table 5 with V_{CCIF} = 3.3V and 5V. For the highest conversion gain, high-Q wire-wound chip inductors are recommended for L1 and L2, especially when using V_{CCIF} = 3.3V. Low-cost multilayer chip inductors may be substituted, with a slight reduction in conversion gain.

Table 5. Performance Comparison with V_{CCIF} = 3.3V and 5V (RF = 900MHz, High-Side LO, IF = 190MHz)

V_{CCIF}	I_{CCIF}	G_C	P1dB	IIP3	NF
3.3V	96	7.9	11	25.9	9.9
5V	99	7.9	14.5	25.9	10.0

APPLICATIONS INFORMATION

The IFBIAS pin (pin 20) is available for reducing the DC current consumption of the IF amplifier, at the expense of IIP3. This pin should be left open-circuited for optimum performance. The internal bias circuit produces a 4mA reference for the IF amplifier, which causes the amplifier to draw approximately 96mA. If resistor R1 is connected to pin 20 as shown in Figure 7, a portion of the reference current can be shunted to ground, resulting in reduced IF amplifier current. For example, R1 = 1kΩ will shunt away 1.5mA from pin 20 and the IF amplifier current will be reduced by 38% to approximately 59mA. The nominal, open-circuit DC voltage at pin 20 is 2.1V. Table 6 lists RF performance at 900MHz versus IF amplifier current.

Table 6. Mixer Performance with Reduced IF Amplifier Current (RF = 900MHz, High-Side LO, IF = 190MHz, V_{CC} = V_{CCIF} = 3.3V)

R1 (kΩ)	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	96	7.9	25.9	11.0	9.9
4.7	86	7.7	25.3	11.1	9.9
2.2	77	7.6	24.7	11.3	9.9
1	59	7.3	23.0	10.8	9.8

(RF = 900MHz, Low-Side LO, IF = 190MHz, V_{CC} = V_{CCIF} = 3.3V)

R1 (kΩ)	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	96	7.0	24.4	11.0	10.6
4.7	86	6.9	23.4	11.0	10.6
2.2	77	6.8	23.2	11.1	10.6
1	59	6.3	22.4	10.5	10.5

Shutdown Interface

Figure 11 shows a simplified schematic of the SHDN pin interface. To disable the chip, the SHDN voltage must be higher than 3.0V. If the shutdown function is not required, the SHDN pin should be connected directly to GND. The voltage at the SHDN pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

The SHDN pin must be pulled high or low. If left floating, then the on/off state of the IC will be indeterminate. If a three-state condition can exist at the SHDN pin, then a pull-up or pull-down resistor must be used.

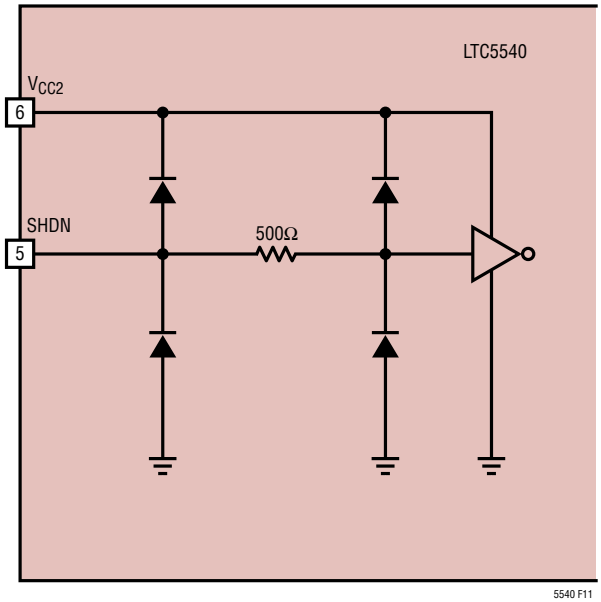


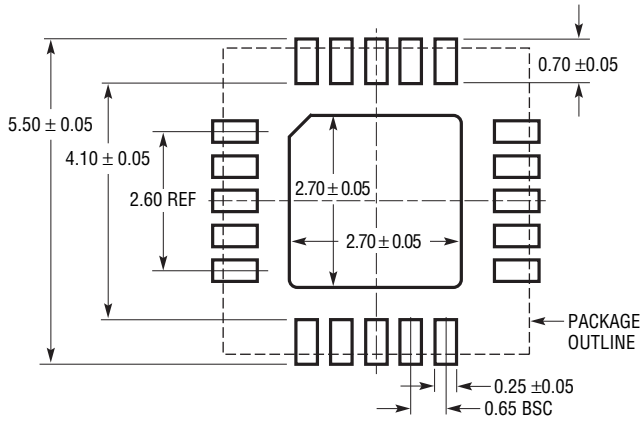
Figure 11. Shutdown Input Circuit

Supply Voltage Ramping

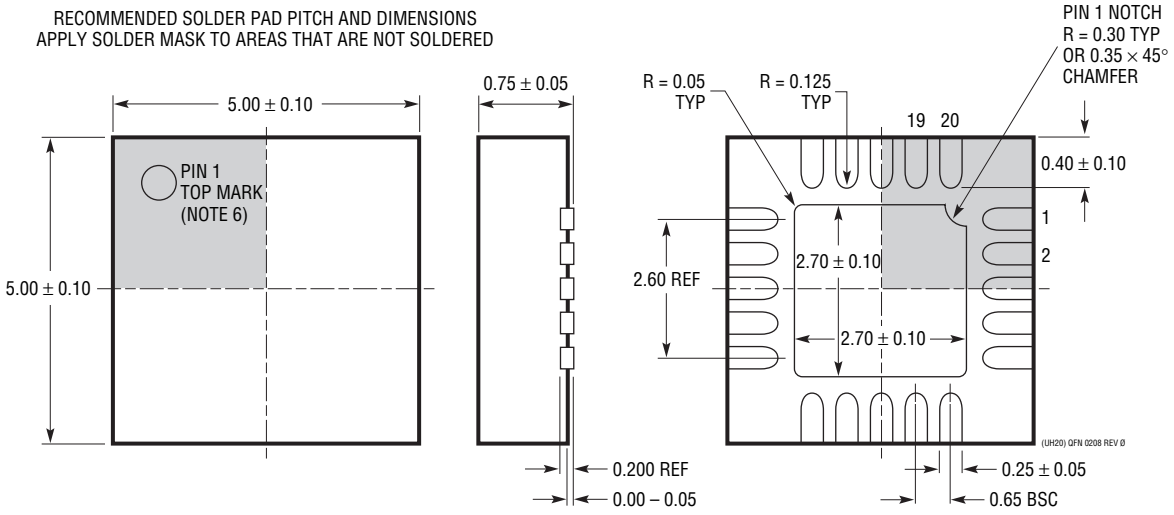
Fast ramping of the supply voltage can cause a current glitch in the internet ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

PACKAGE DESCRIPTION

UH Package
20-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1818 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE