300MHz to 3.5GHz Ultra-High Dynamic Range Downconverting Mixer

FEATURES

- **+36dBm Input IP3**
- **2.4dB Conversion Gain**
- **Low Noise Figure: <10dB**
- **+18dBm Ultra High Input P1dB**
- **670mW Power Consumption**
- **2.5V to 3.6V Operation**
- **50Ω Single-Ended RF and LO Inputs**
- 0dBm LO Drive Level
- Low Power Mode
- –40°C to 105°C Operation (T_C)
- Small Solution Size
- Enable Pin
- 16-Lead (4mm × 4mm) QFN Package

APPLICATIONS

- GSM, LTE, LTE-Advanced Basestations
- Repeaters
- DPD Observation Receiver
- Public Safety Radios, Military and Defense
- Avionics Radios and TCAS Transponders
- Active Phased-Array Antennas
- White-Space Radio Receiver

DESCRIPTION

The LTC®5551 is a 2.5V to 3.6V mixer optimized for RF downconverting mixer applications that require very high dynamic range. **The LTC5551 covers the 300MHz to 3.5GHz RF Frequency range with LO frequency range of 200MHz to 3.5GHz.** The LTC5551 provides very high IIP3 and P1dB with low power consumption. A typical application is a basestation receiver covering 700MHz to 2.7GHz frequency range. The RF input can be matched for a wide range of frequencies and the IF is usable up to 1GHz.

A low power mode is activated by pulling the ISEL pin high, reducing the power consumption by about 1/3, however, with a corresponding reduction in IIP3 to approximately +29dBm. The mixer can also be turned on or off by using the EN pin.

The LTC5551's high level of integration minimizes the total solution cost, board space and system level variation, while providing the highest dynamic range for demanding receiver applications.

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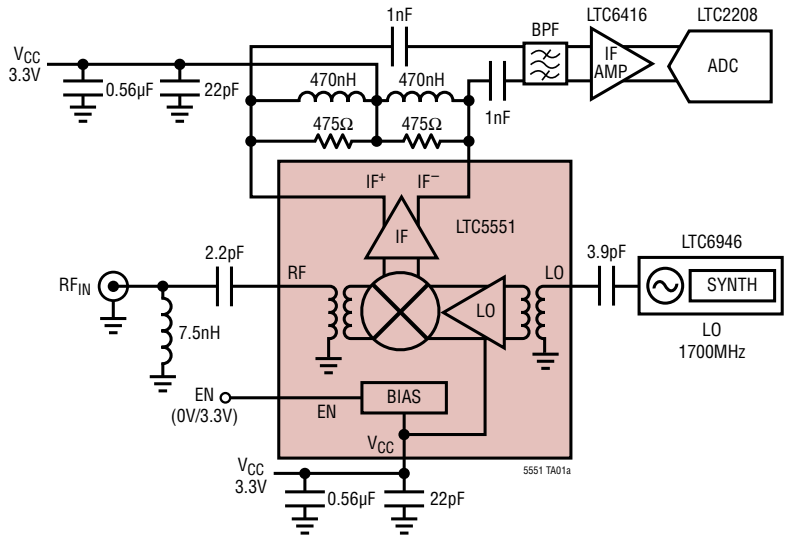
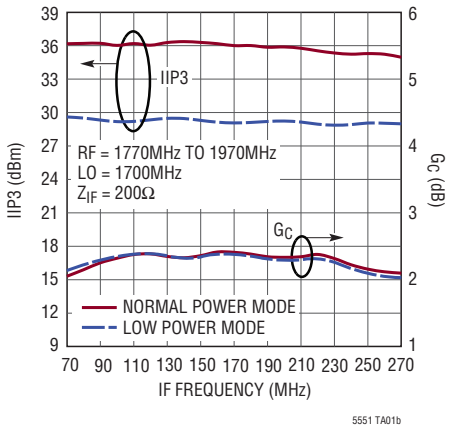
TYPICAL APPLICATION

Wideband Receiver



Mixer Conversion Gain and IIP3 vs IF Frequency (Low-Side LO)



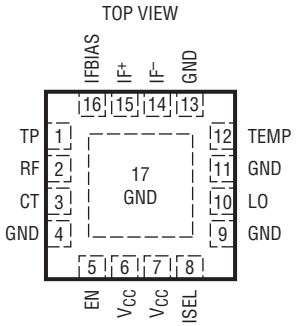
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}, IF^+, IF^-) 4V
Enable Input Voltage (EN) ..... –0.3V to V_{CC} + 0.3V
Power Select Voltage (ISEL) ..... –0.3V to V_{CC} + 0.3V
LO Input Power (0.2GHz to 3.5GHz) ..... +10dBm
LO Input DC Voltage ..... ±0.1V
RF Input Power (0.3GHz to 3.5GHz) ..... +20dBm
RF Input DC Voltage ..... ±0.1V
TEMP Diode Continuous DC Input Current 10mA
TEMP Diode Input Voltage ..... ±1V
IFBIAS Voltage 2.5V
Operating Temperature Range (T_C) ..... –40°C to 105°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (T_J) ..... 150°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTC5551.

PIN CONFIGURATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 6°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5551IUF#PBF	LTC5551IUF#TRPBF	5551	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, ISEL = Low, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LO Input Frequency Range		●		200 to 3500		MHz
RF Input Frequency Range		●		300 to 3500		MHz
IF Output Frequency Range	Requires External Matching			5 to 1000		MHz
RF Input Return Loss	Z_O = 50Ω, 1100MHz to 2700MHz, X1 = 7.5nH, C1 = 2.2pF			>12		dB
LO Input Return Loss	Z_O = 50Ω, 1000MHz to 3500MHz, C2 = 3.9pF			>12		dB
IF Output Impedance	Differential at 153MHz			950Ω||1.2pF		R||C
LO Input Power	LO = 200MHz to 3500MHz		–6	0	6	dBm
LO to RF Leakage	LO = 200MHz to 3500MHz			< –25		dBm
LO to IF Leakage	LO = 200MHz to 3500MHz			< –21		dBm
RF to LO Isolation	RF = 300MHz to 3500MHz			>55		dB
RF to IF Isolation	RF = 300MHz to 3500MHz			>23		dB

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for 2-tone tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)

0.3GHz to 3.5GHz Downmixer Application: IF = 153MHz, ISEL = Low, unless otherwise noted. (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Conversion Gain	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			3.2 2.8 2.4 1.7		dB dB dB dB
Conversion Gain Flatness	RF = 1870MHz ±100MHz, LO = 1700MHz, IF = 170 ±100MHz			±0.2		dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, RF = 1950MHz, Low Side LO			–0.013		dB/°C
2-Tone Input 3rd Order Intercept (Δf = 2MHz)	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			33.2 35.2 35.5 38.1		dBm dBm dBm dBm
2-Tone Input 2nd Order Intercept (Δf = 154MHz = f_{IM2})	RF = 400MHz (477MHz/323MHz), LO = 553MHz RF = 850MHz (927MHz/773MHz), LO = 1053MHz RF = 1950MHz (2027MHz/1873MHz), LO = 1797MHz RF = 2700MHz (2777MHz/2623MHz), LO = 2547MHz			65.8 68.2 58.4 57.1		dBm dBm dBm dBm
SSB Noise Figure	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			10.6 9.1 9.7 10.9		dB dB dB dB
SSB Noise Figure Under Blocking	RF = 850MHz, High Side LO, 750MHz Blocker at 5dBm RF = 1950MHz, Low Side LO, 2050MHz Blocker at 5dBm			16.5 16.9		dB dB
1/2 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	850MHz: RF = 926.5MHz at –3dBm, LO = 1003MHz 1950MHz: RF = 1873.5MHz at –3dBm, LO = 1797MHz			–66 –68		dBc dBc
1/3 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	850MHz: RF = 952MHz at –3dBm, LO = 1003MHz 1950MHz: RF = 1848MHz at –3dBm, LO = 1797MHz			–97 –93		dBc dBc
Input 1dB Compression	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			17.1 17.8 18.0 18.7		dBm dBm dBm dBm

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, EN = High, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for 2-tone tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)

Low Power Mode, 0.3GHz to 3.5GHz Downmixer Application: IF = 153MHz, ISEL = High (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Conversion Gain	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			3.0 2.7 2.4 1.7		dB dB dB dB
Input 3rd Order Intercept	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			27.3 28.0 29.3 29.7		dBm dBm dBm dBm
SSB Noise Figure	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			9.8 8.2 8.3 9.2		dB dB dB dB
Input 1dB Compression	RF = 400MHz, High Side LO RF = 850MHz, High Side LO RF = 1950MHz, Low Side LO RF = 2700MHz, Low Side LO			14.8 16.2 16.7 17.7		dBm dBm dBm dBm

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, ISEL = Low, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Requirements						
Supply Voltage (V_{CC})		●	2.5	3.3	3.6	VDC
Supply Current (ISEL = Low)	EN = High, No LO Applied EN = High, with LO Applied EN = Low			148 204	 234 100	mA mA µA
Supply Current – Low Power Mode (ISEL = High)	EN = High, No LO Applied EN = High, with LO Applied EN = Low			128 142	 100	mA mA µA
Enable Logic Input (EN)						
Input High Voltage (On)		●	1.2			VDC
Input Low Voltage (Off)		●			0.3	VDC
Input Current	–0.3V to V_{CC} + 0.3V		–30		100	µA
Turn On Time	LO Applied			0.4		µs
Turn Off Time	LO Applied			0.5		µs
Power Select Logic Input (ISEL)						
Input High Voltage (Low Power Mode)		●	1.2			VDC
Input Low Voltage (High Power Mode)		●			0.3	VDC
Input Current	–0.3V to V_{CC} + 0.3V		–30		100	µA
Temperature Sensing Diode (TEMP)						
DC Voltage at T_J = 25°C	I_{IN} = 10µA I_{IN} = 80µA			726 783		mV mV
Voltage Temperature Coefficient	I_{IN} = 10µA I_{IN} = 80µA	● ●		–1.72 –1.53		mV/°C mV/°C

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

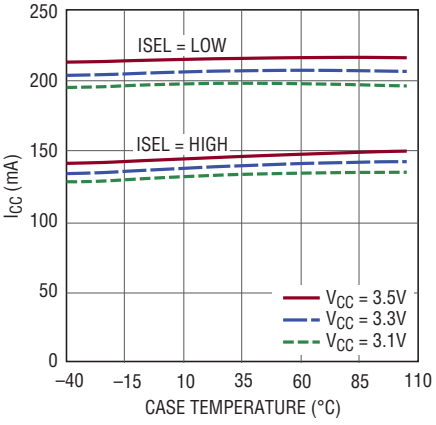
Note 2: The LTC5551 is guaranteed functional over the –40°C to 105°C case temperature range.

Note 3: SSB Noise Figure measurements performed with a small-signal noise source, bandpass filter and 6dB matching pad on RF input, bandpass filter and 6dB matching pad on the LO input, bandpass filter on the IF output and no other RF signals applied.

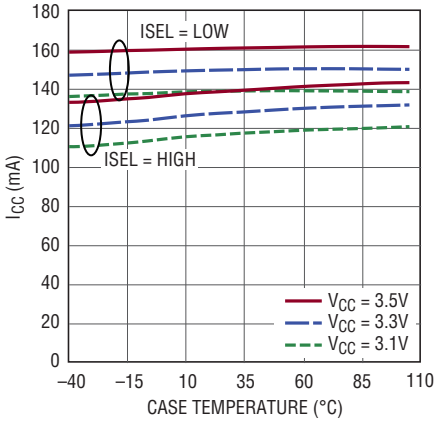
TYPICAL DC PERFORMANCE CHARACTERISTICS

EN = High, Test circuit shown in Figure 1.

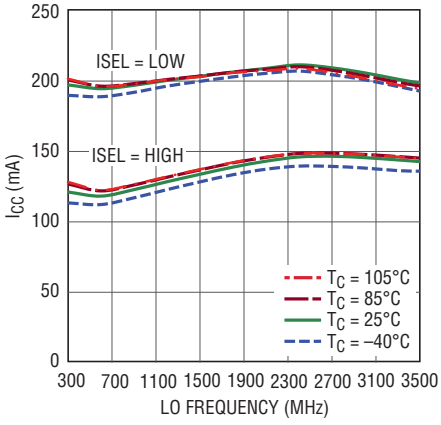
Supply Current vs Supply Voltage, LO = 1800MHz at 0dBm



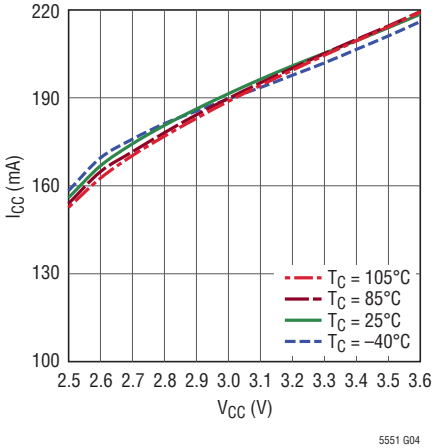
Supply Current vs Supply Voltage, No LO Applied



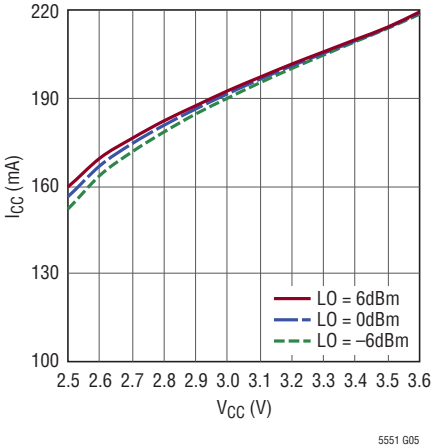
Supply Current vs LO Frequency (P_{LO} = 0dBm)



Supply Current vs V_{CC} LO = 1800MHz at 0dBm



Supply Current vs V_{CC} LO = 1800MHz at T_C = 25°C

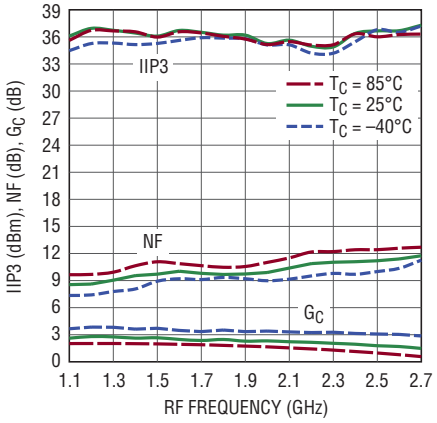


TYPICAL AC PERFORMANCE CHARACTERISTICS

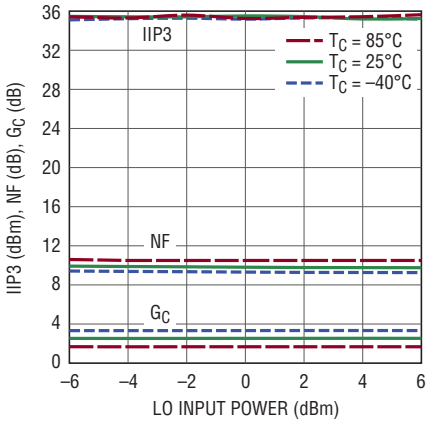
1100MHz to 2700MHz application.

V_{CC} = 3.3V, EN = High, ISEL = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted. Test circuit shown in Figure 1.

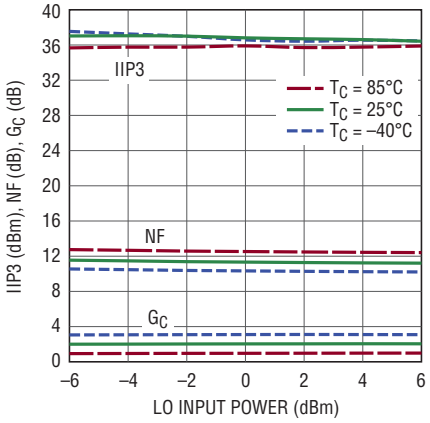
Conversion Gain, IIP3 and NF vs RF Frequency (Low Side LO)



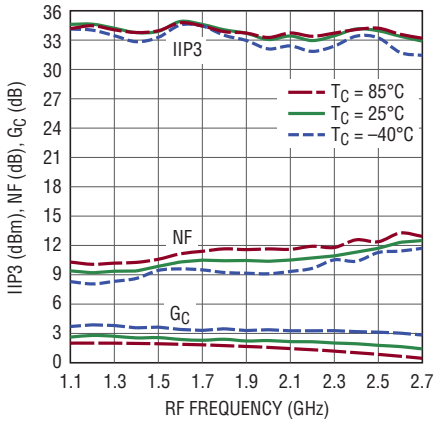
1950MHz Conversion Gain, IIP3 and NF vs LO Power (Low Side LO)



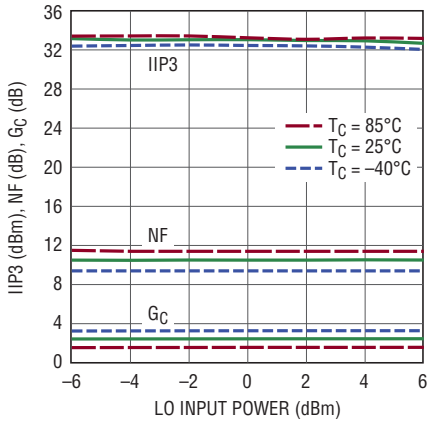
2550MHz Conversion Gain, IIP3 and NF vs LO Power (Low Side LO)



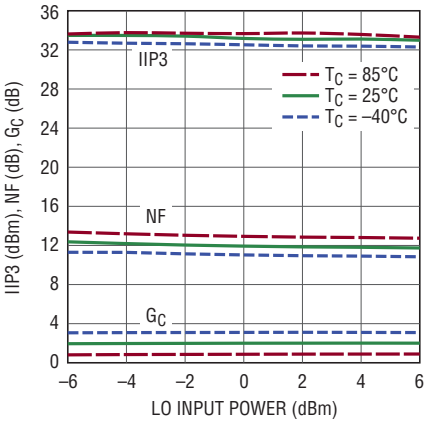
Conversion Gain, IIP3 and NF vs RF Frequency (High Side LO)



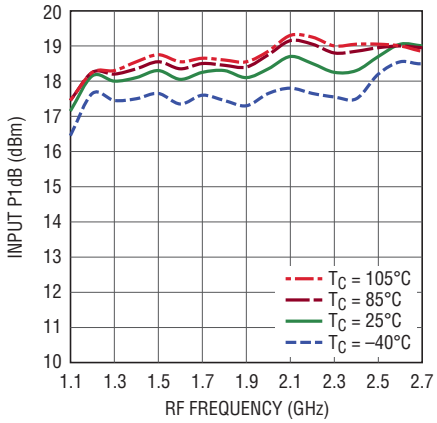
1950MHz Conversion Gain, IIP3 and NF vs LO Power (High Side LO)



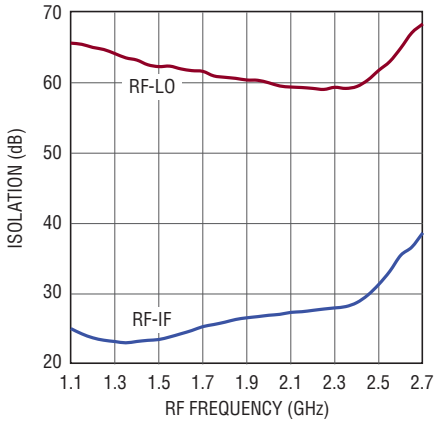
2550MHz Conversion Gain, IIP3 and NF vs LO Power (High Side LO)



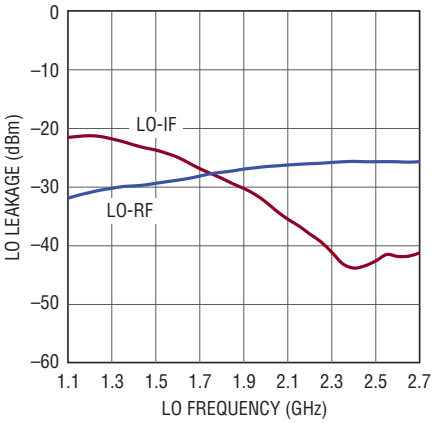
Input P1dB vs RF Frequency (Low Side LO)



RF Isolation vs Frequency



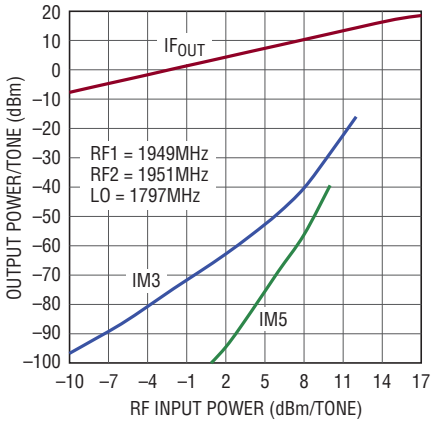
LO Leakage vs LO Frequency



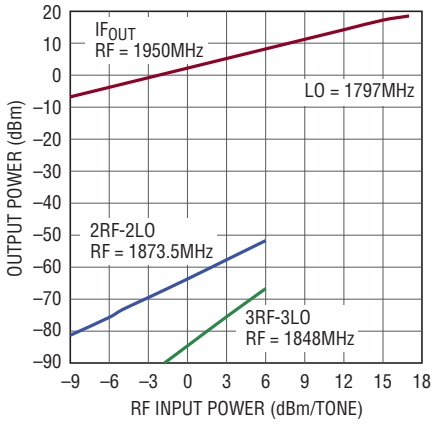
TYPICAL AC PERFORMANCE CHARACTERISTICS

1100MHz to 2700MHz application.
V_{CC} = 3.3V, EN = High, ISEL = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted. Test circuit shown in Figure 1.

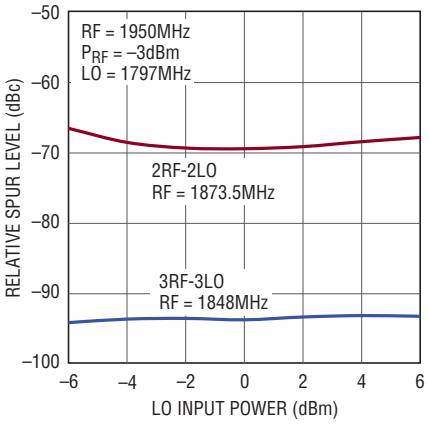
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



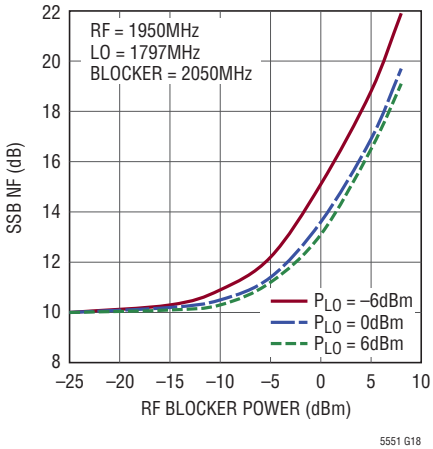
Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



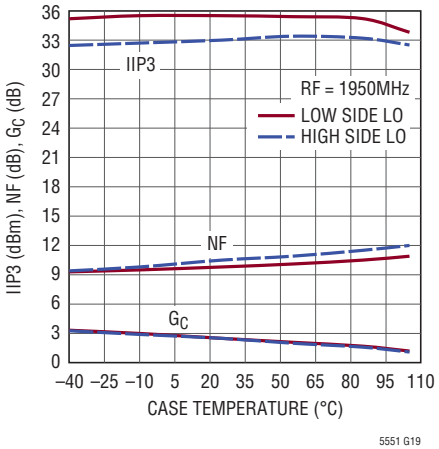
2 × 2 and 3 × 3 Spurs vs LO Power



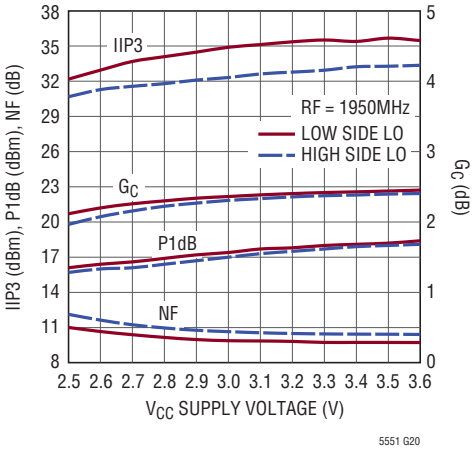
SSB Noise Figure vs RF Blocker Level



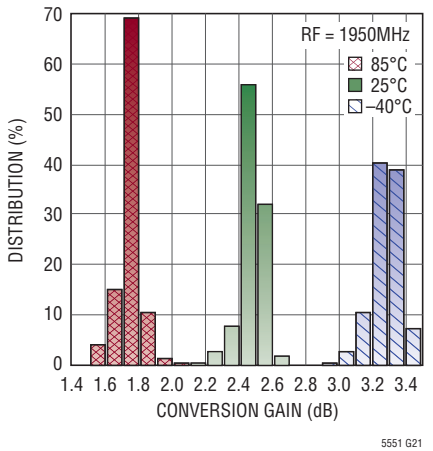
Conversion Gain, IIP3 and SSB NF vs Temperature



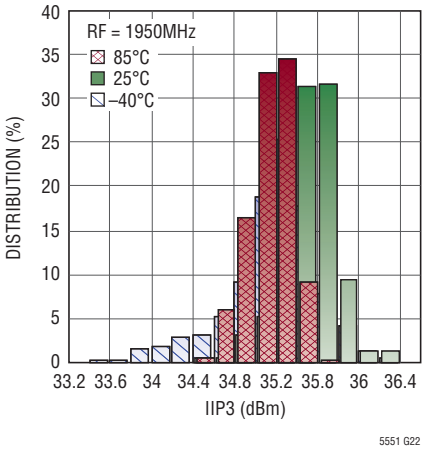
Conversion Gain, IIP3, P1dB and SSB NF vs Supply Voltage



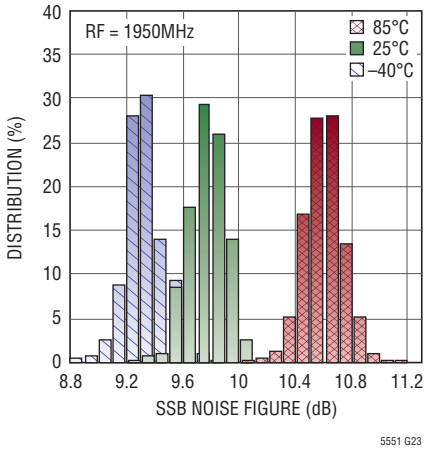
1950MHz Conversion Gain Histogram



1950MHz IIP3 Histogram



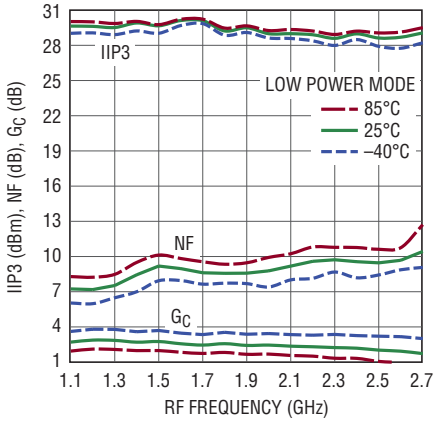
1950MHz SSB NF Histogram



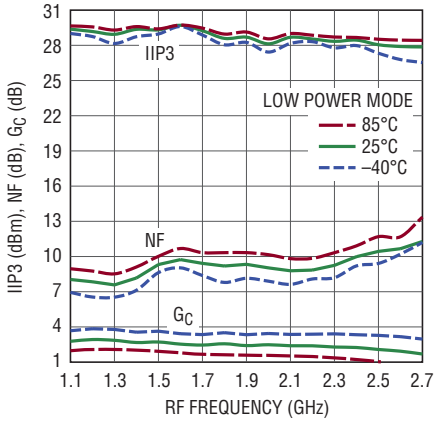
TYPICAL AC PERFORMANCE CHARACTERISTICS

1100MHz to 2700MHz application. Low Power Mode. V_{CC} = 3.3V, EN = High, ISEL = High, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted. Test circuit shown in Figure 1.

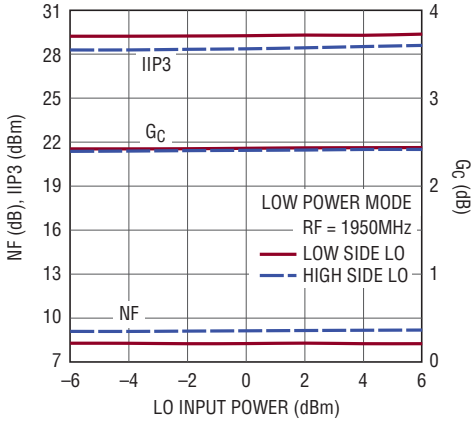
Conversion Gain, IIP3 and NF vs RF Frequency (Low Side LO)



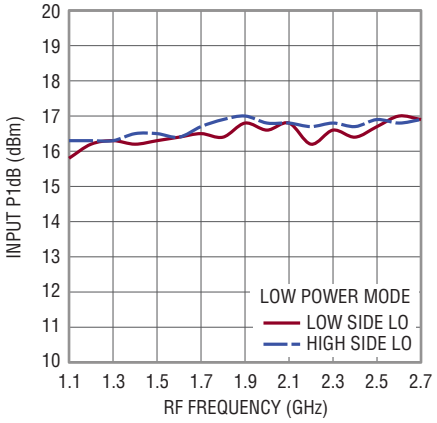
Conversion Gain, IIP3 and NF vs RF Frequency (High Side LO)



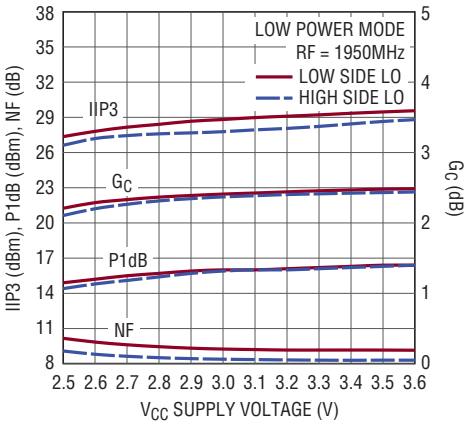
1950MHz Conversion Gain, IIP3 and NF vs LO Power



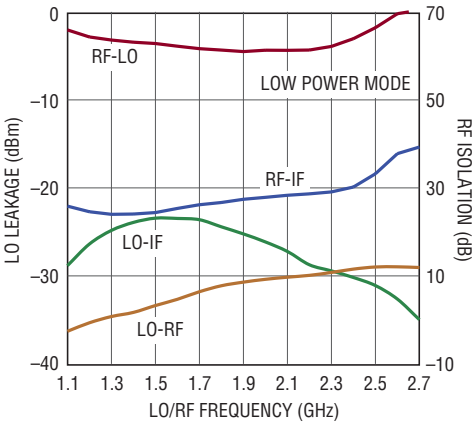
Input P1dB vs RF Frequency



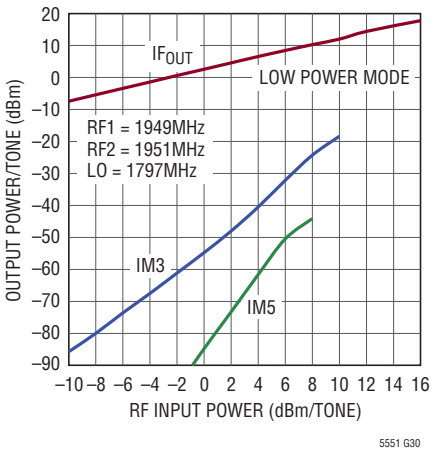
Conversion Gain, IIP3, P1dB and NF vs Supply Voltage



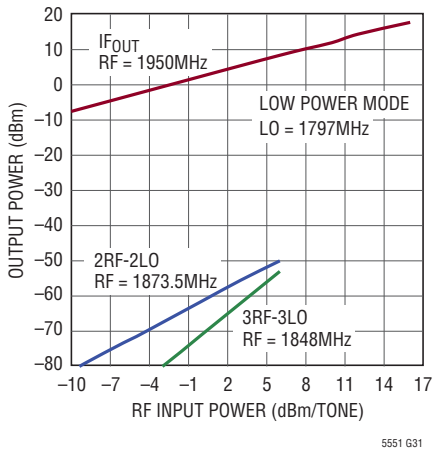
LO Leakage and RF Isolation



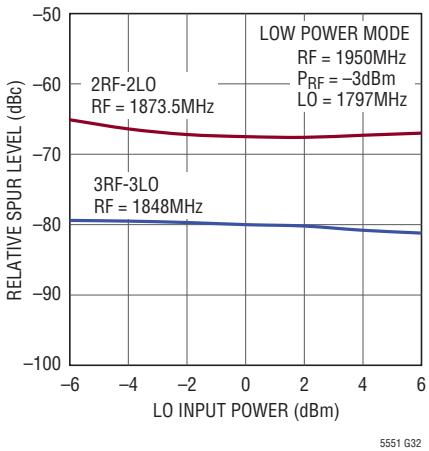
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



Single Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



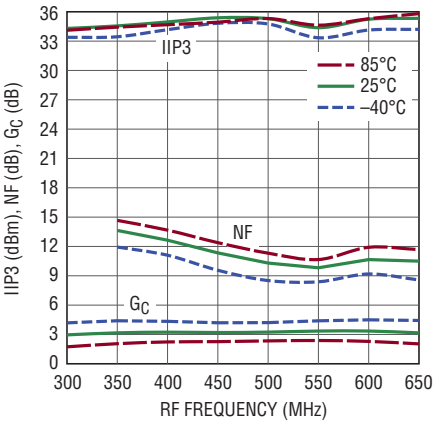
2 × 2 and 3 × 3 Spurs vs LO Power



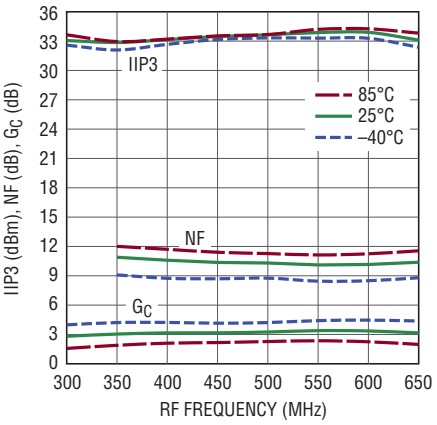
TYPICAL AC PERFORMANCE CHARACTERISTICS

300MHz to 650MHz application.
V_{CC} = 3.3V, EN = High, ISEL = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted. Test circuit shown in Figure 1.

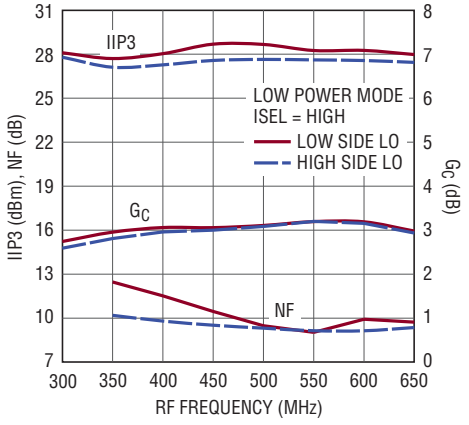
Conversion Gain, IIP3 and NF vs RF Frequency (Low Side LO)



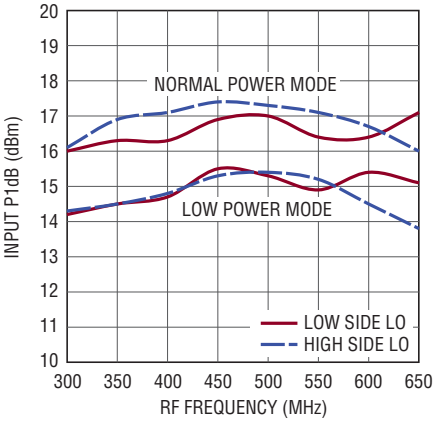
Conversion Gain, IIP3 and NF vs RF Frequency (High Side LO)



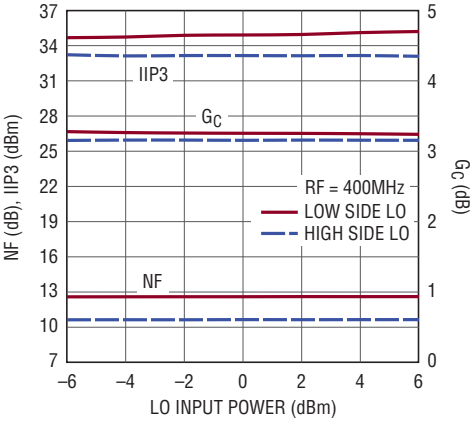
Conversion Gain, IIP3 and NF vs RF Frequency



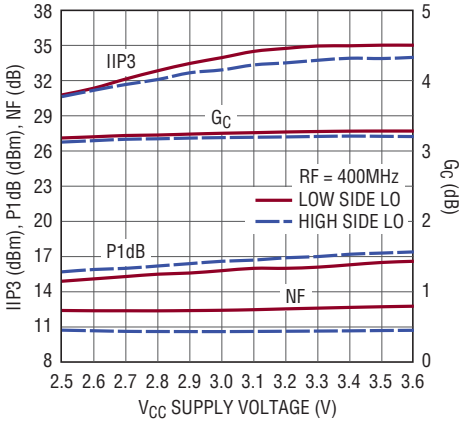
Input P1dB vs Frequency



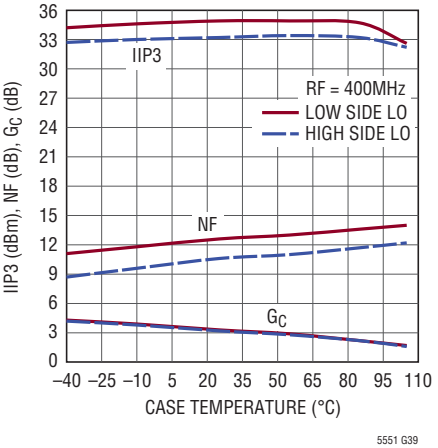
400MHz Conversion Gain, IIP3 and NF vs LO Power



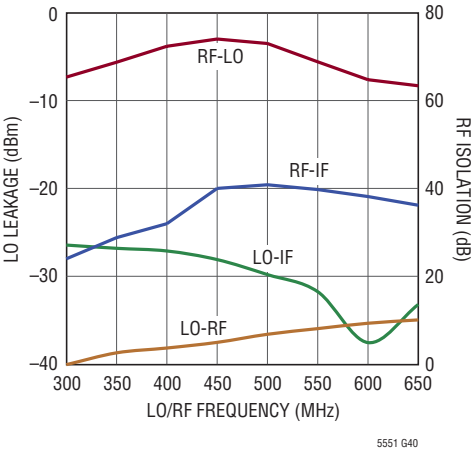
Conversion Gain, IIP3, P1dB and NF vs Supply Voltage



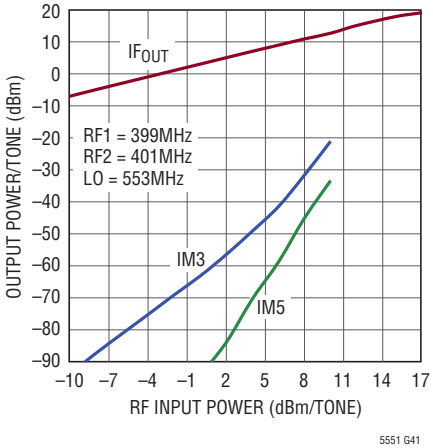
Conversion Gain, IIP3 and SSB NF vs Temperature



LO Leakage and RF Isolation



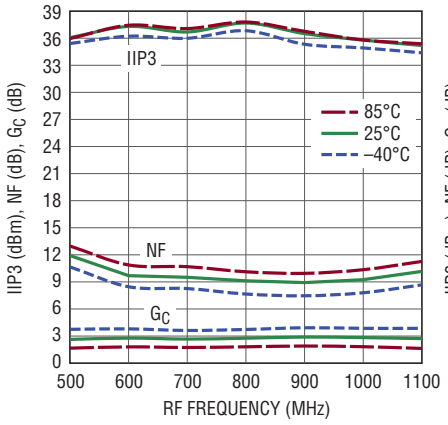
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



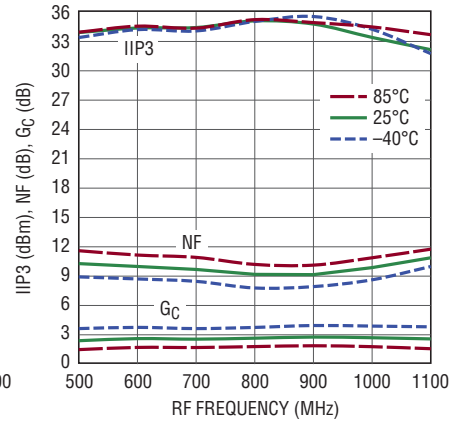
TYPICAL AC PERFORMANCE CHARACTERISTICS

500MHz to 1100MHz application.
V_{CC} = 3.3V, EN = High, ISEL = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted. Test circuit shown in Figure 1.

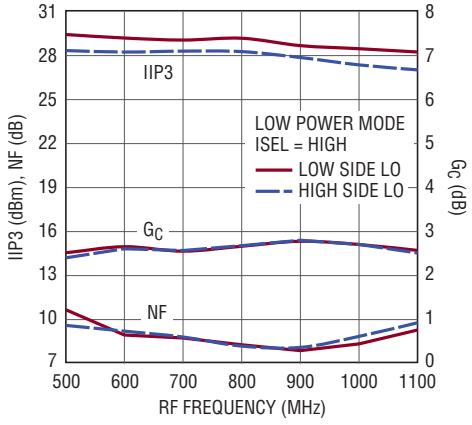
Conversion Gain, IIP3 and NF vs RF Frequency (Low Side LO)



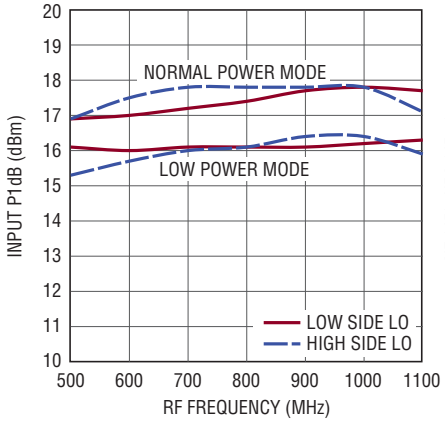
Conversion Gain, IIP3 and NF vs RF Frequency (High Side LO)



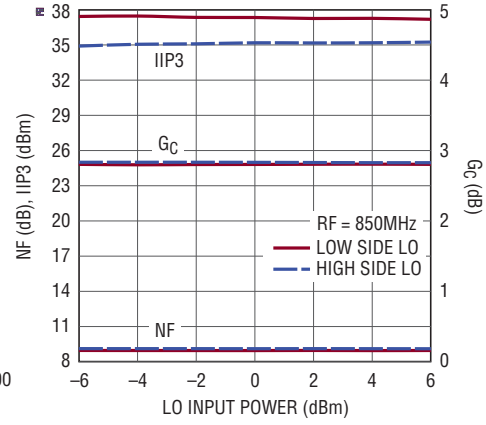
Conversion Gain, IIP3 and NF vs RF Frequency



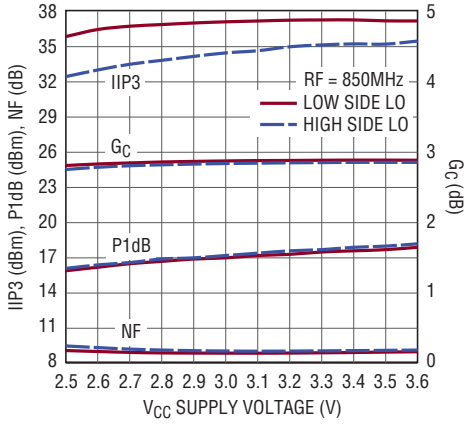
Input P1dB vs RF Frequency



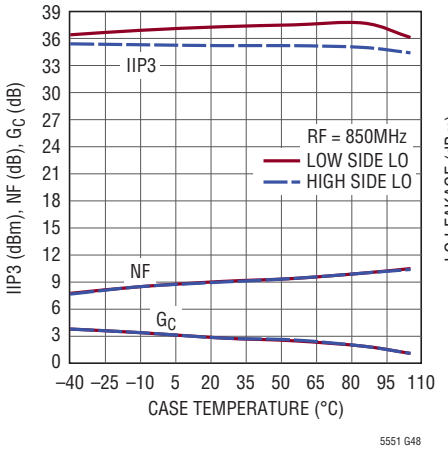
850MHz Conversion Gain, IIP3 and NF vs LO Power



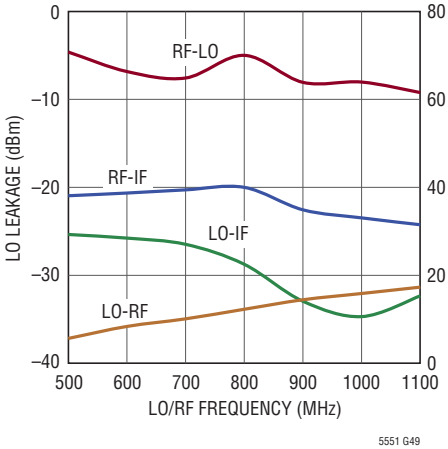
Conversion Gain, IIP3, P1dB and NF vs Supply Voltage



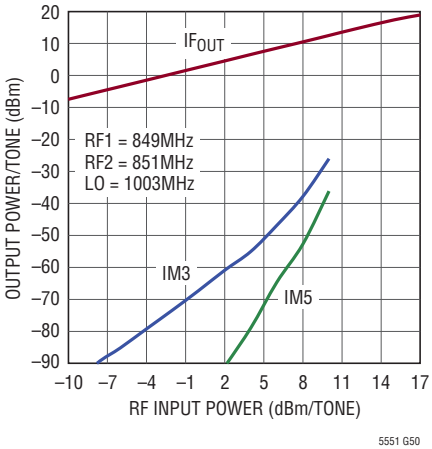
Conversion Gain, IIP3 and SSB NF vs Temperature



LO Leakage and RF Isolation



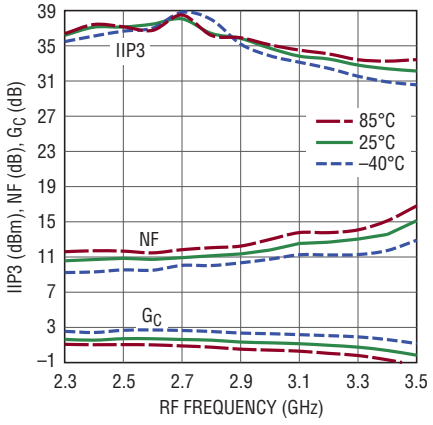
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



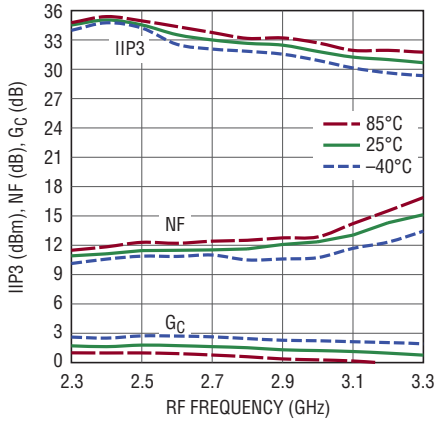
TYPICAL AC PERFORMANCE CHARACTERISTICS

2300MHz to 3500MHz application.
V_{CC} = 3.3V, EN = High, ISEL = Low, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = 0dBm (0dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted. Test circuit shown in Figure 1.

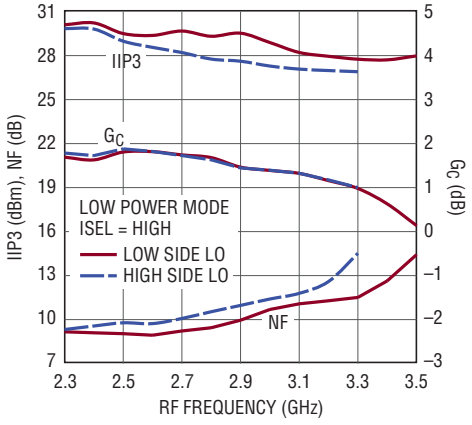
Conversion Gain, IIP3 and NF vs RF Frequency (Low Side LO)



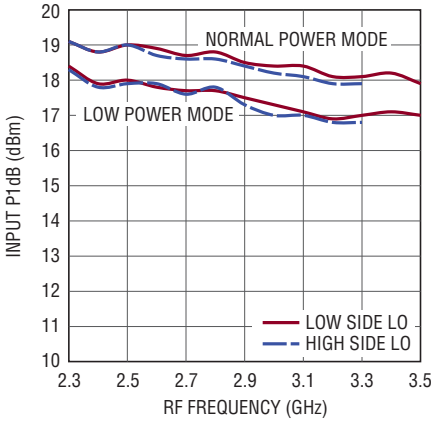
Conversion Gain, IIP3 and NF vs RF Frequency (High Side LO)



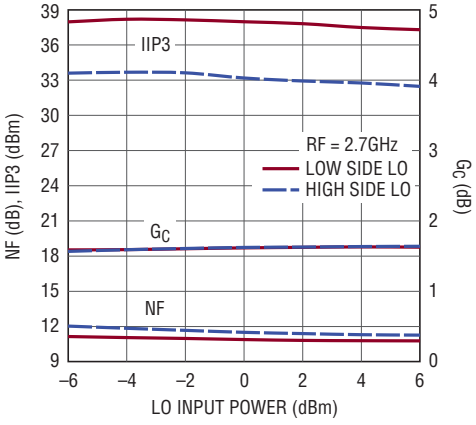
Conversion Gain, IIP3 and NF vs RF Frequency



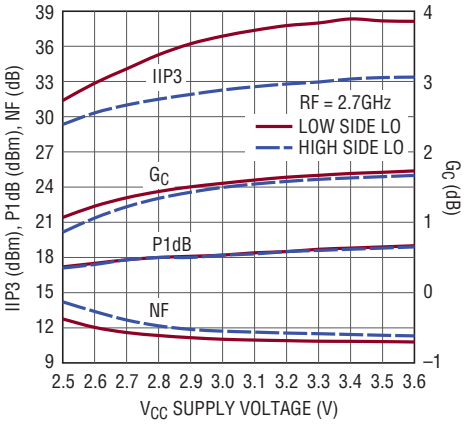
Input P1dB vs RF Frequency



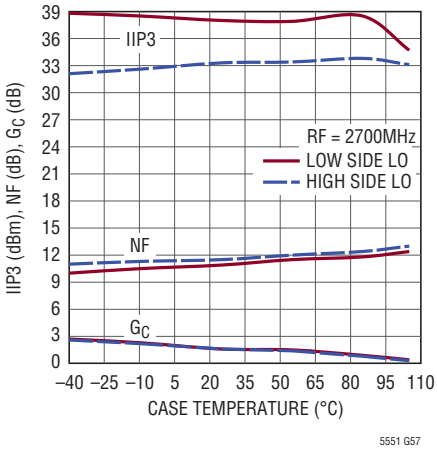
2.7GHz Conversion Gain, IIP3 and NF vs LO Power



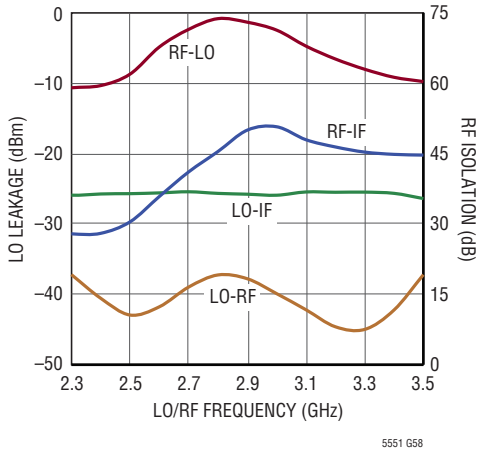
Conversion Gain, IIP3, P1dB and NF vs Supply Voltage



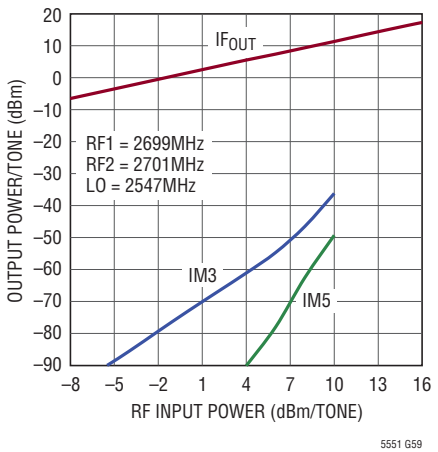
Conversion Gain, IIP3 and SSB NF vs Temperature



LO Leakage and RF Isolation



2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



PIN FUNCTIONS

TP (Pin 1): Test Point. It is used for manufacture measurement only. It is recommended to be connected to ground.

RF (Pin 2): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **A series DC-blocking capacitor should be used to avoid damage to the integrated transformer when DC voltage is present at the RF input.** The RF input impedance is matched under the condition that the LO input is driven with a 0dBm ±6dB source between 0.2GHz and 3.5GHz.

CT (Pin 3): RF Transformer Secondary Center-Tap. This pin must be connected to ground with minimum parasitic resistance and inductance to complete the Mixer's DC current path. Typical DC current is 80mA with LO disabled and 134mA when LO signal is applied.

GND (Pins 4, 9, 11, 13, Exposed Pad Pin 17): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

EN (Pin 5): Enable Pin. When the input voltage is greater than 1.2V, the mixer is enabled. When the input voltage is less than 0.3V or left open, the mixer is disabled. Typical input current is less than 30µA. This pin has an internal pull-down resistor.

V_{CC} (Pins 6, 7): Power Supply Pins. These pins are internally connected and must be externally connected to a regulated 2.5V to 3.6V supply, with bypass capacitors located close to the pin. Typical current consumption is 70mA through these pins.

ISEL (Pin 8): Low Power Select Pin. When this pin is pulled low (<0.3V) or left open, the mixer is biased at the normal current level for best RF performance. When greater than 1.2V is applied, the mixer operates at reduced current mode, which provides reasonable performance at lower power consumption. This pin has an internal pull-down resistor.

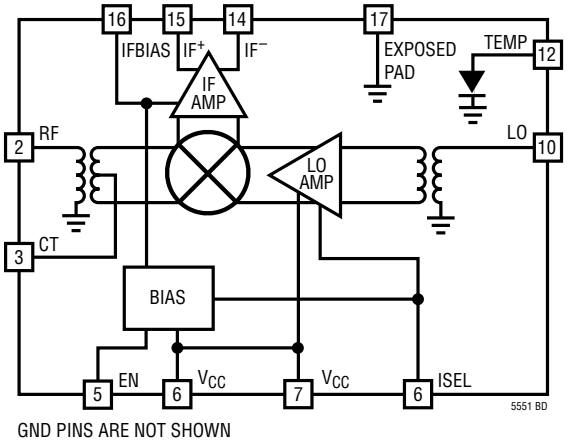
LO (Pin 10): Single-Ended Input for the Local Oscillator. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **A series DC blocking capacitor should be used to avoid damage to the integrated transformer when DC voltage is present at the LO input.**

TEMP (Pin 12): Temperature Sensing Diode. This pin is connected to the anode of a diode that may be used to measure the die temperature, by forcing a current and measuring the voltage.

IF^- (Pin 14) and IF^+ (Pin 15): Open-Collector Differential Outputs for the IF Amplifier. These pins must be connected to a DC supply through impedance matching inductors, or a transformer center-tap. Typical DC current consumption is 67mA into each pin.

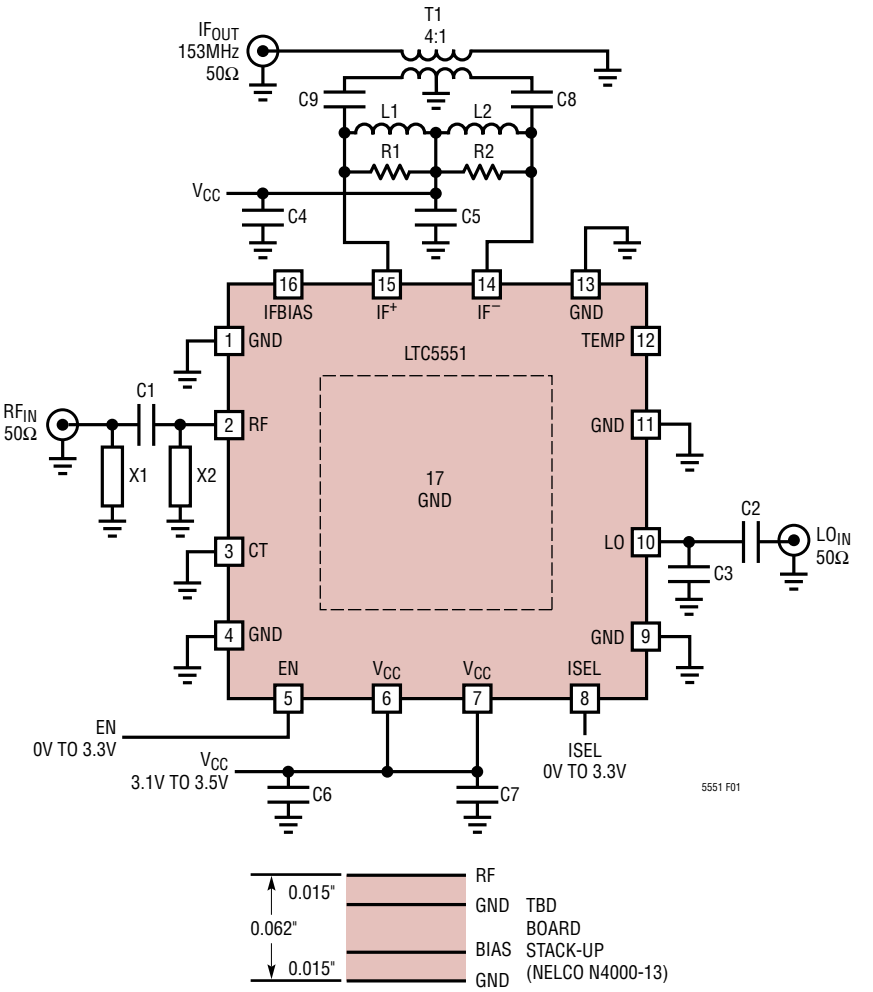
IFBIAS (Pin 16): This Pin Allows Adjustment of the IF Amplifier Current. Typical DC voltage is 2.1V. This pin should be left floating for optimum performance.

BLOCK DIAGRAM



GND PINS ARE NOT SHOWN

TEST CIRCUIT



APPLICATION		RF MATCH			LO MATCH		IF TRANSFORMER	
RF (MHz)	LO	X1	C1	X2	C2	C3	T1	VENDOR
300 to 650	HS	15nH	15pF	15pF	15pF	8.2pF	TC4-1W-7ALN+	Mini-Circuits
500 to 1100	HS	13nH	6.8pF	4.7pF	8.2pF	2.2pF	WBC4-6TLB	Coilcraft
1100 to 2700	LS, HS	7.5nH	2.2pF	–	3.9pF	–	TC4-1W-7ALN+	Mini-Circuits
2300 to 3500	LS, HS	1.2pF	22pF	2.2nH	3.9pF	–	TC4-1W-7ALN+	Mini-Circuits

REF DES	VALUE	SIZE	VENDOR	REF DES	VALUE	SIZE	VENDOR
C4, C6	0.56µF	0603	Murata	R1, R2	475Ω, 1%	0402	Vishay
C5, C7	22pF	0402	AVX	L1, L2	470nH, 2%	0603	Coilcraft 0603LS
C8, C9	1nF	0402	AVX				

Figure 1. Standard Downmixer Test Circuit Schematic (153MHz IF)

APPLICATIONS INFORMATION

Introduction

The LTC5551 consists of a high linearity double-balanced mixer core, IF buffer amplifier, LO buffer amplifier and bias/enable circuits. See the Block Diagram section for a description of each pin function. The RF and LO inputs are single-ended. The IF output is differential. Low side or high side LO injection can be used. The evaluation circuit, shown in Figure 1, utilizes bandpass IF output matching and an IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

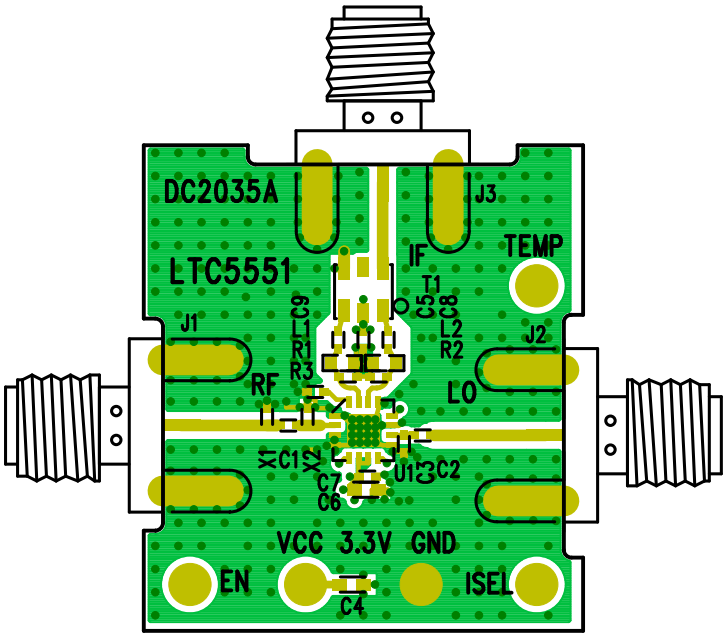


Figure 2. Evaluation Board Layout

RF Input

The mixer's RF input, shown in Figure 3, is connected to the primary winding of an integrated transformer. A 50Ω match can be realized with a π-network as shown in Figures 1 and 3. The primary side of the RF transformer is DC-grounded internally and the DC resistance of the primary is approximately 4Ω. A DC blocking capacitor is needed if the RF source has DC voltage present.

The secondary winding of the RF transformer is internally connected to the mixer core. The center-tap of the transformer secondary is connected to Pin 3 (CT). Pin 3 needs to be connected to ground with a minimum parasitic resistance and inductance.

For the RF input to be matched, the LO input must be driven. Using components listed in Figure 1, the RF input can be matched from 300MHz to 3.5GHz. The measured RF input return loss is shown in Figure 4 for LO frequencies of 0.5GHz, 1.0GHz. 1.8GHz and 2.8GHz. These LO frequencies correspond to the lower, middle and upper values of the LO range.

The RF input impedance and input reflection coefficient, versus RF frequency, is listed in Table 1. The reference plane for this data is Pin 2 of the IC, with no external matching, and the LO is driven at 1.8GHz.

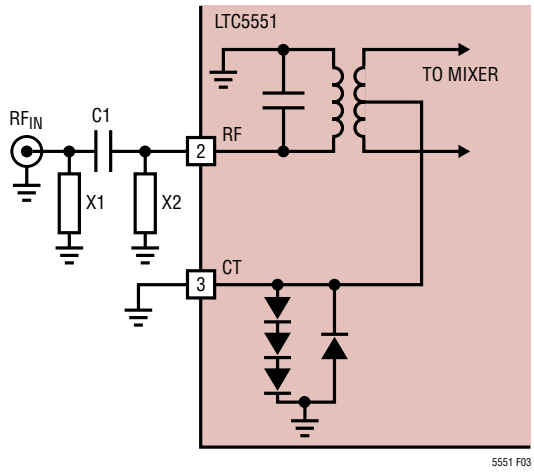


Figure 3. RF Input Schematic

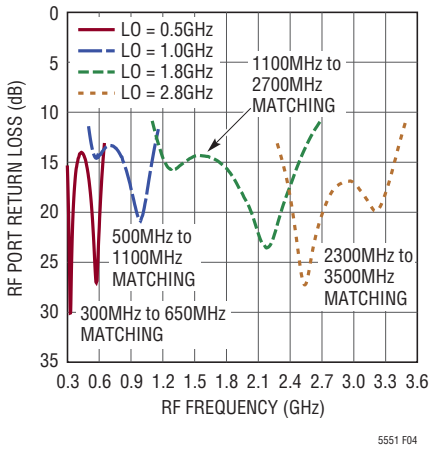


Figure 4. RF Input Return Loss

APPLICATIONS INFORMATION

Table 1. RF Input Impedance and S11 (at Pin 2, No External Matching, LO Input Driven at 1.8GHz)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
0.3	7.6 + j8.4	0.74	160.4
0.7	11.7 + j15.2	0.65	144.5
1.1	17.7 + j 22.2	0.55	127.4
1.5	29.3 + j27.8	0.41	107.4
1.9	46.7 + j21.8	0.22	85.8
2.3	49.6 – j1.3	0.01	–106.3
2.7	31.1 – j9.0	0.26	–148.2
3.1	18.2 – j1.8	0.47	–175.2
3.5	11.8 + j8.4	0.63	159.8

LO Input

The mixer's LO input circuit, shown in Figure 5, consists of a balun transformer and a two-stage high speed limiting differential amplifier to drive the mixer core. The LTC5551's LO amplifiers are optimized for the 200MHz to 3.5GHz LO frequency range. LO frequencies above or below this frequency range may be used with degraded performance.

The mixer's LO input is directly connected to the primary winding of an integrated transformer. The LO is 50Ω matched from 1GHz to 3.5GHz with a single 3.9pF series capacitor on the input. Matching to LO frequencies below 1GHz is easily accomplished by adding shunt capacitor C3 shown in Figure 5. Measured LO input return loss is shown in Figure 6.

The nominal LO input level is 0dBm although the limiting amplifiers will deliver excellent performance over a ±6dB input power range. LO input power of –9dBm may be used with slightly degraded performance.

The LO input impedance and input reflection coefficient, versus frequency, is shown in Table 2.

Table 2. LO Input Impedance vs Frequency (at Pin 10, No External Matching)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
0.3	4.8 + j12.0	0.84	152.7
0.7	13.4 + j28.1	0.67	118.5
1.1	32.7 + j39.1	0.47	88.6
1.5	56.8 + j31.1	0.29	61.5
1.9	62.8 + j9.3	0.14	31.4
2.3	54.1 – j1.4	0.04	–18.3
2.7	45.1 – j1.4	0.05	–163.6
3.1	39.8 + j3.6	0.12	158.6
3.5	37.2 + j10.4	0.19	134.1

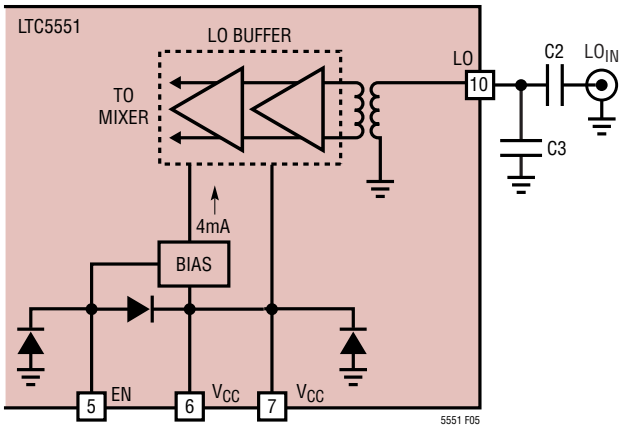


Figure 5. LO Input Schematic

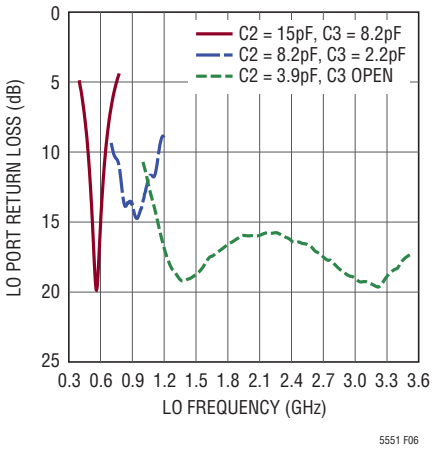


Figure 6. LO Input Return Loss

APPLICATIONS INFORMATION

IF Output

The IF amplifier, shown in Figure 7, has differential open-collector outputs (IF^+ and IF^-), and a pin for modifying the internal bias (IFBIAS). The IF outputs must be biased at the supply voltage (V_{CC}), which is applied through matching inductors L1 and L2. Alternatively, the IF outputs can be biased through the center tap of a transformer. Each IF output pin draws approximately 67mA of DC supply current (134mA total). For the highest performance, high-Q wire-wound chip inductors are recommended for L1 and L2. Low cost multilayer chip inductors may be substituted, with a slight degradation in performance.

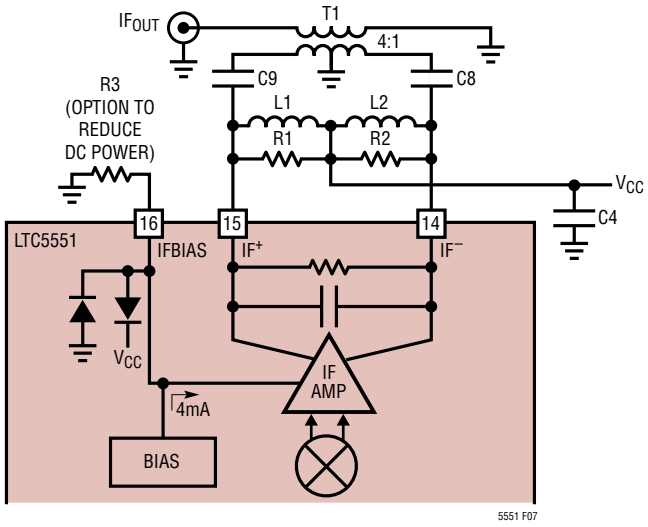


Figure 7. IF Amplifier Schematic with Transformer-Based Bandpass Match

For optimum single-ended performance, the differential IF outputs must be combined through an external IF transformer or discrete IF balun circuit. The evaluation board (see Figures 1 and 2) uses a 4:1 ratio IF transformer for impedance transformation and differential to single-ended transformation. It is also possible to eliminate the IF transformer and drive differential filters or amplifiers directly.

The IF output impedance can be modeled as 950Ω in parallel with 1.2pF at IF frequencies. An equivalent small-signal model is shown in Figure 8. Frequency-dependent differential IF output impedance is listed in Table 3. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics.

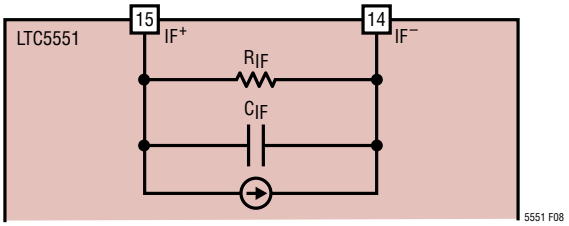


Figure 8. IF Output Small-Signal Model

Table 3. IF Output Impedance vs Frequency

FREQUENCY (MHz)	DIFFERENTIAL OUTPUT IMPEDANCE (R_{IF} || X_{IF} (C_{IF}))
90	954 || –j1442 (1.2pF)
140	950 || –j848 (1.2pF)
190	945 || –j681 (1.2pF)
240	942 || –j539 (1.2pF)
380	938 || –j338 (1.2pF)
456	926 || –j281 (1.2pF)

Transformer-Based Bandpass IF Matching

The IF output can be matched using the bandpass IF matching shown in Figures 1 and 7. L1 and L2 resonate with the internal IF output capacitance at the desired IF frequency. The value of L1, L2 is calculated as follows:

$$L1, L2 = 1/[(2\,\pi\,f_{IF})^2 \bullet 2 \bullet C_{IF}]$$

where C_{IF} is the internal IF capacitance (listed in Table 3).

Values of L1 and L2 are tabulated in Figure 1 for various IF frequencies.

For IF Frequency below 80MHz, the inductor values become unreasonably high and the high pass impedance matching network described in a later section is preferred, due to its lower inductor values.

Table 4 summarizes the optimum IF matching inductor values vs IF center frequency, to be used in the standard downmixer test circuit shown in Figure 1. The inductor values listed are less than the ideal calculated values due to the additional capacitance of the 4:1 transformer. Measured IF output return losses are shown in Figure 9.

APPLICATIONS INFORMATION

Table 4. Bandpass Matching Elements Values vs IF Frequency

L1, L2 vs IF Frequencies

IF (MHz)	L1, L2 (nH)	COMMENTS
120	810	Coilcraft 0603 LS
153	470	Coilcraft 0603 LS
240	180	Coilcraft 0603 CS
305	120	Coilcraft 0603 CS
380	56	Coilcraft 0603 CS
456	33	Coilcraft 0603 CS

The resistors R1 and R2 which are connected between the IF^+ and IF^- is used to assist the IF impedance matching. A lower value of R1, R2 will help improve the IF return loss and broaden the IF bandwidth. However, it will results in lower conversion gain with minor impact to linearity and noise figure performances.

Other 4:1 transformers can be used to replace the TC4-1-7ALN+ that is used in the standard demoboards. The insertion loss and parasitics of the transformer will impact the overall circuit performance. For IF frequency higher than 300MHz, the TC4-1-17LN+ from Mini-Circuits or the WBC4-6TLB from Coilcraft is preferred.

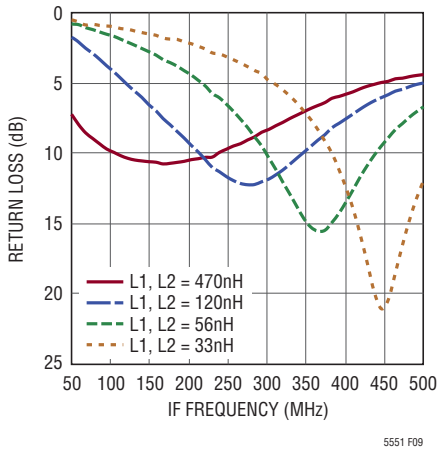


Figure 9. IF Output Return Loss Bandpass Matching with 4:1 Transformer

Highpass IF Matching

The highpass IF matching circuits shown in Figure 10 can be used when higher conversion gain than that from the standard demoboard is desired. The highpass matching network will have less IF bandwidth than the bandpass matching. It also use smaller inductance values; an advantage when designing for IF center frequency well lower than 80MHz.

Referring to the small-signal output network schematic in Figure 10, the reactive matching element values (L1, L2, C8 and C9) are calculated using the following equations. The source resistance (R_S) is the parallel combination of external resistors R1 + R2 and the internal IF resistance, R_{IF} taken from Table 3. The differential load resistance (R_L) is typically 200Ω, but can be less. C_{IF}, the IF output capacitance, is taken from Table 3. Choosing R_S in the 380Ω to 450Ω range will yield power conversion gains around 4dB.

$$R_S = R_{IF} \,||\, 2 \bullet R1 \qquad (R1 = R2)$$

$$Q = \sqrt{(R_S / R_L - 1)} \qquad (R_S > R_L)$$

$$Y_L = Q / R_S + (\omega_{IF} \bullet C_{IF})$$

$$L1, L2 = 1 / (2 \bullet Y_L \bullet \omega_{IF})$$

$$C7, C8 = 2 / (Q \bullet R_L \bullet \omega_{IF})$$

To demonstrate the highpass impedance transformer output matching, these equations were used to calculate the element values for a 80MHz IF frequency and 200Ω differential load resistance. The measured performance with L1, L2 = 330nH, C8, C9 = 15pF is shown in Figure 11. The test conditions are: P_{RF} = –6dBm, P_{LO} = 0dBm with low side LO injection.

APPLICATIONS INFORMATION

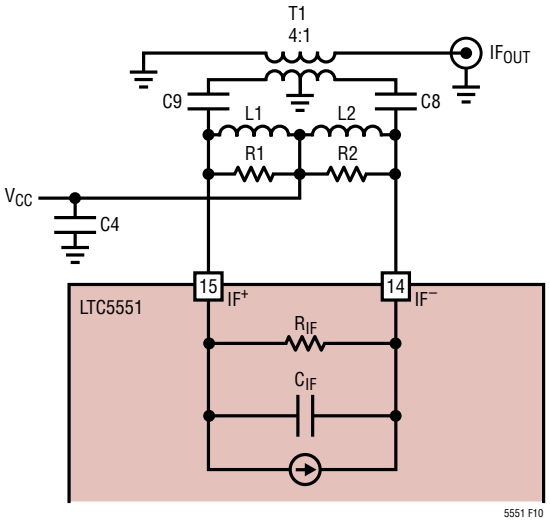


Figure 10. IF Output Circuit for Highpass Matching Element Value Calculations

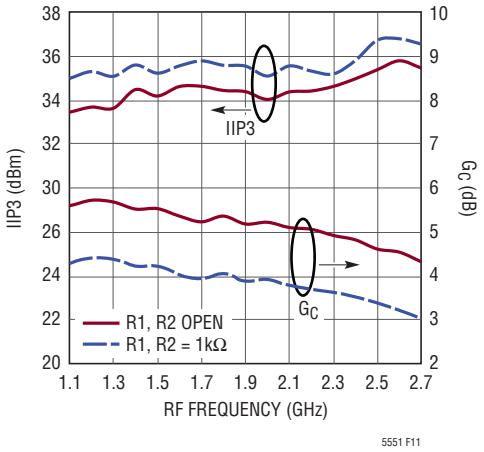


Figure 11. Performance Using 80MHz Highpass IF Matching Network

APPLICATIONS INFORMATION

Wideband Differential IF Output

Wide IF bandwidth and high input 1dB compression are obtained by reducing the IF output resistance with resistors R1 and R2. This will reduce the mixer's conversion gain, but will not degrade the IIP3 or noise figure.

The IF matching shown in Figure 12 uses 249Ω resistors and 470nH supply chokes to produce a wideband 200Ω differential output. This differential output is suitable for driving a wideband differential amplifier, filter, or a wideband 4:1 transformer.

The complete test circuit, shown in Figure 13, uses resistive impedance matching attenuators (L-pads) on the evaluation board to transform each 100Ω IF output to 50Ω. An external 0°/180° power combiner is then used to convert the 100Ω differential output to 50Ω single-ended, to facilitate measurement.

Measured conversion gain and IIP3 at the 200Ω differential output are plotted in Figure 14. As shown, the conversion gain is flat within 1dB over the 50MHz to 490MHz IF output frequency range.

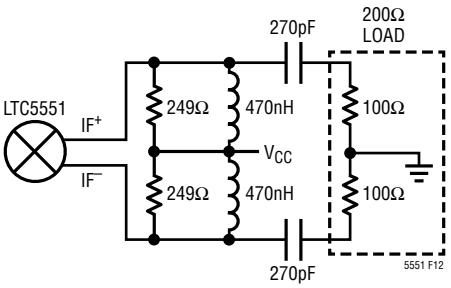


Figure 12. Wideband 200Ω Differential Output

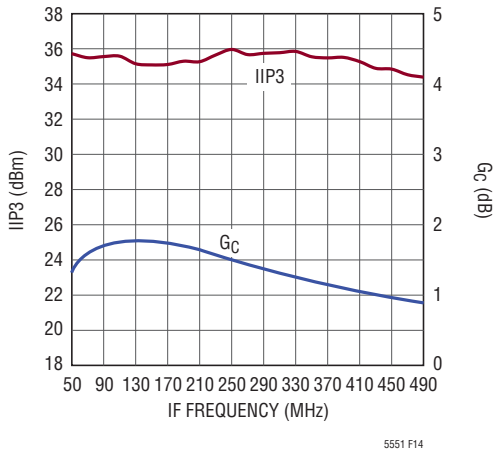


Figure 14. Conversion Gain and IIP3 vs IF Output Frequency for Wideband 200Ω Differential IF

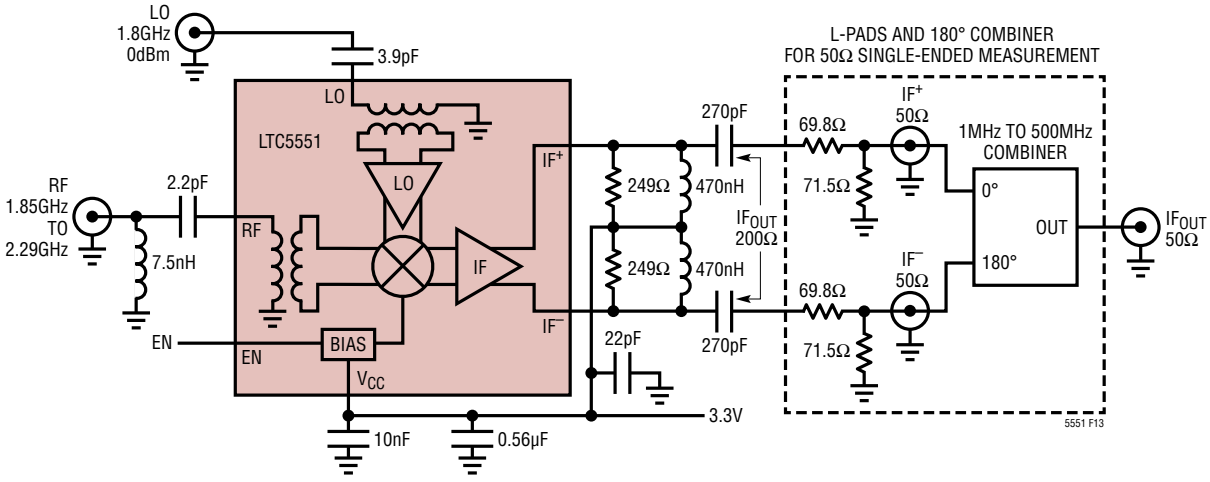


Figure 13. Test Circuit for Wideband 200Ω Differential Output

APPLICATIONS INFORMATION

The IFBIAS pin (Pin 16) is available for reducing the DC current consumption of the IF amplifier, at the expense of reduced performance. This pin should be left open-circuited for optimum performance. The internal bias circuit produces a 4mA reference for the IF amplifier, which causes the amplifier to draw approximately 134mA. If resistor R3 is connected to Pin 16 as shown in Figure 7, a portion of the reference current can be shunted to ground, resulting in reduced IF amplifier current. For example, R3 = 1kΩ will shunt away 1.5mA from Pin 16 and the IF amplifier current will be reduced to approximately 90mA. The nominal, open-circuit DC voltage at Pin 16 is 2.1V. Table 5 lists RF performance at 1950MHz vs IF amplifier current.

Table 5. Mixer Performance with Reduced IF Amplifier Current (RF = 1950MHz, Low Side LO, IF = 153MHz, V_{CC} = 3.3V)

R3 (kΩ)	I_{CC} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	204	2.4	35.5	18.0	9.7
4.7	194	2.4	35.0	17.9	9.4
2.2	186	2.4	34.2	17.8	9.2
1.0	164	2.4	31.9	17.3	8.7

(RF = 1950MHz, High Side LO, IF = 153MHz, V_{CC} = 3.3V)

R3 (kΩ)	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	204	2.4	33.0	17.9	10.5
4.7	194	2.3	32.6	17.8	10.2
2.2	186	2.3	32.1	17.6	9.9
1.0	164	2.3	30.5	17.0	9.4

Low Power Mode

The LTC5551 can be set to low power mode using a digital voltage applied to the ISEL pin (Pin 8). This allows the flexibility to reduce current when lower RF performance is acceptable. Figure 15 shows a simplified schematic of the ISEL pin interface. When ISEL is set low (<0.3V), the mixer operates at maximum DC current. When ISEL is set high (>1.2V), the DC current is reduced, thus reducing power consumption. When floating, the ISEL is pulled low by an internal pull-down resistor, and operates at maximum supply current. The performance in low power mode and nominal power mode are compared in Table 6.

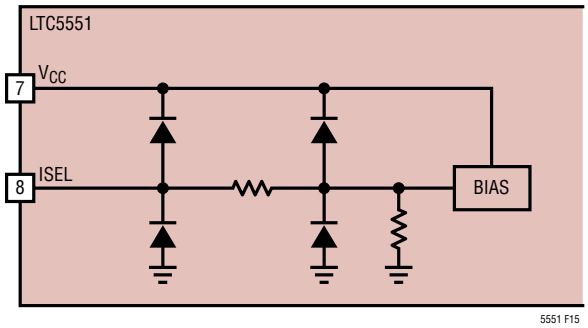


Figure 15. ISEL Interface Schematic

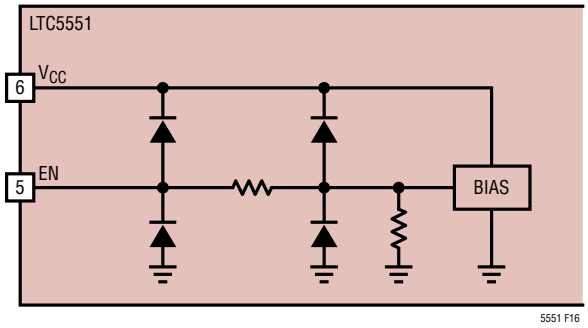


Figure 16. Enable Input Circuit

Table 6. Performance Comparison – Low Power vs High Power Mode RF = 1950MHz, Low Side LO, IF = 153MHz, EN = High

ISEL	I_{CC} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
Low	204	2.4	35.5	18.0	9.7
High	139	2.4	29.3	16.7	8.3

Enable Interface

Figure 16 shows a simplified schematic of the EN pin interface. To enable the chip, the EN voltage must be higher than 1.2V. The EN voltage at the pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

If the EN pin is left floating, its voltage will be pulled low by the internal pull-down resistor and the chip will be disabled.

APPLICATIONS INFORMATION

Temperature Diode

The LTC5551 provides an on-chip diode at Pin 12 (TEMP) for chip temperature measurement. Pin 12 is connected to the anode of an internal ESD diode with its cathode connected to internal ground. The chip temperature can be measured by injecting a constant DC current into Pin 12 and measuring its DC voltage. The voltage vs temperature coefficient of the diode is about –1.72mV/°C with 10µA current injected into the TEMP pin. Figure 17 shows a typical temperature-voltage behavior when 10µA and 80µA currents are injected into Pin 12.

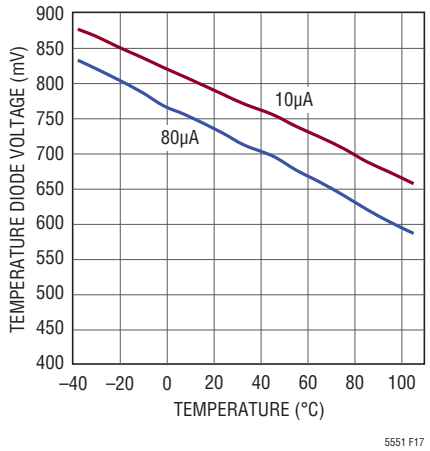


Figure 17. TEMP Diode Voltage vs Junction Temperature (T_J)

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

Spurious Output Levels

Mixer spurious output levels versus harmonics of the RF and LO are tabulated in Table 7. The spur levels were measured on a standard evaluation board using the test circuit shown in Figure 1. The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) – (N \bullet f_{LO})$$

Table 7. IF Output Spur Levels (dBc)

RF = 1950MHz, P_{RF} = 0dBm, P_{LO} = 0dBm, IF = 153MHz, Low Side LO, V_{CC} = 3.3V, EN = High, ISEL = Low, T_C = 25°C

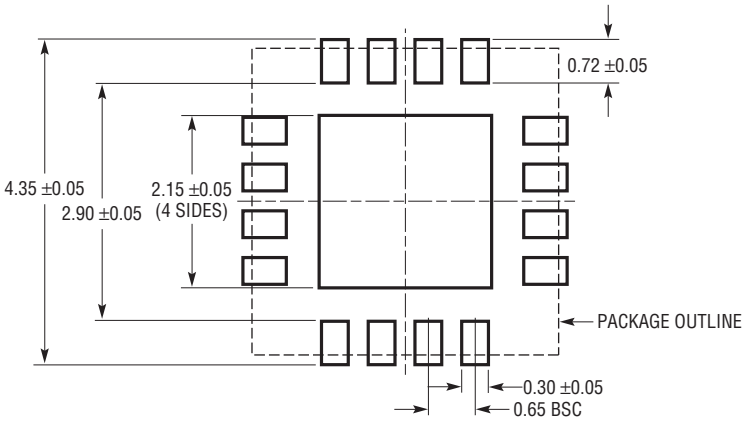
		N									
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
M	**0**		–26	–36	–40	–40	–61	–70	–57	–60	*
	1	–28	0	–43	–26	–60	–43	–64	–49	–62	–63
	2	–83	–66	–70	–69	–83	*	*	–81	*	–79
	3	*	–81	*	*	*	*	*	*	*	*
	4	*	*	*	*	*	*	*	*	*	*
	5	*	*	*	*	*	*	*	*	*	*
	6	–84	*	*	*	*	*	*	*	*	*
	7	–82	*	*	–84	*	*	*	*	*	*

*Less than –85dBc

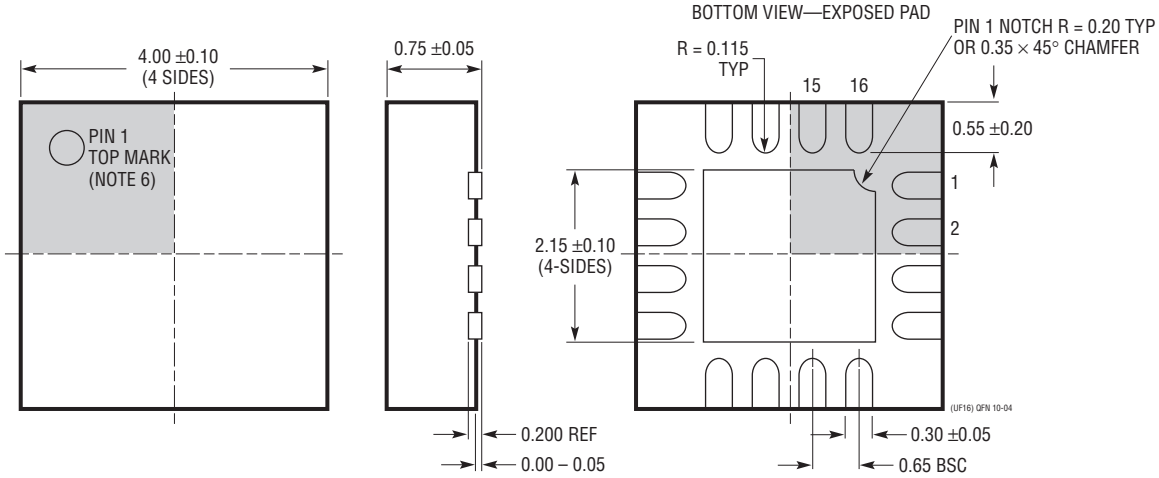
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/13	Added U.S. Patent number	1
		Corrected transformer T1 part number	13

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.