300MHz to 6GHz High Signal Level Active Downconverting Mixer

FEATURES

- **+30dBm IIP3**
- **+15dBm Input P1dB**
- **0dB Conversion Gain**
- **Wideband Differential IF Output**
- **Very Low 2 × 2 and 3 × 3 Spurs**
- **IF Frequency Range Up to 1.5GHz**
- **Low LO-RF Leakage**
- LO Input 50Ω Matched when Shutdown
- –40°C to 105°C Operation (T_C)
- Very Small Solution Size
- 16-Lead (4mm × 4mm) QFN package

APPLICATIONS

- Wireless Infrastructure Receivers
- DPD Observation Receivers
- CATV Infrastructure

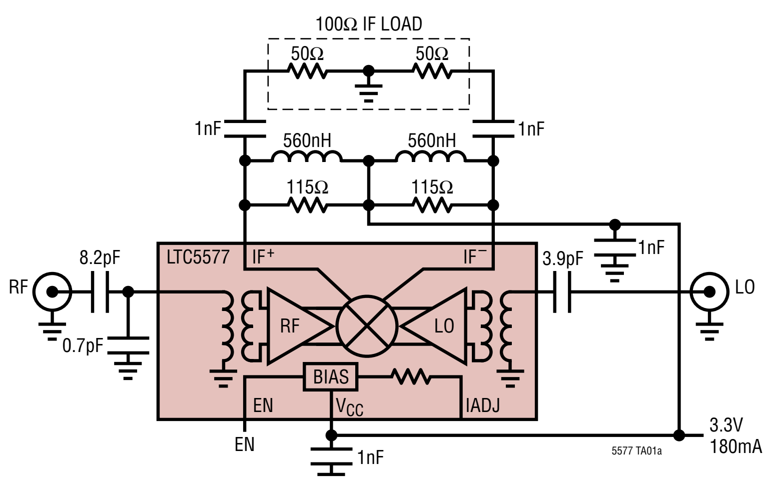
DESCRIPTION

The LTC®5577 active mixer is optimized for RF downconverting applications that require high input signal handling capability and wide bandwidth. The wideband IF output uses external resistors to set the output impedance, allowing the flexibility to match directly into differential IF loads, such as filters and amplifiers. The part is characterized and specified with a 100Ω differential output impedance, although it can be used with output impedances ranging from 50Ω to 400Ω, with higher gain and reduced IIP3 and P1dB at the higher impedance levels. The IF output is usable up to 1.5GHz.

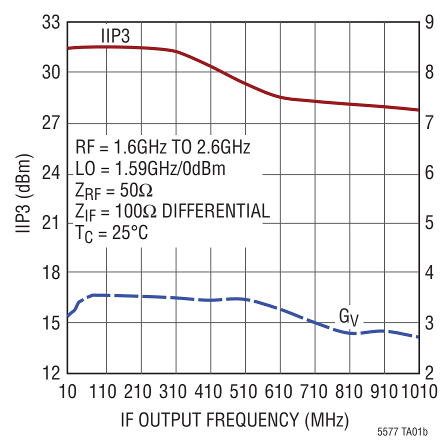
In receiver applications, the high input P1dB and IIP3 allow the use of higher gain low noise amplifiers, resulting in higher receiver sensitivity. Integrated transformers on the RF and LO inputs provide single-ended 50Ω interfaces, while minimizing the solution size.

TYPICAL APPLICATION

Wideband Downconverting Mixer with 1GHz IF Bandwidth and +15dBm Input P1dB into 100Ω Load



Voltage Conversion Gain and IIP3 vs IF Output Frequency



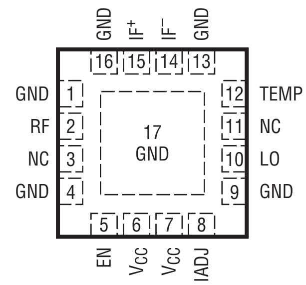
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}, IF^+, IF^-) 4.0V
Enable Input Voltage (EN) ....–0.3V to V_{CC} + 0.3V
LO Input Power (300MHz to 6GHz).................... +10dBm
LO Input DC Voltage... ±0.1V
RF Input Power (300MHz to 6GHz).................... +18dBm
RF Input DC Voltage... ±0.1V
TEMP Monitor Input Current.................................10mA
Operating Temperature Range (T_C)........ –40°C to 105°C
Junction Temperature (T_J) .... 150°C
Storage Temperature Range .... –65°C to 150°C

PIN CONFIGURATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

CAUTION: THIS PART IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD). PROPER ESD HANDLING PRECAUTIONS MUST BE OBSERVED.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5577IUF#PBF	LTC5577IUF#TRPBF	5577	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C, V_{CC} = 3.3V, EN = High. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Input Frequency Range	External Matching Required	●		300 to 6000		MHz
LO Input Frequency Range	External Matching Required	●		300 to 6000		MHz
IF Output Frequency Range	External Matching Required	●		1 to 1500		MHz
RF Input Return Loss	Z_O = 50Ω, 1300MHz to 4300MHz, C3 = 8.2pF, C4 = 0.7pF			>10		dB
LO Input Return Loss	Z_O = 50Ω, 930MHz to 4000MHz, C5 = 3.9pF			>10		dB
IF^+, IF^- Output Return Loss	Z_O = 50Ω, 20MHz to 500MHz, L1, L2 = 560nH, R1, R2 = 115Ω			>10		dB
LO Input Power			–6	0	6	dBm
RF to LO Isolation	RF = 300MHz to 2500MHz RF = 2500MHz to 4000MHz RF = 4000MHz to 6000MHz			>64 >50 >40		dB dB dB
RF to IF Isolation	RF = 300MHz to 6000MHz			>30		dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{LO} = 0dBm, IF = 153MHz, P_{RF} = –3dBm (–3dBm/tone for 2-tone tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Conversion Gain	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1900MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO RF = 4900MHz, Low Side LO, IF = 900MHz RF = 5900MHz, Low Side LO, IF = 900MHz		 –1.0	–0.5 0.5 0.7 0.5 0.2 0.1 –0.7		dB dB dB dB dB dB dB
Conversion Gain Flatness	RF = 1900 ±140MHz, LO = 1747MHz, IF = 153 ±140MHz			±0.2		dB
Conversion Gain vs Temperature	T_C = –40°C to 105ºC, RF = 1900MHz, Low Side LO	●		–0.013		dB/°C
2-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1900MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO RF = 4900MHz, Low Side LO, IF = 900MHz RF = 5900MHz, Low Side LO, IF = 900MHz			29.5 29.8 30.2 31.0 28.0 24.0 26.0		dBm dBm dBm dBm dBm dBm dBm
2-Tone Input 2nd Order Intercept (Δf_{RF} = 154MHz = f_{IM2})	RF = 450MHz (527MHz/373MHz), LO = 603MHz RF = 850MHz (927MHz/773MHz), LO = 1003MHz RF = 1900MHz (1977MHz/1823MHz), LO = 1747MHz RF = 2550MHz (2627MHz/2473MHz), LO = 2397MHz RF = 3500MHz (3577MHz/3423MHz), LO = 3347MHz			68 68 61 60 66		dBm dBm dBm dBm dBm
SSB Noise Figure	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1900MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO RF = 4900MHz, Low Side LO, IF = 900MHz RF = 5900MHz, Low Side LO, IF = 900MHz			13.4 11.7 11.8 12.5 14.3 15.2 15.0	 14.0	dB dB dB dB dB dB dB
SSB Noise Figure Under Blocking	RF = 850MHz, High Side LO, 750MHz Blocker at 5dBm RF = 1900MHz, Low Side LO, 2000MHz Blocker at 5dBm			16.1 15.8		dB dB
1/2IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	850MHz: f_{RF} = 926.5MHz at –3dBm, f_{LO} = 1003MHz 1900MHz: f_{RF} = 1823.5MHz at –3dBm, f_{LO} = 1747MHz			–85 –79		dBc dBc
1/3IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	850MHz: f_{RF} = 952MHz at –3dBm, f_{LO} = 1003MHz 1900MHz: f_{RF} = 1798MHz at –3dBm, f_{LO} = 1747MHz			–86 –81		dBc dBc
Input 1dB Compression	RF = 450MHz, High Side LO RF = 850MHz, High Side LO RF = 1900MHz, Low Side LO RF = 2550MHz, Low Side LO RF = 3500MHz, Low Side LO RF = 4900MHz, Low Side LO, IF = 900MHz RF = 5900MHz, Low Side LO, IF = 900MHz			15.7 15.3 15.2 15.6 15.4 14.0 13.5		dBm dBm dBm dBm dBm dBm dBm
LO to RF Leakage	LO = 300MHz to 2500MHz LO = 2500MHz to 5200MHz LO = 5200MHz to 6000MHz			≤60 ≤50 ≤35		dBm dBm dBm
LO to IF Leakage	LO = 300MHz to 1800MHz LO = 1800MHz to 6000MHz			≤28 ≤33		dBm dBm

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C, V_{CC} = 3.3V, EN = High, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})			●	3.0	3.3	3.6	V
Supply Current	Enabled Disabled	EN = High EN = Low			180	217 200	mA µA
Enable Logic Input (EN)							
Input High Voltage (On)			●	2.5			V
Input Low Voltage (Off)			●			0.3	V
Input Current		–0.3V to V_{CC} + 0.3V		–60		200	µA
Turn-On Time					0.3		µs
Turn-Off Time					0.1		µs
Mixer DC Current Adjust (IADJ)							
Open-Circuit DC Voltage					2.2		V
Short-Circuit DC Current		Pin Shorted to Ground			3.6		mA
Temperature Sensing Diode (TEMP)							
DC Voltage at T_J = 25°C		I_{IN} = 10µA I_{IN} = 80µA			716 773		mV mV
Voltage Temperature Coefficient		I_{IN} = 10µA I_{IN} = 80µA	● ●		–1.75 –1.56		mV/°C mV/°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5577 is guaranteed functional over the –40°C to 105°C case temperature range (θ_{JC} = 8°C/W).

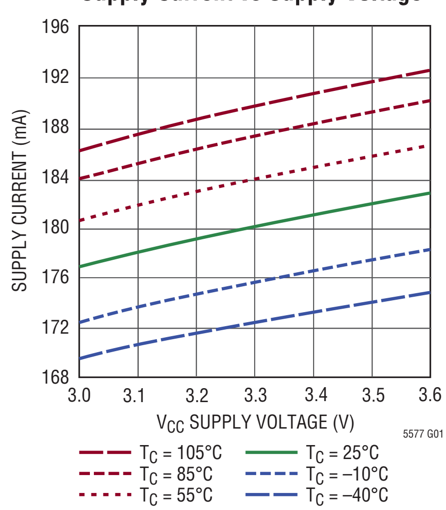
Note 3: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 2dB matching pad on RF input, and bandpass filter on the LO input.

Note 4: Specified performance excludes external 180° IF combiner loss.

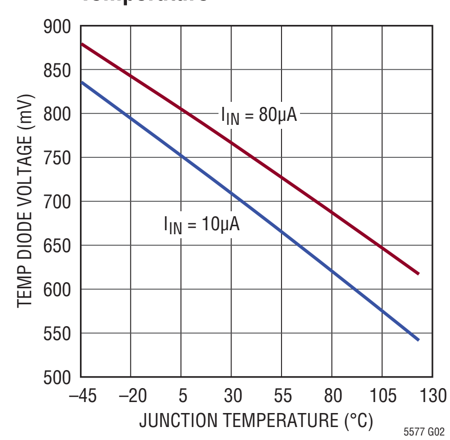
TYPICAL DC PERFORMANCE CHARACTERISTICS

EN = High, Test circuit shown in Figure 1.

Supply Current vs Supply Voltage



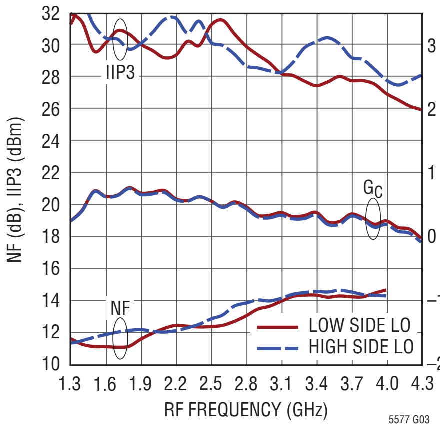
TEMP Diode Voltage vs Junction Temperature



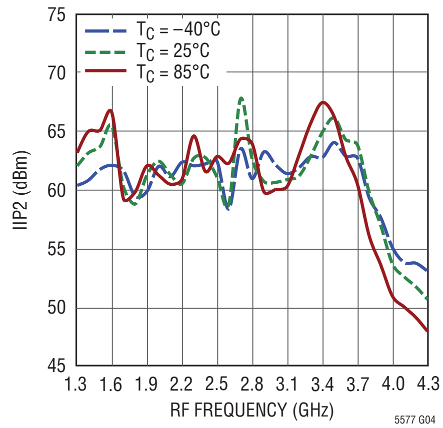
TYPICAL PERFORMANCE CHARACTERISTICS

1300MHz to 4300MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted.

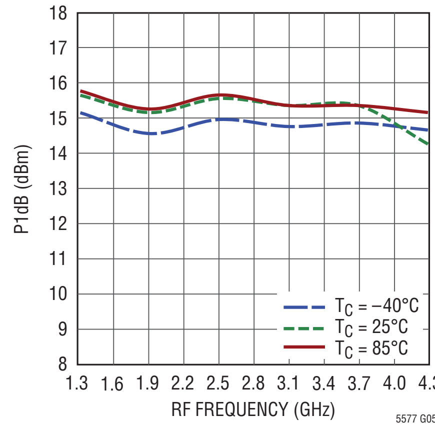
Conversion Gain, IIP3 and NF vs RF Frequency



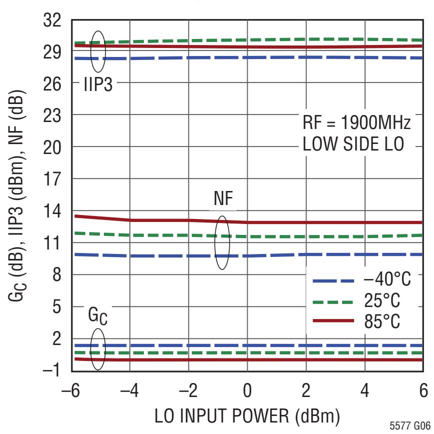
2-Tone IIP2 vs RF Frequency (Δf_{RF} = 154MHz = f_{IM2})



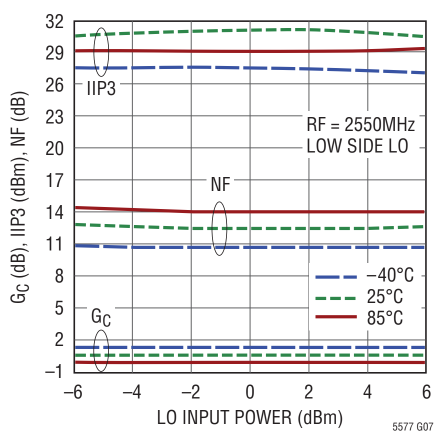
RF Input P1dB vs RF Frequency



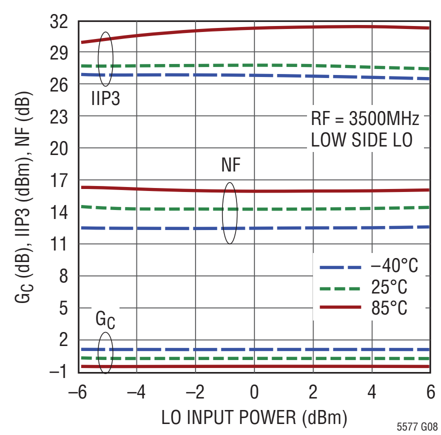
1900MHz Conversion Gain, IIP3 and NF vs LO Power



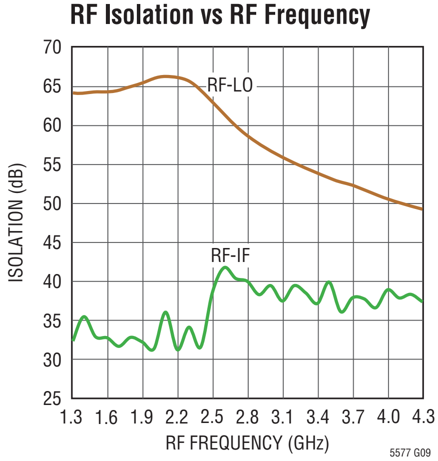
2550MHz Conversion Gain, IIP3 and NF vs LO Power



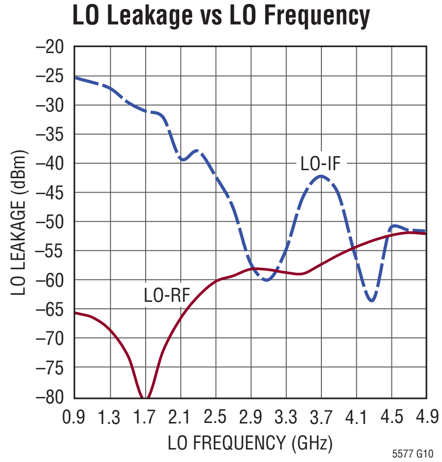
3500MHz Conversion Gain, IIP3 and NF vs LO Power



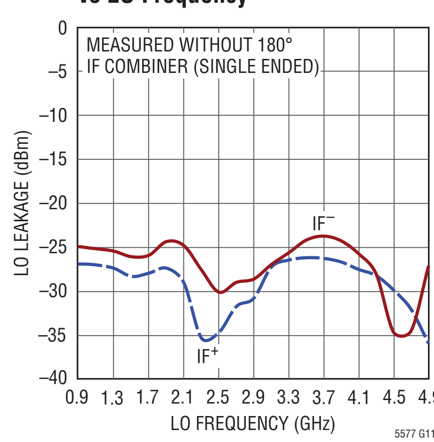
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



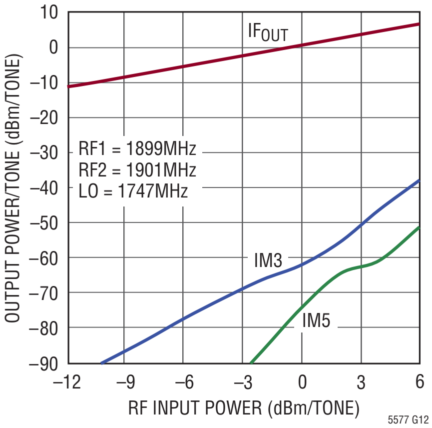
LO to Unbalanced IF Port Leakage vs LO Frequency



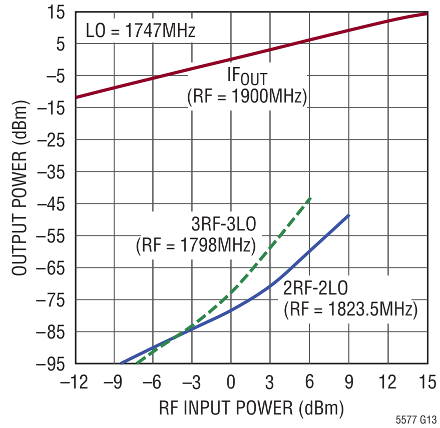
TYPICAL PERFORMANCE CHARACTERISTICS

1300MHz to 4300MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted.

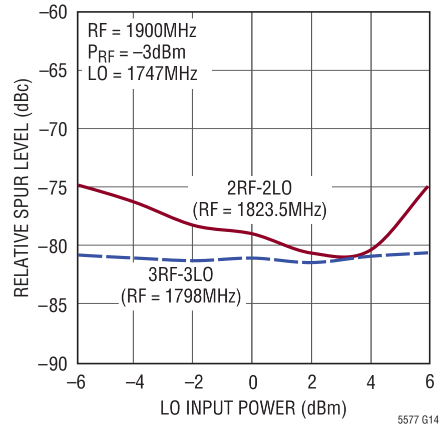
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



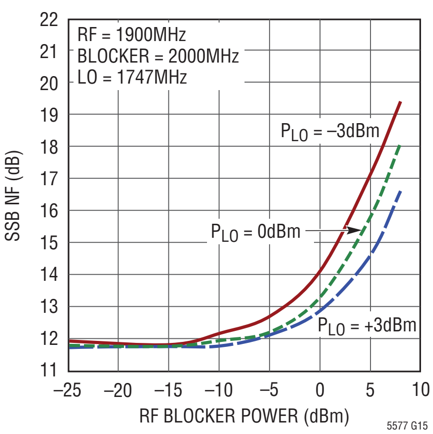
Single Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



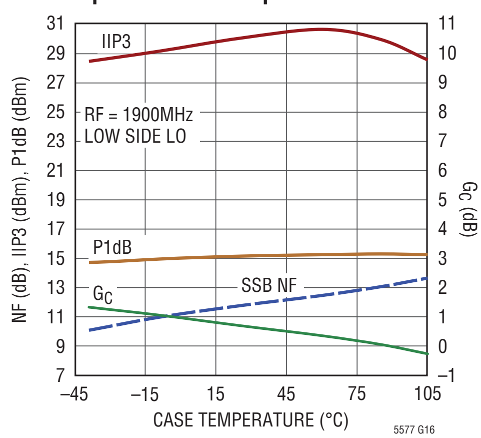
2 × 2 and 3 × 3 Spur Suppression vs LO Power



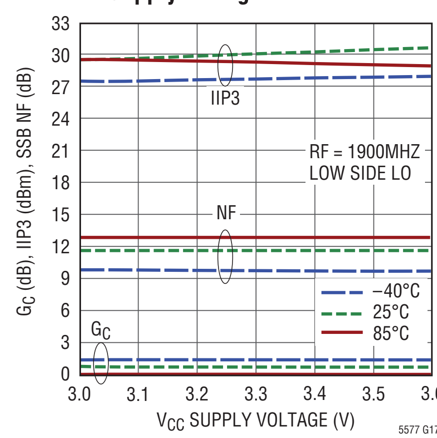
SSB Noise Figure vs RF Blocker Level



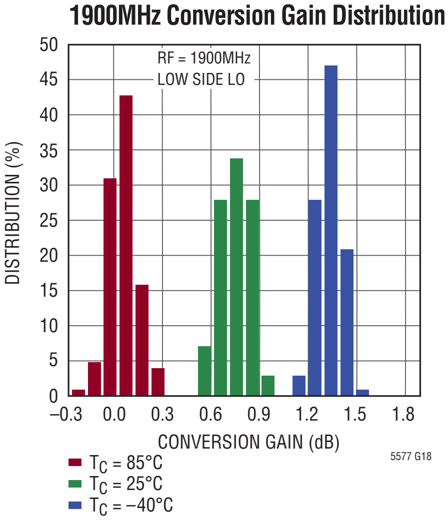
Conversion Gain, IIP3, NF and RF Input P1dB vs Temperature



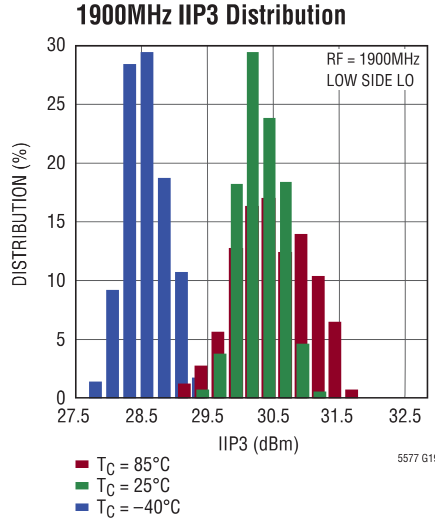
Conversion Gain, IIP3 and NF vs Supply Voltage



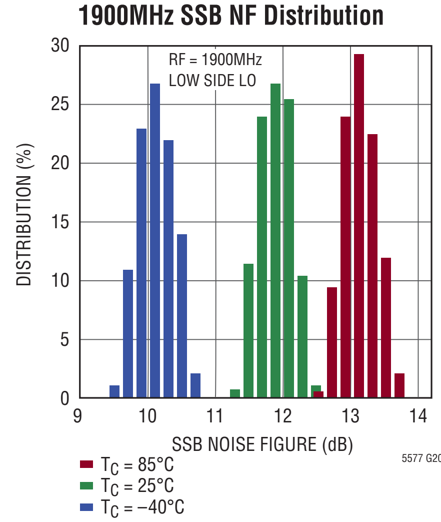
1900MHz Conversion Gain Distribution



1900MHz IIP3 Distribution



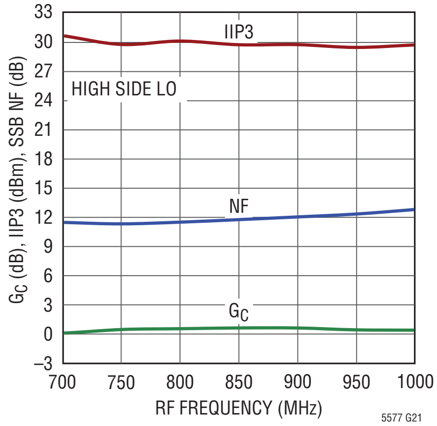
1900MHz SSB NF Distribution



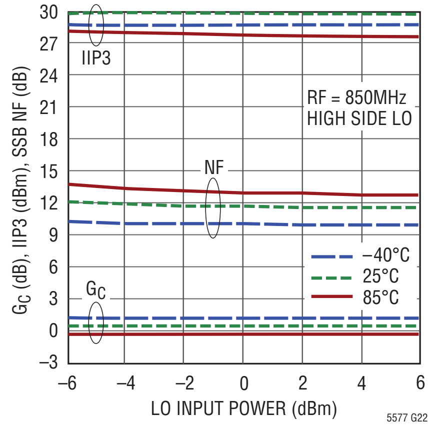
TYPICAL PERFORMANCE CHARACTERISTICS

700MHz to 1000MHz application. Test circuit shown in Figure 1. $V_{CC} = 3.3V$, $T_C = 25°C$, $P_{LO} = 0dBm$, $P_{RF} = –3dBm$ (–3dBm/tone for 2-tone IIP3 tests, $\Delta f = 2MHz$), IF = 153MHz, unless otherwise noted.

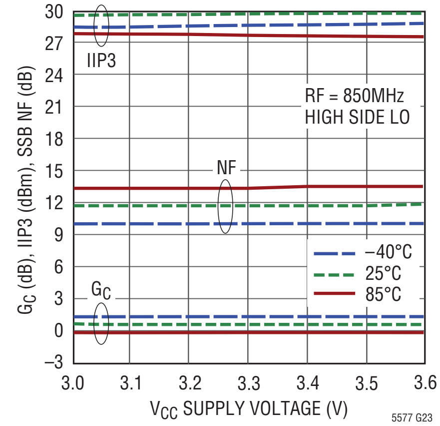
Conversion Gain, IIP3 and NF vs RF Frequency



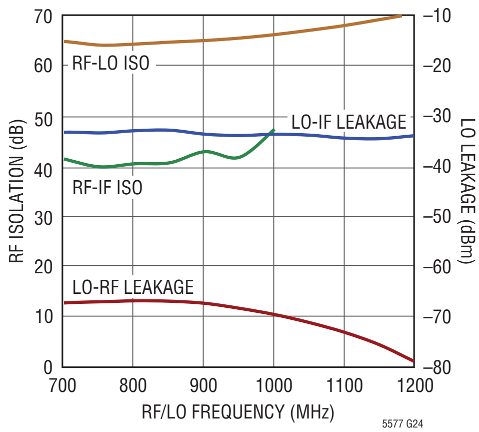
850MHz Conversion Gain, IIP3 and NF vs LO Power



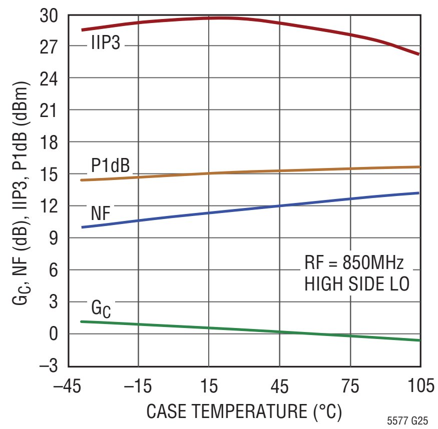
850MHz Conversion Gain, IIP3 and NF vs Supply Voltage



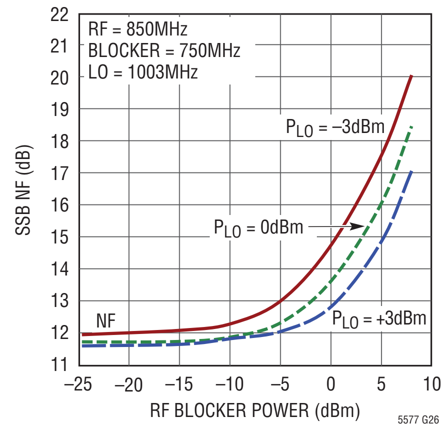
RF Isolation and LO Leakage vs Frequency



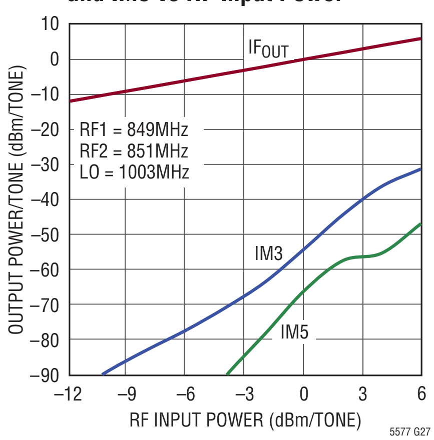
Conversion Gain, IIP3, NF and RF Input P1dB vs Temperature



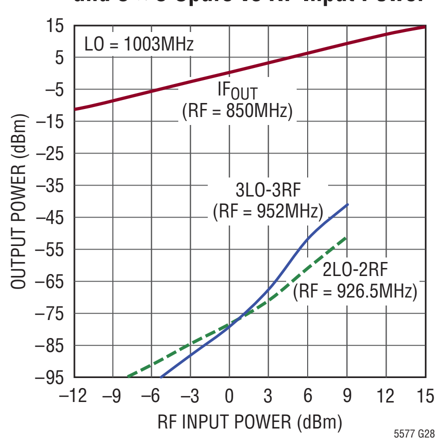
SSB Noise Figure vs RF Blocker Power



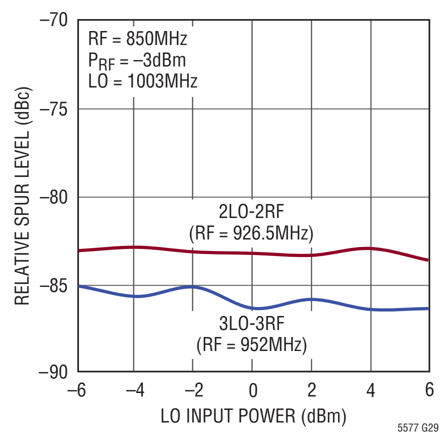
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



Single Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



2 × 2 and 3 × 3 Spur Suppression vs LO Power



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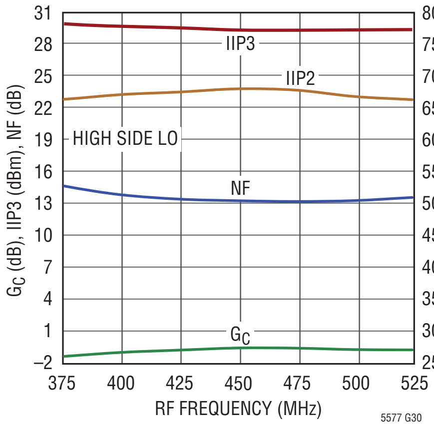
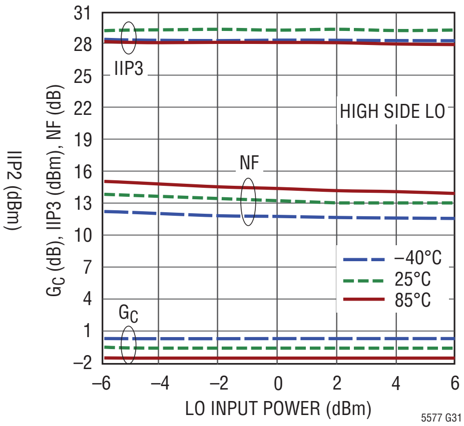
TYPICAL PERFORMANCE CHARACTERISTICS

375MHz to 525MHz application. Test circuit shown in Figure 1. $V_{CC} = 3.3V$, $T_C = 25°C$, $P_{LO} = 0dBm$, $P_{RF} = –3dBm$ (–3dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 153MHz, unless otherwise noted.

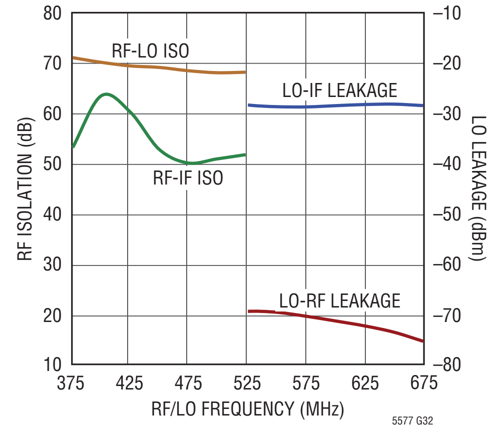
Conversion Gain, IIP3, IIP2 and NF vs RF Frequency



450MHz Conversion Gain, IIP3 and NF vs LO Power

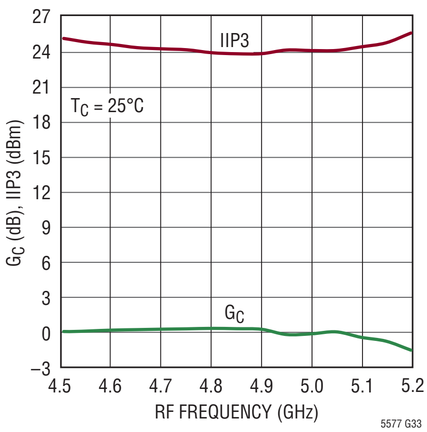


RF Isolation and LO Leakage vs Frequency

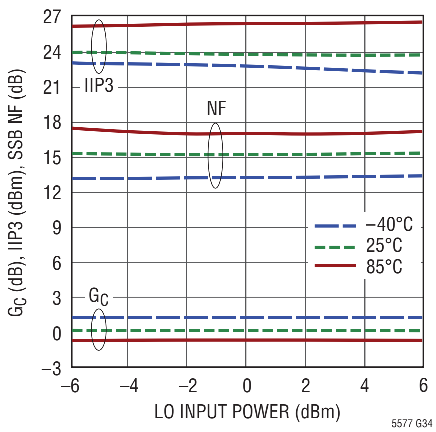


4.9GHz and 5.9GHz applications. IF = 900MHz, Low Side LO, $P_{LO} = 0dBm$. Test circuit shown in Figure 1.

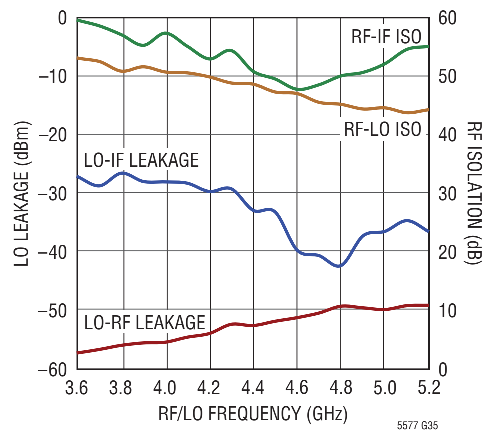
Conversion Gain and IIP3 vs RF Frequency (4.9GHz Application)



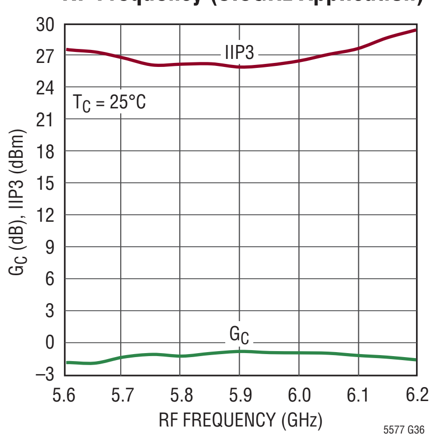
4.9GHz Conversion Gain, IIP3 and NF vs LO Power



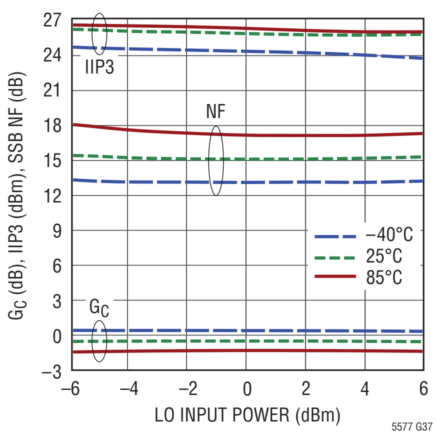
RF Isolation and LO Leakage vs Frequency (4.9GHz Application)



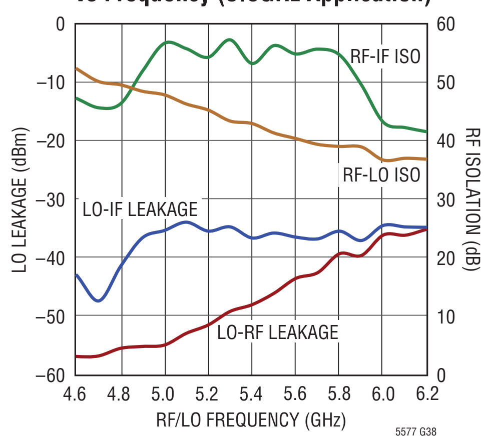
Conversion Gain and IIP3 vs RF Frequency (5.9GHz Application)



5.9GHz Conversion Gain, IIP3 and NF vs LO Power



RF Isolation and LO Leakage vs Frequency (5.9GHz Application)



PIN FUNCTIONS

GND (Pins 1, 4, 9, 13, 16, Exposed Pad Pin 17): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

RF (Pin 2): Single-Ended RF Input. This pin is internally connected to the primary winding of the integrated RF transformer, which has low DC resistance to ground. **A series DC-blocking capacitor must be used if the RF source has DC voltage present.** The RF input is 50Ω impedance matched, using the matching element values shown in Figure 1, when the mixer is enabled.

NC (Pins 3, 11): These pins are not connected internally. They can be left floating, connected to ground, or to V_{CC}.

EN (Pin 5): Enable Pin. When the input voltage is greater than 2.5V, the mixer is enabled. When the input voltage is less than 0.3V, the mixer is disabled. Typical input current is less than 30µA. This pin has an internal pull-down resistor.

V_{CC} (Pins 6, 7): Power Supply Pins. These pins must be connected to a regulated 3.3V supply, with a bypass capacitor located close to the pin. Typical DC current consumption is 68mA.

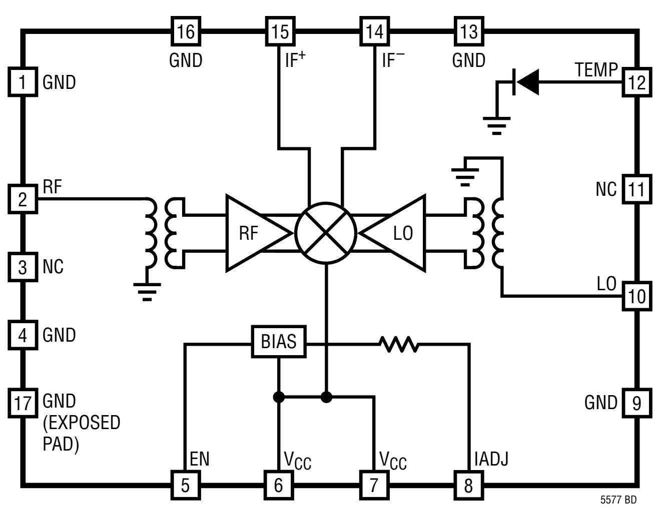
IADJ (Pin 8): Mixer Core Current Adjust Pin. Connecting a resistor between this pin and ground will reduce the mixer core DC supply current. Typical open-circuit DC voltage is 2.2V. This pin should be left floating for optimum performance.

LO (Pin 10): Single-Ended Local Oscillator Input. This pin is internally connected to the primary winding of an integrated transformer, which has low DC resistance to ground. **A series DC-blocking capacitor must be used to avoid damage to the internal transformer.** This input is 50Ω impedance matched from 930MHz to 4GHz, even when the IC is disabled. Operation down to 300MHz or up to 6GHz is possible with the external matching shown in Figure 1.

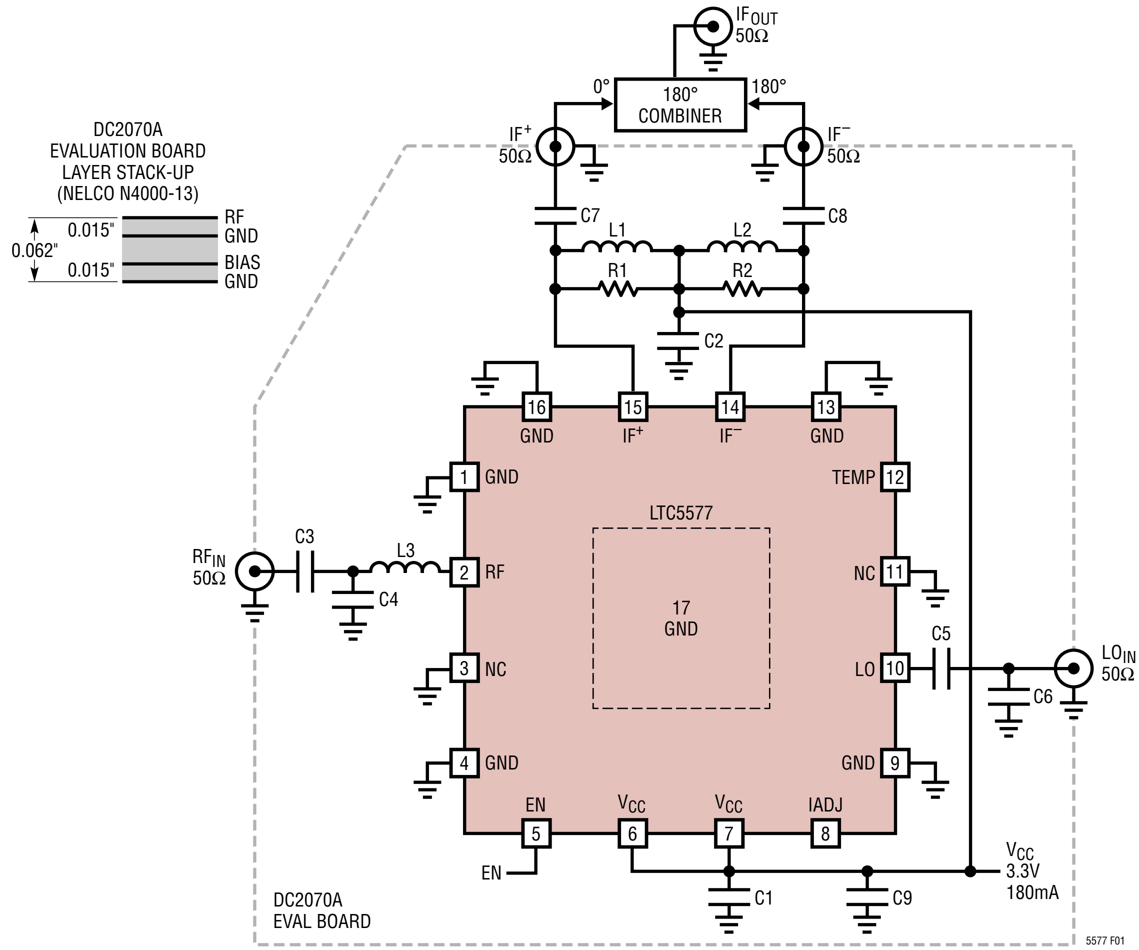
TEMP (Pin 12): Temperature Sensing Diode. This pin is connected to the anode of a diode that may be used to measure the die temperature, by forcing a current and measuring the voltage.

IF^+/IF^- (Pin 15/Pin 14): Open-Collector Differential IF Output. These pins must be connected to the V_{CC} supply through impedance-matching inductors or a transformer center tap. Typical DC current consumption is 56mA into each pin.

BLOCK DIAGRAM



TEST CIRCUIT



APPLICATION		RF MATCH			LO MATCH		IF MATCH
RF (MHz)	LO	C3	C4	L3	C5	C6	L1, L2
300 to 400	HS	330pF	18pF	2.2nH	47pF	15pF	560nH
375 to 525	HS	330pF	15pF	2nH	27pF	8.2pF	560nH
700 to 1000	HS	330pF	6pF	—	6.8pF	2.7pF	560nH
1300 to 4300	LS, HS	8.2pF	0.7pF	—	3.9pF	—	560nH
4900	LS	1.8nH (L)	0.7pF	—	1pF	—	10nH*
5900	LS	0.25pF	—	—	1pF	—	10nH*

LS = Low side, HS = High side. *IF = 900MHz

REF DES	VALUE	SIZE	VENDOR
C1, C2, C7, C8	1nF	0402	Murata
C3 - C6	See Table	0402	Murata
R1, R2	115Ω, 1%	0402	
C9	1µF	0603	AVX
L1, L2	See Table	0603	Coilcraft 0603LS
L3	See Table	0402	Coilcraft 0402HP

Figure 1. Standard Downmixer Test Circuit Schematic (Wideband 100Ω Differential IF Output)

APPLICATIONS INFORMATION

Introduction

The LTC5577 incorporates a high linearity double-balanced active mixer, a high-speed limiting LO buffer and bias/enable circuits. See the Pin Functions and Block Diagram sections for a description of each pin. A test circuit schematic showing all external components required for the data sheet specified performance is shown in Figure 1. A few additional components may be used to modify the DC supply current or frequency response, which will be discussed in the following sections.

The LO and RF inputs are single ended. The test circuit, shown in Figure 1, is configured with a 100Ω differential IF output. An external broadband 180° passive combiner is used to combine the differential IF outputs to 50Ω single-ended for characterization and test purposes. The evaluation board layout is shown in Figure 2.

RF Input

A simplified schematic of the mixer's RF input is shown in Figure 3. As shown, one terminal of the integrated RF transformer's primary winding is connected to Pin 2, while the other terminal is DC-grounded internally. For this reason, a series DC-blocking capacitor (C3) is needed if the RF source has DC voltage present. The DC resistance of the primary winding is approximately 3Ω. The secondary winding of the RF transformer is internally connected to the RF buffer amplifier.

ESD protection diodes are not used on the RF input due to the high RF voltage swing associated with the LTC5577's high IIP3 and input P1dB. The internal RF transformer provides some protection for the RF matching capacitor against human-body model ESD strikes up to 3kV. Proper ESD handling techniques must be employed to avoid damaging this capacitor.

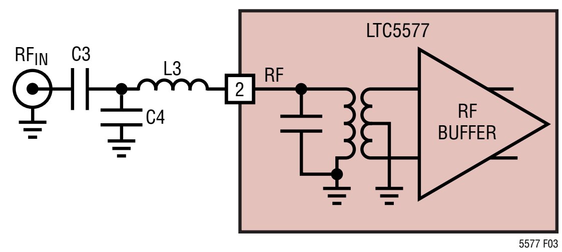


Figure 3. RF Input Schematic

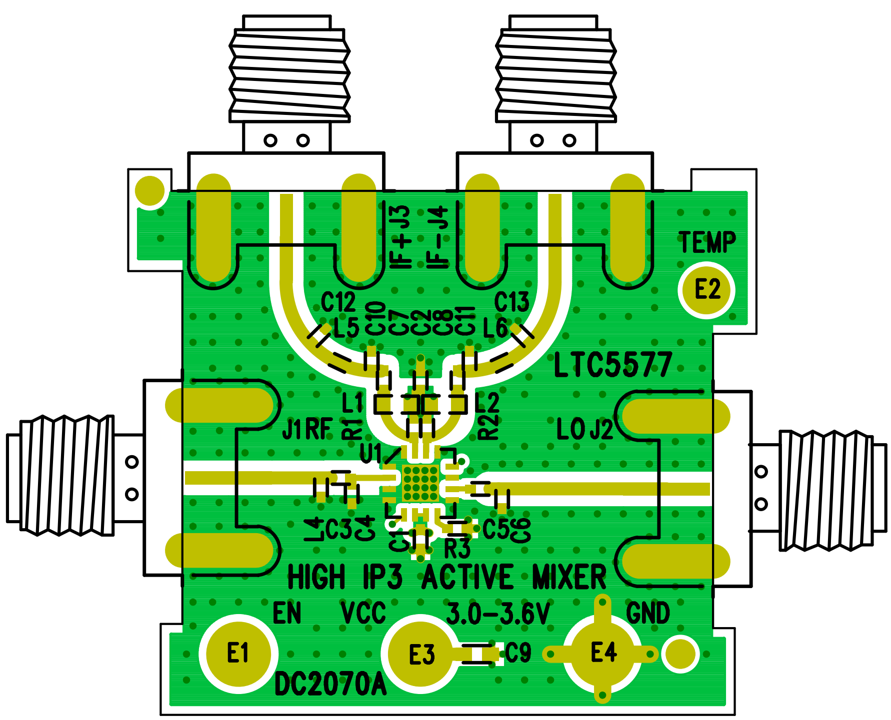


Figure 2. Evaluation Board Layout

APPLICATIONS INFORMATION

The RF input is 50Ω matched from 1300MHz to 4300MHz using C3 = 8.2pF and C4 = 0.7pF. Matching to RF frequencies above or below this frequency range is easily accomplished by using the the element values shown in Figure 1. For RF frequencies below 500MHz, series inductor L3 is also needed. The evaluation board does not have provisions for L3, so the RF input trace needs to be cut to install it in series. Measured RF input return losses are shown in Figure 4. The RF input impedance and input reflection coefficient, versus frequency are listed in Table 1.

Table 1. RF Input Impedance and S11 (at Pin 2, No External Matching, Mixer Enabled)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
200	4.4 + j8.5	0.84	163
350	6.6 + j12.0	0.78	153
450	8.3 + j14.4	0.74	147
575	10.1 + j17.2	0.69	141
700	12.0 + j19.9	0.66	136
900	15.4 + j22.8	0.60	127
1100	18.9 + j25.9	0.55	120
1400	25.2 + j29.5	0.48	109
1700	33.2 + j30.9	0.40	98
1950	40.0 + j29.1	0.33	91
2200	45.2 + j24.3	0.25	87
2450	47.1 + j18.0	0.18	89
2700	44.7 + j12.8	0.15	105
3000	39.1 + j10.7	0.17	129
3300	33.0 + j13.8	0.26	132
3600	28.4 + j20.1	0.36	123
3900	25.2 + j29.1	0.48	109
4200	23.5 + j39.1	0.57	95
4500	22.8 + j52.1	0.66	82
4800	23.6 + j66.1	0.72	70
5400	28.6 + j98.2	0.80	51
6000	38.0 + j134.4	0.84	38

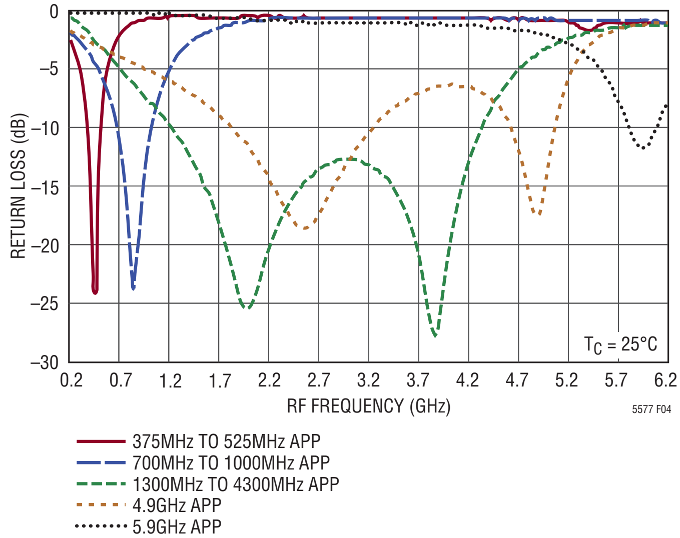


Figure 4. RF Input Return Loss

LO Input

A simplified schematic of the LO input, with external components is shown in Figure 5. Similar to the RF input, the integrated LO transformer's primary winding is DC-grounded internally, and therefore requires an external DC-blocking capacitor. Capacitor C5 provides the necessary DC-blocking, and optimizes the LO input match over the 930MHz to 4GHz frequency range. The nominal LO input level is 0dBm although the limiting amplifiers will deliver excellent performance over a ±6dB input power range. LO input power greater than +6dBm may cause conduction of the internal ESD diodes.

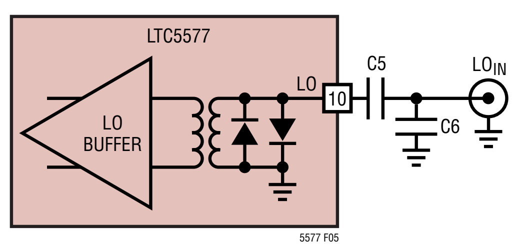


Figure 5. LO Input Schematic

APPLICATIONS INFORMATION

To optimize the LO input match for frequencies below 1GHz, the value of C5 is increased and shunt capacitor C6 is added. A summary of values for C5 and C6, versus LO frequency range is listed in Table 2. Measured LO input return losses are shown in Figure 6. Finally, LO input impedance and input reflection coefficient, versus frequency is shown in Table 3.

Table 2. LO Input Matching Values vs LO Frequency Range

FREQUENCY (MHz)	C5 (pF)	C6 (pF)
285 to 392	330	33
338 to 415	330	22
415 to 505	56	18
525 to 700	27	8.2
645 to 803	15	7.5
800 to 1150	6.8	2.7
930 to 4000	3.9	—
3500 to 6000	1.0	—

The LO buffers have been designed such that the LO input impedance does not change significantly when the IC is disabled. This feature only requires that supply voltage is applied. The actual performance of this feature is shown in Figure 7. As shown, the LO input return loss is better than 10dB over the 1GHz to 4GHz frequency range when the IC is enabled or disabled.

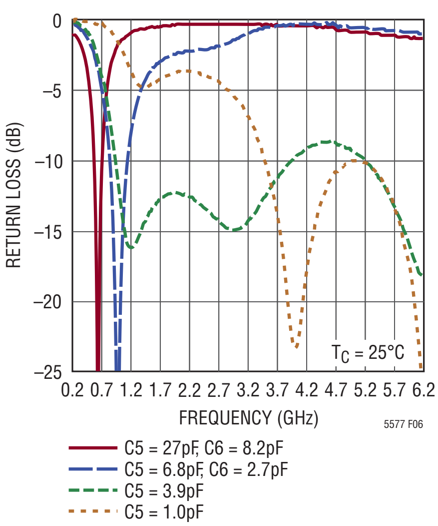


Figure 6. LO Input Return Loss

Table 3. LO Input Impedance and S11 (at Pin 10, No External Matching, Mixer Enabled)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
350	5.2 + j14.9	0.83	146.5
400	6.0 + j17.3	0.81	141.7
450	6.6 + j19.5	0.80	137.0
500	7.2 + j21.5	0.78	132.7
600	9.1 + j26.5	0.75	123.6
800	15.1 + j35.7	0.67	106.0
1000	24.9 + j43.6	0.58	89.5
1500	67.5 + j36.4	0.33	47.1
2000	61.7 – j4.2	0.11	–18.3
2500	40.3 – j7.1	0.13	–139.4
3000	31.7 + j1.8	0.23	173.1
3500	29.8 + j12.3	0.29	140.0
4000	31.5 + j22.9	0.35	113.2
4500	36.0 + j32.4	0.38	92.8
5000	59.0 + j40.6	0.36	57.1
5500	64.2 + j30.8	0.29	50.1
6000	57.4 + j19.7	0.19	59.0

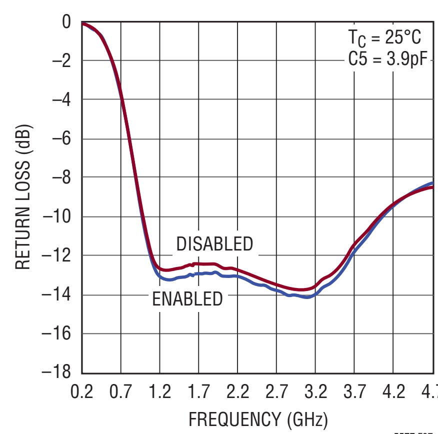


Figure 7. LO Input Return Loss—Mixer Enabled and Disabled

APPLICATIONS INFORMATION

IF Output

The IF output schematic with external matching components is shown in Figure 8. As shown, the output is differential open collector. Each IF output pin must be biased at the supply voltage (V_{CC}), which is applied through the external matching inductors (L1 and L2) shown in Figure 8. Each pin draws approximately 56mA of DC supply current (112mA total). Inductors with less than 1Ω DC resistance, such as Coilcraft 0603LS, are required for the highest IIP3 and P1dB.

The differential IF output impedance can be modeled as a frequency-dependent parallel R-C circuit, using the values listed in Table 4. This data is referenced to the package pins (with no external components) and includes the effects of the IC and package parasitics. Resistors R1 and R2 are used to reduce the output resistance, which increases the IF bandwidth and input P1dB, but reduces the conversion gain.

100Ω Differential IF Output Matching

The standard downmixer test circuit shown in Figure 1 uses 115Ω resistors to realize a 100Ω differential output. 560nH pull-up inductors are used to deliver a broadband IF output from 10MHz to greater than 600MHz. C7 and C8 are 1nF DC-blocking capacitors.

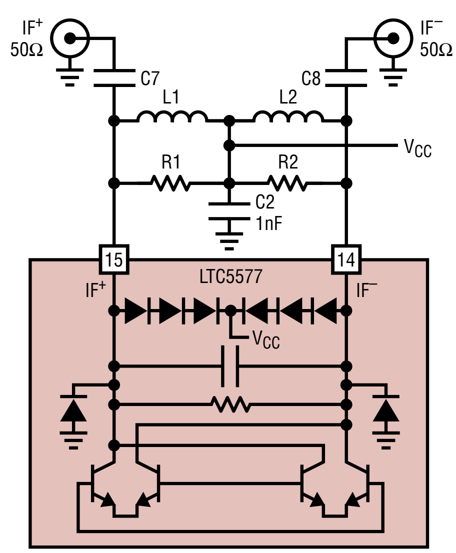


Figure 8. IF Output Schematic with External Matching

To match the IF output for frequencies greater than 600MHz, the values of L1 and L2 are selected to resonate with the internal IF capacitance (C_{IF}) at the desired IF center frequency, using the following equation:

$$L1, L2 = \frac{1}{(2 \bullet \pi \bullet f_{IF})^2 \bullet 2 \bullet C_{IF}}$$

Table 4 summarizes the optimum IF matching element values, versus IF center frequency, to be used in the standard downmixer test circuit shown in Figure 1. The inductor values are slightly less than the ideal calculated values due to the additional capacitance of the evaluation board traces. Measured differential IF output return losses are shown in Figure 9.

Table 4. IF Output Impedance and Bandpass Matching Element Values vs IF Frequency.

IF FREQUENCY (MHz)	DIFFERENTIAL IF OUTPUT IMPEDANCE (R_{IF}‖C_{IF})	EXTERNAL MATCHING ELEMENT VALUES (100Ω DIFFERENTIAL OUTPUT)	
		L1, L2	R1, R2
10-600	390Ω‖1.55pF	560nH	115Ω
450	390Ω‖1.55pF	39nH	115Ω
800	367Ω‖1.68pF	10nH	115Ω
1000	343Ω‖1.73pF	6nH	133Ω
1200	317Ω‖1.81pF	3.3nH	191Ω
1400	261Ω‖1.91pF		
1600	212Ω‖2.02pF		
1800	156Ω‖2.19pF		
2000	105Ω‖2.43pF		

APPLICATIONS INFORMATION

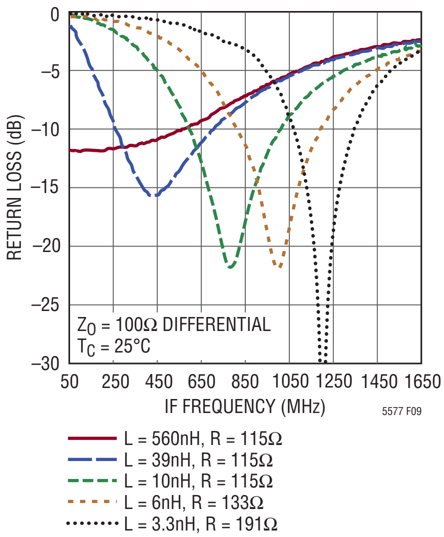


Figure 9. Differential IF Output Return Loss—100Ω Differential Load

Wideband 50Ω Single-Ended IF Output Matching

For applications that require a 50Ω single-ended IF output, a 2:1 transformer can be added to the 100Ω differential output as shown in Figure 10. Recommended transformers include the Mini-Circuits TC2-1T+, or Coilcraft WBC2-1T. No other IF matching element changes are required.

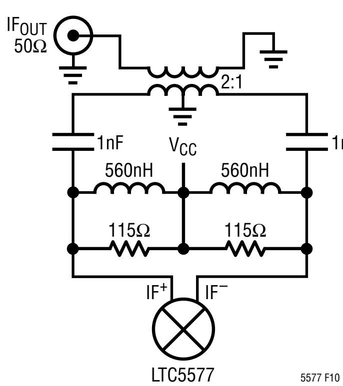


Figure 10. 50Ω Single-Ended IF Output

Measured conversion gain and IIP3 using a Mini-Circuits TC2-1T+ (2:1) IF transformer are shown in Figure 11, with the measured performance of the standard 100Ω differential output for comparison. As shown, the single-ended conversion gain is about 0.5dB less up to 700MHz due to the transformer loss. Above 700MHz, the IF transformer loss increases rapidly. Up to 600MHz, both solutions have similar IIP3. Above 600MHz, the transformer version has about 1dB lower IIP3.

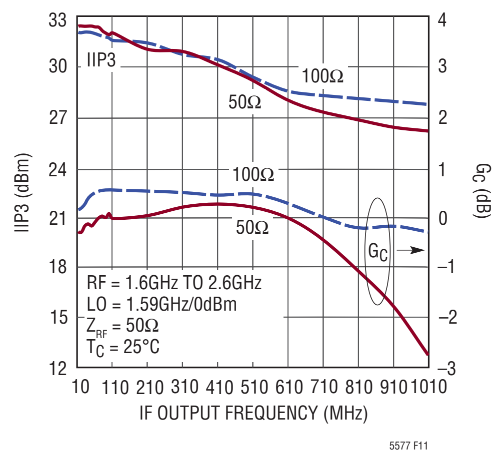


Figure 11. Conversion Gain and IIP3 vs IF Output Frequency. 50Ω Single-Ended Output Using a Transformer vs 100Ω Differential Output

APPLICATIONS INFORMATION

Mixer Bias Current Reduction

The IADJ pin (Pin 8) is available for reducing the mixer core DC current consumption at the expense of linearity and P1dB. For the highest performance, this pin should be left floating. As shown in Figure 12, an internal bias circuit produces a 6mA reference current for the mixer core. If a resistor is connected to Pin 8, as shown in Figure 12, a portion of the reference current can be shunted to ground, resulting in reduced mixer core current. For example, R3 = 220Ω will shunt away 3mA from Pin 8 and reduce the mixer core current by 50%. The nominal, open-circuit DC voltage at the IADJ pin is 2.2V. Table 5 lists DC supply current and RF performance at 1900MHz for various values of R3.

Table 5. Mixer Performance with Reduced Current (RF = 1900MHz, Low Side LO, IF = 153MHz)

R3 (Ω)	I_{CC} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
Open	180	0.7	30.2	15.2	11.8
2k	166	0.6	28.0	15.0	11.1
1k	156	0.5	26.7	14.8	10.9
220	133	0.2	23.9	13.4	10.4
120	125	0.0	22.3	12.4	10.3
75	122	0.0	22.0	12.0	10.3

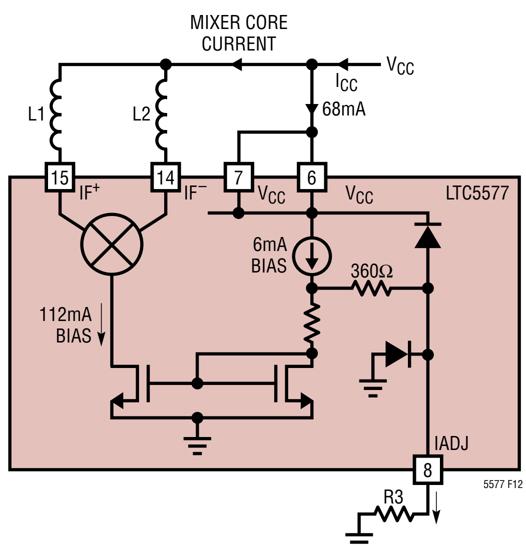


Figure 12. IADJ Interface

APPLICATIONS INFORMATION

Enable Interface

Figure 13 shows a simplified schematic of the enable interface. To enable the mixer, the EN voltage must be higher than 2.5V. If the enable function is not required, the pin should be connected directly to V_{CC}. The voltage at the EN pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

The EN pin has an internal 300k pull-down resistor. Therefore, the mixer will be disabled with the enable pin left floating.

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD clamp circuits connected to the V_{CC} pin. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the 4.0V maximum rating. A supply voltage ramp time greater than 1ms is recommended.

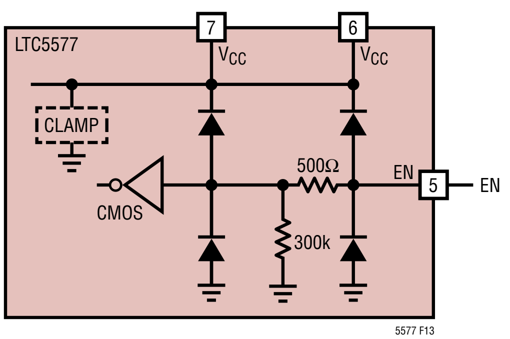


Figure 13. Enable Input Circuit

Spurious Output Levels

Mixer spurious output levels versus harmonics of the RF and LO are tabulated in Table 6. The spur levels were measured on a standard evaluation board using the test circuit shown in Figure 1. Table 6a shows the relative spur levels with an RF input power level of –3dBm while Table 6b shows the same relative spur levels with the RF input power reduced to –6dBm.

The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) – (N \bullet f_{LO})$$

Table 6. IF Output Spur Levels (dBc). RF = 1900MHz, IF = 153MHz, Low Side LO, P_{LO} = 0dBm, V_{CC} = 3.3V, T_C = 25°C

Table 6a. P_{RF} = –3dBm

		N								
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
M	**0**		–25	–35	–35	–39	–55	–35	–58	–55
	1	–34	0	–34	–18	–46	–41	–71	–53	–72
	2	–72	–59	–70	–65	–81	*	–81	*	–76
	3	*	–70	*	–79	*	–86	*	–83	*
	4	–88	*	–90	*	*	*	*	*	*
	5	*	*	*	*	*	*	*	*	*
	6	*	–88	*	*	*	*	*	*	*
	7	*	–88	*	*	*	*	*	*	*

*Less than –90dBc

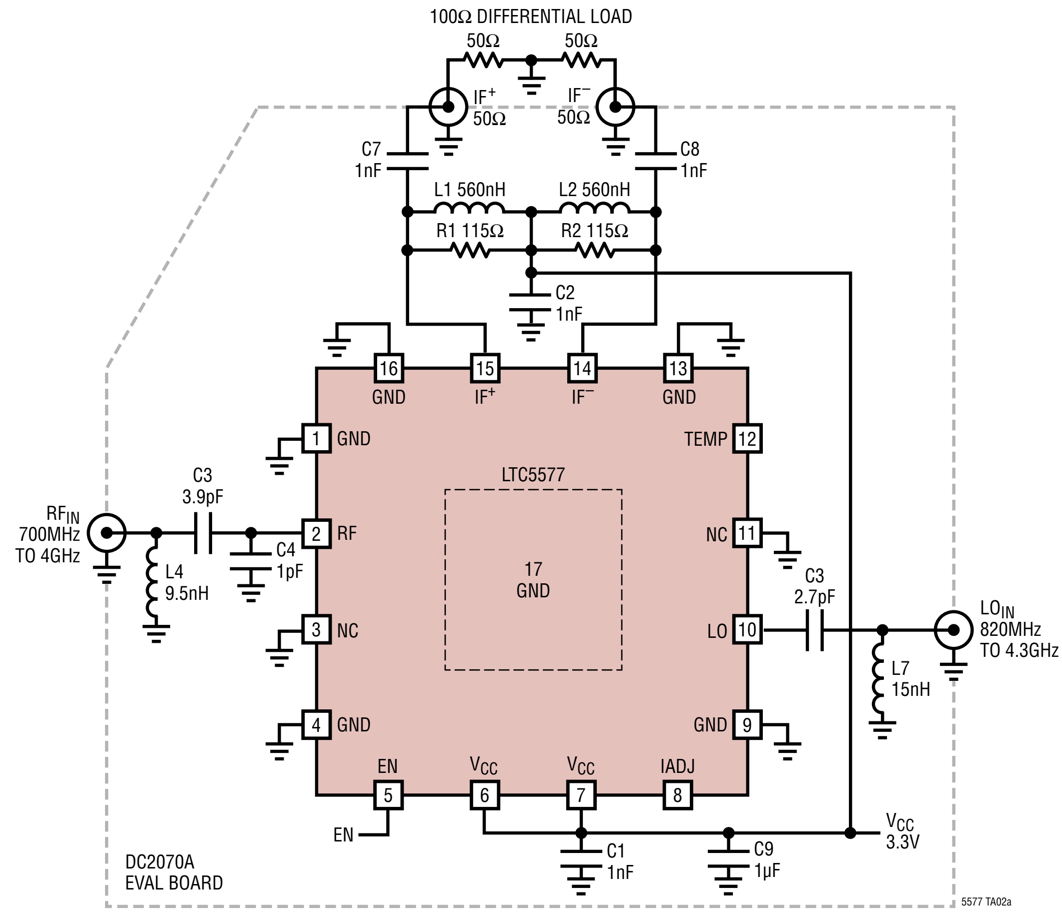
Table 6b. P_{RF} = –6dBm

		N								
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
M	**0**		–22	–31	–18	–36	–41	–32	–55	–51
	1	–34	0	–34	–68	–46	–86	–71	–53	–73
	2	–76	–62	–73	–84	–84	*	–85	*	–80
	3	–87	–76	*	*	*	*	*	*	*
	4	*	*	–87	*	*	*	*	*	*
	5	*	–87	*	*	*	*	*	*	*
	6	*	*	*	*	*	*	*	*	*
	7	*	–86	*	*	*	*	*	*	*

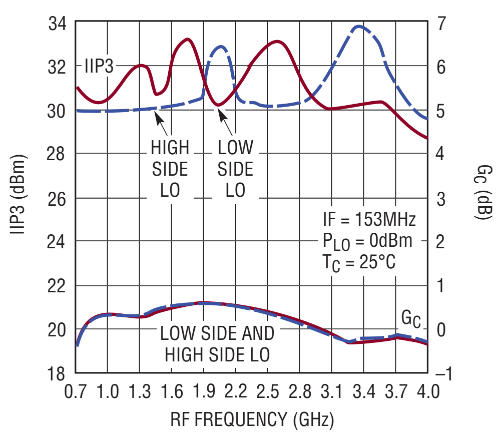
*Less than –90dBc

TYPICAL APPLICATIONS

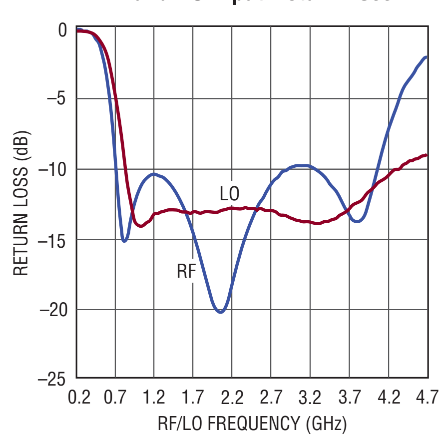
700MHz to 4GHz Wideband RF Application



Conversion Gain and IIP3 vs RF Input Frequency



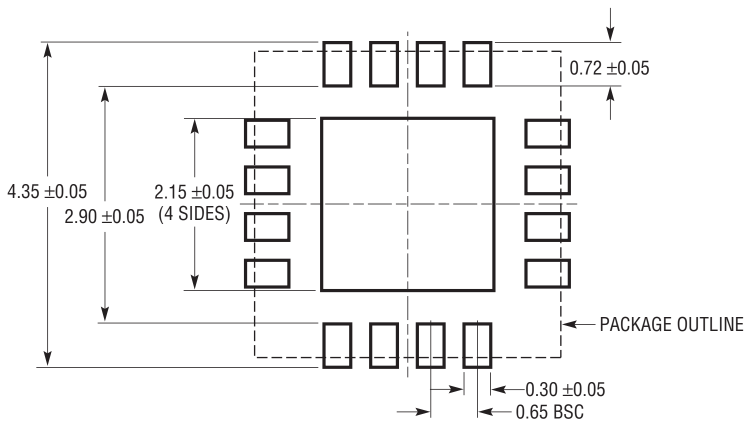
RF and LO Input Return Loss



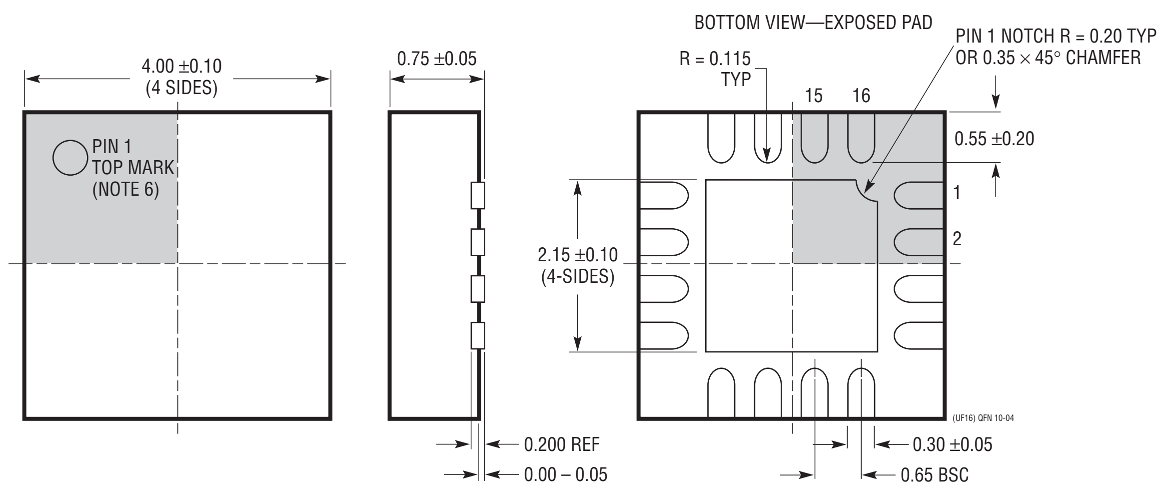
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE