Precision Dual/Quad CMOS Rail-to-Rail Input/ Output Amplifiers

FEATURES

- **Maximum Offset Voltage: 70μV (25°C)**
- **Maximum Offset Drift: 0.8μV/°C**
- **Maximum Input Bias: 1pA (25°C) 40pA (T_A ≤ 85°C)**
- Open Loop Voltage Gain: 120dB Typ
- Gain Bandwidth Product: 3.6MHz
- CMRR: 100dB Min
- PSRR: 98dB Min
- 0.1Hz to 10Hz Noise: 1.3μV_{P-P}
- Supply Current: 330μA
- Rail-to-Rail Inputs and Outputs
- Unity Gain Stable
- 2.7V to 5.5V Operation Voltage
- Dual LTC6081 in 8-Lead MSOP and 10-Lead DFN10 Packages; Quad LTC6082 in 16-Lead SSOP and DFN Packages

APPLICATIONS

- Photodiode Amplifier
- Strain Gauge
- High Impedance Sensor Amplifier
- Microvolt Accuracy Threshold Detection
- Instrumentation Amplifiers
- Thermocouple Amplifiers

DESCRIPTION

The LTC®6081/LTC6082 are dual/quad low offset, low drift, low noise CMOS operational amplifiers with rail-to-rail input/output swing.

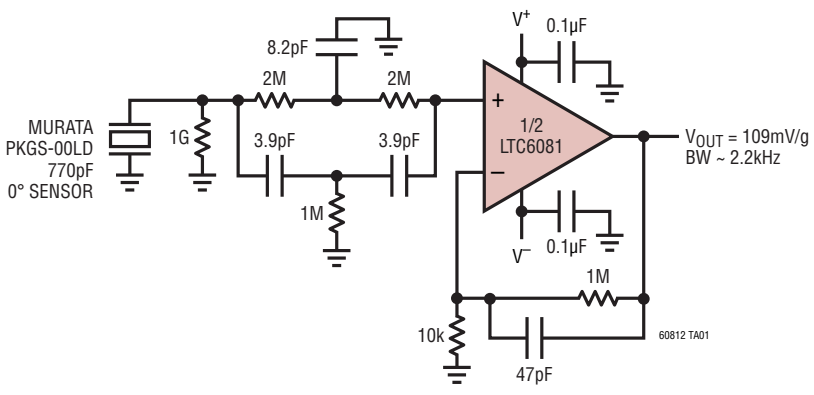
The 70μV maximum offset, 1pA input bias current, 120dB open loop gain and 1.3μV_{P-P} 0.1Hz to 10Hz noise make it perfect for precision signal conditioning. The LTC6081/LTC6082 features 100dB CMRR and 98dB PSRR.

Each amplifier consumes only 330μA of current on a 3V supply. The 10-lead DFN has an independent shutdown function that reduces each amplifier's supply current to 1μA.

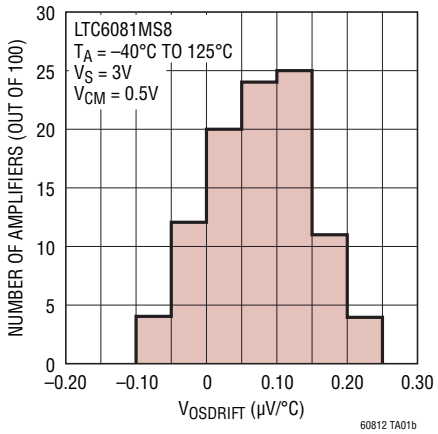
LTC6081/LTC6082 is specified for power supply voltages of 3V and 5V from –40°C to 125°C. The dual LTC6081 is available in 8-lead MSOP and 10-lead DFN10 packages. The quad LTC6082 is available in 16-lead SSOP and DFN packages.

TYPICAL APPLICATION

Shock Sensor Amplifier (Accelerometer)



V_{OS} Drift Histogram



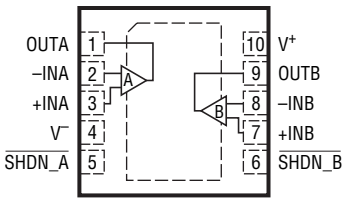
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 6V
Input Voltage ..... V^- to V^+
Output Short Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range (Note 3)
LTC6081C, LTC6082C ..... –40°C to 85°C
LTC6081I, LTC6082I ..... –40°C to 85°C
LTC6081H, LTC6082H ..... –40°C to 125°C
(H Temperature Range Not Available in DFN Package)
Specified Temperature Range (Note 4)
LTC6081C, LTC6082C ..... 0°C to 70°C
LTC6081I, LTC6082I ..... –40°C to 85°C
LTC6081H, LTC6082H ..... –40°C to 125°C
Junction Temperature
DFN Packages ..... 125°C
All Other Packages ..... 150°C
Storage Temperature Range
DFN Packages ..... –65°C to 125°C
All Other Packages ..... –65°C to 150°C
Lead Temperature (Soldering, 10 Sec) ..... 300°C

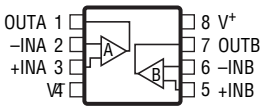
PIN CONFIGURATION

TOP VIEW



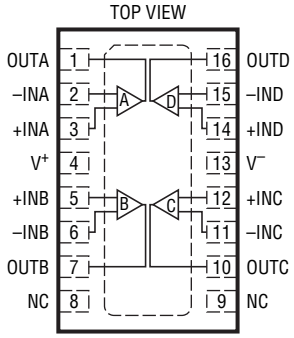
DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
UNDERSIDE METAL CONNECTED TO V^-

TOP VIEW



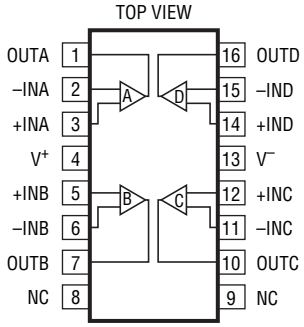
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 200°C/W

TOP VIEW



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
UNDERSIDE METAL CONNECTED TO V^-

TOP VIEW



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6081CDD#PBF	LTC6081CDD#TRPBF	LCJP	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6081IDD#PBF	LTC6081IDD#TRPBF	LCJP	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6081CMS8#PBF	LTC6081CMS8#TRPBF	LTCJN	8-Lead Plastic MSOP	0°C to 70°C
LTC6081IMS8#PBF	LTC6081IMS8#TRPBF	LTCJN	8-Lead Plastic MSOP	–40°C to 85°C
LTC6081HMS8#PBF	LTC6081HMS8#TRPBF	LTCJN	8-Lead Plastic MSOP	–40°C to 125°C
LTC6082CDHC#PBF	LTC6082CDHC#TRPBF	6082	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC6082IDHC#PBF	LTC6082IDHC#TRPBF	6082	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6082CGN#PBF	LTC6082CGN#TRPBF	6082	16-Lead Plastic SSOP	0°C to 70°C
LTC6082IGN#PBF	LTC6082IGN#TRPBF	6082I	16-Lead Plastic SSOP	–40°C to 85°C
LTC6082HGN#PBF	LTC6082HGN#TRPBF	6082H	16-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 3V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C, I SUFFIXES MIN	C, I SUFFIXES TYP	C, I SUFFIXES MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
V_{OS}	Offset Voltage	LTC6081MS8, LTC6082GN V_{CM} = 0.5V, 2.5V		–70		70	–70		70	µV
		LTC6081MS8, LTC6082GN V_{CM} = 0.5V, 2.5V	●	–90		90	–90		90	µV
		LTC6081DD, LTC6082DHC V_{CM} = 0.5V, 2.5V		–70		70				µV
		LTC6081DD, LTC6082DHC V_{CM} = 0.5V, 2.5V	●	–90		90				µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 5)		●		±0.2	±0.8		±0.2	±0.8	µV/°C
I_B	Input Bias Current (Note 6)				0.2	1		0.2	1	pA
			●			40			500	pA
I_{OS}	Input Offset Current				0.1			0.1		pA
			●			15			100	pA
e_n	Input Referred Noise	Noise Density at f = 1kHz			13			13		$nV/\sqrt{Hz}$
		Integrated Noise From 0.1Hz to 10Hz			1.3			1.3		μV_{P-P}
I_n	Input Noise Current Density (Note 7)				0.5			0.5		$fA/\sqrt{Hz}$
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{DIFF}	Differential Input Capacitance				3			3		pF
C_{CM}	Common Mode Input Capacitance				7			7		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 1.5V		95	105		95	105		dB
		V_{CM} = 0V to 1.5V	●	88	100		86	100		dB
		V_{CM} = 0V to 3V		93	105		93	105		dB
		V_{CM} = 0V to 3V	●	88	100		86	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V		98	110		98	110		dB
			●	96			96			dB
V_{OUT}	Output Voltage, High, Either Output Pin	No Load			1			1		mV
		I_{SOURCE} = 0.5mA	●	–32			–35			mV
		I_{SOURCE} = 5mA	●	–320			–350			mV
	Output Voltage, Low, Either Output Pin (Referred to V^-)	No Load			1			1		mV
		I_{SINK} = 0.5mA	●			33			40	mV
		I_{SINK} = 5mA	●			300			360	mV
A_{VOL}	Large-Signal Voltage Gain	R_{LOAD} = 10k, 0.5V < V_{OUT} < 2.5V	●	110	120		110	120		dB
I_{SC}	Output Short-Circuit Current	Source	●	17			15			mA
		Sink	●	17			15			mA
SR	Slew Rate	A_V = 1			1			1		V/µs
GBW	Gain-Bandwidth Product (f_{TEST} = 50kHz)	R_L = 100k		2.5	3.6		2.5	3.6		MHz
			●	1.8			1.5			MHz
Φ_0	Phase Margin	R_L = 10k			70			70		Deg
t_S	Settling Time 0.1%	A_V = 1, 1V Step			6			6		µs
I_S	Supply Current (Per Amplifier)	No Load			330	400		330	400	µA
			●			435			460	µA
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\overline{SHDN}} \leq 0.8V$			0.5					µA
			●			2				µA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7		5.5	2.7		5.5	V
	Channel Separation	f_S = 10kHz, R_L = 10k			–120			–120		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 3V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C, I SUFFIXES MIN	C, I SUFFIXES TYP	C, I SUFFIXES MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
	Shutdown Logic	$\overline{SHDN}$ High $\overline{SHDN}$ Low	● ●	2		 0.8	2		 0.8	V V
THD	Total Harmonic Distortion	f = 10kHz, V^+ = 3V, V_{OUT} = $1V_{P-P}$, R_L = 10k			–90			–90		dB
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.8V to 2V			10			10		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 2V to 0.8V			2			2		µs
	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0V	●			2				µA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C, I SUFFIXES MIN	C, I SUFFIXES TYP	C, I SUFFIXES MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
V_{OS}	Offset Voltage	LTC6081MS8, LTC6082GN V_{CM} = 0.5V LTC6081MS8, LTC6082GN V_{CM} = 0.5V LTC6081DD, LTC6082DHC V_{CM} = 0.5V LTC6081DD, LTC6082DHC V_{CM} = 0.5V	 ● ●	–70 –90 –70 –90		70 90 70 90	–70 –90		70 90	µV µV µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 8)		●		±0.2	±0.8		±0.2	±0.8	µV/°C
I_B	Input Bias Current		 ●		0.2	 40		0.2	 500	pA pA
I_{OS}	Input Offset Current		 ●		0.1	 15		0.1	 100	pA pA
e_n	Input Referred Noise	f = 1kHz 0.1Hz to 10Hz			13 1.3			13 1.3		nV/√Hz μV_{P-P}
I_n	Input Noise Current Density (Note 7)				0.5			0.5		fA/√Hz
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{DIFF}	Differential Input Capacitance				3			3		pF
C_{CM}	Common Mode Input Capacitance				7			7		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3.5V V_{CM} = 0V to 3.5V V_{CM} = 0V to 5V	 ● ●	100 95 86	110 110 95		100 94 86	110 110 95		dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V	 ●	98 96	110		98 96	110		dB dB
V_{OUT}	Output Voltage, High, Either Output Pin (Referred to V^+)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 5mA	 ● ●	 –24 –200	1	 	 –25 –220	1	 	mV mV mV
	Output Voltage, Low, Either Output Pin (Referred to V^-)	No Load I_{SINK} = 0.5mA I_{SINK} = 5mA	 ● ●		1	 27 210		1	 32 240	mV mV mV
A_{VOL}	Large-Signal Voltage Gain	R_{LOAD} = 10k, 0.5V < V_{OUT} < 4.5V	●	110	120		110	120		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C, I SUFFIXES MIN	C, I SUFFIXES TYP	C, I SUFFIXES MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
I_{SC}	Output Short-Circuit Current	Source Sink	● ●	24 24			21 21			mA mA
SR	Slew Rate	A_V = 1			1			1		V/µs
GBW	Gain-Bandwidth Product (f_{TEST} = 50kHz)	R_L = 100k	 ●	2.5 1.8	3.5		2.5 1.5	3.5		MHz MHz
Φ_0	Phase Margin	R_L = 10k			70			70		Deg
t_S	Settling Time 0.1%	A_V = 1, 1V Step			6			6		µs
I_S	Supply Current (Per Amplifier)	No Load	 ●		340	425 465		340	425 490	µA µA
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\overline{SHDN}} \leq 1.2V$	●			6				µA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7		5.5	2.7		5.5	V
	Channel Separation	f_s = 10kHz, R_L = 10k			–120			–120		dB
	Shutdown Logic	$\overline{SHDN}$ High $\overline{SHDN}$ Low	● ●	3.5		 1.2	3.5		 1.2	V V
THD	Total Harmonic Distortion	f = 10kHz, V^+ = 5V, $V_{OUT} = 2V_{P-P}$, R_L = 10k			–90			–90		dB
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 1.2V to 3.5V			10			10		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 3.5V to 1.2V			2			2		µs
	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0V	●			2				µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted.

Note 3: The LTC6081C/LTC6082C and LTC6081I/LTC6082I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6081H/LTC6082H are guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 4: The LTC6081C/LTC6082C are guaranteed to meet specified performance from 0°C to 70°C. The LTC6081C/LTC6082C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LTC6081I/LTC6082I are guaranteed to meet specified performance from –40°C to 85°C. The LTC6081H/LTC6082H are guaranteed to meet specified performance from –40°C to 125°C.

Note 5: Input offset drift is computed from the limits of the V_{OS} test divided by the temperature range. This is a conservative estimate of worst case drift. Consult the Typical Performance Characteristics section for more information on input offset drift.

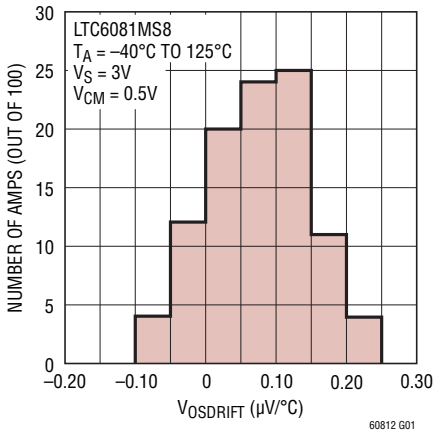
Note 6: I_B guaranteed by the V_S = 5V test.

Note 7: Current noise is calculated from $I_n = \sqrt{2qI_B}$, where $q = 1.6 \bullet 10^{-19}$ coulomb.

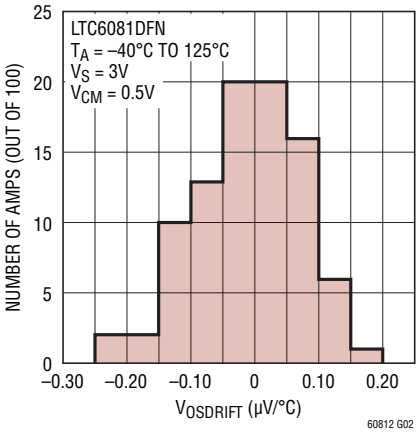
Note 8: V_{OS} drift is guaranteed by the V_S = 3V test.

TYPICAL PERFORMANCE CHARACTERISTICS

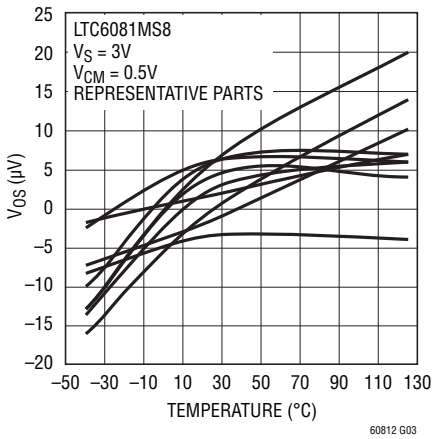
V_{OS} Drift Histogram



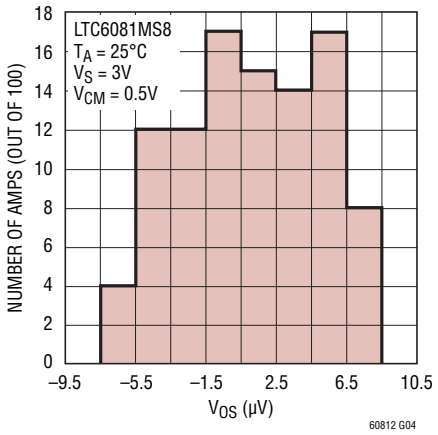
V_{OS} Drift Histogram



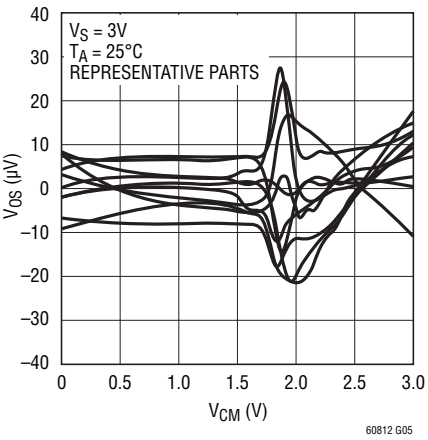
V_{OS} vs Temperature



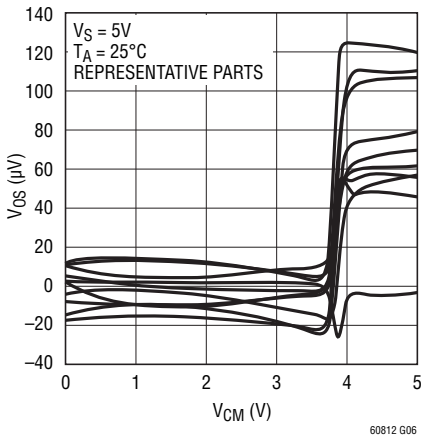
V_{OS} Histogram



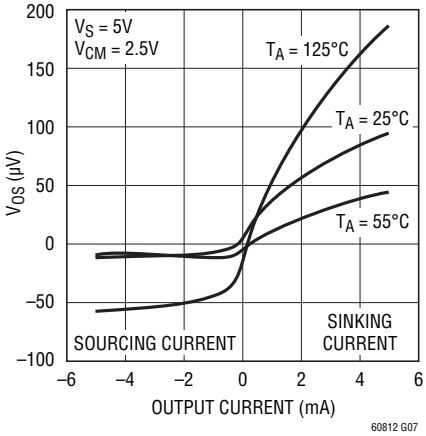
V_{OS} vs V_{CM}



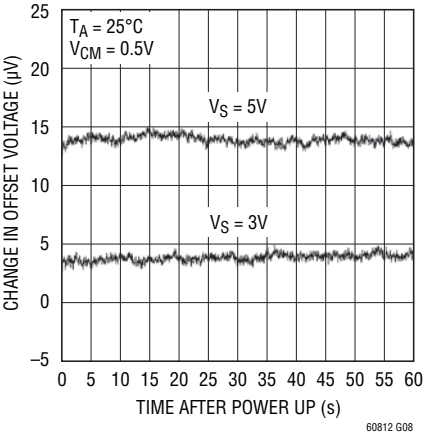
V_{OS} vs V_{CM}



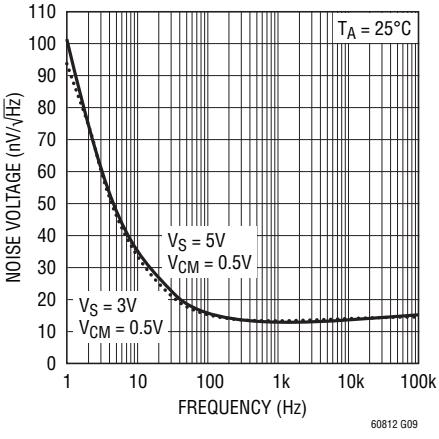
V_{OS} vs Output Current



Warm-Up Drift vs Time

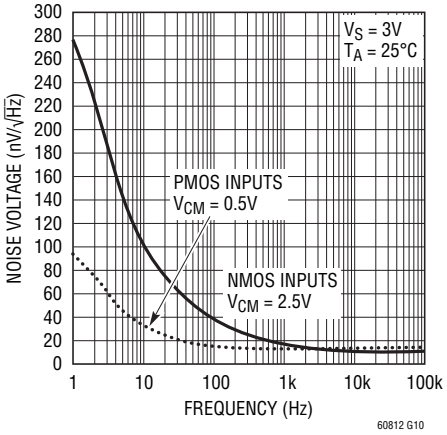


Noise Voltage vs Frequency

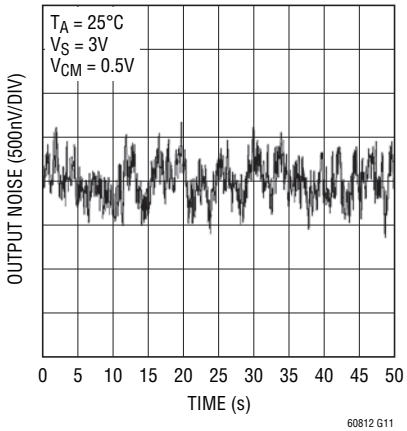


TYPICAL PERFORMANCE CHARACTERISTICS

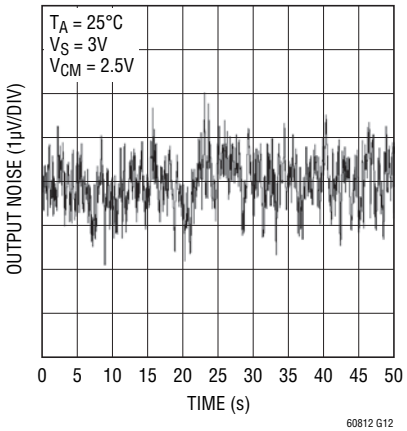
Noise Voltage vs Frequency



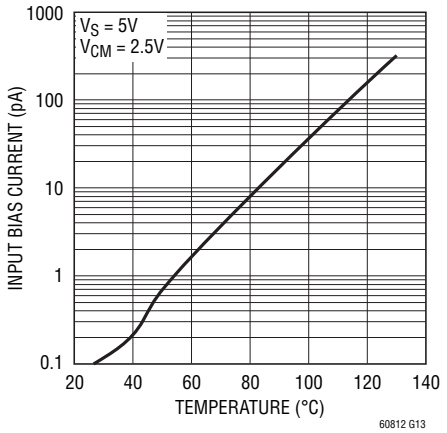
0.1Hz to 10Hz Output Voltage Noise



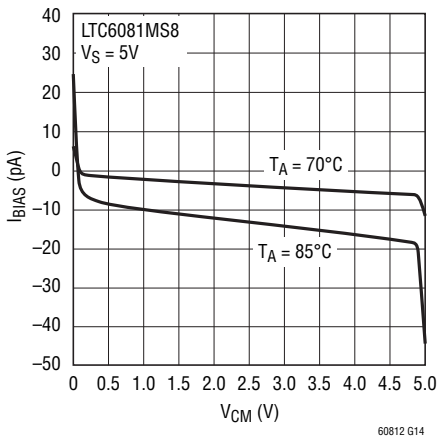
0.1Hz to 10Hz Output Voltage Noise



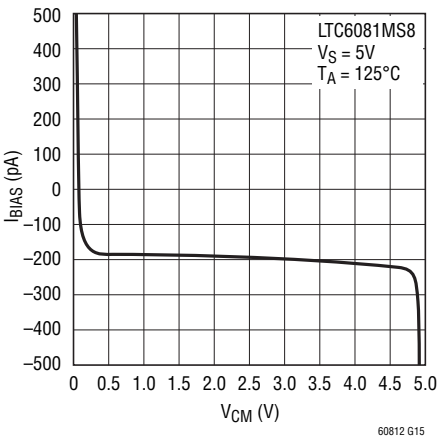
Input Bias Current vs Temperature



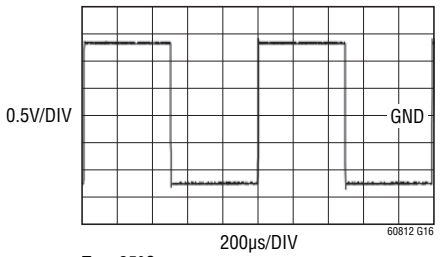
I_{BIAS} vs V_{CM}



I_{BIAS} vs V_{CM}

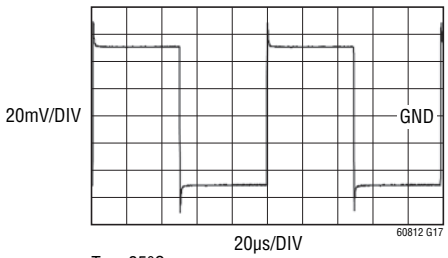


Large Signal Transient



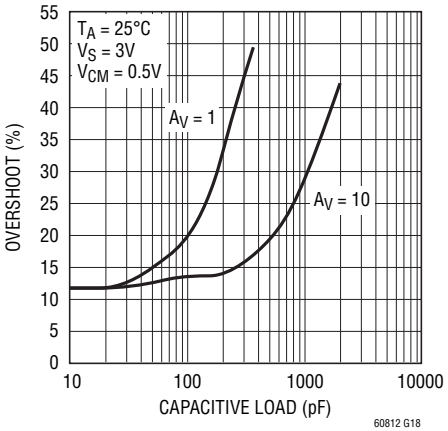
T_A = 25°C
V_S = ±1.5V
R_L = 10k
C_L = 100pF

Small Signal Transient



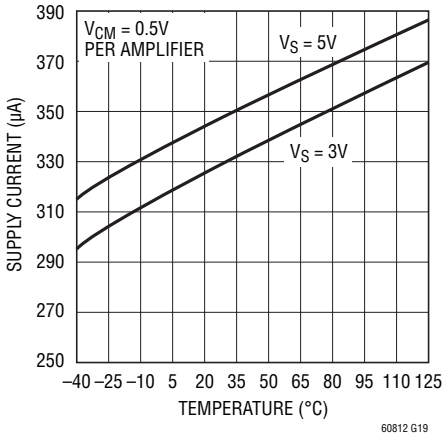
T_A = 25°C
V_S = ±1.5V
R_L = 10k
C_L = 100pF

Overshoot vs C_L

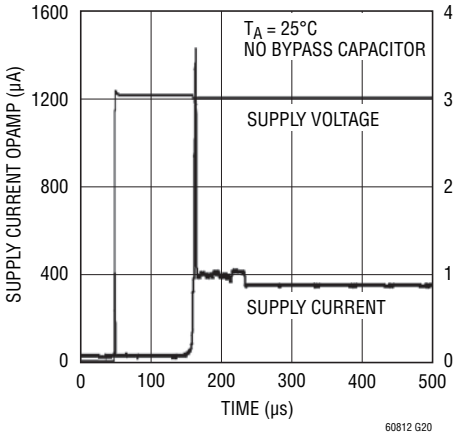


TYPICAL PERFORMANCE CHARACTERISTICS

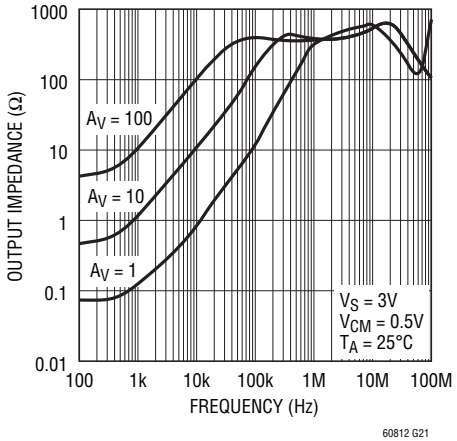
Supply Current vs Temperature



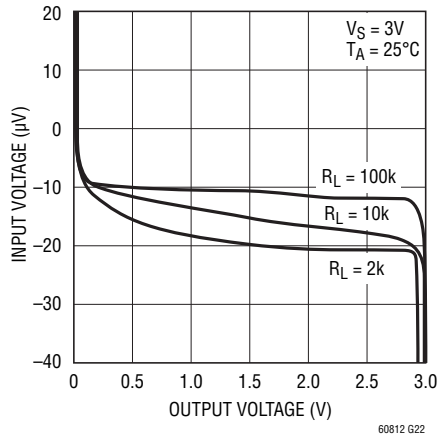
Supply Current vs Time



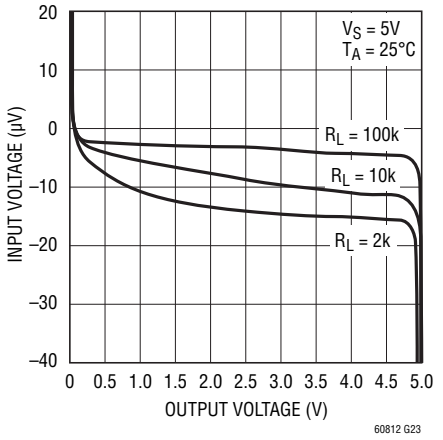
Output Impedance vs Frequency



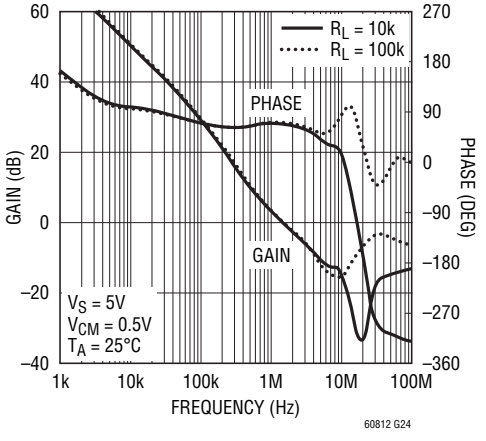
Open Loop Gain



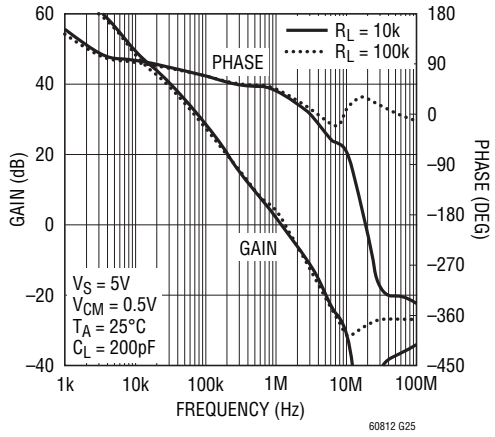
Open Loop Gain



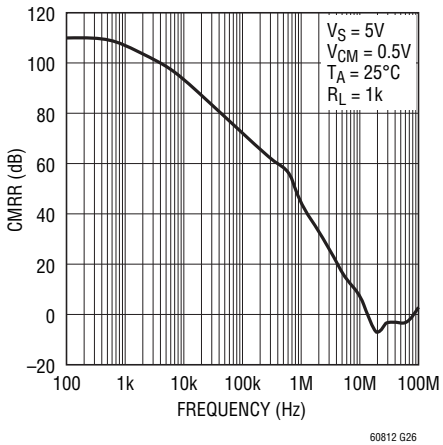
Open Loop Gain vs Frequency



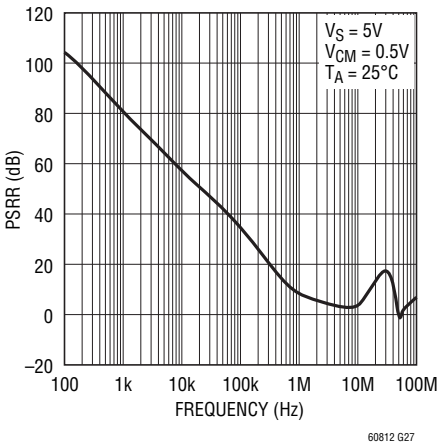
Open Loop Gain vs Frequency



CMRR vs Frequency

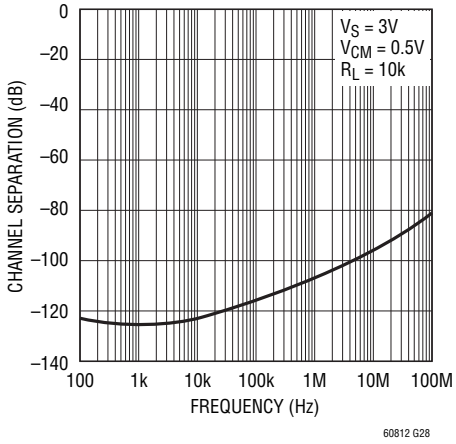


PSRR vs Frequency

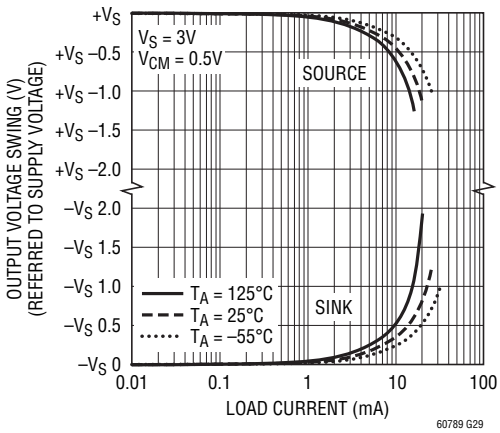


TYPICAL PERFORMANCE CHARACTERISTICS

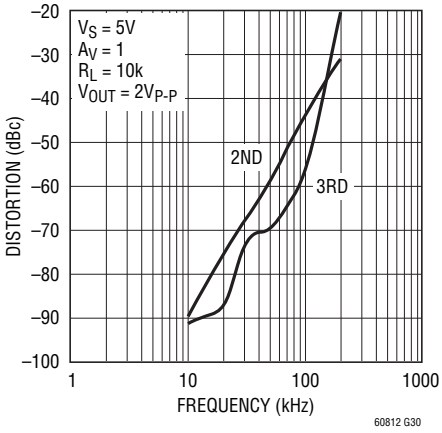
Channel Separation vs Frequency



Output Voltage Swing vs Load Current



Distortion vs Frequency



PIN FUNCTIONS

OUT: Amplifier Output

–IN: Inverting Input

+IN: Noninverting Input

V+: Positive Supply

V–: Negative Supply

$\overline{\text{SHDN\_A}}$: Shutdown Pin of Amplifier A, active low and only valid for LTC6081DD. An internal current source pulls the pin to V+ when floating.

$\overline{\text{SHDN\_B}}$: Shutdown Pin of Amplifier B, active low and only valid for LTC6081DD. An internal current source pulls the pin to V+ when floating.

NC: Not internally connected.

Exposed Pad: Connected to V–.

APPLICATIONS INFORMATION

Preserving Input Precision

Preserving input accuracy of the LTC6081/LTC6082 requires that the application circuit and PC board layout do not introduce errors comparable or greater than the 5µV typical offset of the amplifiers. Temperature differentials across the input connections can generate thermocouple voltages of 10's of microvolts so the connections to the input leads should be short, close together and away from heat dissipating components. Air current across the board can also generate temperature differentials.

The extremely low input bias currents (0.1pA typical) allow high accuracy to be maintained with high impedance sources and feedback resistors. Leakage currents on the PC board can be higher than the input bias current. For example, 10GΩ of leakage between a 5V supply lead and an input lead will generate 500pA! Surround the input leads with a guard ring driven to the same potential as the input common mode voltage to avoid excessive leakage in high impedance applications.

Capacitive Load

LTC6081/LTC6082 can drive capacitive load up to 200pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load further increases the amount of capacitance the amplifier can drive.

$\overline{\text{SHDN}}$ Pins

Pins 5 and 6 are used for power shutdown on the LTC6081 in the DD package. If they are floating, internal current sources pull Pins 5 and 6 to V^+ and the amplifiers operate normally. In shutdown, the amplifier output is high impedance, and each amplifier draws less than 2µA current.

Rail-to-Rail Input

The input stage of LTC6081/LTC6082 combines both PMOS and NMOS differential pairs, extending its input common mode voltage range to both positive and negative supply voltages. At high input common mode range, the NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between 1.3V and 0.9V below the positive supply. LTC6081 has better low frequency noise performance with PMOS input on due to its lower flicker noise (see Voltage Noise vs Frequency and 0.1Hz to 10Hz Input Voltage Noise in Typical Performance Characteristics).

Thermal Hysteresis

Figure 1 shows the input offset voltage hysteresis of the LTC6081IMS8 for 3 thermal cycles from –45°C to 90°C. The typical offset shift is ±4µV. The data was taken with the ICs in stress free sockets. Mounting to PC boards may cause additional hysteresis due to mechanical stress. The LTC6081 will meet offset voltage specifications in the electrical characteristics table even after 15µV of additional error from thermal hysteresis.

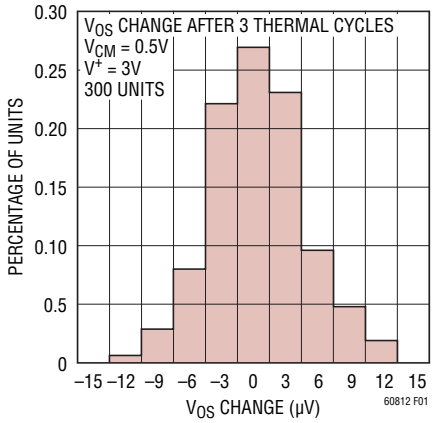


Figure 1. V_{OS} Thermal Hysteresis of LTC6081MS8

APPLICATIONS INFORMATION

PC Board Layout

Mechanical stress on a PC board and soldering-induced stress can cause the V_{OS} and V_{OS} drift to shift. The DD and DHC packages are more sensitive to stress. A simple way to reduce the stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board edge acts as a stress boundary, or a region where the flexure of the board is minimum. The package should always be mounted so that the leads absorb the stress and not the package. The package is generally aligned with the leads perpendicular to the long side of the PC board (see Figure 2).

The most effective technique to relieve the PC board stress is to cut slots in the board around the op amp. These slots can be cut on three sides of the IC and the leads can exit on the fourth side. Figure 2 shows the layout of a LTC6081DD with slots at three sides.

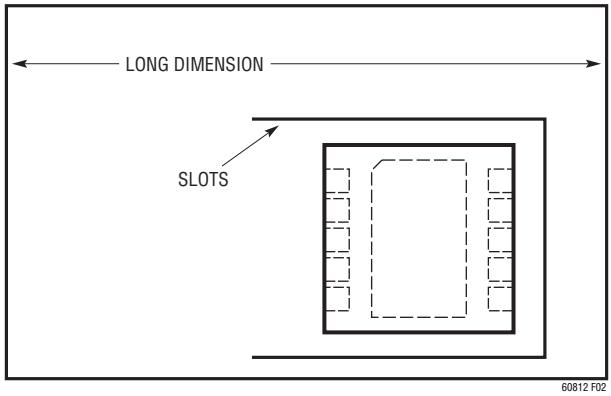
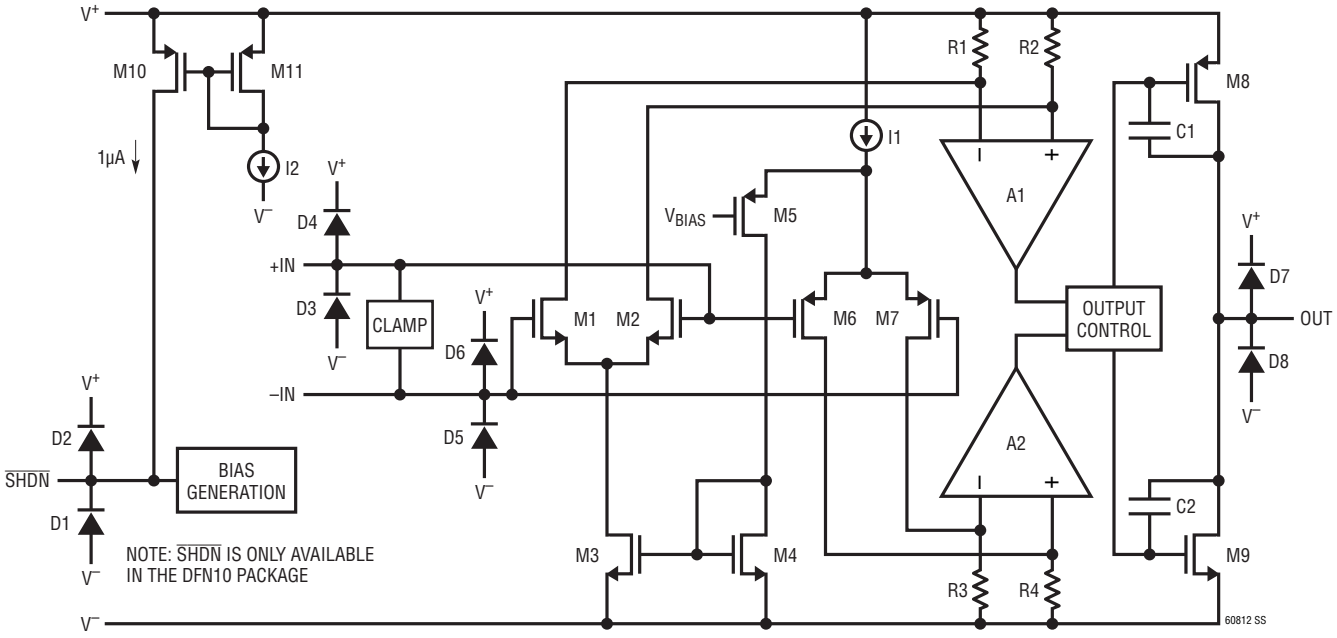


Figure 2. Vertical Orientation of LTC6081DD with Slots

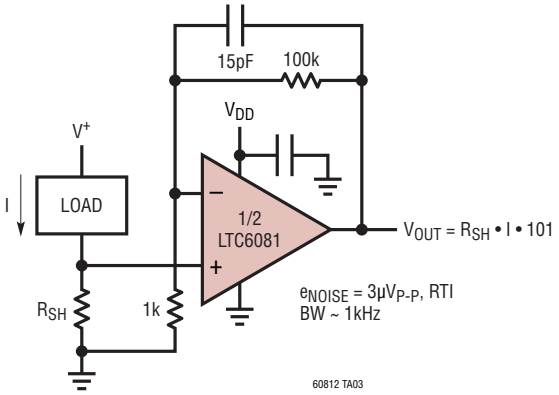
SIMPLIFIED SCHEMATIC

Simplified Schematic of the Amplifier

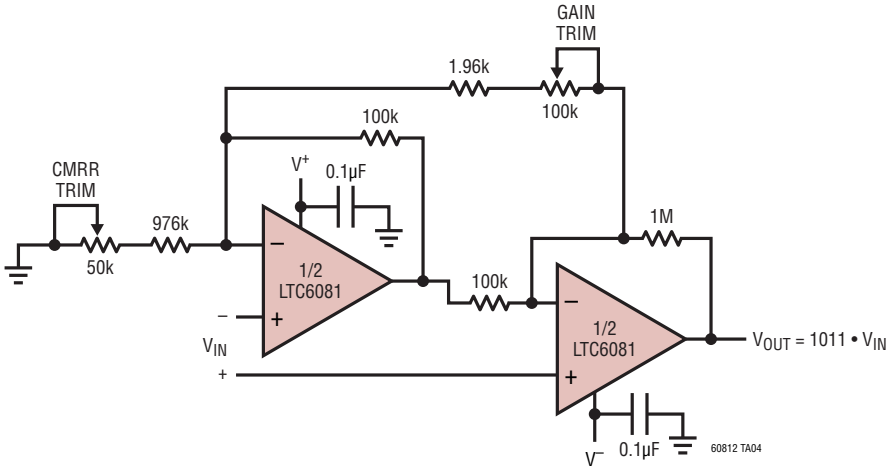


TYPICAL APPLICATIONS

Low Side Current Sense

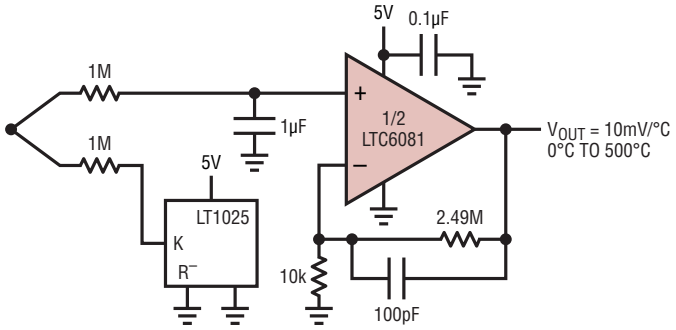


Two Op-Amp Instrumentation Amplifier



TYPICAL APPLICATIONS

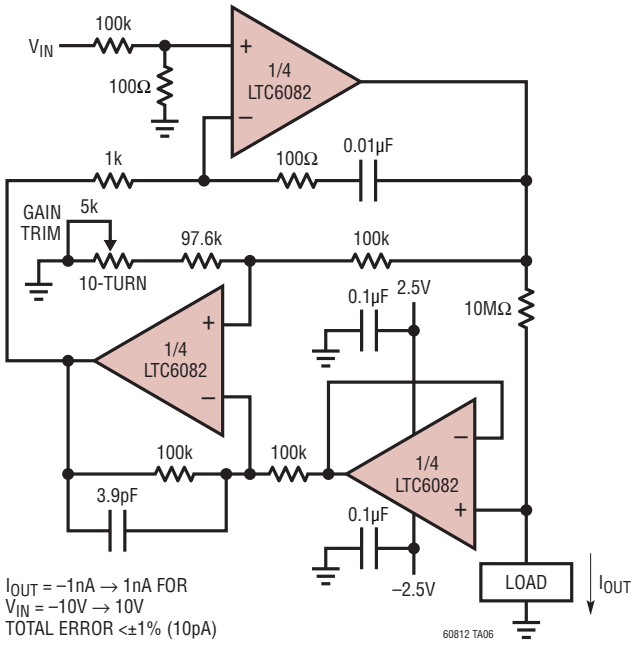
Thermocouple Amplifier



SENSOR: OMEGA 5TC-TT-K-30-36 K-TYPE THERMOCOUPLE
1M RESISTORS PROTECT CIRCUIT TO ±350V WITH NO PHASE REVERSAL OF AMPLIFIER OUTPUT
1pA MAX I_{BIAS} TRANSLATES TO 0.05°C ERROR
20µV V_{OS} → 0.5°C OFFSET

60812 TA05

Precision Nanoamp Bidirectional Current Source



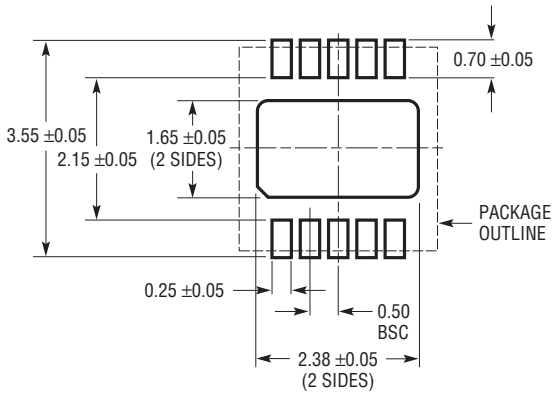
I_{OUT} = –1nA → 1nA FOR
V_{IN} = –10V → 10V
TOTAL ERROR <±1% (10pA)

60812 TA06

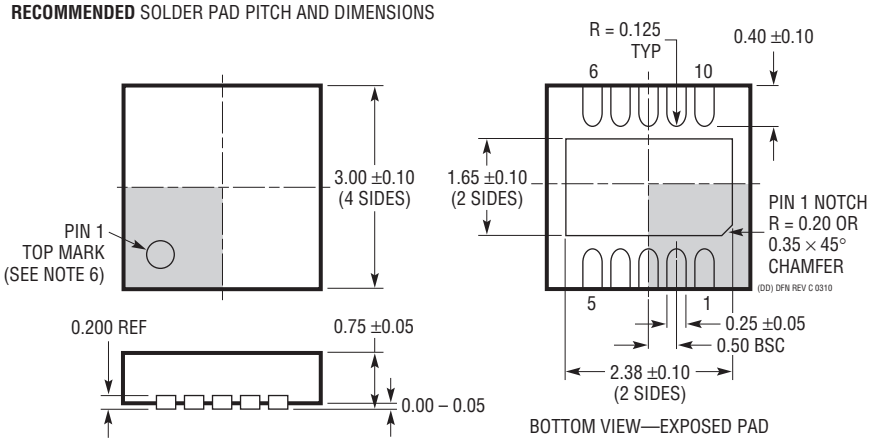
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



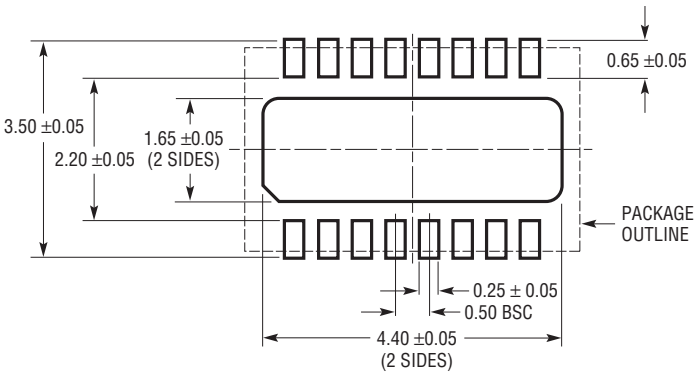
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

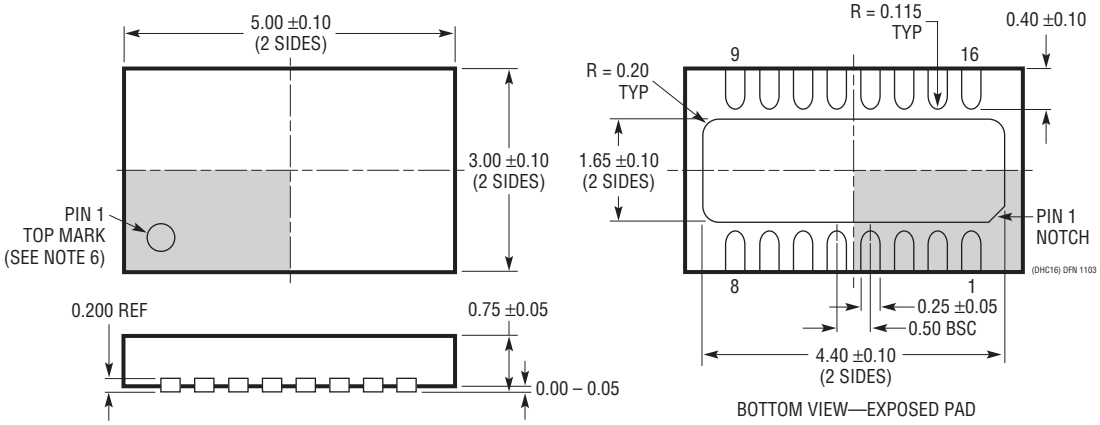
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



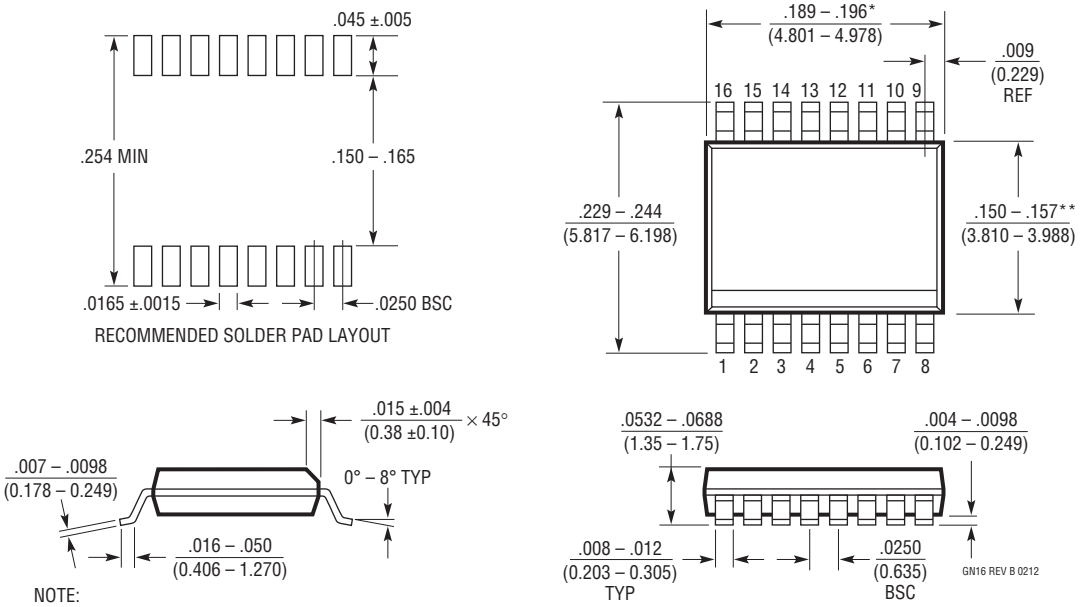
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

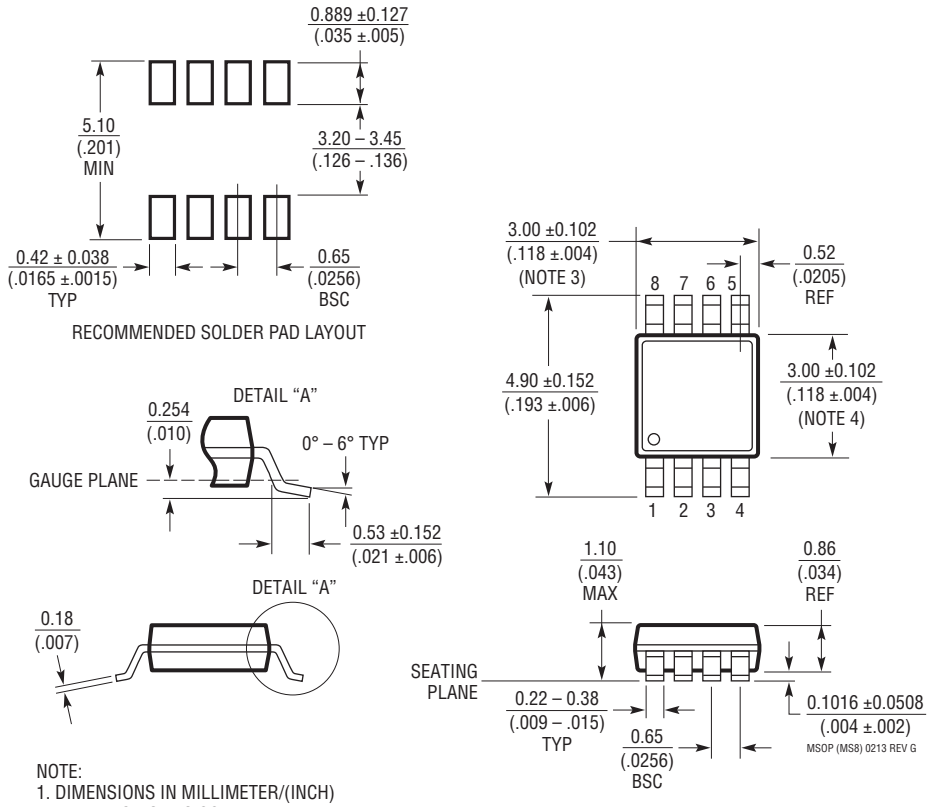
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	3/10	Change LT to LTC on all part numbers in Order Information Section.	3
C	07/10	Update to Simplified Schematic	12
D	12/13	Corrected resistor value (10M)	14