

# Precision Dual/Quad CMOS Rail-to-Rail Input/Output Amplifiers

## FEATURES

- **Maximum Offset Voltage: 70 $\mu$ V (25 $^{\circ}$ C)**
- **Maximum Offset Drift: 0.8 $\mu$ V/ $^{\circ}$ C**
- **Maximum Input Bias: 1pA (25 $^{\circ}$ C) 40pA ( $T_A \leq 85^{\circ}$ C)**
- Open Loop Voltage Gain: 120dB Typ
- Gain Bandwidth Product: 3.6MHz
- CMRR: 100dB Min
- PSRR: 98dB Min
- 0.1Hz to 10Hz Noise: 1.3 $\mu$ V<sub>P-P</sub>
- Supply Current: 330 $\mu$ A
- Rail-to-Rail Inputs and Outputs
- Unity Gain Stable
- 2.7V to 5.5V Operation Voltage
- Dual LTC6081 in 8-Lead MSOP and 10-Lead DFN10 Packages; Quad LTC6082 in 16-Lead SSOP and DFN Packages

## APPLICATIONS

- Photodiode Amplifier
- Strain Gauge
- High Impedance Sensor Amplifier
- Microvolt Accuracy Threshold Detection
- Instrumentation Amplifiers
- Thermocouple Amplifiers

## DESCRIPTION

The **LTC<sup>®</sup>6081/LTC6082** are dual/quad low offset, low drift, low noise CMOS operational amplifiers with rail-to-rail input/output swing.

The 70 $\mu$ V maximum offset, 1pA input bias current, 120dB open loop gain and 1.3 $\mu$ V<sub>P-P</sub> 0.1Hz to 10Hz noise make it perfect for precision signal conditioning. The LTC6081/LTC6082 features 100dB CMRR and 98dB PSRR.

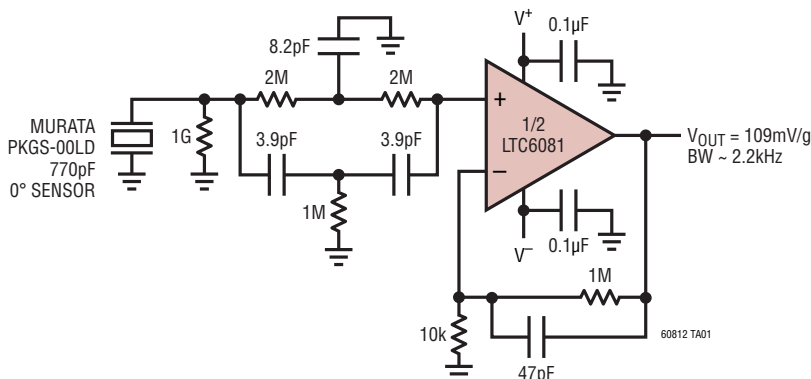
Each amplifier consumes only 330 $\mu$ A of current on a 3V supply. The 10-lead DFN has an independent shutdown function that reduces each amplifier's supply current to 1 $\mu$ A.

LTC6081/LTC6082 is specified for power supply voltages of 3V and 5V from -40 $^{\circ}$ C to 125 $^{\circ}$ C. The dual LTC6081 is available in 8-lead MSOP and 10-lead DFN10 packages. The quad LTC6082 is available in 16-lead SSOP and DFN packages.

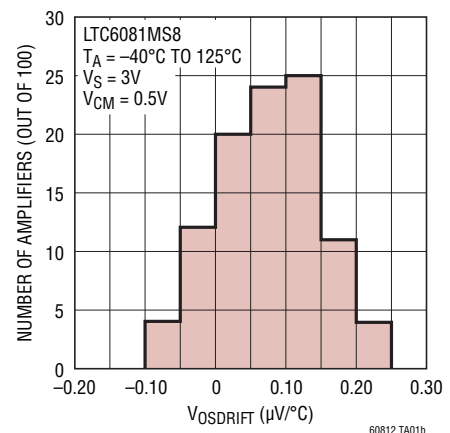
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## TYPICAL APPLICATION

**Shock Sensor Amplifier (Accelerometer)**



**V<sub>OS</sub> Drift Histogram**



# LTC6081/LTC6082

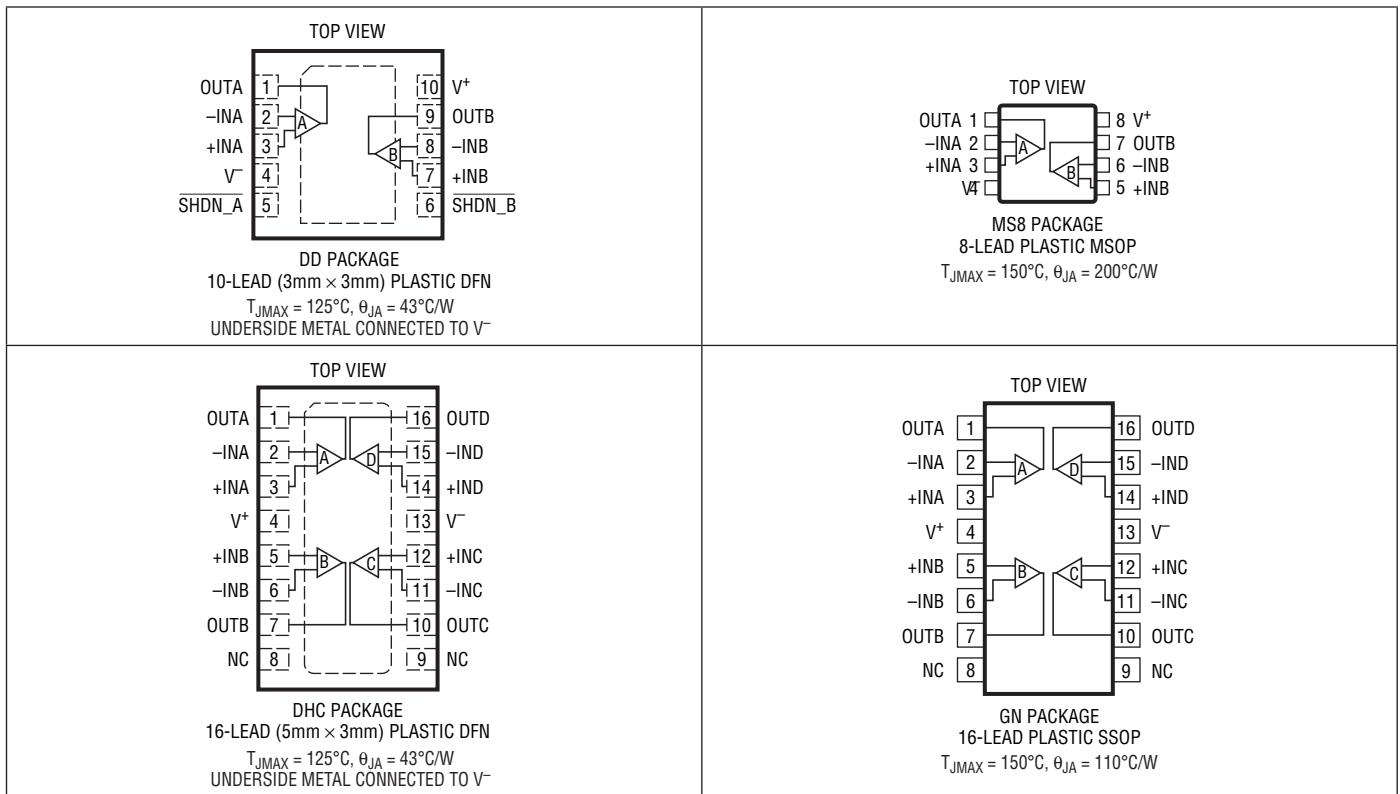
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ( $V^+$ to $V^-$ ).....	6V
Input Voltage.....	$V^-$ to $V^+$
Output Short Circuit Duration (Note 2).....	Indefinite
Operating Temperature Range (Note 3)	
LTC6081C, LTC6082C .....	-40°C to 85°C
LTC6081I, LTC6082I .....	-40°C to 85°C
LTC6081H, LTC6082H .....	-40°C to 125°C
(H Temperature Range Not Available in DFN Package)	

Specified Temperature Range (Note 4)	
LTC6081C, LTC6082C .....	0°C to 70°C
LTC6081I, LTC6082I .....	-40°C to 85°C
LTC6081H, LTC6082H .....	-40°C to 125°C
Junction Temperature	
DFN Packages .....	125°C
All Other Packages .....	150°C
Storage Temperature Range	
DFN Packages .....	-65°C to 125°C
All Other Packages .....	-65°C to 150°C
Lead Temperature (Soldering, 10 Sec).....	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6081CDD#PBF	LTC6081CDD#TRPBF	LCJP	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6081IDD#PBF	LTC6081IDD#TRPBF	LCJP	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6081CMS8#PBF	LTC6081CMS8#TRPBF	LTCJN	8-Lead Plastic MSOP	0°C to 70°C
LTC6081IMS8#PBF	LTC6081IMS8#TRPBF	LTCJN	8-Lead Plastic MSOP	-40°C to 85°C
LTC6081HMS8#PBF	LTC6081HMS8#TRPBF	LTCJN	8-Lead Plastic MSOP	-40°C to 125°C
LTC6082CDHC#PBF	LTC6082CDHC#TRPBF	6082	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC6082IDHC#PBF	LTC6082IDHC#TRPBF	6082	16-Lead (5mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6082CGN#PBF	LTC6082CGN#TRPBF	6082	16-Lead Plastic SSOP	0°C to 70°C
LTC6082IGN#PBF	LTC6082IGN#TRPBF	6082I	16-Lead Plastic SSOP	-40°C to 85°C
LTC6082HGN#PBF	LTC6082HGN#TRPBF	6082H	16-Lead Plastic SSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

# LTC6081/LTC6082

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C, I SUFFIXES			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{\text{OS}}$	Offset Voltage	LTC6081MS8, LTC6082GN	$V_{\text{CM}} = 0.5\text{V}, 2.5\text{V}$	●	-70	70	-70	70	$\mu\text{V}$
		LTC6081MS8, LTC6082GN	$V_{\text{CM}} = 0.5\text{V}, 2.5\text{V}$	●	-90	90	-90	90	$\mu\text{V}$
		LTC6081DD, LTC6082DHC	$V_{\text{CM}} = 0.5\text{V}, 2.5\text{V}$	●	-70	70			$\mu\text{V}$
		LTC6081DD, LTC6082DHC	$V_{\text{CM}} = 0.5\text{V}, 2.5\text{V}$	●	-90	90			$\mu\text{V}$
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift (Note 5)		●	$\pm 0.2$	$\pm 0.8$	$\pm 0.2$	$\pm 0.8$	$\mu\text{V}/^\circ\text{C}$	
$I_{\text{B}}$	Input Bias Current (Note 6)		●	0.2	1 40	0.2	1 500	$\text{pA}$ $\text{pA}$	
$I_{\text{OS}}$	Input Offset Current		●	0.1	15	0.1	100	$\text{pA}$ $\text{pA}$	
$e_{\text{n}}$	Input Referred Noise	Noise Density at $f = 1\text{kHz}$ Integrated Noise From 0.1Hz to 10Hz		13 1.3		13 1.3		$\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{V}_{\text{P-P}}$	
$I_{\text{n}}$	Input Noise Current Density (Note 7)			0.5		0.5		$\text{fA}/\sqrt{\text{Hz}}$	
	Input Common Mode Range		●	$V^-$	$V^+$	$V^-$	$V^+$	V	
$C_{\text{DIFF}}$	Differential Input Capacitance			3		3		pF	
$C_{\text{CM}}$	Common Mode Input Capacitance			7		7		pF	
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = 0\text{V}$ to 1.5V	●	95	105	95	105	dB	
		$V_{\text{CM}} = 0\text{V}$ to 1.5V	●	88	100	86	100	dB	
		$V_{\text{CM}} = 0\text{V}$ to 3V	●	93	105	93	105	dB	
		$V_{\text{CM}} = 0\text{V}$ to 3V	●	88	100	86	100	dB	
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = 2.7\text{V}$ to 5.5V	●	98 96	110	98 96	110	dB dB	
$V_{\text{OUT}}$	Output Voltage, High, Either Output Pin	No Load $I_{\text{SOURCE}} = 0.5\text{mA}$ $I_{\text{SOURCE}} = 5\text{mA}$	● ●	-32 -320	1	-35 -350	1	$\text{mV}$ $\text{mV}$ $\text{mV}$	
	Output Voltage, Low, Either Output Pin (Referred to $V^-$ )	No Load $I_{\text{SINK}} = 0.5\text{mA}$ $I_{\text{SINK}} = 5\text{mA}$	● ●		1 33 300		1 40 360	$\text{mV}$ $\text{mV}$ $\text{mV}$	
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$R_{\text{LOAD}} = 10\text{k}$ , $0.5\text{V} < V_{\text{OUT}} < 2.5\text{V}$	●	110	120	110	120	dB	
$I_{\text{SC}}$	Output Short-Circuit Current	Source	●	17		15		$\text{mA}$	
		Sink	●	17		15		$\text{mA}$	
SR	Slew Rate	$A_{\text{V}} = 1$		1		1		$\text{V}/\mu\text{s}$	
GBW	Gain-Bandwidth Product ( $f_{\text{TEST}} = 50\text{kHz}$ )		●	2.5 1.8	3.6	2.5 1.5	3.6	$\text{MHz}$ $\text{MHz}$	
				70		70		Deg	
$\Phi_0$	Phase Margin	$R_{\text{L}} = 10\text{k}$		70		70		Deg	
$t_{\text{S}}$	Settling Time 0.1%	$A_{\text{V}} = 1$ , 1V Step		6		6		$\mu\text{s}$	
$I_{\text{S}}$	Supply Current (Per Amplifier)	No Load	●	330	400 435	330	400 460	$\mu\text{A}$ $\mu\text{A}$	
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\text{SHDN}} \leq 0.8\text{V}$	●	0.5	2			$\mu\text{A}$ $\mu\text{A}$	
$V_{\text{S}}$	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7	5.5	2.7	5.5	V	
	Channel Separation	$f_{\text{S}} = 10\text{kHz}$ , $R_{\text{L}} = 10\text{k}$		-120		-120		dB	

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**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C, I SUFFIXES			H SUFFIX			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
	Shutdown Logic	SHDN High SHDN Low	● ●	2		0.8	2		0.8	V V
THD	Total Harmonic Distortion	$f = 10\text{kHz}$ , $V^+ = 3\text{V}$ , $V_{\text{OUT}} = 1\text{V}_{\text{P-P}}$ , $R_L = 10\text{k}$			-90			-90		dB
$t_{\text{ON}}$	Turn-On Time	$V_{\text{SHDN}} = 0.8\text{V}$ to $2\text{V}$			10			10		$\mu\text{s}$
$t_{\text{OFF}}$	Turn-Off Time	$V_{\text{SHDN}} = 2\text{V}$ to $0.8\text{V}$			2			2		$\mu\text{s}$
	SHDN Pin Current	$V_{\text{SHDN}} = 0\text{V}$	●			2				$\mu\text{A}$

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C, I SUFFIXES			H SUFFIX			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{\text{OS}}$	Offset Voltage	LTC6081MS8, LTC6082GN $V_{\text{CM}} = 0.5\text{V}$	●	-70		70	-70		70	$\mu\text{V}$
		LTC6081MS8, LTC6082GN $V_{\text{CM}} = 0.5\text{V}$	●	-90		90	-90		90	$\mu\text{V}$
		LTC6081DD, LTC6082DHC $V_{\text{CM}} = 0.5\text{V}$	●	-70		70				$\mu\text{V}$
		LTC6081DD, LTC6082DHC $V_{\text{CM}} = 0.5\text{V}$	●	-90		90				$\mu\text{V}$
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift (Note 8)		●	$\pm 0.2$		$\pm 0.8$	$\pm 0.2$		$\pm 0.8$	$\mu\text{V}/^\circ\text{C}$
$I_{\text{B}}$	Input Bias Current		●		0.2		0.2		500	pA pA
$I_{\text{OS}}$	Input Offset Current		●		0.1		0.1		100	pA pA
$e_{\text{n}}$	Input Referred Noise	$f = 1\text{kHz}$ $0.1\text{Hz}$ to $10\text{Hz}$			13		13			$\text{nV}/\sqrt{\text{Hz}}$
					1.3		1.3			$\mu\text{V}_{\text{P-P}}$
$I_{\text{n}}$	Input Noise Current Density (Note 7)				0.5		0.5			$\text{fA}/\sqrt{\text{Hz}}$
	Input Common Mode Range		●	$V^-$		$V^+$	$V^-$		$V^+$	V
$C_{\text{DIFF}}$	Differential Input Capacitance				3		3			pF
$C_{\text{CM}}$	Common Mode Input Capacitance				7		7			pF
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = 0\text{V}$ to $3.5\text{V}$	●	100		110	100		110	dB
		$V_{\text{CM}} = 0\text{V}$ to $3.5\text{V}$	●	95		110	94		110	dB
		$V_{\text{CM}} = 0\text{V}$ to $5\text{V}$	●	86		95	86		95	dB
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = 2.7\text{V}$ to $5.5\text{V}$		98		110	98		110	dB
			●	96			96			dB
$V_{\text{OUT}}$	Output Voltage, High, Either Output Pin (Referred to $V^+$ )	No Load			1		1			mV
		$I_{\text{SOURCE}} = 0.5\text{mA}$	●	-24			-25			mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●	-200			-220			mV
$V_{\text{OUT}}$	Output Voltage, Low, Either Output Pin (Referred to $V^-$ )	No Load			1		1			mV
		$I_{\text{SINK}} = 0.5\text{mA}$	●			27		32		mV
		$I_{\text{SINK}} = 5\text{mA}$	●			210		240		mV
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$R_{\text{LOAD}} = 10\text{k}$ , $0.5\text{V} < V_{\text{OUT}} < 4.5\text{V}$	●	110		120	110		120	dB

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C, I SUFFIXES			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{\text{SC}}$	Output Short-Circuit Current	Source	●	24			21		mA
			●	24			21		mA
SR	Slew Rate	$A_V = 1$		1		1		V/ $\mu\text{s}$	
GBW	Gain-Bandwidth Product ( $f_{\text{TEST}} = 50\text{kHz}$ )	$R_L = 100\text{k}$	●	2.5 1.8	3.5	2.5 1.5	3.5	MHz MHz	
$\Phi_0$	Phase Margin	$R_L = 10\text{k}$		70		70		Deg	
$t_S$	Settling Time 0.1%	$A_V = 1$ , 1V Step		6		6		$\mu\text{s}$	
$I_S$	Supply Current (Per Amplifier)	No Load	●	340	425 465	340	425 490	$\mu\text{A}$ $\mu\text{A}$	
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\text{SHDN}} \leq 1.2\text{V}$	●		6			$\mu\text{A}$	
$V_S$	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7	5.5	2.7	5.5	V	
	Channel Separation	$f_s = 10\text{kHz}$ , $R_L = 10\text{k}$		-120		-120		dB	
	Shutdown Logic	$\overline{\text{SHDN}}$ High $\overline{\text{SHDN}}$ Low	● ●	3.5	1.2	3.5	1.2	V V	
THD	Total Harmonic Distortion	$f = 10\text{kHz}$ , $V^+ = 5\text{V}$ , $V_{\text{OUT}} = 2V_{\text{P-P}}$ , $R_L = 10\text{k}$		-90		-90		dB	
$t_{\text{ON}}$	Turn-On Time	$V_{\text{SHDN}} = 1.2\text{V}$ to $3.5\text{V}$		10		10		$\mu\text{s}$	
$t_{\text{OFF}}$	Turn-Off Time	$V_{\text{SHDN}} = 3.5\text{V}$ to $1.2\text{V}$		2		2		$\mu\text{s}$	
	$\overline{\text{SHDN}}$ Pin Current	$V_{\text{SHDN}} = 0\text{V}$	●		2			$\mu\text{A}$	

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted.

**Note 3:** The LTC6081C/LTC6082C and LTC6081I/LTC6082I are guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6081H/LTC6082H are guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 4:** The LTC6081C/LTC6082C are guaranteed to meet specified performance from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . The LTC6081C/LTC6082C are designed,

characterized and expected to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  but are not tested or QA sampled at these temperatures. The LTC6081I/LTC6082I are guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6081H/LTC6082H are guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 5:** Input offset drift is computed from the limits of the  $V_{\text{OS}}$  test divided by the temperature range. This is a conservative estimate of worst case drift. Consult the Typical Performance Characteristics section for more information on input offset drift.

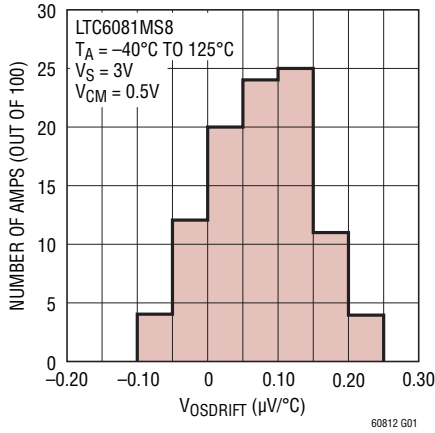
**Note 6:**  $I_B$  guaranteed by the  $V_S = 5\text{V}$  test.

**Note 7:** Current noise is calculated from  $I_n = \sqrt{2qI_B}$ , where  $q = 1.6 \cdot 10^{-19}$  coulomb.

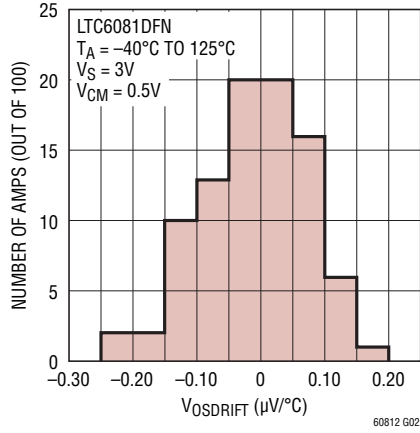
**Note 8:**  $V_{\text{OS}}$  drift is guaranteed by the  $V_S = 3\text{V}$  test.

# TYPICAL PERFORMANCE CHARACTERISTICS

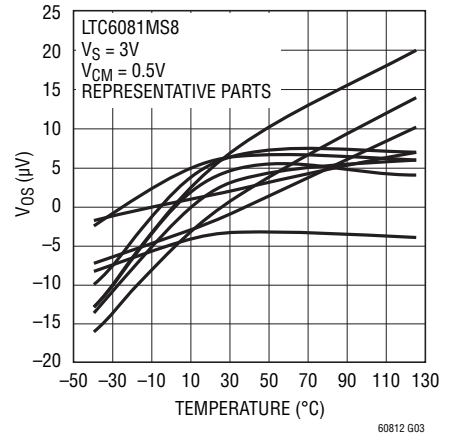
**V<sub>OS</sub> Drift Histogram**



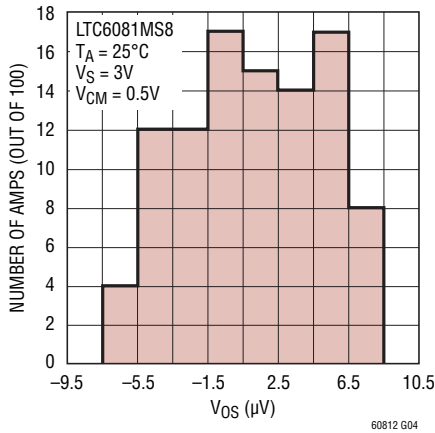
**V<sub>OS</sub> Drift Histogram**



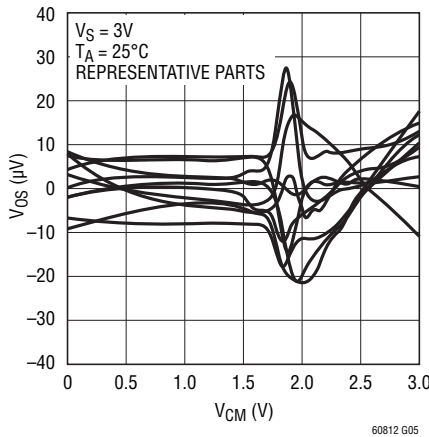
**V<sub>OS</sub> vs Temperature**



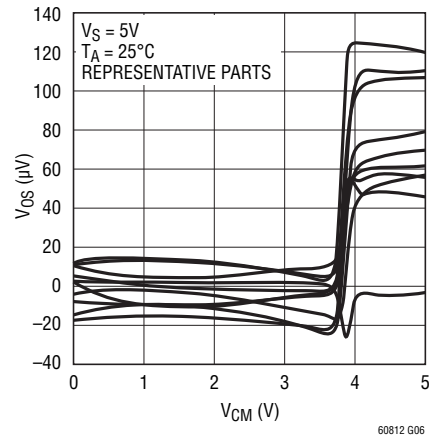
**V<sub>OS</sub> Histogram**



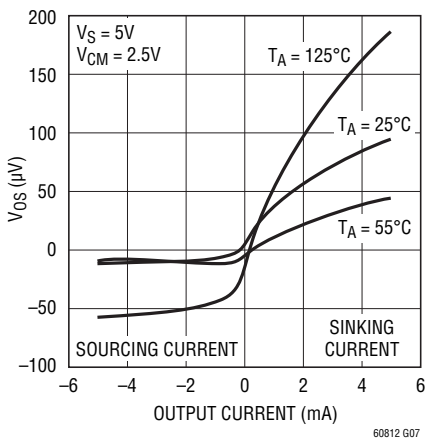
**V<sub>OS</sub> vs V<sub>CM</sub>**



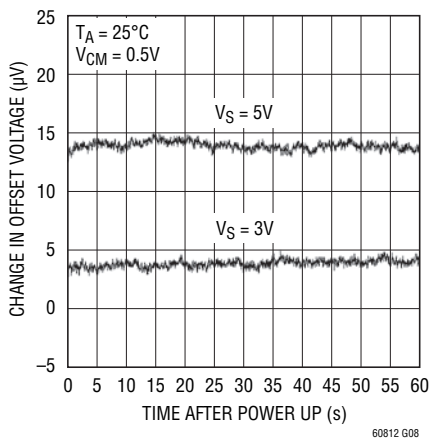
**V<sub>OS</sub> vs V<sub>CM</sub>**



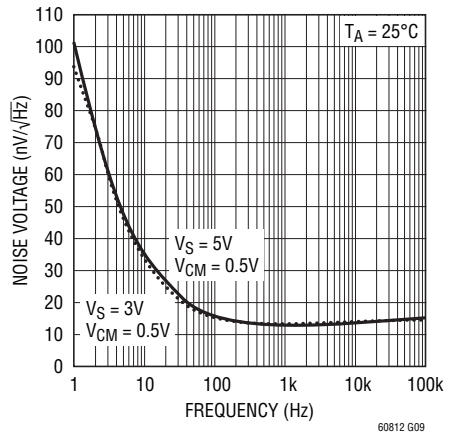
**V<sub>OS</sub> vs Output Current**



**Warm-Up Drift vs Time**

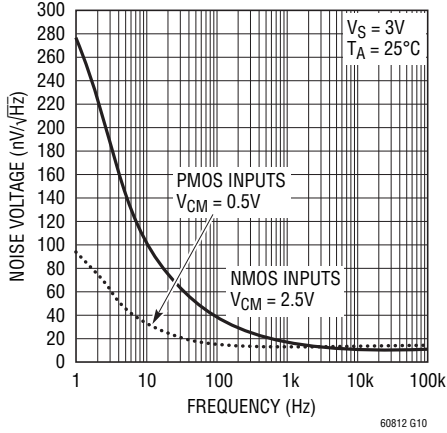


**Noise Voltage vs Frequency**

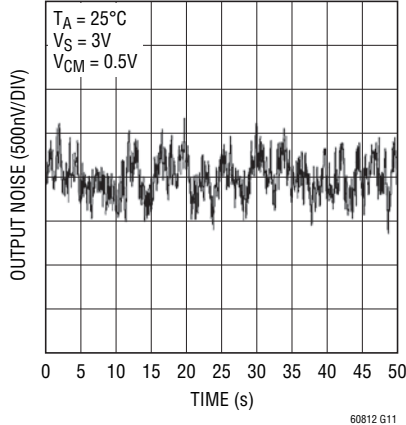


## TYPICAL PERFORMANCE CHARACTERISTICS

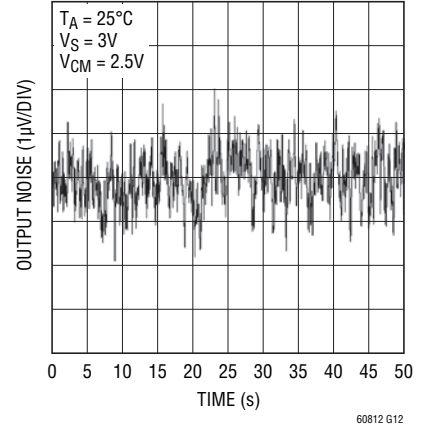
### Noise Voltage vs Frequency



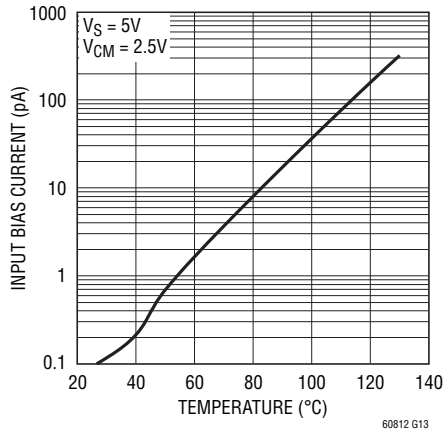
### 0.1Hz to 10Hz Output Voltage Noise



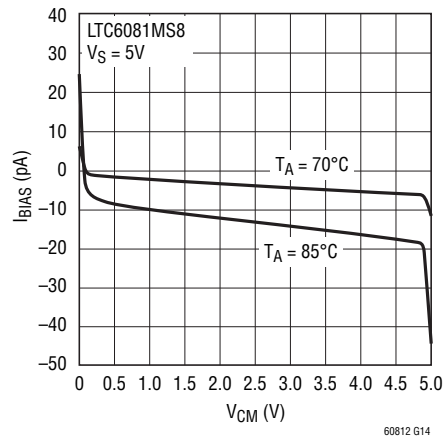
### 0.1Hz to 10Hz Output Voltage Noise



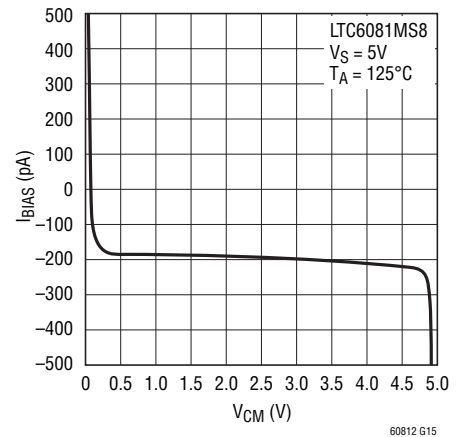
### Input Bias Current vs Temperature



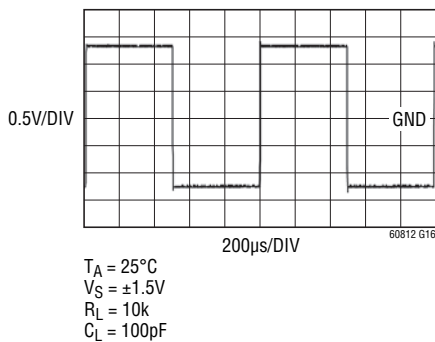
### IBIAS vs VCM



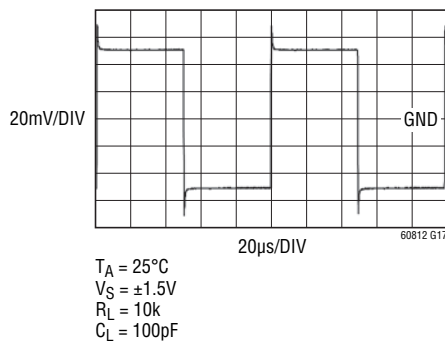
### IBIAS vs VCM



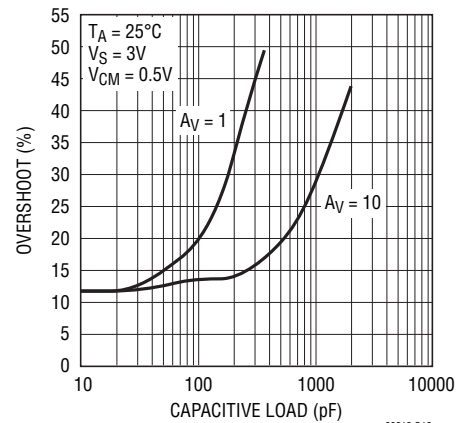
### Large Signal Transient



### Small Signal Transient



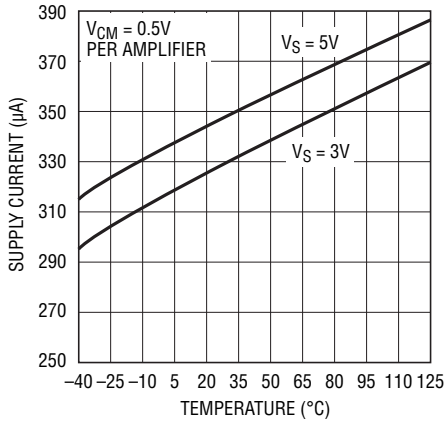
### Overshoot vs CL



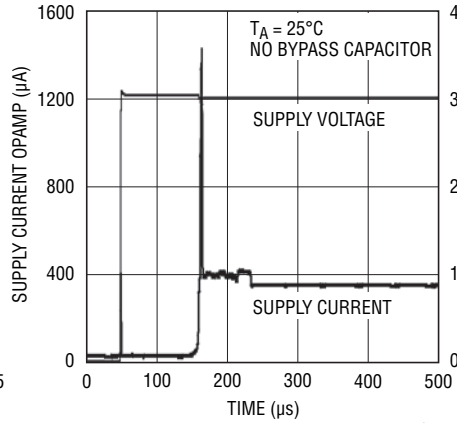


# TYPICAL PERFORMANCE CHARACTERISTICS

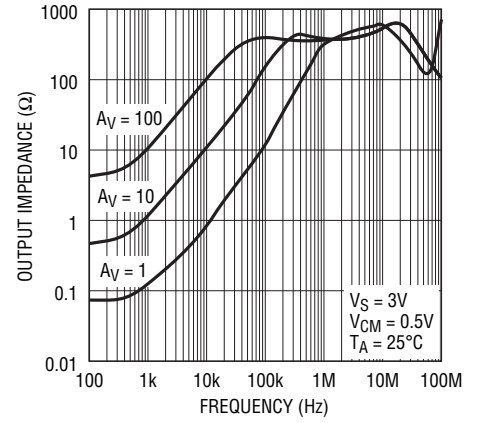
Supply Current vs Temperature



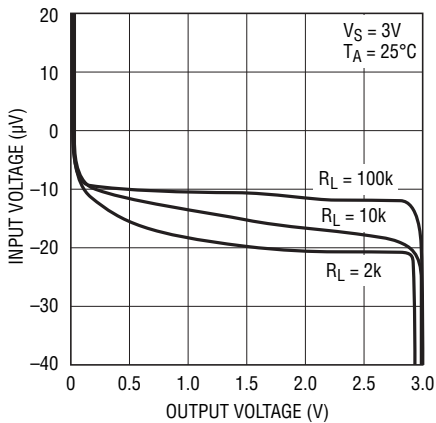
Supply Current vs Time



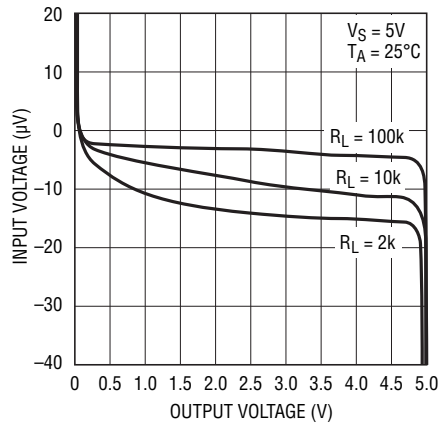
Output Impedance vs Frequency



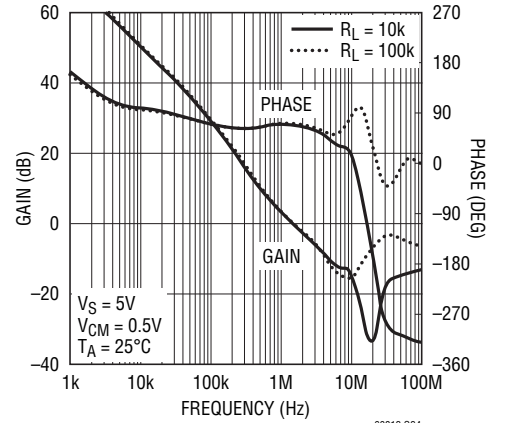
Open Loop Gain



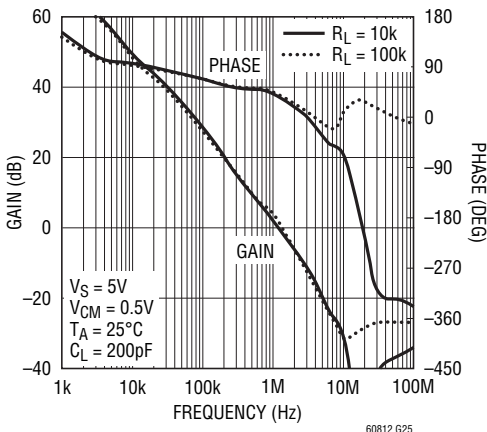
Open Loop Gain



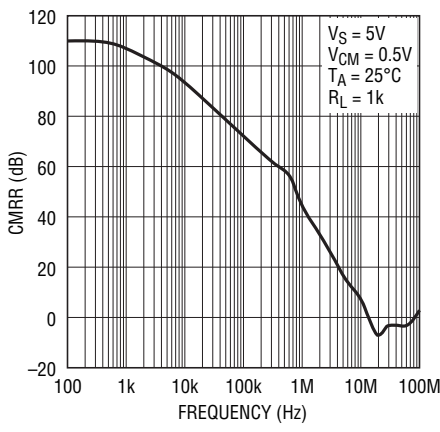
Open Loop Gain vs Frequency



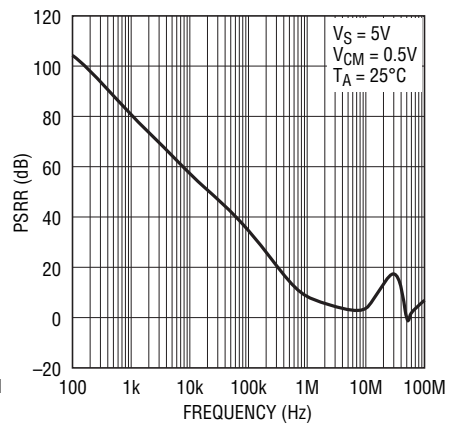
Open Loop Gain vs Frequency



CMRR vs Frequency

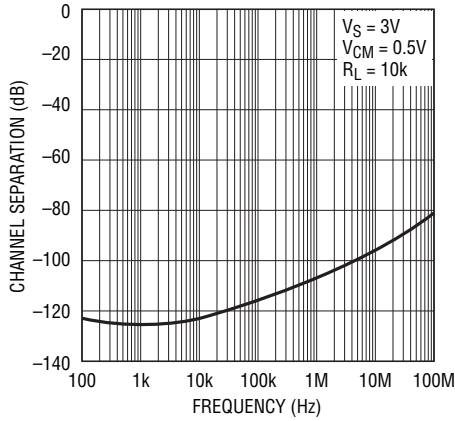


PSRR vs Frequency

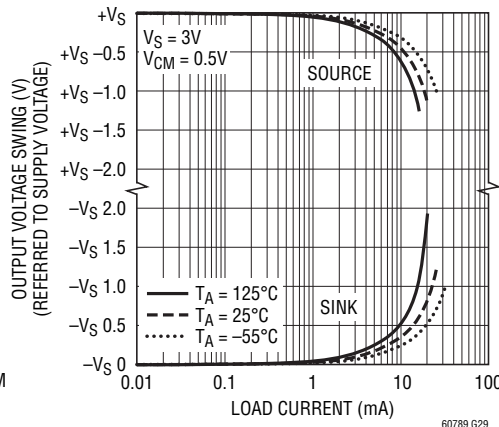


## TYPICAL PERFORMANCE CHARACTERISTICS

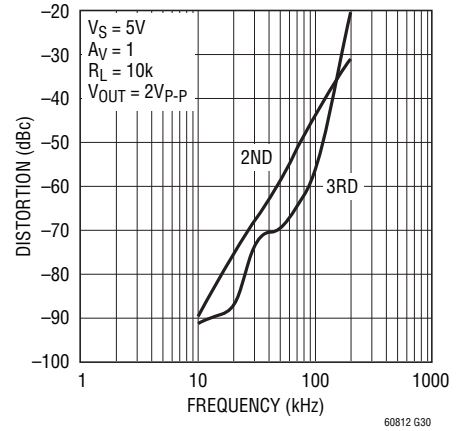
Channel Separation vs Frequency



Output Voltage Swing vs Load Current



Distortion vs Frequency



## PIN FUNCTIONS

**OUT:** Amplifier Output

**-IN:** Inverting Input

**+IN:** Noninverting Input

**V+:** Positive Supply

**V-:** Negative Supply

**SHDN\_A:** Shutdown Pin of Amplifier A, active low and only valid for LTC6081DD. An internal current source pulls the pin to V+ when floating.

**SHDN\_B:** Shutdown Pin of Amplifier B, active low and only valid for LTC6081DD. An internal current source pulls the pin to V+ when floating.

**NC:** Not internally connected.

**Exposed Pad:** Connected to V-.

## APPLICATIONS INFORMATION

### Preserving Input Precision

Preserving input accuracy of the LTC6081/LTC6082 requires that the application circuit and PC board layout do not introduce errors comparable or greater than the  $5\mu\text{V}$  typical offset of the amplifiers. Temperature differentials across the input connections can generate thermocouple voltages of 10's of microvolts so the connections to the input leads should be short, close together and away from heat dissipating components. Air current across the board can also generate temperature differentials.

The extremely low input bias currents ( $0.1\text{pA}$  typical) allow high accuracy to be maintained with high impedance sources and feedback resistors. Leakage currents on the PC board can be higher than the input bias current. For example,  $10\text{G}\Omega$  of leakage between a  $5\text{V}$  supply lead and an input lead will generate  $500\text{pA}$ ! Surround the input leads with a guard ring driven to the same potential as the input common mode voltage to avoid excessive leakage in high impedance applications.

### Capacitive Load

LTC6081/LTC6082 can drive capacitive load up to  $200\text{pF}$  in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load further increases the amount of capacitance the amplifier can drive.

### SHDN Pins

Pins 5 and 6 are used for power shutdown on the LTC6081 in the DD package. If they are floating, internal current sources pull Pins 5 and 6 to  $V^+$  and the amplifiers operate normally. In shutdown, the amplifier output is high impedance, and each amplifier draws less than  $2\mu\text{A}$  current.

### Rail-to-Rail Input

The input stage of LTC6081/LTC6082 combines both PMOS and NMOS differential pairs, extending its input common mode voltage range to both positive and negative supply voltages. At high input common mode range, the NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between  $1.3\text{V}$  and  $0.9\text{V}$  below the positive supply. LTC6081 has better low frequency noise performance with PMOS input on due to its lower flicker noise (see Voltage Noise vs Frequency and  $0.1\text{Hz}$  to  $10\text{Hz}$  Input Voltage Noise in Typical Performance Characteristics).

### Thermal Hysteresis

Figure 1 shows the input offset voltage hysteresis of the LTC6081MS8 for 3 thermal cycles from  $-45^\circ\text{C}$  to  $90^\circ\text{C}$ . The typical offset shift is  $\pm 4\mu\text{V}$ . The data was taken with the ICs in stress free sockets. Mounting to PC boards may cause additional hysteresis due to mechanical stress. The LTC6081 will meet offset voltage specifications in the electrical characteristics table even after  $15\mu\text{V}$  of additional error from thermal hysteresis.

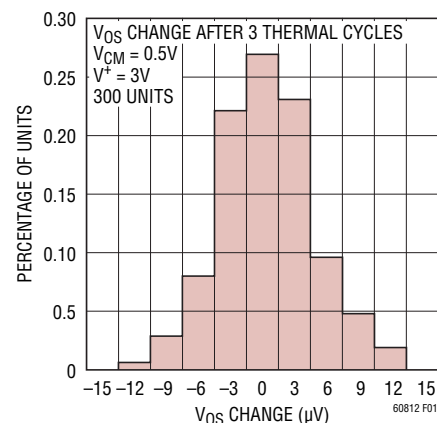


Figure 1.  $V_{OS}$  Thermal Hysteresis of LTC6081MS8

## APPLICATIONS INFORMATION

### PC Board Layout

Mechanical stress on a PC board and soldering-induced stress can cause the  $V_{OS}$  and  $V_{OS}$  drift to shift. The DD and DHC packages are more sensitive to stress. A simple way to reduce the stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board edge acts as a stress boundary, or a region where the flexure of the board is minimum. The package should always be mounted so that the leads absorb the stress

and not the package. The package is generally aligned with the leads perpendicular to the long side of the PC board (see Figure 2).

The most effective technique to relieve the PC board stress is to cut slots in the board around the op amp. These slots can be cut on three sides of the IC and the leads can exit on the fourth side. Figure 2 shows the layout of a LTC6081DD with slots at three sides.

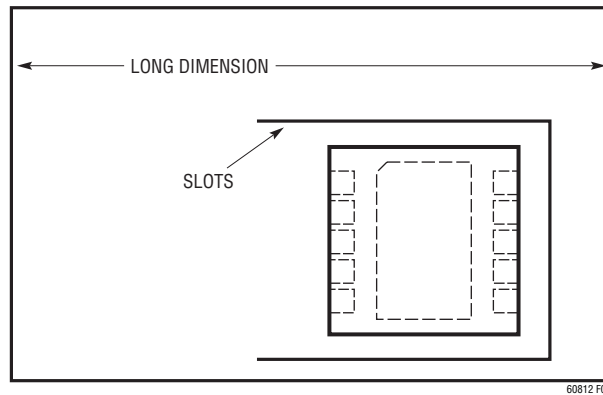
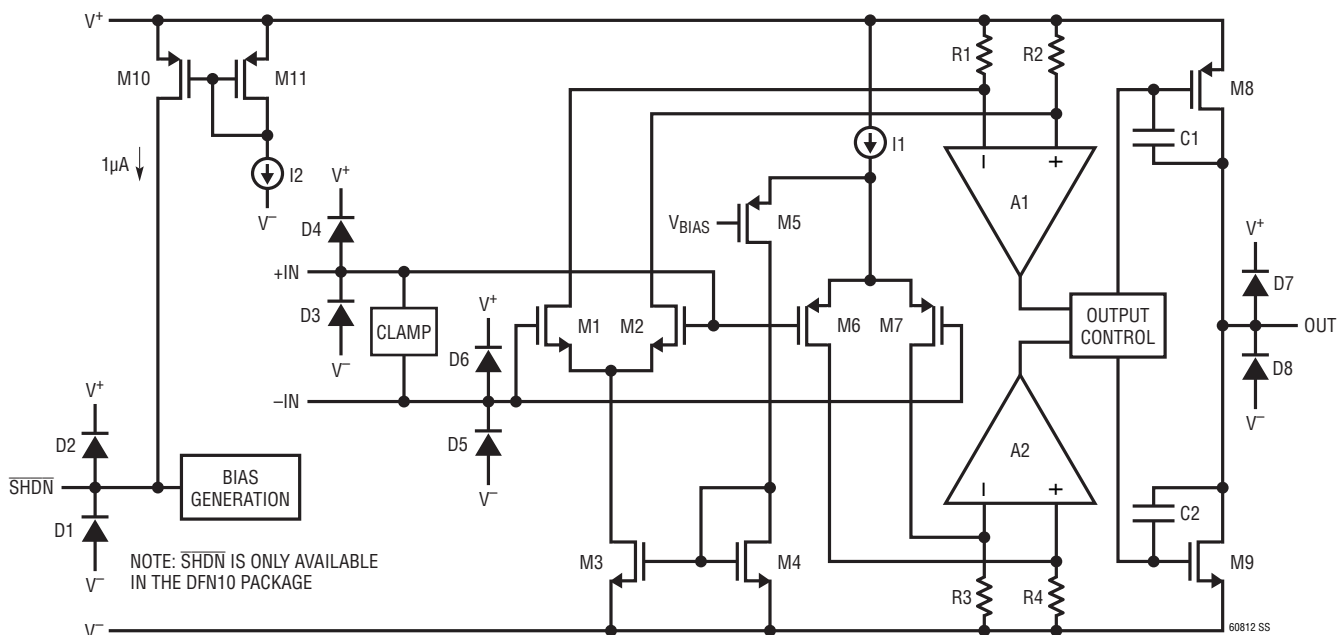


Figure 2. Vertical Orientation of LTC6081DD with Slots

## SIMPLIFIED SCHEMATIC

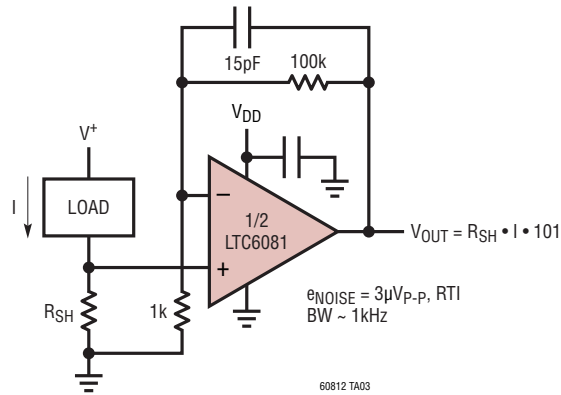
### Simplified Schematic of the Amplifier



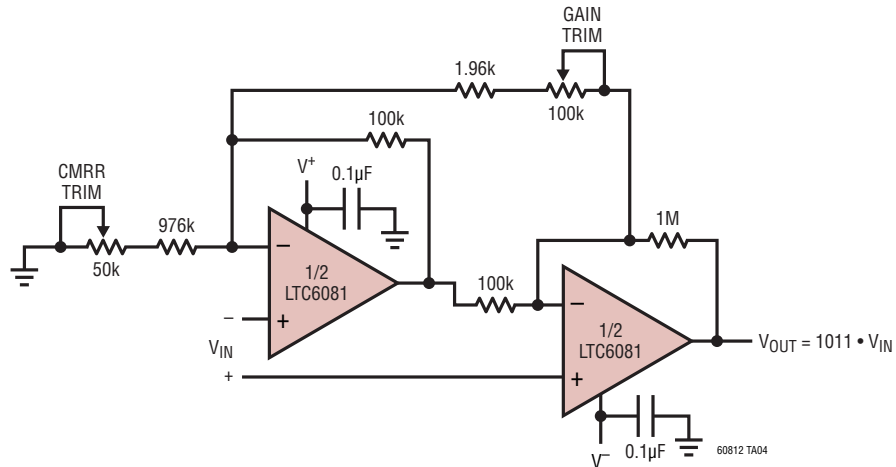
60812fd

## TYPICAL APPLICATIONS

## Low Side Current Sense

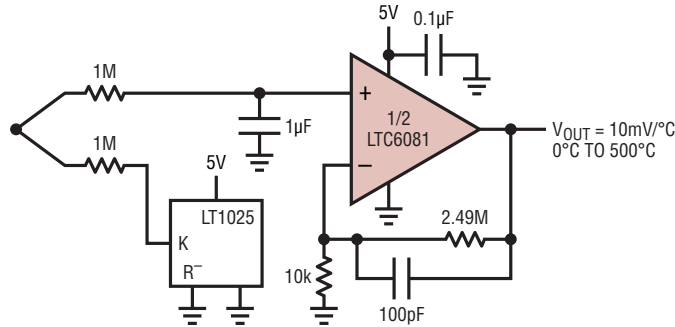


## Two Op-Amp Instrumentation Amplifier



## TYPICAL APPLICATIONS

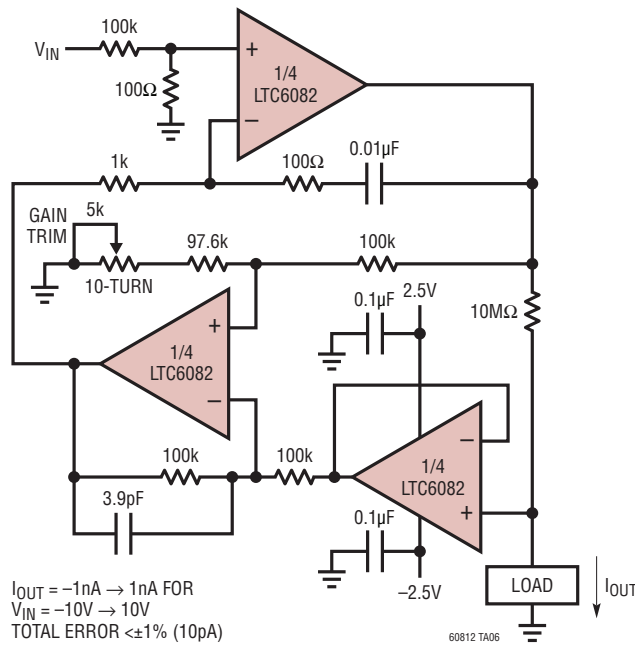
### Thermocouple Amplifier



SENSOR: OMEGA 5TC-TT-K-30-36 K-TYPE THERMOCOUPLE  
 1M RESISTORS PROTECT CIRCUIT TO  $\pm 350V$  WITH NO PHASE REVERSAL OF AMPLIFIER OUTPUT  
 1pA MAX  $I_{BIAS}$  TRANSLATES TO 0.05°C ERROR  
 20µV  $V_{OS}$   $\rightarrow$  0.5°C OFFSET

60812 TA05

### Precision Nanoamp Bidirectional Current Source

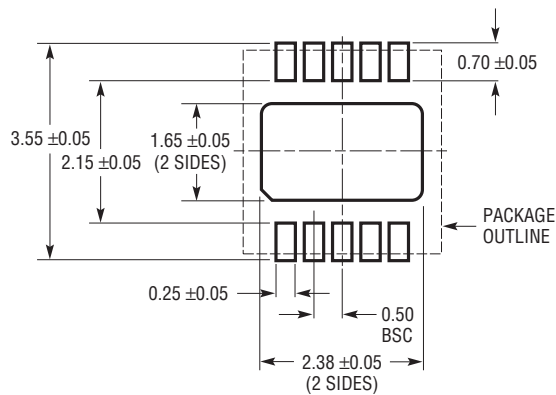


60812 TA06

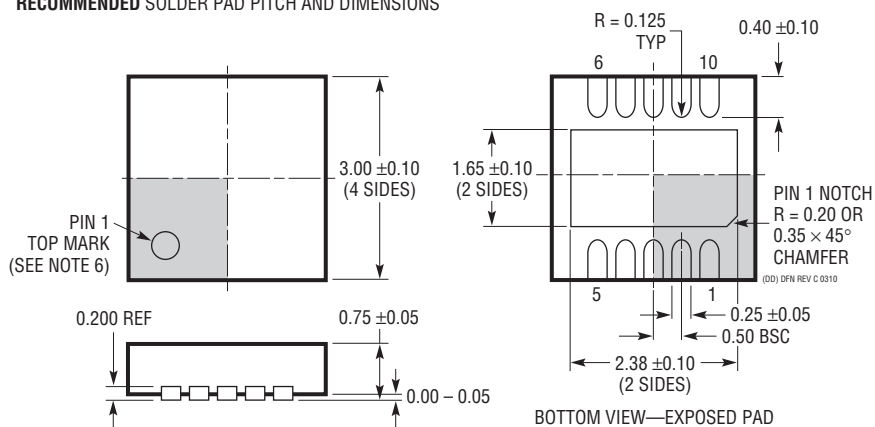
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

### DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699 Rev C)



#### RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



#### NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

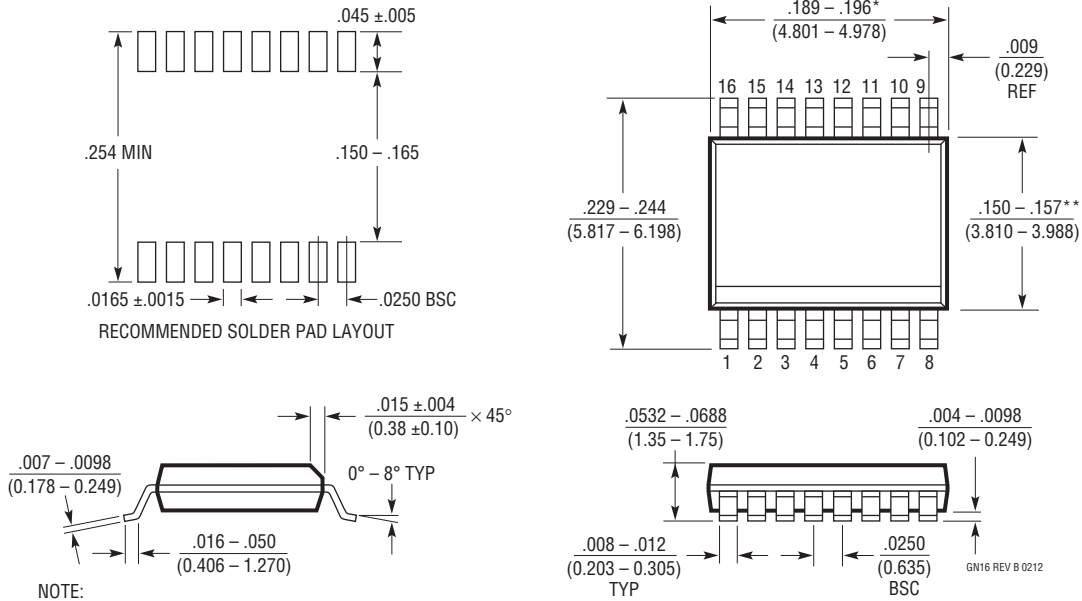




# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

## GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641 Rev B)

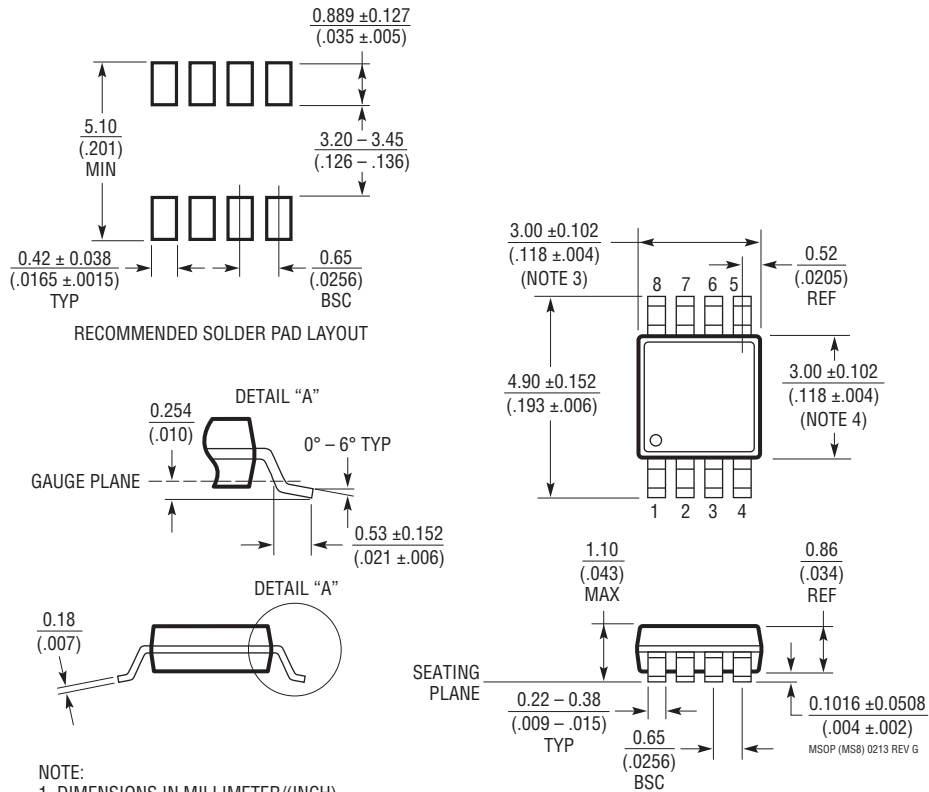


- NOTE:
1. CONTROLLING DIMENSION: INCHES
  2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
  3. DRAWING NOT TO SCALE
  4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE
- \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
- \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

### MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660 Rev G)



**NOTE:**

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

**REVISION HISTORY** (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	3/10	Change LT to LTC on all part numbers in Order Information Section.	3
C	07/10	Update to Simplified Schematic	12
D	12/13	Corrected resistor value (10M)	14