

## Dual/Quad 14MHz, Rail-to-Rail CMOS Amplifiers

### FEATURES

- Low Offset Voltage: 750 $\mu$ V Maximum
- Low Offset Drift: 5 $\mu$ V/ $^{\circ}$ C Maximum
- Input Bias Current:  
 1pA (Typical at 25 $^{\circ}$ C)  
 15pA (Typical at 85 $^{\circ}$ C)
- Rail-to-Rail Inputs and Outputs
- Gain Bandwidth Product: 14MHz
- CMRR: 70dB Minimum
- PSRR: 93dB Minimum
- Input Noise Voltage Density: 12nV/ $\sqrt{\text{Hz}}$
- Supply Current: 1.05mA per Amp
- Shutdown Current: 2.3 $\mu$ A per Amp
- 2.7V to 5.5V Operation Voltage
- Available in 8-Lead MSOP and 10-Lead DFN Packages (LTC6087), 16-Lead SSOP and DFN Packages (LTC6088)

### APPLICATIONS

- Portable Test Equipment
- Medical Equipment
- Audio
- Data Acquisition
- High Impedance Transducer Amplifier

### DESCRIPTION

The LTC<sup>®</sup>6087/LTC6088 are dual/quad, low noise, low offset, rail-to-rail input/output, unity-gain stable CMOS operational amplifiers that feature 1pA of input bias current. A 14MHz gain bandwidth and 7.2V/ $\mu$ s slew rate, combined with low noise (10nV/ $\sqrt{\text{Hz}}$ ) and a low 0.75mV offset, make the LTC6087/LTC6088 useful in a variety of applications. The 1.05mA supply current and the shutdown mode are ideal for signal processing applications which demand performance with minimal power.

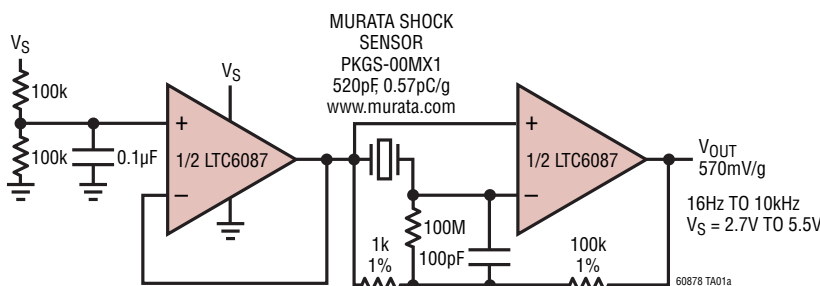
The LTC6087/LTC6088 has an output stage which swings within 30mV of either supply rail to maximize signal dynamic range in low supply applications. The input common mode range includes the entire supply voltage. These op amps are specified on power supply voltages of 3V and 5V from -40 $^{\circ}$ C to 125 $^{\circ}$ C.

The dual amplifier LTC6087 is available in 8-lead MSOP and 10-lead DFN packages. The quad amplifier LTC6088 is available in 16-lead SSOP and DFN packages.

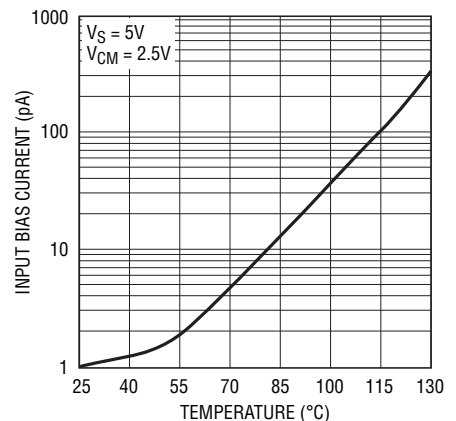
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### TYPICAL APPLICATION

Single Supply Shock/Vibration Sensor Amplifier



LTC6087 Input Bias Current vs Temperature



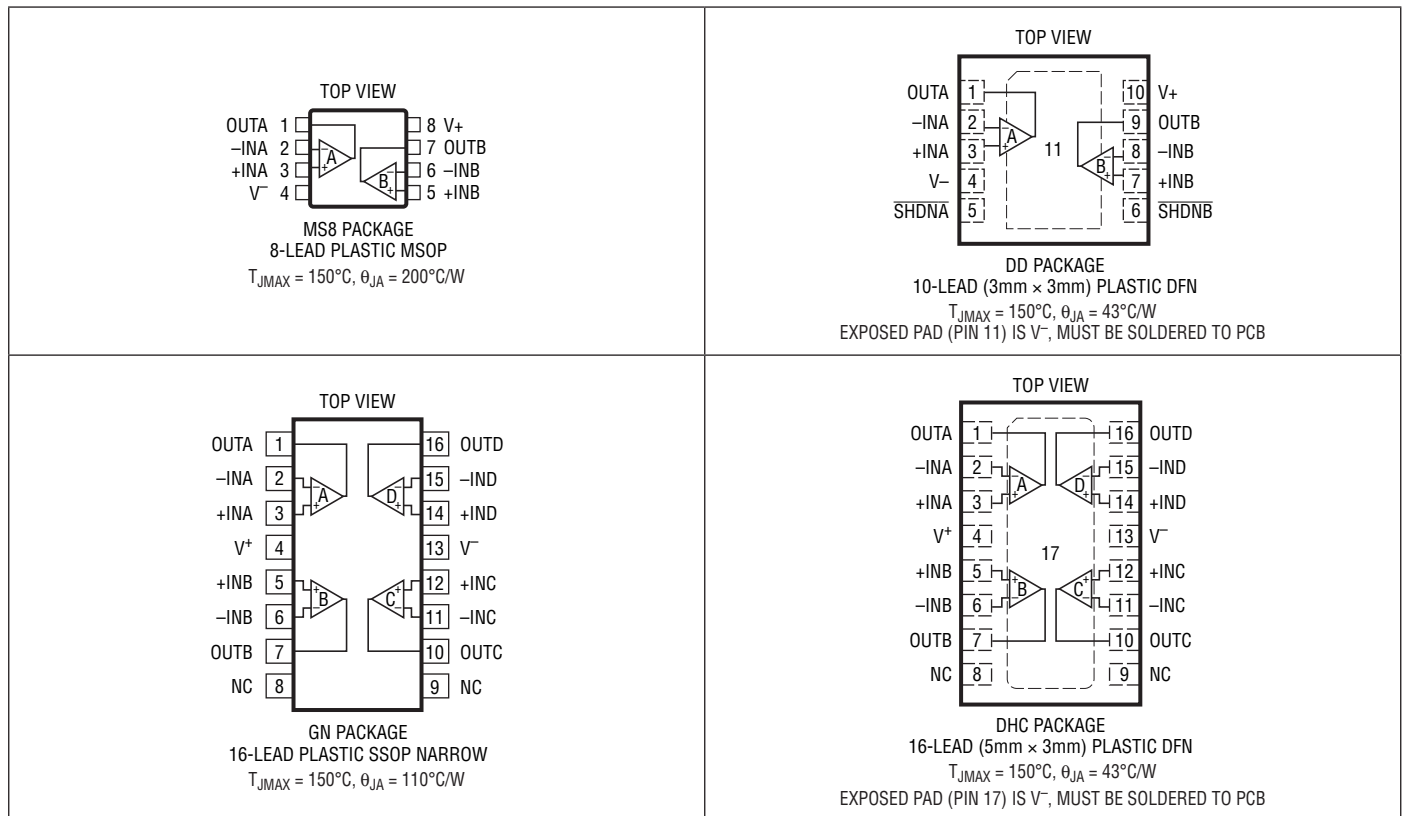
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# LTC6087/LTC6088

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ( $V^+$ to $V^-$ ) .....	6V	Specified Temperature Range (Note 4)	
Input Voltage.....	$V^-$ to $V^+$	LTC6087C/LTC6088C .....	0°C to 70°C
Input Current.....	$\pm 10\text{mA}$	LTC6087H/LTC6088H .....	-40°C to 125°C
SHDNA/SHDNB Voltage .....	$V^-$ to $V^+$	Junction Temperature .....	150°C
Output Short-Circuit Duration (Note 2) .....	Indefinite	Storage Temperature Range .....	-65°C to 150°C
Operating Temperature Range (Note 3)		Lead Temperature (Soldering, 10 sec)	
LTC6087C/LTC6088C .....	-40°C to 85°C	MS8, GN16 Only .....	300°C
LTC6087H/LTC6088H .....	-40°C to 125°C		

## PIN CONFIGURATION



## ORDER INFORMATION

(<http://www.linear.com/product/LTC6087-X#orderinfo>)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6087CDD#PBF	LTC6087CDD#TRPBF	LCTX	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6087HDD#PBF	LTC6087HDD#TRPBF	LCTX	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC6087CMS8#PBF	LTC6087CMS8#TRPBF	LTCTY	8-Lead Plastic MSOP	-40°C to 85°C
LTC6087HMS8#PBF	LTC6087HMS8#TRPBF	LTCTY	8-Lead Plastic MSOP	-40°C to 125°C
LTC6088CDHC#PBF	LTC6088CDHC#TRPBF	6088	16-Lead (5mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6088HDHC#PBF	LTC6088HDHC#TRPBF	6088	16-Lead (5mm × 3mm) Plastic DFN	-40°C to 125°C
LTC6088CGN#PBF	LTC6088CGN#TRPBF	6088	16-Lead Plastic SSOP	-40°C to 85°C
LTC6088HGN#PBF	LTC6088HGN#TRPBF	6088H	16-Lead Plastic SSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C SUFFIX			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Offset Voltage (Note 5)	LTC6087MS8, LTC6088GN		±330	±750	±330	±750	μV	
		LTC6087DD, LTC6088DHC		±330	±1100	±330	±1100	μV	
		LTC6087MS8, LTC6088GN	●		±900		±1100	μV	
		LTC6087DD, LTC6088DHC	●		±1350		±1600	μV	
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	LTC6087MS8, LTC6088GN	●	±2	±5	±2	±5	μV/°C	
		LTC6087DD, LTC6088DHC	●	±2	±5	±2	±5	μV/°C	
$I_B$	Input Bias Current (Notes 5, 7)	Guaranteed by 5V Test	●	1		1		pA	
					40		500	pA	
$I_{OS}$	Input Offset Current (Notes 5, 7)	Guaranteed by 5V Test	●	0.5		0.5		pA	
					30		150	pA	
$e_n$	Input Noise Voltage Density	f = 1kHz		12		12		nV/√Hz	
		f = 10kHz		10		10		nV/√Hz	
	Input Noise Voltage	0.1Hz to 10Hz		2.5		2.5		μV <sub>P-P</sub>	
$i_n$	Input Noise Current Density (Note 8)	f = 1Hz		0.56		0.56		fA/√Hz	
			Input Common Mode Range	●	V <sup>-</sup>	V <sup>+</sup>	V <sup>-</sup>	V <sup>+</sup>	V
$C_{IN}$	Input Capacitance Differential Mode Common Mode	f = 100kHz		2.7		2.7		pF	
					4.2		4.2	pF	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 3\text{V}$	●	64	80	64	80	dB	
				63		61		dB	
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V to } 5.5\text{V}$	●	93	115	93	115	dB	
				90		85		dB	
$V_{OUT}$	Output Voltage, High (Referred to V <sup>+</sup> )	No Load	●	5	15	5	20	mV	
		$I_{SOURCE} = 1\text{mA}$	●		25	50	25	50	mV
		$I_{SOURCE} = 5\text{mA}$	●		120	210	120	230	mV
	Output Voltage, Low (Referred to V <sup>-</sup> )	No Load	●	5	25	5	30	mV	
		$I_{SINK} = 1\text{mA}$	●		25	50	25	60	mV
		$I_{SINK} = 5\text{mA}$	●		120	210	120	240	mV

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# LTC6087/LTC6088

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C SUFFIX			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$R_{\text{LOAD}} = 10\text{k}$ , $0.5\text{V} \leq V_{\text{OUT}} \leq 2.5\text{V}$	●	500 300	3000	500 30	3000	V/mV V/mV	
$I_{\text{SC}}$	Output Short-Circuit Current	Source and Sink	●	25 21	35	25 18	35	mA mA	
SR	Slew Rate	$A_V = 1$		7.2		7.2		V/ $\mu\text{s}$	
GBW	Gain Bandwidth Product ( $f_{\text{TEST}} = 20\text{kHz}$ )	$R_{\text{LOAD}} = 50\text{k}$ , $V_{\text{CM}} = 1.5\text{V}$	●	10 9	14	10 8	14	MHz MHz	
$\Phi_0$	Phase Margin	$R_L = 10\text{k}$ , $C_L = 5\text{pF}$ , $A_V = 1$ , $V_{\text{CM}} = V_S/2$		45		45		Deg	
$t_S$	Settling Time 0.1%	$V_{\text{STEP}} = 2\text{V}$ , $A_V = -1$ , $R_L = 1\text{k}$		1		1		$\mu\text{s}$	
$I_S$	Supply Current (per Amplifier)	No Load	●	1.05 1.05	1.20 1.25	1.05 1.05	1.20 1.35	mA mA	
	Shutdown Current (per Amplifier)	Shutdown, $V_{\text{SHDNx}} \leq 0.8\text{V}$	●	0.2	1	0.2	1	$\mu\text{A}$	
$V_S$	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7	5.5	2.7	5.5	V	
	Channel Separation	$f_S = 10\text{kHz}$		-120		-120		dB	
	Shutdown Logic	SHDNx High SHDNx Low	● ●	2	0.8	2	0.8	V V	
$t_{\text{ON}}$	Turn-On Time	$V_{\text{SHDNx}} = 0.8\text{V}$ to 2V		6		6		$\mu\text{s}$	
$t_{\text{OFF}}$	Turn-Off Time	$V_{\text{SHDNx}} = 2\text{V}$ to 0.8V		2		2		$\mu\text{s}$	
	Leakage of SHDN Pin	$V_{\text{SHDNx}} = 0\text{V}$	●	0.1	0.5	0.1	0.5	$\mu\text{A}$	

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C SUFFIX			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{\text{OS}}$	Offset Voltage (Note 5)	LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC	● ●	$\pm 330$ $\pm 330$	$\pm 750$ $\pm 1100$ $\pm 900$ $\pm 1350$	$\pm 330$ $\pm 330$	$\pm 750$ $\pm 1100$ $\pm 1100$ $\pm 1600$	$\mu\text{V}$ $\mu\text{V}$ $\mu\text{V}$ $\mu\text{V}$	
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift (Note 6)	LTC6087MS8, LTC6088GN LTC6087DD, LTC6088DHC	● ●	$\pm 2$ $\pm 2$	$\pm 5$ $\pm 5$	$\pm 2$ $\pm 2$	$\pm 5$ $\pm 5$	$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$	
$I_B$	Input Bias Current (Notes 5, 7)		●	1	40	1	500	pA pA	
$I_{\text{OS}}$	Input Offset Current (Notes 5, 7)		●	0.5	30	0.5	150	pA pA	
$e_n$	Input Noise Voltage Density	$f = 1\text{kHz}$ $f = 10\text{kHz}$		12 10		12 10		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$	
	Input Noise Voltage	0.1Hz to 10Hz		2.5		2.5		$\mu\text{V}_{\text{P-P}}$	
$i_n$	Input Noise Current Density (Note 8)	$f = 1\text{Hz}$		0.56		0.56		$\text{fA}/\sqrt{\text{Hz}}$	
	Input Common Mode Range		●	$V^-$	$V^+$	$V^-$	$V^+$	V	
$C_{\text{IN}}$	Input Capacitance Differential Mode Common Mode	$f = 100\text{kHz}$		2.7 4.2		2.7 4.2		pF pF	

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 0.5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C SUFFIX			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 5\text{V}$	●	70 68	84	70 66	84	dB dB	
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V}$ to $5.5\text{V}$	●	93 90	115	93 85	115	dB dB	
$V_{\text{OUT}}$	Output Voltage, High (Referred to $V^+$ )	No Load $I_{\text{SOURCE}} = 1\text{mA}$ $I_{\text{SOURCE}} = 5\text{mA}$	● ● ●		5 20 110	15 50 190	5 20 110	20 50 210	mV mV mV
	Output Voltage, Low (Referred to $V^-$ )	No Load $I_{\text{SINK}} = 1\text{mA}$ $I_{\text{SINK}} = 5\text{mA}$	● ● ●		5 20 110	25 50 200	5 20 110	30 60 220	mV mV mV
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$R_{\text{LOAD}} = 10\text{k}\Omega$ , $0.5\text{V} \leq V_{\text{OUT}} \leq 4.5\text{V}$	●	1000 500	6000	1000 50	6000	V/mV V/mV	
$I_{\text{SC}}$	Output Short-Circuit Current	Source and Sink	●	28 25	45	28 22	45	mA mA	
SR	Slew Rate	$A_V = 1$			7.2		7.2	V/ $\mu\text{s}$	
GBW	Gain Bandwidth Product ( $f_{\text{TEST}} = 20\text{kHz}$ )	$R_{\text{LOAD}} = 50\text{k}\Omega$ , $V_{\text{CM}} = 2.5\text{V}$	●	10 9	14	10 8	14	MHz MHz	
$\Phi_0$	Phase Margin	$R_L = 10\text{k}\Omega$ , $C_L = 5\text{pF}$ , $A_V = 1$ , $V_{\text{CM}} = V_S/2$			47		47	Deg	
$t_S$	Settling Time 0.1%	$V_{\text{STEP}} = 2\text{V}$ , $A_V = -1$ , $R_L = 1\text{k}\Omega$			0.8		0.8	$\mu\text{s}$	
$I_S$	Supply Current (per Amplifier)	No Load	●		1.05 1.05	1.25 1.30	1.05 1.05	1.25 1.40	mA mA
	Shutdown Current (per Amplifier)	Shutdown, $V_{\text{SHDNx}} \leq 1.2\text{V}$	●		2.3	5	2.3	5	$\mu\text{A}$
$V_S$	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7		5.5	2.7	5.5	V
	Channel Separation	$f_S = 10\text{kHz}$			-120		-120		dB
	Shutdown Logic	$\overline{\text{SHDNx}}$ High $\overline{\text{SHDNx}}$ Low	● ●	3.5		1.2	3.5	1.2	V V
	$t_{\text{ON}}$	Turn-On Time			6		6		$\mu\text{s}$
$t_{\text{OFF}}$	Turn-Off Time	$V_{\text{SHDNx}} = 3.5\text{V}$ to $1.2\text{V}$			2		2		$\mu\text{s}$
	Leakage of $\overline{\text{SHDN}}$ Pin	$V_{\text{SHDNx}} = 0\text{V}$	●		0.4	1	0.4	1	$\mu\text{A}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and the total output current.

**Note 3:** The LTC6087C/LTC6088C are guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6087H/LTC6088H are guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 4:** The LTC6087C/LTC6088C are guaranteed to meet specified performance from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . The LTC6087C/LTC6088C are designed, characterized and expected to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  but are not tested or QA sampled at these temperatures.

The LTC6087H/LTC6088H are guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 5:** ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6087/LTC6088; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

**Note 6:** This parameter is not 100% tested.

**Note 7:** This specification is limited by high speed automated test capability. See Typical Performance Characteristic curves for actual performance.

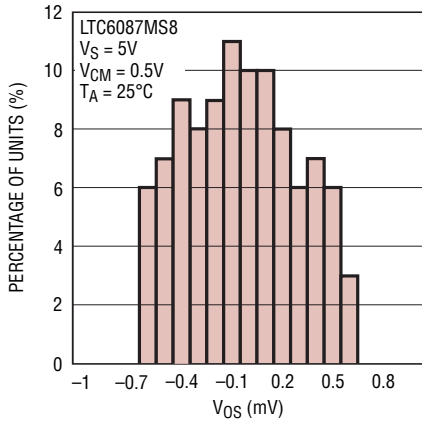
**Note 8:** Current noise is calculated from:

$$i_n = \sqrt{2qI_B}$$

where  $q = 1.6 \cdot 10^{-19}$  coulombs.

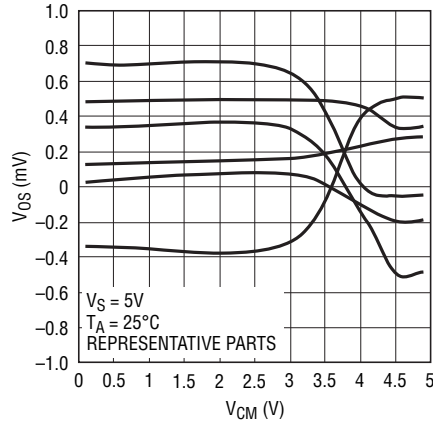
## TYPICAL PERFORMANCE CHARACTERISTICS

### $V_{OS}$ Distribution



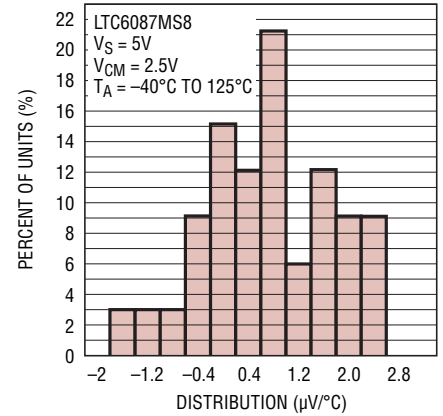
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### $V_{OS}$ vs $V_{CM}$



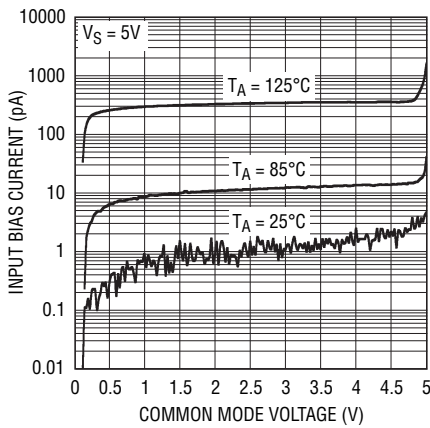
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### $V_{OS}$ Drift Distribution



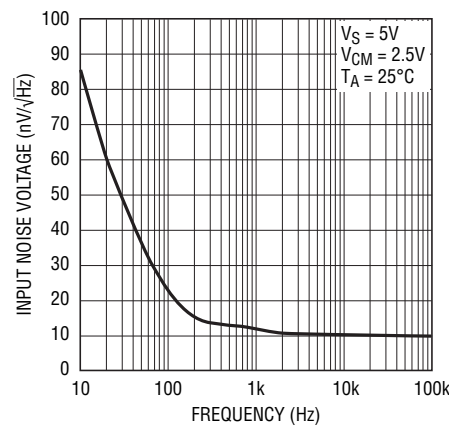
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### Input Bias Current vs Common Mode Voltage



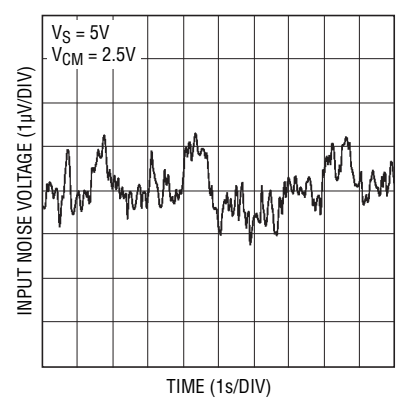
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### Input Noise Voltage vs Frequency



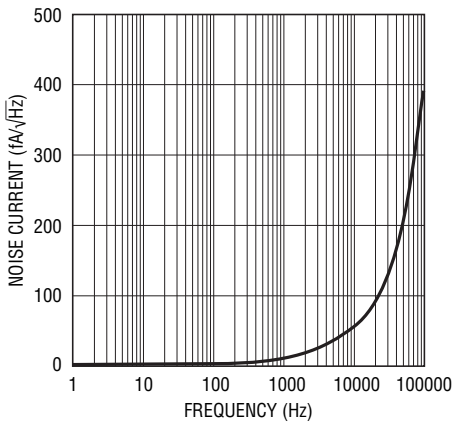
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### 0.1Hz to 10Hz Output Voltage Noise



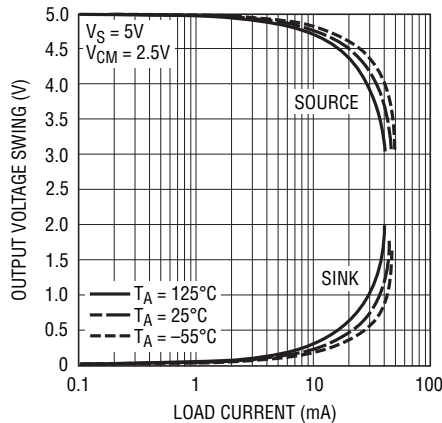
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### Input Noise Current vs Frequency



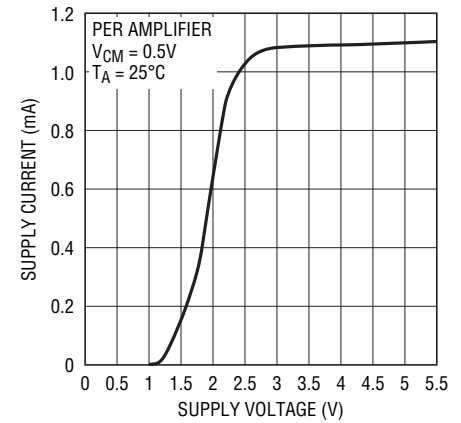
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### Output Voltage Swing vs Load Current



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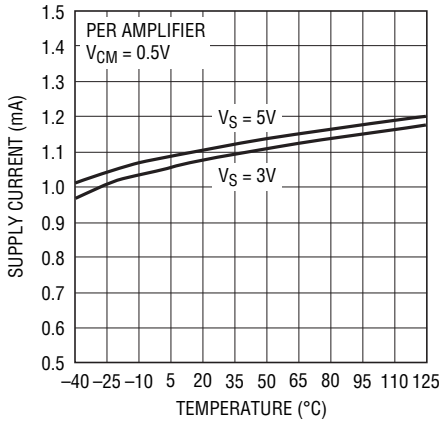
### Supply Current vs Supply Voltage



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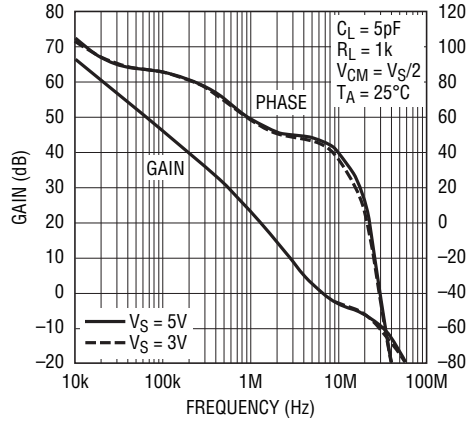
# TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current vs Temperature**



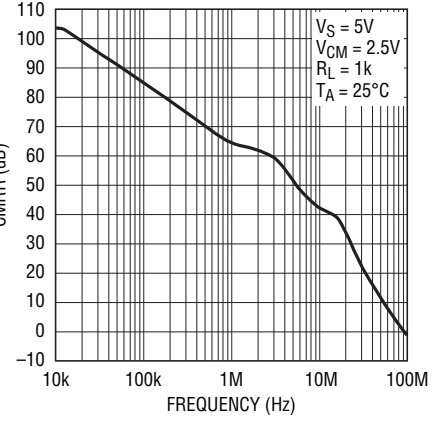
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**Open-Loop Gain vs Frequency**



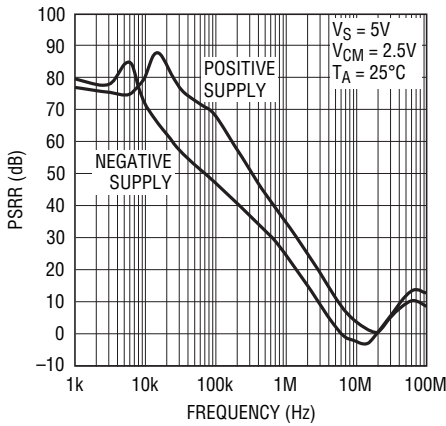
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**CMRR vs Frequency**



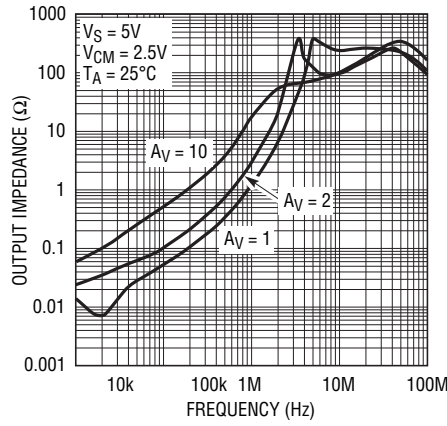
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**PSRR vs Frequency**



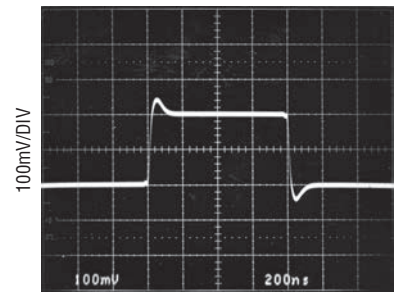
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**Output Impedance vs Frequency**



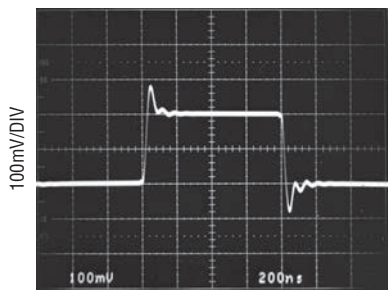
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**Small-Signal Response**



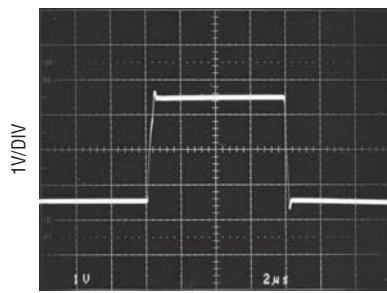
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**Small-Signal Response**



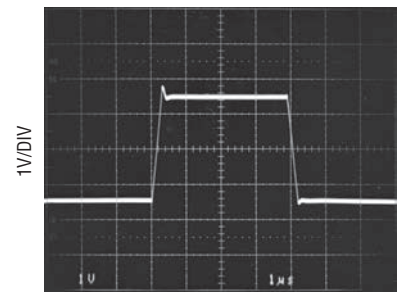
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**Large-Signal Response**



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**Large-Signal Response**

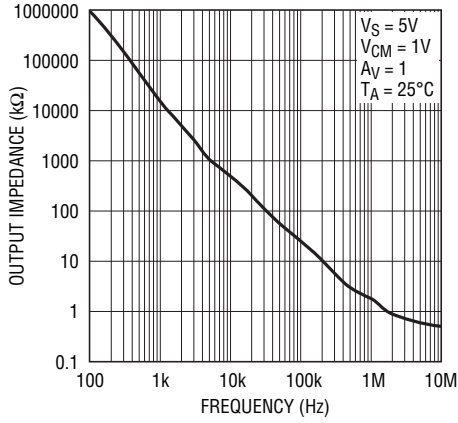


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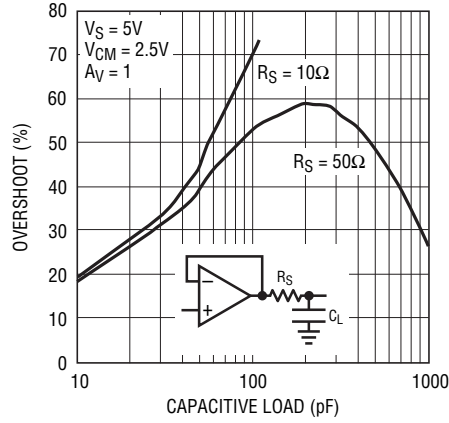
## TYPICAL PERFORMANCE CHARACTERISTICS

**Disabled Output Impedance vs Frequency**



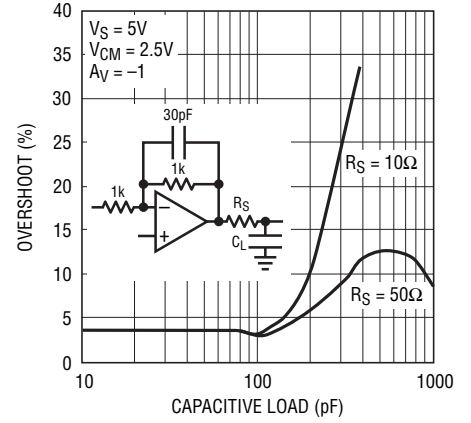
60878 G20

**Overshoot vs Capacitive Load**



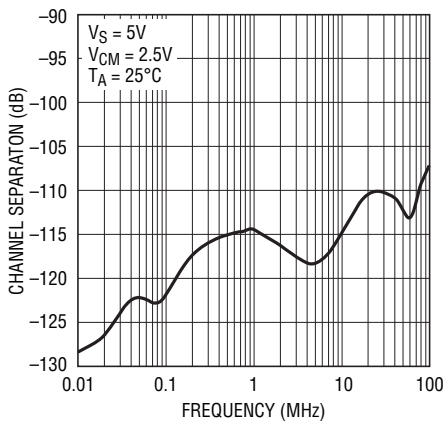
60878 G21

**Overshoot vs Capacitive Load**



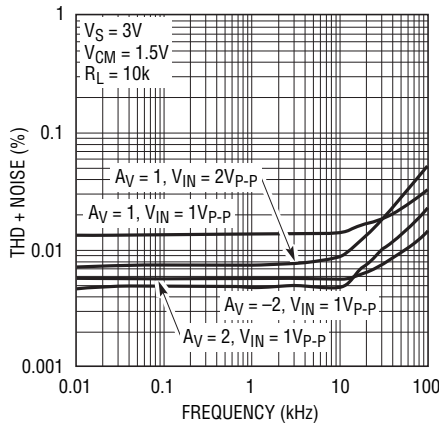
60878 G22

**Channel Separation vs Frequency**



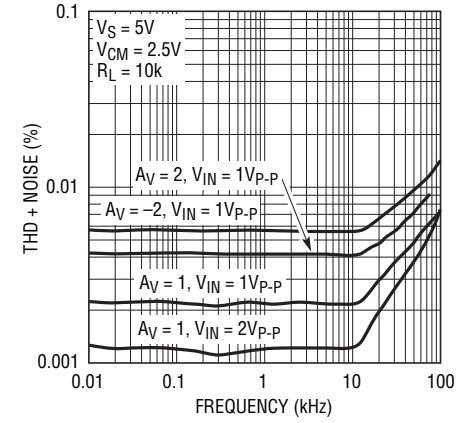
60878 G23

**Total Harmonic Distortion + Noise vs Frequency**



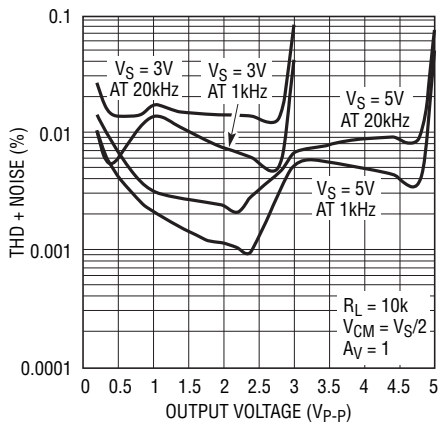
60878 G24

**Total Harmonic Distortion + Noise vs Frequency**



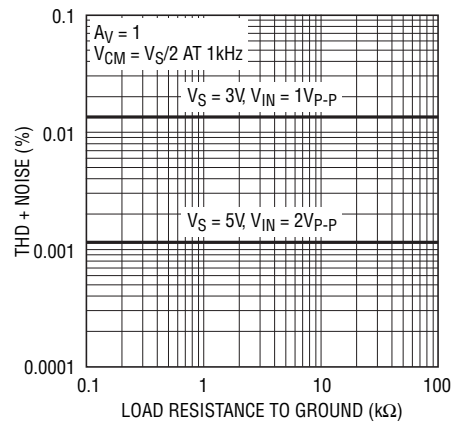
60878 G25

**Total Harmonic Distortion + Noise vs Output Voltage**



60878 G26

**Total Harmonic Distortion + Noise vs Load Resistance**



60878 G27



## PIN FUNCTIONS

**OUT:** Amplifier Output.

**-IN:** Inverting Input.

**+IN:** Noninverting Input.

**V<sup>+</sup>:** Positive Supply.

**V<sup>-</sup>:** Negative Supply.

**SHDNA:** Shutdown Pin of Amplifier A, active low and only available with the LTC6087DD. An internal current source pulls the pin to V<sup>+</sup> when floating.

**SHDNB:** Shutdown Pin of Amplifier B, active low and only available with the LTC6087DD. An internal current source pulls the pin to V<sup>+</sup> when floating.

**NC:** Not internally connected

**Exposed Pad:** Connected to V<sup>-</sup>.

## APPLICATIONS INFORMATION

### Rail-to-Rail Input

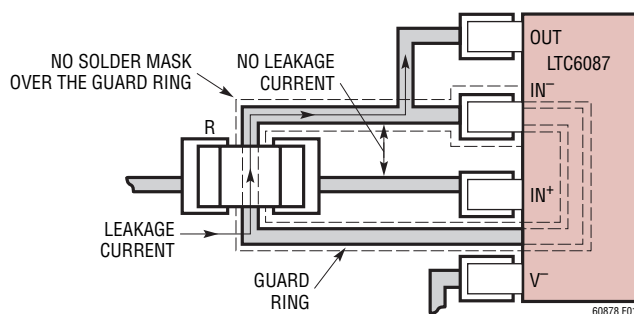
The input stage of LTC6087/LTC6088 combines both PMOS and NMOS differential pairs, extending its input common mode voltage to both positive and negative supply voltages. At high input common mode range, the NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between 1.3V and 0.9V below the positive supply.

### Achieving Low Input Bias Current

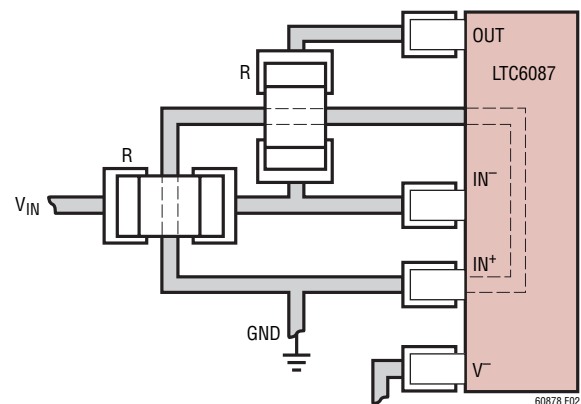
The DD and DHC packages are leadless and make contact to the PCB beneath the package. Solder flux used during the attachment of the part to the PCB can create leakage current paths and can degrade the input bias current performance of the part. All inputs are susceptible because the backside paddle is connected to V<sup>-</sup> internally. As the input voltage or V<sup>-</sup> changes, a leakage path can be formed and alter the observed input bias current. For lowest bias current use the LTC6087/LTC6088 in the leaded MSOP/

GN package. With fine PCB design rules, you can also provide a guard ring around the inputs.

For example, in high source impedance applications such as pH probes, photo diodes, strain gauges, et cetera, the low input bias current of these parts requires a clean board layout to minimize additional leakage current into a high impedance signal node. A mere 100GΩ of PC board resistance between a 5V supply trace and input trace near ground potential adds 50pA of leakage current. This leakage is far greater than the bias current of the operational amplifier. A guard ring around the high impedance input traces driven by a low impedance source equal to the input voltage prevents such leakage problems. The guard ring should extend as far as necessary to shield the high impedance signal from any and all leakage paths. Figure 1 shows the use of a guard ring in a unity-gain configuration. In this case the guard ring is connected to the output and is shielding the high impedance noninverting input from V<sup>-</sup>. Figure 2 shows the inverting gain configuration.



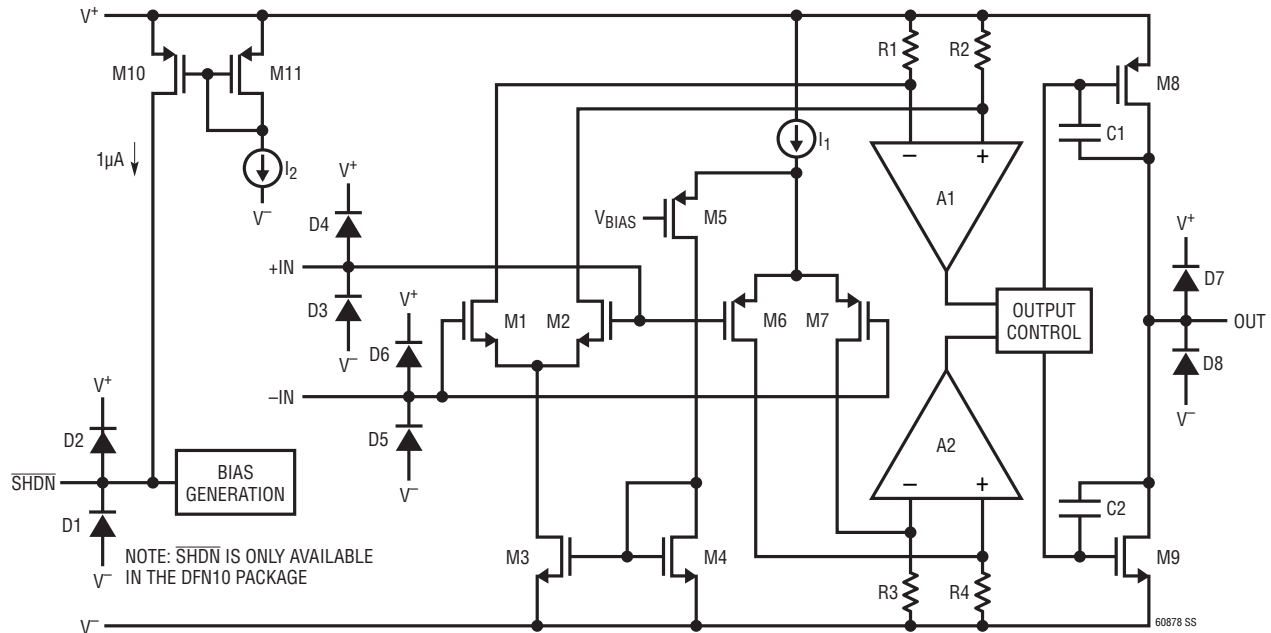
**Figure 1. Sample Layout. Unity-Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage**



**Figure 2. Sample Layout. Inverting Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage**



# SIMPLIFIED SCHEMATIC

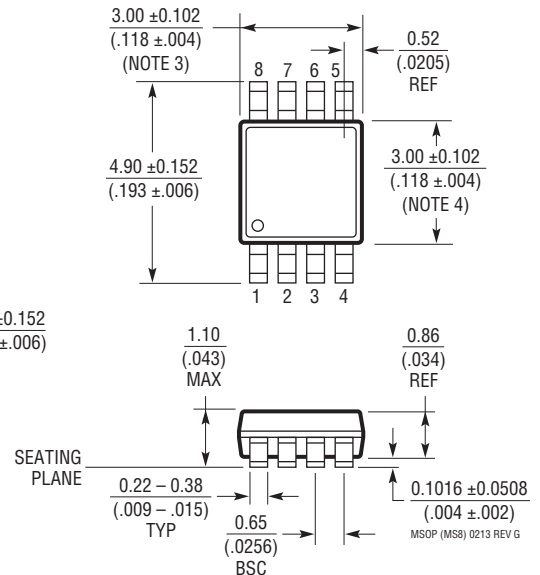
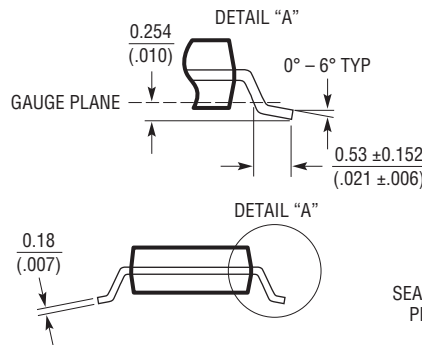
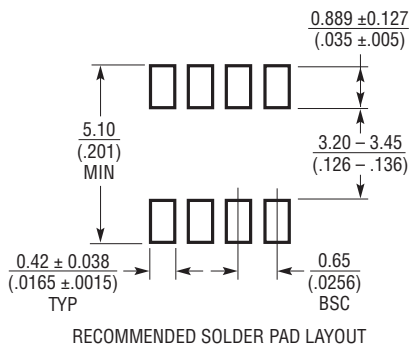


# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC6087#packaging> for the most recent package drawings.

## MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev G)



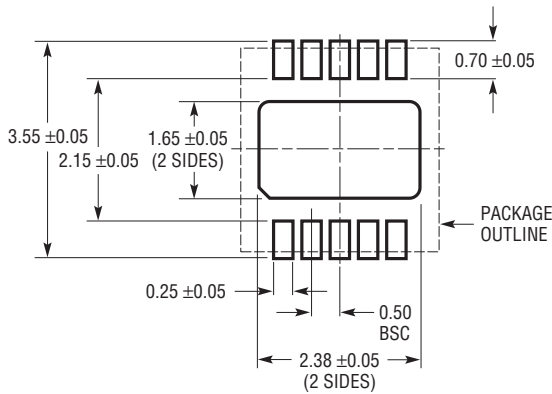
- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
  2. DRAWING NOT TO SCALE
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

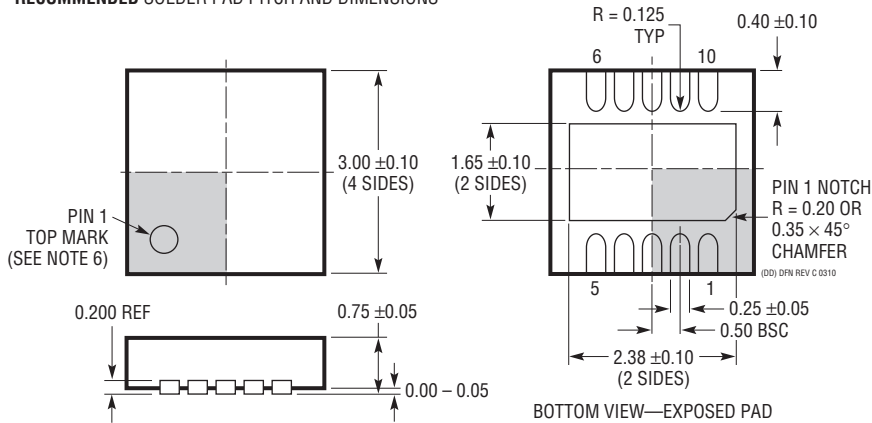
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC6087#packaging> for the most recent package drawings.

**DD Package**  
**10-Lead Plastic DFN (3mm × 3mm)**  
 (Reference LTC DWG # 05-08-1699 Rev C)



**RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS**

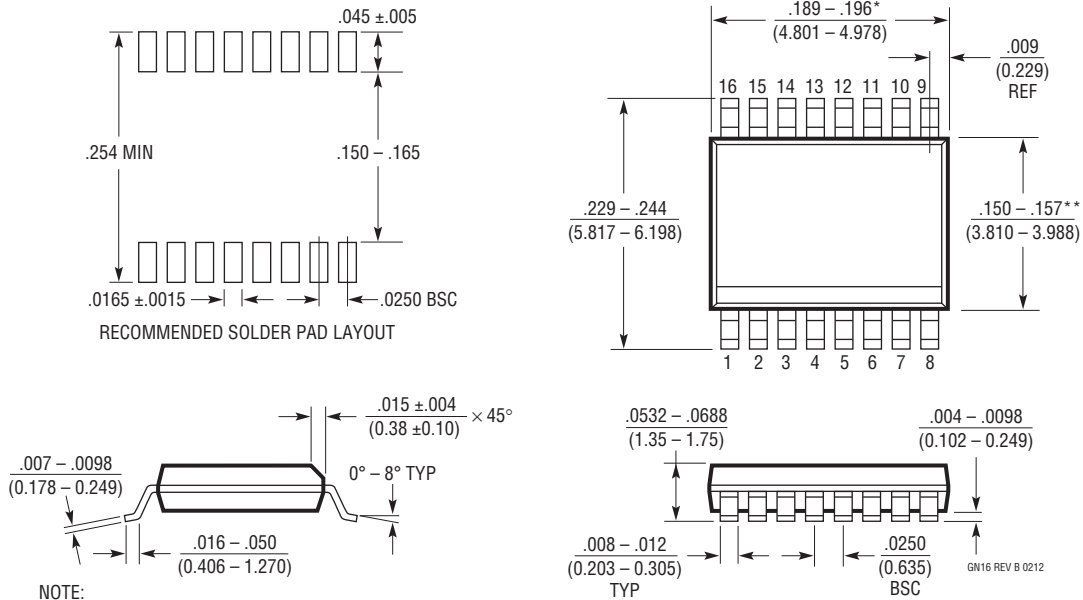


- NOTE:**
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC6087#packaging> for the most recent package drawings.

## GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641 Rev B)



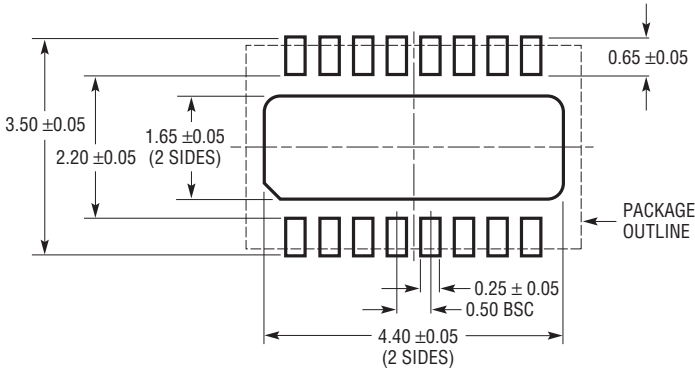
**NOTE:**

1. CONTROLLING DIMENSION: INCHES
  2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
  3. DRAWING NOT TO SCALE
  4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE
- \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
- \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

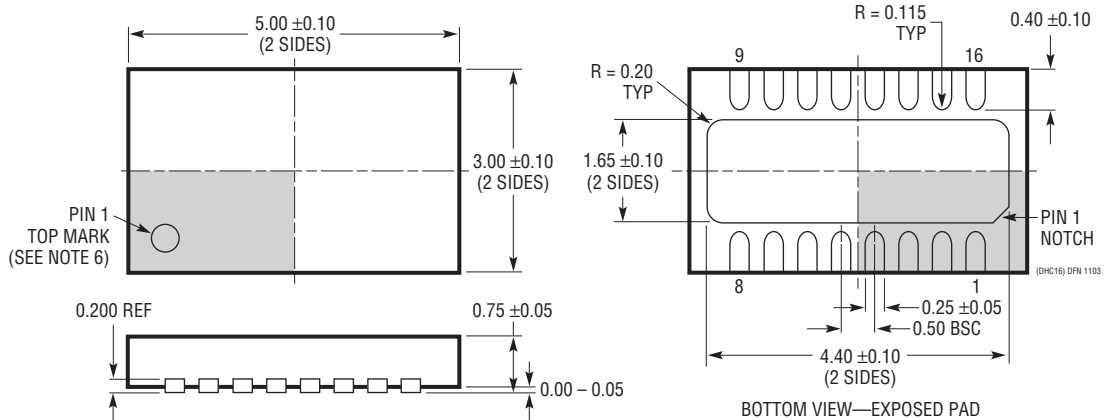
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC6087#packaging> for the most recent package drawings.

**DHC Package**  
**16-Lead Plastic DFN (5mm × 3mm)**  
 (Reference LTC DWG # 05-08-1706 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



- NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

**REVISION HISTORY** (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	7/12	Corrected Supply Current value. Provided $V_{CM}$ condition for GBW specification.	1 4, 5
D	6/17	Provided $V_{CM}$ condition for Phase Margin specification.	4, 5