Precision Zero Drift Current Sense Amplifier

FEATURES

- **Supply Range:**
  4V to 60V, 70V Maximum (LTC6102)
  5V to 100V, 105V Maximum (LTC6102HV)
- **±10µV Input Offset Maximum**
- **±50nV/°C Input Offset Drift Maximum**
- **Fast Response: 1µs Step Response**
- **Gain Configurable with Two Resistors**
- Low Input Bias Current: 3nA Maximum
- PSRR 130dB Minimum
- Output Currents up to 1mA
- Operating Temperature Range: –40°C to 125°C
- Disable Mode (LTC6102-1 Only): 1µA Maximum
- Available in 8-Lead MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- Current Shunt Measurement
- Battery Monitoring
- Remote Sensing
- Load Protection
- Motor Control
- Automotive Controls

DESCRIPTION

The LTC®6102/LTC6102HV are versatile, high voltage, high-side current sense amplifiers. Their high supply voltage rating allows their use in many high side applications, while the low drift and offset ensure accuracy across a wide range of operating conditions. The LTC6102-1 is a version of the LTC6102 that includes a low power disable mode to conserve system standby power.

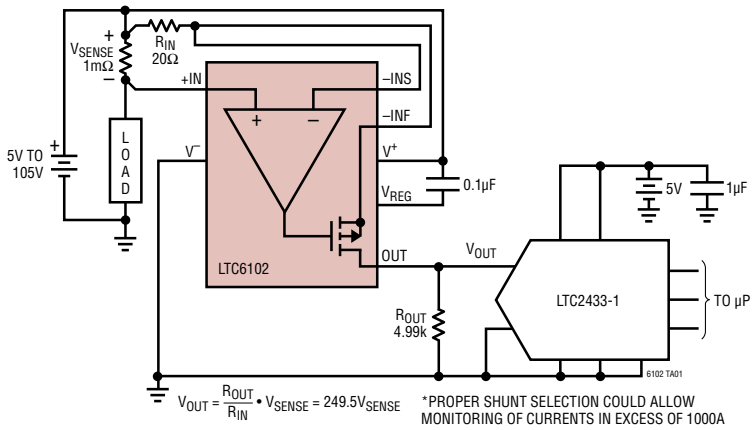
The LTC6102/LTC6102HV monitor current via the voltage across an external sense resistor (shunt resistor). Internal circuitry converts input voltage to output current, allowing a small sense signal on a large common mode voltage to be translated to a ground-referred signal. Low DC offset allows the use of very low shunt resistor values and large gain-setting resistors. As a result, power loss in the shunt is reduced.

The wide operating supply and high accuracy make the LTC6102 ideal for a large array of applications, from automotive, to industrial and power management. A maximum input sense voltage of 2V allows a wide range of currents and voltages to be monitored. Fast response makes the LTC6102 the perfect choice for load current warnings and shutoff protection control.

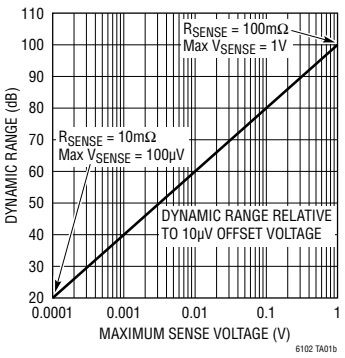
All versions of the LTC6102 are available in 8-lead MSOP and 3mm × 3mm DFN packages.

TYPICAL APPLICATION

10A Current Sense with 10mA Resolution and 100mW Maximum Dissipation



Dynamic Current Measurement Range



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-):
- LTC6102/LTC6102-1 ..... 70V
- LTC6102HV 105V

Input Voltage Range
- –INF, –INS ..... (V^+ – 4V to V^+ + 0.3V)
- +IN ..... (V^+ – 20V to V^+ + 1V)
- EN ..... (V^- – 0.3V to V^- + 9V)
- Differential (–INS – +IN), 1 Second 60V

Output Voltage Range
- LTC6102/LTC6102HV ..... (V^- – 0.3V to V^- + 9V)
- LTC6102-1 ..... (V^- – 0.3V to V^- + 15V)

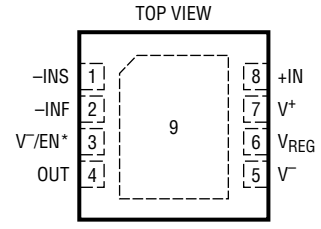
Input Current
- –INF, –INS ..... ±10mA
- +IN ..... –10mA
- EN ..... ±10mA

Output Current ..... (–1mA, +10mA)
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range: (Note 2)
- LTC6102C/LTC6102C-1/LTC6102HVC .. –40°C to 85°C
- LTC6102I/LTC6102I-1/LTC6102HVI ..... –40°C to 85°C
- LTC6102H/LTC6102H-1
- LTC6102HVH ..... –40°C to 125°C

Specified Temperature Range: (Note 2)
- LTC6102C/LTC6102C-1/LTC6102HVC ..... 0°C to 70°C
- LTC6102I/LTC6102I-1/LTC6102HVI ..... –40°C to 85°C
- LTC6102H/LTC6102H-1
- LTC6102HVH ..... –40°C to 125°C

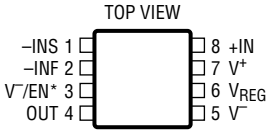
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB
*V^- FOR THE LTC6102/LTC6102HV, EN FOR THE LTC6102-1



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 200°C/W
*V^- FOR THE LTC6102/LTC6102HV, EN FOR THE LTC6102-1

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6102CDD#PBF	LTC6102CDD#TRPBF	LCKH	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6102IDD#PBF	LTC6102IDD#TRPBF	LCKH	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6102HDD#PBF	LTC6102HDD#TRPBF	LCKH	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6102CDD-1#PBF	LTC6102CDD-1#TRPBF	LDYB	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6102IDD-1#PBF	LTC6102IDD-1#TRPBF	LDYB	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6102HDD-1#PBF	LTC6102HDD-1#TRPBF	LDYB	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6102HVCDD#PBF	LTC6102HVCDD#TRPBF	LCVC	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6102HVIDD#PBF	LTC6102HVIDD#TRPBF	LCVC	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6102HVHDD#PBF	LTC6102HVHDD#TRPBF	LCVC	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6102CMS8#PBF	LTC6102CMS8#TRPBF	LTCKJ	8-Lead Plastic MSOP	0°C to 70°C
LTC6102IMS8#PBF	LTC6102IMS8#TRPBF	LTCKJ	8-Lead Plastic MSOP	–40°C to 85°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6102HMS8#PBF	LTC6102HMS8#TRPBF	LTCKJ	8-Lead Plastic MSOP	–40°C to 125°C
LTC6102CMS8-1#PBF	LTC6102CMS8-1#TRPBF	LTDXZ	8-Lead Plastic MSOP	0°C to 70°C
LTC6102IMS8-1#PBF	LTC6102IMS8-1#TRPBF	LTDXZ	8-Lead Plastic MSOP	–40°C to 85°C
LTC6102HMS8-1#PBF	LTC6102HMS8-1#TRPBF	LTDXZ	8-Lead Plastic MSOP	–40°C to 125°C
LTC6102HVCMS8#PBF	LTC6102HVCMS8#TRPBF	LTCVB	8-Lead Plastic MSOP	0°C to 70°C
LTC6102HVIMS8#PBF	LTC6102HVIMS8#TRPBF	LTCVB	8-Lead Plastic MSOP	–40°C to 85°C
LTC6102HVHMS8#PBF	LTC6102HVHMS8#TRPBF	LTCVB	8-Lead Plastic MSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**SPECIFIED TEMPERATURE RANGE**
LTC6102CDD	LTC6102CDD#TR	LCKH	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6102IDD	LTC6102IDD#TR	LCKH	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6102HDD	LTC6102HDD#TR	LCKH	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6102CDD-1	LTC6102CDD-1#TR	LDYB	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6102IDD-1	LTC6102IDD-1#TR	LDYB	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6102HDD-1	LTC6102HDD-1#TR	LDYB	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6102HVCDD	LTC6102HVCDD#TR	LCVC	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6102HVIDD	LTC6102HVIDD#TR	LCVC	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6102HVHDD	LTC6102HVHDD#TR	LCVC	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6102CMS8	LTC6102CMS8#TR	LTCKJ	8-Lead Plastic MSOP	0°C to 70°C
LTC6102IMS8	LTC6102IMS8#TR	LTCKJ	8-Lead Plastic MSOP	–40°C to 85°C
LTC6102HMS8	LTC6102HMS8#TR	LTCKJ	8-Lead Plastic MSOP	–40°C to 125°C
LTC6102CMS8-1	LTC6102CMS8-1#TR	LTDXZ	8-Lead Plastic MSOP	0°C to 70°C
LTC6102IMS8-1	LTC6102IMS8-1#TR	LTDXZ	8-Lead Plastic MSOP	–40°C to 85°C
LTC6102HMS8-1	LTC6102HMS8-1#TR	LTDXZ	8-Lead Plastic MSOP	–40°C to 125°C
LTC6102HVCMS8	LTC6102HVCMS8#TR	LTCVB	8-Lead Plastic MSOP	0°C to 70°C
LTC6102HVIMS8	LTC6102HVIMS8#TR	LTCVB	8-Lead Plastic MSOP	–40°C to 85°C
LTC6102HVHMS8	LTC6102HVHMS8#TR	LTCVB	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

(LTC6102, LTC6102-1) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. R_{IN} = 10Ω, R_{OUT} = 10k, $V_{SENSE}^+ = V^+$ (see Figure 1 for details), V^+ = 12V, V^- = 0V, V_{EN} = 2.2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Supply Voltage Range			4		60	V
V_{OS}	Input Offset Voltage (Note 3)	V_{SENSE} = 100µV 6V ≤ V^+ ≤ 60V V^+ = 4V	 	 	 3 5	 10 25	 µV µV
	Input Offset Voltage (Note 4)	V_{SENSE} = 100µV 6V ≤ V^+ ≤ 60V V^+ = 4V	 	 	 3 5	 35 50	 µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 3)	V_{SENSE} = 100µV LTC6102C, LTC6102I, LTC6102C-1, LTC6102I-1 LTC6102H, LTC6102H-1	 ● ●	 	 25 25	 50 75	 nV/°C nV/°C
I_B	Input Bias Current (Note 5)	R_{IN} = 40k, V_{SENSE} = 2mV LTC6102C, LTC6102I, LTC6102C-1, LTC6102I-1 LTC6102H, LTC6102H-1	 ● ●	 	60 	 3 20	pA nA nA
PSRR	Power Supply Rejection Ratio	V_{SENSE} = 100µV, V^+ = 6V to 60V	 ●	130 125	150 	 	dB dB
		V_{SENSE} = 100µV, V^+ = 4V to 60V	 ●	120 115	140 	 	dB dB
$V_{SENSE(MAX)}$	Input Sense Voltage Full Scale ($V^+ - V_{IN}^+$)	Error <1%, R_{IN} = 10k, R_{OUT} = 10k 6V ≤ V^+ ≤ 60V V^+ = 4V	 ● ●	 2 0.8	 	 	 V V
V_{OUT}	Maximum Output Voltage (LTC6102)	V_{SENSE} = 2mV, R_{OUT} = 100k 12V ≤ V^+ ≤ 60V V^+ = 6V V^+ = 4V	 ● ● ●	 8 3 1	 	 	 V V V
	Maximum Output Voltage (LTC6102-1)	V_{SENSE} = 2mV, R_{OUT} = 100k V^+ = 60V V^+ = 12V V^+ = 4V	 ● ● ●	 14 11.7 3.8	 	 	 V V V
I_{OUT}	Maximum Output Current	6V ≤ V^+ ≤ 60V, R_{IN} = 1k, R_{OUT} = 1k, V_{SENSE} = 1.1V V^+ = 4V, R_{IN} = 10Ω, R_{OUT} = 1k, V_{SENSE} = 11mV	● ●	1 0.5	 	 	mA mA
t_r	Input Step Response (to 2.5V on a 5V Output Step)	ΔV_{SENSE} = 100mV Transient, 6V ≤ V^+ ≤ 60V, R_{IN} = 100Ω, R_{OUT} = 4.99k, I_{OUT} = 100µA			1		µs
		V^+ = 4V			1.5		µs
BW	Signal Bandwidth	I_{OUT} = 200µA, R_{IN} = 100Ω, R_{OUT} = 4.99k I_{OUT} = 1mA, R_{IN} = 100Ω, R_{OUT} = 4.99k			140 200		kHz kHz
e_N	Input Noise Voltage	0.1Hz to 10Hz			2		μV_{P-P}
I_S	Supply Current	V^+ = 4V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k	 ●		275 	400 475	µA µA
		V^+ = 6V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k	 ●		290 	425 500	µA µA
		V^+ = 12V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k	 ●		300 	450 525	µA µA
		V^+ = 60V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k			420	575	µA
		LTC6102C, LTC6102I, LTC6102C-1, LTC6102I-1	●			650	µA
		LTC6102H, LTC6102H-1	●			675	µA
I_{DIS}	Supply Current in Disable Mode (LTC6102-1 Only)	V_{EN} = 0.8V, V^+ = 12V V_{EN} = 0.8V, V^+ = 60V	 ●			1 18	µA µA
V_{ENL}	Enable Input Voltage Low (LTC6102-1 Only)		●			0.8	V

ELECTRICAL CHARACTERISTICS

(LTC6102, LTC6102-1) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. R_{IN} = 10Ω, R_{OUT} = 10k, $V_{SENSE}^+ = V^+$ (see Figure 1 for details), V^+ = 12V, V^- = 0V, V_{EN} = 2.2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{ENH}	Enable Input Voltage High (LTC6102-1 Only)		●	2.2			V
I_{BEN}	Enable Input Pin Current (LTC6102-1 Only)	V_{EN} = 0V to 9V	●			8	µA
t_{ON}	Turn-On Time (LTC6102-1 Only)	V_{EN} = 2.2V, V_{SENSE} = 1mV, Output Settles to Within 1% of Final Value			500		µs
t_{OFF}	Turn-Off Time (LTC6102-1 Only)	V_{EN} = 0.8V, V_{SENSE} = 1mV, Supply Current Drops to Less Than 10% of Nominal Value			100		µs
f_S	Sampling Frequency				10		kHz

ELECTRICAL CHARACTERISTICS

(LTC6102HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. R_{IN} = 10Ω, R_{OUT} = 10k, $V_{SENSE}^+ = V^+$ (see Figure 1 for details), V^+ = 12V, V^- = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Supply Voltage Range			5		100	V
V_{OS}	Input Offset Voltage (Note 3)	V_{SENSE} = 100µV 6V ≤ V^+ ≤ 100V V^+ = 5V			 3 5	 10 25	 µV µV
	Input Offset Voltage (Note 4)	V_{SENSE} = 100µV 6V ≤ V^+ ≤ 100V V^+ = 5V			 3 5	 35 50	 µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 3)	V_{SENSE} = 100µV LTC6102HVC, LTC6102HVI LTC6102HVH	 ● ●		 25 25	 50 75	 nV/°C nV/°C
I_B	Input Bias Current (Note 5)	R_{IN} = 40k, V_{SENSE} = 2mV LTC6102HVC, LTC6102HVI LTC6102HVH	 ● ●		60	 3 20	pA nA nA
PSRR	Power Supply Rejection Ratio	V_{SENSE} = 100µV, V^+ = 6V to 100V	 ●	130 125	150		dB dB
		V_{SENSE} = 100µV, V^+ = 5V to 100V	 ●	120 115	 140		dB dB
$V_{SENSE(MAX)}$	Input Sense Voltage Full Scale ($V^+ - V_{+IN}$)	Error <1%, R_{IN} = 10k, R_{OUT} = 10k 6V ≤ V^+ ≤ 100V V^+ = 5V	 ● ●	 2 1			 V V
V_{OUT}	Maximum Output Voltage	V_{SENSE} = 2mV, R_{OUT} = 100k 12V ≤ V^+ ≤ 100V V^+ = 5V	 ● ●	 8 3			 V V
I_{OUT}	Maximum Output Current	6V ≤ V^+ ≤ 100V, R_{IN} = 1k, R_{OUT} = 1k, V_{SENSE} = 1.1V V^+ = 5V, R_{IN} = 10Ω, R_{OUT} = 1k, V_{SENSE} = 11mV	● ●	1 0.5			mA mA
t_r	Input Step Response (to 2.5V on a 5V Output Step)	ΔV_{SENSE} = 100mV Transient, 6V ≤ V^+ ≤ 100V, R_{IN} = 100Ω, R_{OUT} = 4.99k, I_{OUT} = 100µA			1		µs
		V^+ = 5V			1.5		µs
BW	Signal Bandwidth	I_{OUT} = 200µA, R_{IN} = 100Ω, R_{OUT} = 4.99k I_{OUT} = 1mA, R_{IN} = 100Ω, R_{OUT} = 4.99k			140 200		kHz kHz
e_N	Input Noise Voltage	0.1Hz to 10Hz			2		μV_{P-P}

ELECTRICAL CHARACTERISTICS

(LTC6102HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. R_{IN} = 10Ω, R_{OUT} = 10k, $V_{SENSE}^+ = V^+$ (see Figure 1 for details), V^+ = 12V, V^- = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current	V^+ = 5V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k	 ●		275	400 475	µA µA
		V^+ = 6V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k	 ●		280	425 500	µA µA
		V^+ = 12V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k	 ●		290	450 525	µA µA
		V^+ = 100V, I_{OUT} = 0, R_{IN} = 10k, R_{OUT} = 100k			420	575	µA
		LTC6102HVC, LTC6102HVI	●			650	µA
		LTC6102HVH	●			675	µA
f_S	Sampling Frequency				10		kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. In addition to the Absolute Maximum Ratings, the output current of the LTC6102 must be limited to ensure that the power dissipation in the LTC6102 does not allow the die temperature to exceed 150°C. See the Applications Information "Output Current Limitations Due to Power Dissipation" for further information.

Note 2: The LTC6102C/LTC6102C-1/LTC6102HVC are guaranteed to meet specified performance from 0°C to 70°C. The LTC6102C/LTC6102C-1/LTC6102HVC are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. LTC6102I/LTC6102I-1/LTC6102HVI are guaranteed to meet specified performance from –40°C to 85°C. The LTC6102H/LTC6102H-1/LTC6102HVH are guaranteed to meet specified performance from –40°C to 125°C.

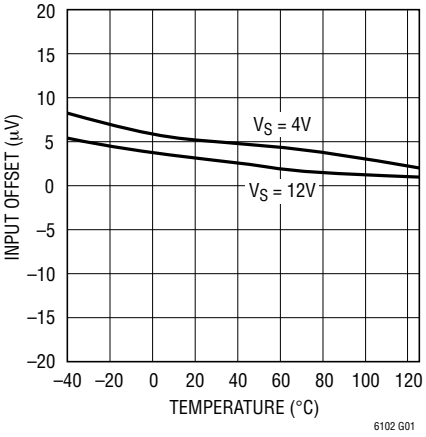
Note 3: These Parameters are guaranteed by design and are not 100% tested. Thermocouple effects preclude measurements of these voltage levels during automated testing.

Note 4: Limits are fully tested. Limit is determined by high speed automated test capability.

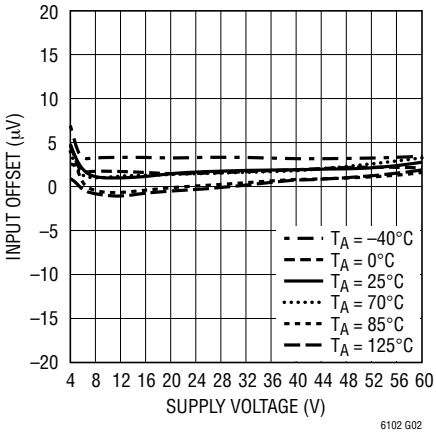
Note 5: I_B specification is limited by practical automated test resolution. Please refer to the Typical Performance Characteristics section for more information regarding actual typical performance. For tighter specifications, please contact LTC Marketing.

TYPICAL PERFORMANCE CHARACTERISTICS

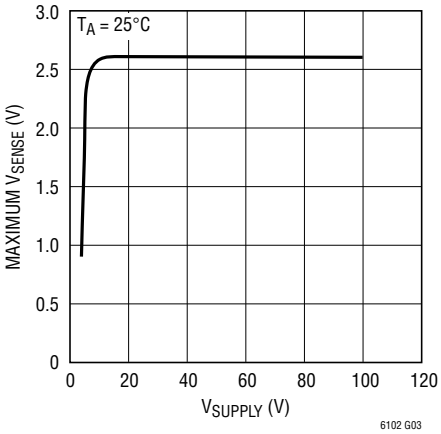
Input V_{OS} vs Temperature



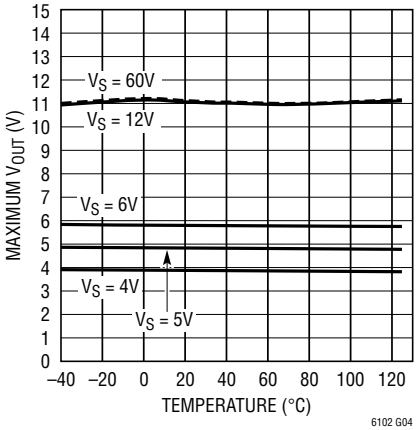
Input V_{OS} vs Supply Voltage



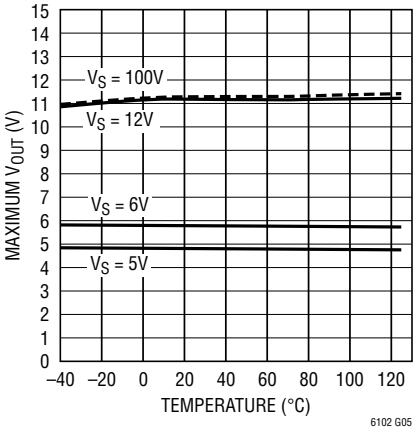
Input Sense Range



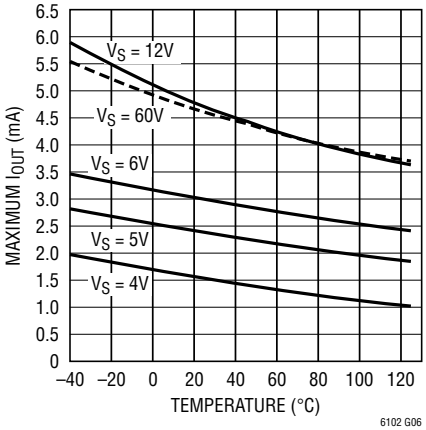
LTC6102: V_{OUT} Maximum vs Temperature



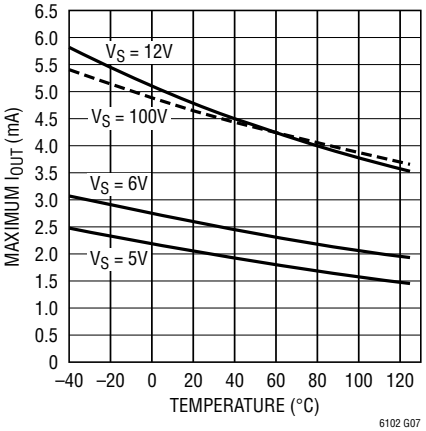
LTC6102HV: V_{OUT} Maximum vs Temperature



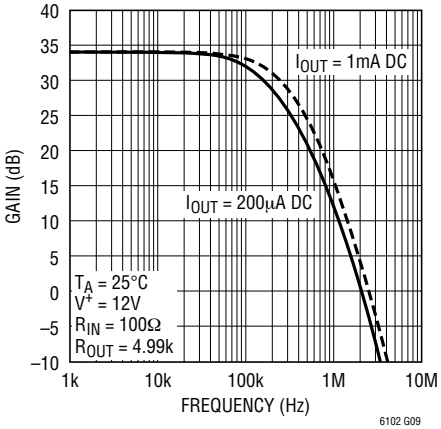
LTC6102/LTC6102-1: I_{OUT} Maximum vs Temperature



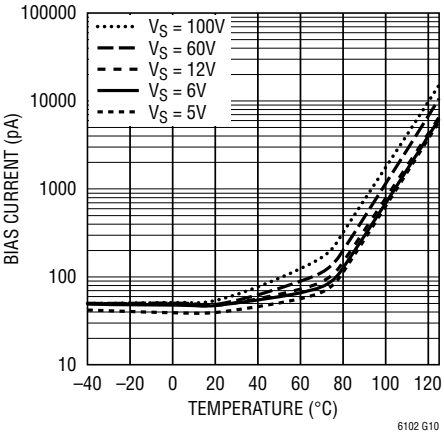
LTC6102HV: I_{OUT} Maximum vs Temperature



Gain vs Frequency

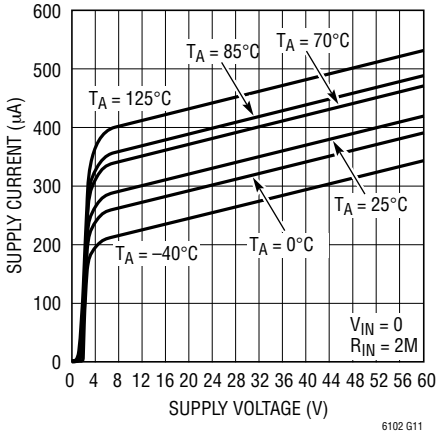


Input Bias Current vs Temperature

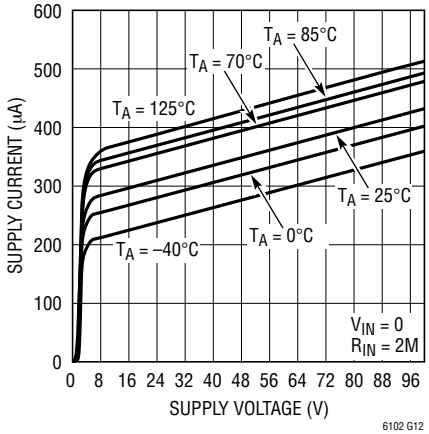


TYPICAL PERFORMANCE CHARACTERISTICS

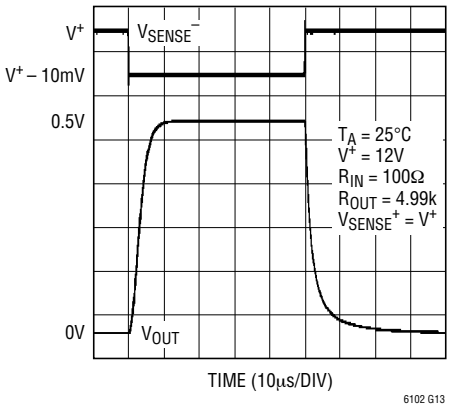
LTC6102: Supply Current vs Supply Voltage



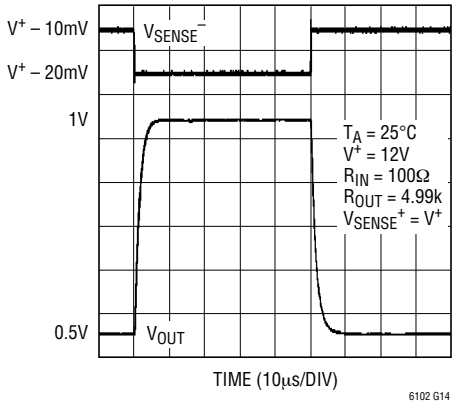
LTC6102HV: Supply Current vs Supply Voltage



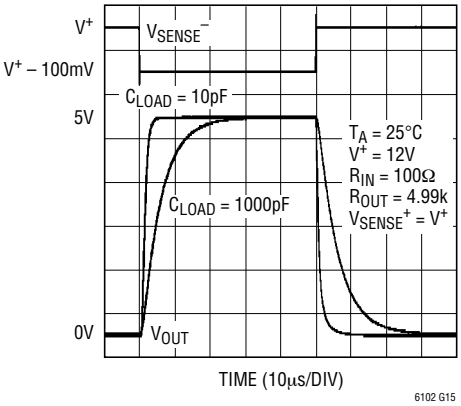
Step Response 0mV to 10mV



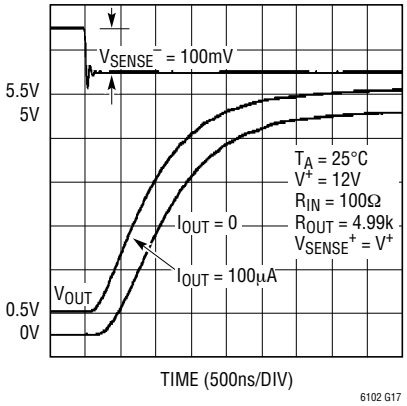
Step Response 10mV to 20mV



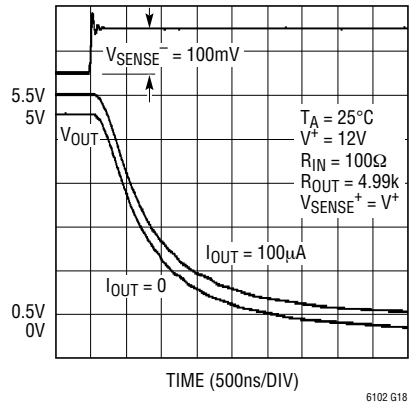
Step Response 100mV



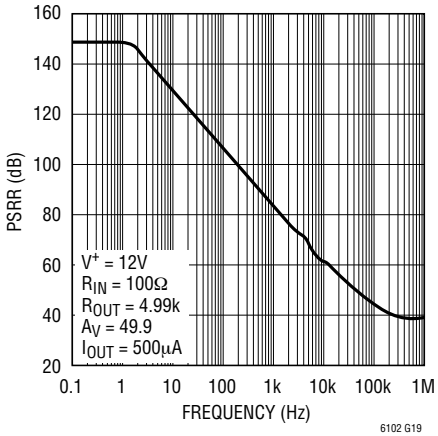
Step Response Rising Edge



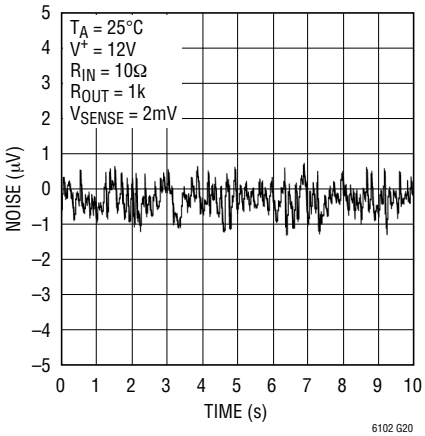
Step Response Falling Edge



PSRR vs Frequency

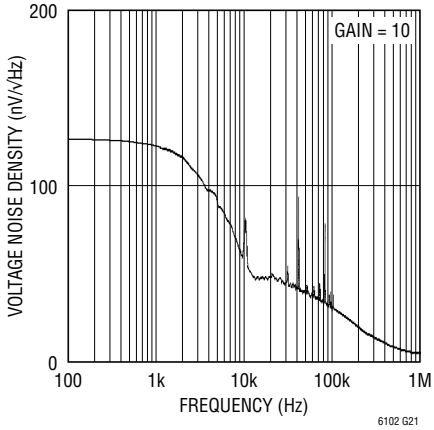


Input Referred Noise 0.1Hz to 10Hz

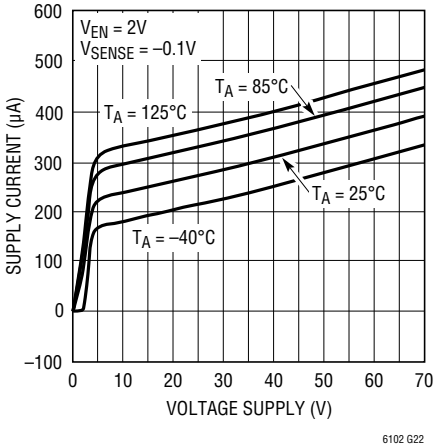


TYPICAL PERFORMANCE CHARACTERISTICS

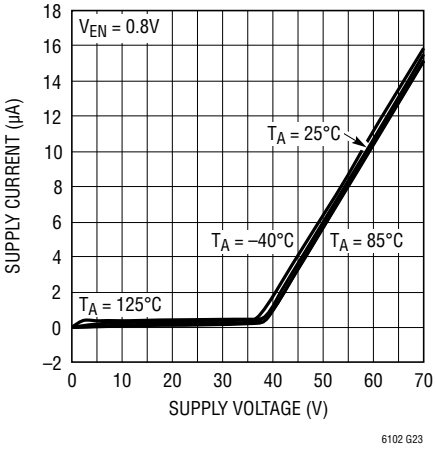
Noise Spectral Density



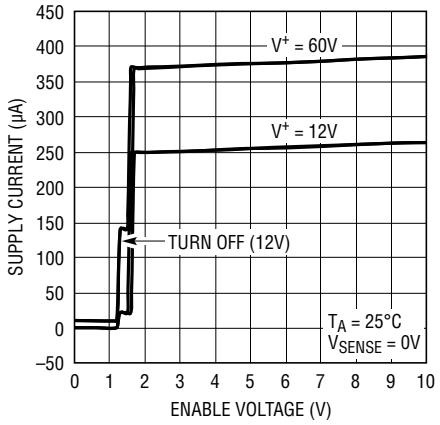
LTC6102-1: Supply Current vs Supply Voltage



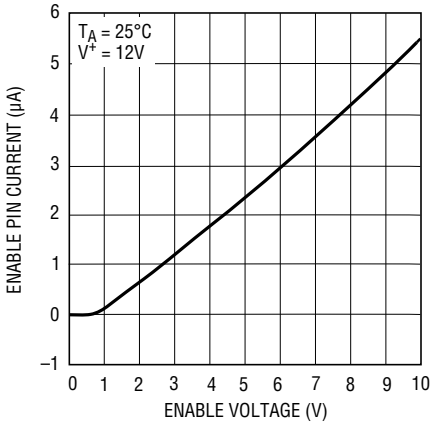
LTC6102-1: Supply Current vs Supply Voltage when Disabled



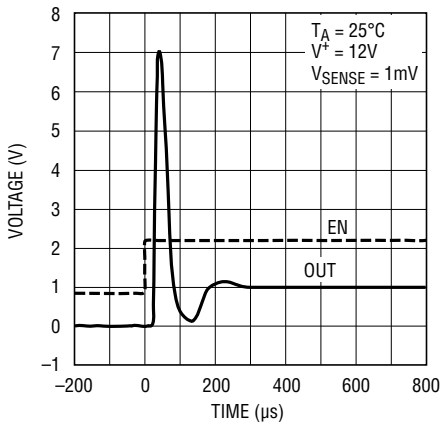
LTC6102-1: Supply Current vs Enable Voltage



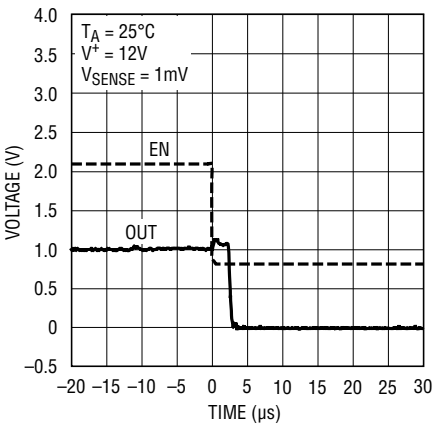
LTC6102-1: Enable Pin Current vs Enable Voltage



LTC6102-1: Turn-On Time



LTC6102-1: Turn-Off Time



PIN FUNCTIONS

–INS (Pin 1): Amplifier Inverting Input. When tied to –INF, the internal sense amplifier will drive –INS to the same potential as +IN.

–INF (Pin 2): Force Input. This pin carries the input current from R_{IN} and must be tied to –INS near R_{IN}. A resistor (R_{IN}) tied from V^+ to –INF sets the output current $I_{OUT} = V_{SENSE}/R_{IN}$. V_{SENSE} is the voltage across the external R_{SENSE}.

V^- (Pin 3, LTC6102/LTC6102HV Only): Negative Supply.

EN (Pin 3, LTC6102-1 Only): Enable Pin, Referenced to the Negative Supply. When the enable pin is pulled high, the LTC6102-1 is active. When the enable pin is pulled low or left floating, the LTC6102-1 is disabled.

OUT (Pin 4): Open-Drain Current output. OUT will source a current that is proportional to the sense voltage into an external resistor. I_{OUT} is the same current that enters –INF.

V^- (Pin 5): Negative Supply.

V_{REG} (Pin 6): Internal Regulated Supply. A 0.1µF (or larger) capacitor should be tied from V_{REG} to V^+. V_{REG} is not designed to drive external circuits.

V^+ (Pin 7): Positive Supply. Supply current is drawn through this pin.

+IN (Pin 8): Amplifier Noninverting Input. Must be tied to the system load end of the sense resistor. The +IN pin has an internal 5k series resistor designed to allow large input voltage transients or accidental disconnection of the sense resistor. This pin can be held up to 20V below the –INS pin indefinitely, or up to 60V below the –INS pin for up to one second (see Absolute Maximum Ratings).

Exposed Pad (Pin 9, DFN Only): V^-. The Exposed Pad must be soldered to PCB.

BLOCK DIAGRAM

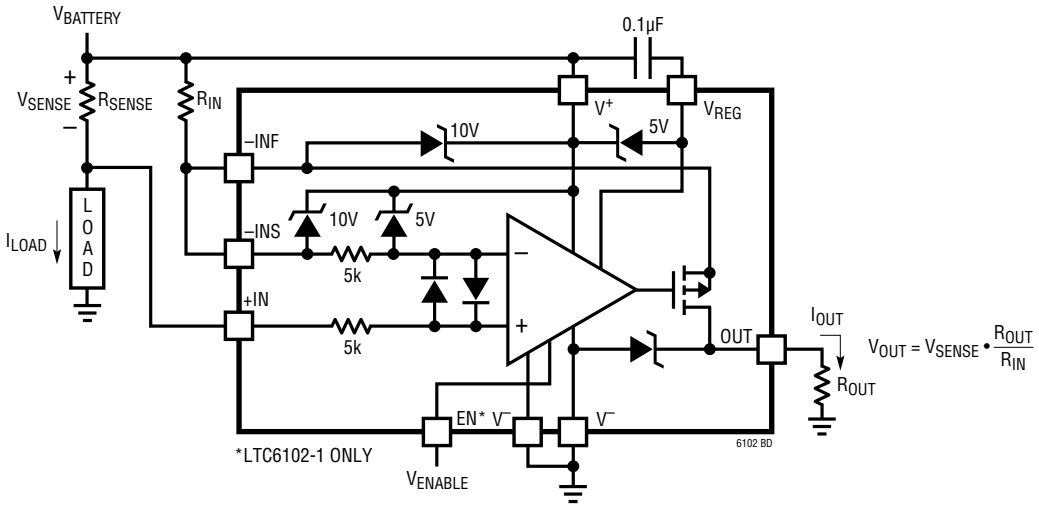


Figure 1. Block Diagram and Typical Connection

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The LTC6102 high side current sense amplifier (Figure 1) provides accurate monitoring of current through a user-selected sense resistor. The sense voltage is amplified by a user-selected gain and level shifted from the positive power supply to a ground-referred output. The output signal is analog and may be used as is or processed with an output filter.

Theory of Operation

An internal sense amplifier loop forces –INS to have the same potential as +IN. Connecting an external resistor, R_{IN}, between –INS and V^+ forces a potential across R_{IN} that is the same as the sense voltage across R_{SENSE}. A corresponding current, V_{SENSE}/R_{IN}, will flow through R_{IN}. The high impedance inputs of the sense amplifier will not conduct this input current, so it will flow through the –INF pin and an internal MOSFET to the output pin.

The output current can be transformed into a voltage by adding a resistor from OUT to V^-. The output voltage is then $V_O = V^- + I_{OUT} \bullet R_{OUT}$.

Useful Gain Configurations

GAIN	R_{IN}	R_{OUT}	V_{SENSE} AT V_{OUT} = 5V
200	49.9Ω	10k	25mV
500	20Ω	10k	10mV
1000	10Ω	10k	5mV
4990	1Ω	4.99k	1mV

Selection of External Current Sense Resistor

The external sense resistor, R_{SENSE}, has a significant effect on the function of a current sensing system and must be chosen with care.

First, the power dissipation in the resistor should be considered. The system load current will cause both heat dissipation and voltage loss in R_{SENSE}. As a result, the sense resistor should be as small as possible while still providing the input dynamic range required by the measurement. Note that input dynamic range is the difference between the maximum input signal and the minimum accurately reproduced signal, and is limited primarily by input DC offset of the internal amplifier of the LTC6102. In addition, R_{SENSE} must be small enough that V_{SENSE} does not exceed the maximum sense voltage specified by the LTC6102 or the sense resistor, even under peak load conditions. As an example, an application may require that the maximum sense voltage be 100mV. If this application is expected to draw 20A at peak load, R_{SENSE} should be no more than 5mΩ.

Once the maximum R_{SENSE} value is determined, the minimum sense resistor value will be set by the resolution or dynamic range required. The minimum signal that can be accurately represented by this sense amp is limited by the input offset. As an example, the LTC6102 has a typical input offset of 3µV. If the minimum current is 1mA, a sense resistor of 3mΩ will set V_{SENSE} to 3µV. This is the same value as the input offset. A larger sense resistor will reduce the error due to offset by increasing the sense voltage for a given load current.

For this example, choosing a 5mΩ R_{SENSE} will maximize the dynamic range and provide a system that has 100mV across the sense resistor at peak load (20A), while input offset causes an error equivalent to only 0.6mA of load current.

Peak dissipation is 2W. If a 0.5mΩ sense resistor is employed, then the effective current error is 6mA (0.03% of full-scale), while the peak sense voltage is reduced to 10mV at 20A, dissipating only 200mW.

The low offset and corresponding large dynamic range of the LTC6102 make it more flexible than other solutions in this respect. The 3µV typical offset gives 100dB of dynamic range for a sense voltage that is limited to 300mV max, and over 116dB of dynamic range if a maximum of 2V is allowed.

The previous example assumes that a large output dynamic range is required. For circuits that do not require large dynamic range, the wide input range of the LTC6102 may be used to reduce the size of the sense resistor, reducing power loss and increasing reliability. For example, in a 100A circuit requiring 60dB of dynamic range, the input offset and drift of most current-sense solutions will require that the shunt be chosen so that the sense voltage is at least 100mV at full scale so that the minimum input is greater than 100µV. This will cause power dissipation in excess of 10W at full scale! That much power loss can put

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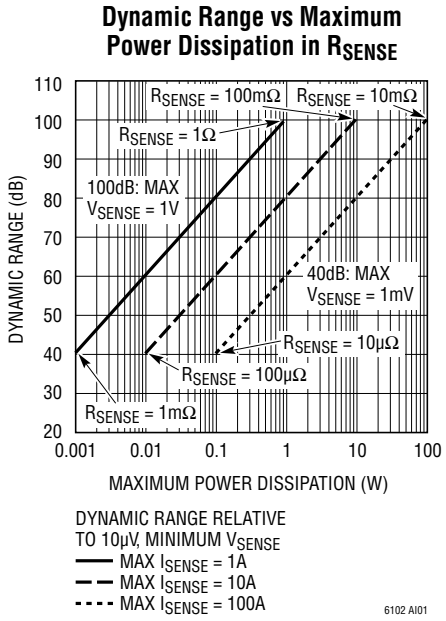
a significant load on the power supply and create thermal design headaches. In addition, heating in the sense resistor can reduce its accuracy and reliability.

In contrast, the large dynamic range of the LTC6102 allows the use of a much smaller sense resistor. The LTC6102 allows the minimum sense voltage to be reduced to less than 10µV. The peak sense voltage would then be 10mV, dissipating only 1W at 100A in a 100µΩ sense resistor! With a specialized sense resistor, the same system would allow peak currents of more than 1000A without exceeding the input range of the LTC6102 or damaging the shunt.



Sense Resistor Connection

Kelvin connection of +IN and –INS to the sense resistor should be used in all but the lowest power applications. Solder connections and PC board interconnections that carry high current can cause significant error in measurement due to their relatively large resistances. One 10mm × 10mm square trace of one-ounce copper is approximately 0.5mΩ. A 1mV error can be caused by as little as 2A flowing through this small interconnect. This will cause a 1% error in a 100mV signal. A 10A load current in the same interconnect will cause a 5% error for the same 100mV signal. An additional error is caused by the change in copper resistance over temperature, which is in excess of 0.4%/°C. By isolating the sense traces from the high-current paths, this error can be reduced by orders of magnitude. A sense resistor with integrated Kelvin sense terminals will give the best results. Figure 2 illustrates the recommended method. Note that the LTC6102 has a Kelvin input structure such that current flows into –INF. The –INS and –INF pins should be tied as close as possible to R_{IN}. This reduces the parasitic series resistance so that R_{IN} may be as low as 1Ω, allowing high gain settings to be used with very little gain error.

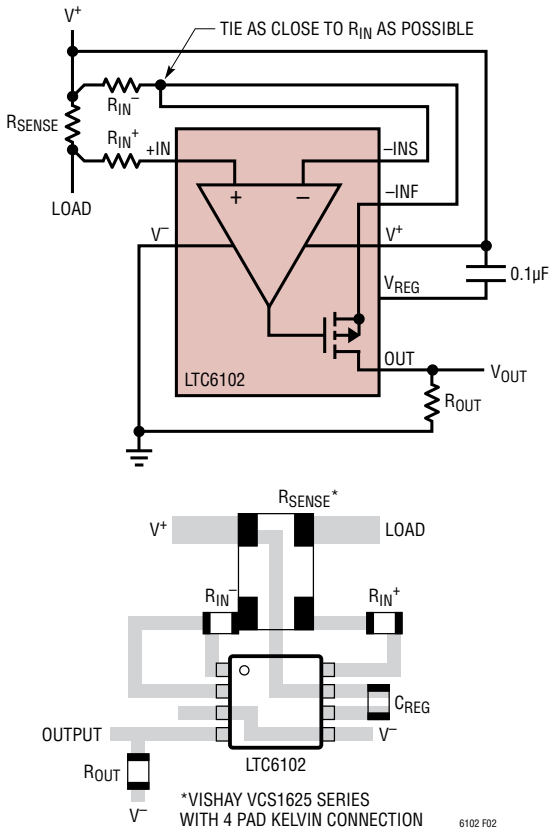


Figure 2. Kelvin Input Connection Preserves Accuracy with Large Load Current and Large Output Current

Selection of External Input Resistor, R_{IN}

The external input resistor, R_{IN}, controls the transconductance of the current sense circuit, $I_{OUT} = V_{SENSE}/R_{IN}$. For example, if R_{IN} = 100, then $I_{OUT} = V_{SENSE}/100$ or I_{OUT} = 1mA for V_{SENSE} = 100mV.

R_{IN} should be chosen to provide the required resolution while limiting the output current. At low supply voltage, I_{OUT} may be as much as 1mA. By setting R_{IN} such that

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the largest expected sense voltage gives I_{OUT} = 1mA, then the maximum output dynamic range is available. Output dynamic range is limited by both the maximum allowed output current (Note 1) and the maximum allowed output voltage, as well as the minimum practical output signal. If less dynamic range is required, then R_{IN} can be increased accordingly, reducing the output current and power dissipation. If small sense currents must be resolved accurately in a system that has very wide dynamic range, a smaller R_{IN} may be used if the max current is limited in another way, such as with a Schottky diode across R_{SENSE} (Figure 3). This will reduce the high current measurement accuracy by limiting the result, while increasing the low current measurement resolution. This approach can be helpful in cases where occasional large burst currents may be ignored.

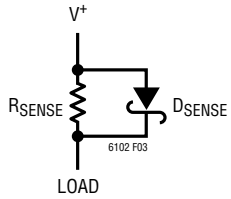

Figure 3. Shunt Diode Limits Maximum Input Voltage to Allow Better Low Input Resolution Without Overranging

Care should be taken when designing the PC board layout for R_{IN}, especially for small R_{IN} values. All trace and interconnect impedances will increase the effective R_{IN} value, causing a gain error. It is important to note that the large temperature drift of copper resistance will cause a change in gain over temperature if proper care is not taken to reduce this effect.

To further limit the effect of trace resistance on gain, maximizing the accuracy of these circuits, the LTC6102 has been designed with a Kelvin input. The inverting terminal (–INS) is separate from the feedback path (–INF). During operation, these two pins must be connected together. The design of the LTC6102 is such that current into –INS is input bias current only, which is typically 60pA at 25°C. Almost all of the current from R_{IN} flows into –INF, through the LTC6102, and into R_{OUT} via the OUT pin. In order to minimize gain error, –INS should be routed in a separate path from –INF to a point as close to R_{IN} as possible. In addition, the higher potential terminal of R_{IN} should be connected directly to the positive terminal of R_{SENSE} (or any input voltage source). For the highest accuracy, R_{IN} should be a four-terminal resistor if it is less than 10Ω.

Selection of External Output Resistor, R_{OUT}

The output resistor, R_{OUT}, determines how the output current is converted to voltage. V_{OUT} is simply $I_{OUT} \bullet R_{OUT}$.

In choosing an output resistor, the max output voltage must first be considered. If the circuit that is driven by the output does not have a limited input voltage, then R_{OUT} must be chosen such that the max output voltage does not exceed the LTC6102 max output voltage rating. If the following circuit is a buffer or ADC with limited input range, then R_{OUT} must be chosen so that $I_{OUT(MAX)} \bullet R_{OUT}$ is less than the allowed maximum input range of this circuit.

In addition, the output impedance is determined by R_{OUT}. If the circuit to be driven has high enough input impedance, then almost any output impedance will be acceptable. However, if the driven circuit has relatively low input impedance, or draws spikes of current, such as an ADC might do, then a lower R_{OUT} value may be required in order to preserve the accuracy of the output. As an example, if the input impedance of the driven circuit is 100 times R_{OUT}, then the accuracy of V_{OUT} will be reduced by 1% since:

$$V_{OUT} = I_{OUT} \bullet \frac{R_{OUT} \bullet R_{IN(DRIVEN)}}{R_{OUT} + R_{IN(DRIVEN)}}$$

$$= I_{OUT} \bullet R_{OUT} \bullet \frac{100}{101} = 0.99 \bullet I_{OUT} \bullet R_{OUT}$$

Error Sources

The current sense system uses an amplifier and resistors to apply gain and level shift the result. The output is then dependent on the characteristics of the amplifier, such as gain and input offset, as well as resistor matching.

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Ideally, the circuit output is:

$$V_{OUT} = V_{SENSE} \bullet \frac{R_{OUT}}{R_{IN}}; V_{SENSE} = R_{SENSE} \bullet I_{SENSE}$$

In this case, the only error is due to resistor mismatch, which provides an error in gain only.

Output Error, E_{OUT}, Due to the Amplifier DC Offset Voltage, V_{OS}

$$E_{OUT(VOS)} = V_{OS} \bullet (R_{OUT}/R_{IN})$$

The DC offset voltage of the amplifier adds directly to the value of the sense voltage, V_{SENSE}. This error is very small (3µV typ) and may be ignored for reasonable values of R_{IN}. See Figure 4. For very high dynamic range, this offset can be calibrated in the system due to its extremely low drift.

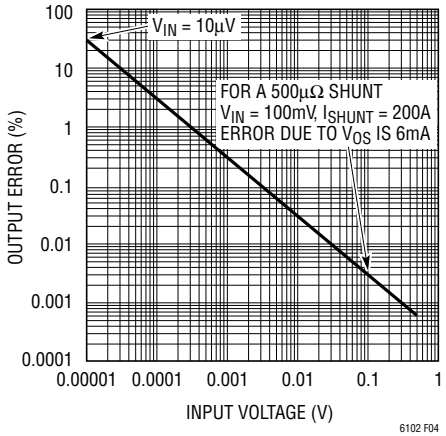

Figure 4. LTC6102 Output Error Due to Typical Input Offset vs Input Voltage

Output Error, E_{OUT}, Due to the Bias Currents, $I_B(+)$ and $I_B(-)$

The input bias current of the LTC6102 is vanishingly small. However, for very high resolution, or at high temperatures where I_B increases due to leakage, the current may be significant.

The bias current $I_B(+)$ flows into the positive input of the internal op amp. $I_B(-)$ flows into the negative input.

$$E_{OUT(IBIAS)} = R_{OUT}((I_B(+) \bullet (R_{SENSE}/R_{IN}) - I_B(-))$$

Since $I_B(+) \approx I_B(-) = I_{BIAS}$, if $R_{SENSE} << R_{IN}$ then,

$$E_{OUT(IBIAS)} \approx -R_{OUT} \bullet I_{BIAS}$$

For instance if I_{BIAS} is 1nA and R_{OUT} is 10k, the output error is –10µV.

Note that in applications where $R_{SENSE} \approx R_{IN}$, $I_B(+)$ causes a voltage offset in R_{SENSE} that cancels the error due to $I_B(-)$ and $E_{OUT(IBIAS)} \approx 0$. In applications where $R_{SENSE} < R_{IN}$, the bias current error can be similarly reduced if an external resistor $R_{IN}(+) = (R_{IN} - R_{SENSE})$ is connected as shown in Figure 5. Under both conditions:

$$E_{OUT(IBIAS)} = \pm R_{OUT} \bullet I_{OS}; I_{OS} = I_B(+) - I_B(-)$$

Adding R_{IN}^+ as described will maximize the dynamic range of the circuit. For less sensitive designs, R_{IN}^+ is not necessary.

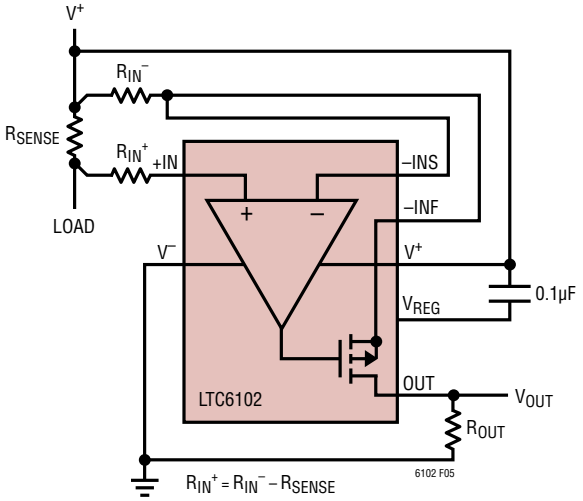

Figure 5. Second Input R Minimizes Error Due to Input Bias Current

Clock Feedthrough, Input Bias Current

The LTC6102 uses auto-zeroing circuitry to achieve an almost zero DC offset over temperature, sense voltage, and power supply voltage. The frequency of the clock used for auto-zeroing is typically 10kHz. The term clock feedthrough is broadly used to indicate visibility of this clock frequency in the op amp output spectrum. There are typically two types of clock feedthrough in auto zeroed amps like the LTC6102.

The first form of clock feedthrough is caused by the settling of the internal sampling capacitor and is input referred; that is, it is multiplied by the internal loop gain

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of the amp. This form of clock feedthrough is independent of the magnitude of the input source resistance or the magnitude of the gain setting resistors. The LTC6102 has a residue clock feedthrough of less then $1\mu V_{RMS}$ input referred at 10kHz.

The second form of clock feedthrough is caused by the small amount of charge injection occurring during the sampling and holding of the amp's input offset voltage. The current spikes are multiplied by the impedance seen at the input terminals of the amp, appearing at the output multiplied by the internal loop gain of the internal op amp. To reduce this form of clock feedthrough, use smaller valued gain setting resistors and minimize the source resistance at the input.

Input bias current is defined as the DC current into the input pins of the op amp. The same current spikes that cause the second form of clock feedthrough described above, when averaged, dominate the DC input bias current of the op amp below 70°C.

As temperature increases, the leakage of the ESD protection diodes on the inputs increases the input bias currents of both inputs in the positive direction, while the current caused by the charge injection stays relatively constant. At temperatures above 70°C, the leakage current dominates and both the negative and positive pins' input bias currents are in the positive direction (into the pins).

Output Current Limitations Due to Power Dissipation

The LTC6102 can deliver more than 1mA continuous current to the output pin. This current flows through R_{IN} and enters the current sense amp via the –INF pin. The power dissipated in the LTC6102 due to the output current is:

$$P_{OUT} = (V_{-INF} - V_{OUT}) \bullet I_{OUT}$$

Since $V_{-INF} \approx V^+$, $P_{OUT} \approx (V^+ - V_{OUT}) \bullet I_{OUT}$

There is also power dissipated due to the quiescent supply current:

$$P_Q = I_S \bullet V^+$$

The total power dissipated is the output current dissipation plus the quiescent dissipation:

$$P_{TOTAL} = P_{OUT} + P_Q$$

At maximum supply and maximum output current, the total power dissipation can exceed 100mW. This will cause significant heating of the LTC6102 die. In order to prevent damage to the LTC6102, the maximum expected dissipation in each application should be calculated. This number can be multiplied by the θ_{JA} value listed in the package section on page 2 to find the maximum expected die temperature. This must not be allowed to exceed 150°C or performance may be degraded.

As an example, if an LTC6102 in the MSOP package is to be biased at 55V ±5V supply with 1mA output current at 80°C:

$$P_{Q(MAX)} = I_{DD(MAX)} \bullet V^+_{(MAX)} = 39mW$$

$$P_{OUT(MAX)} = I_{OUT} \bullet V^+_{(MAX)} = 60mW$$

$$T_{RISE} = \theta_{JA} \bullet P_{TOTAL(MAX)}$$

$$T_{MAX} = T_{AMBIENT} + T_{RISE}$$

T_{MAX} must be < 125°C

$P_{TOTAL(MAX)} \approx 99mW$ and the max die temp will be 100°C

If this same circuit must run at 125°C, the max die temp will increase to 145°C. (Note that supply current, and therefore P_Q, is proportional to temperature. Refer to Typical Performance Characteristics section.) Note that the DD package has a smaller θ_{JA} than the MSOP package, which will substantially reduce the die temperature at similar power levels.

The LTC6102HV can be used at voltages up to 105V. This additional voltage requires that more power be dissipated for a given level of current. This will further limit the allowed output current at high ambient temperatures.

It is important to note that the LTC6102 has been designed to provide at least 1mA to the output when required, and can deliver more depending on the conditions. Care must be taken to limit the maximum output current by proper choice of sense and input resistors and, if input fault conditions are likely, an external clamp.

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Output Filtering

The output voltage, V_{OUT}, is simply $I_{OUT} \bullet Z_{OUT}$. This makes filtering straightforward. Any circuit may be used which generates the required Z_{OUT} to get the desired filter response. For example, a capacitor in parallel with R_{OUT} will give a low pass response. This will reduce unwanted noise from the output, and may also be useful as a charge reservoir to keep the output steady while driving a switching circuit such as a mux or ADC. This output capacitor in parallel with an output resistor will create a pole in the output response at:

$$f_{-3dB} = \frac{1}{2 \bullet \pi \bullet R_{OUT} \bullet C_{OUT}}$$

Useful Equations

Input Voltage: $V_{SENSE} = I_{SENSE} \bullet R_{SENSE}$

Voltage Gain: $\frac{V_{OUT}}{V_{SENSE}} = \frac{R_{OUT}}{R_{IN}}$

Current Gain: $\frac{I_{OUT}}{I_{SENSE}} = \frac{R_{SENSE}}{R_{IN}}$

Transconductance: $\frac{I_{OUT}}{V_{SENSE}} = \frac{1}{R_{IN}}$

Transimpedance: $\frac{V_{OUT}}{I_{SENSE}} = R_{SENSE} \bullet \frac{R_{OUT}}{R_{IN}}$

Input Sense Range

The inputs of the LTC6102 can function from V^+ to (V^+ – 2V). Not only does this allow a wide V_{SENSE} range, it also allows the input reference to be separate from the positive supply (Figure 6). Note that the difference between V_{BAT} and V^+ must be no more than the input sense voltage range listed in the Electrical Characteristics table.

Monitoring Voltages Above V^+ and Level Translation

The LTC6102 may be configured to monitor voltages that are higher than its supply, provided that the negative terminal of the input voltage is within the input sense range of the LTC6102. Figure 7 illustrates a circuit in which the LTC6102 has its supply pin tied to the lower potential terminal of the sense resistor instead of the higher potential terminal. The

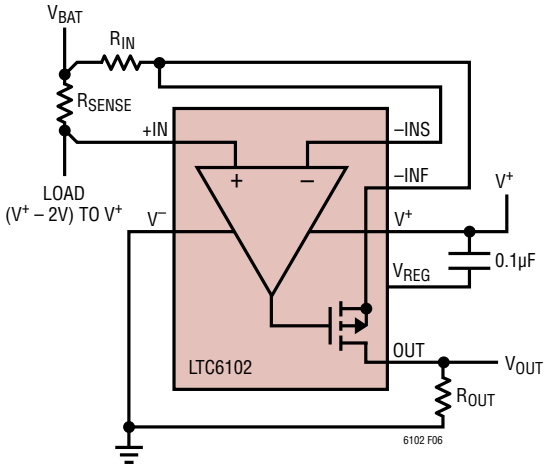


Figure 6. V^+ Powered Separately from Load Supply (V_{BAT})

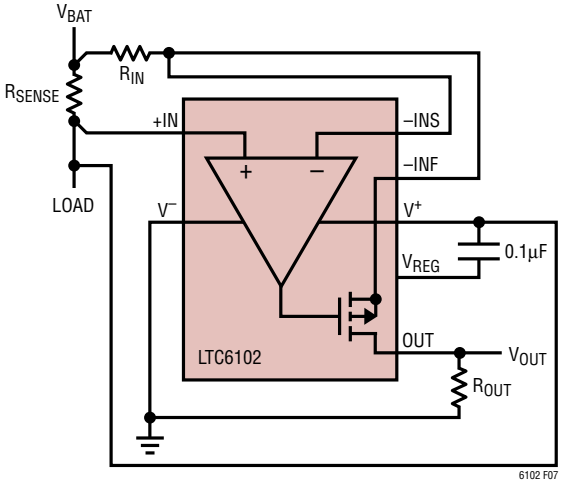


Figure 7. LTC6102 Supply Current Monitored with Load

operation of the LTC6102 is such that the –INS and –INF pins will servo to within a few microvolts of +IN, which is shorted to V^+. Since the input sense range of the LTC6102 includes V^+, the circuit will operate properly. The voltage across R_{SENSE} will be held across R_{IN} by the LTC6102, causing current V_{SENSE}/R_{IN} to flow to R_{OUT}. In this case, the supply current of the LTC6102 is also monitored, as it flows through R_{SENSE}.

Because the voltage across R_{SENSE} is not restricted to the sense range of the LTC6102 in this circuit, V_{SENSE} can be large compared to the allowed sense voltage. This facilitates the sensing of very large voltages, provided that R_{IN} is chosen so that V_{SENSE}/R_{IN} does not exceed

APPLICATIONS INFORMATION

the allowed output current. The gain is still controlled by R_{OUT}/R_{IN}, so either gain or attenuation may be applied to the input signal as it is translated to the output. Finally, the input may be a voltage source rather than a sense resistor, as shown in Figure 8. This circuit allows the translation of a wide variety of input signals across the entire supply range of the LTC6102 with only a tiny offset error while retaining simple gain control set by R_{OUT}/R_{IN}. Again, very large voltages may be sensed as long as R_{IN} is chosen so that I_{OUT} does not exceed the allowed output current. For example, V_{IN} may be as large as 1V with R_{IN} = 1k, or as large as 10V with R_{IN} = 10k. For a 10V maximum input and a 5V maximum output, R_{IN} = 10k and R_{OUT} = 5k will allow the LTC6102HV to translate V_{IN} to V_{OUT} with a common mode voltage of up to 100V. For the case where a large input resistor is used, a similar resistor in series with +IN will reduce error due to input bias current.

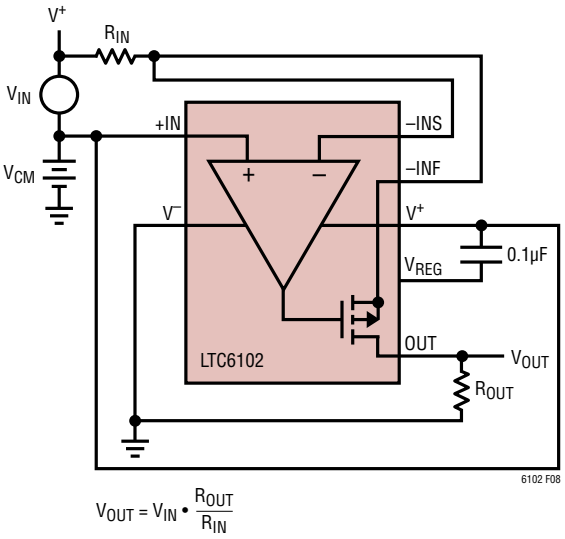


Figure 8. Voltage Level-Shift Circuit

Reverse Supply Current

Some applications may be tested with reverse-polarity supplies due to an expectation of this type of fault during operation. The LTC6102 is not protected internally from external reversal of supply polarity. To prevent damage that may occur during this condition, a Schottky diode should be added in series with V– (Figure 9). This will limit the reverse current through the LTC6102. Note that this diode will limit the low voltage performance of the LTC6102 by effectively reducing the supply voltage to the part by V_D.

In addition, if the output of the LTC6102 is wired to a device that will effectively short it to high voltage (such as through an ESD protection clamp) during a reverse supply condition, the LTC6102's output should be connected through a resistor or Schottky diode (Figure 10).

Response Time

The LTC6102 is designed to exhibit fast response to inputs for the purpose of circuit protection or signal transmission. This response time will be affected by the external circuit in two ways, delay and speed.

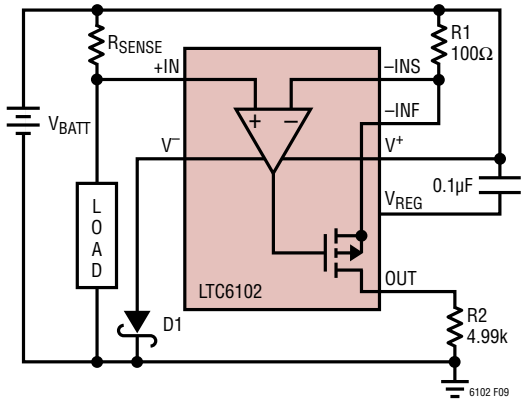


Figure 9. Schottky Prevents Damage During Supply Reversal

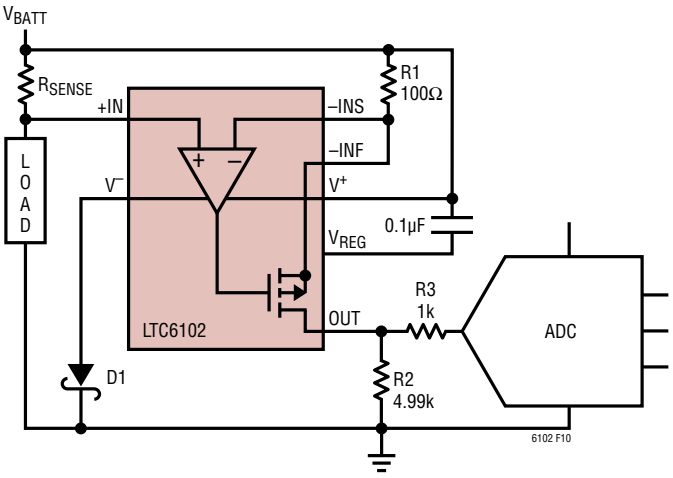


Figure 10. Additional Resistor R3 Protects Output During Supply Reversal

APPLICATIONS INFORMATION

If the output current is very low and an input transient occurs, there may be a delay before the output voltage begins changing. This can be reduced by increasing the minimum output current, either by increasing R_{SENSE} or decreasing R_{IN}. The effect of increased output current is illustrated in the step response curves in the Typical Performance Characteristics section of this datasheet. Note that the curves are labeled with respect to the initial output currents.

The speed is also affected by the external circuit. In this case, if the input changes very quickly, the internal amplifier will slew the gate of the internal output FET (Figure 1) in order to close the internal loop. This results in current flowing through R_{IN} and the internal FET. This current slew rate will be determined by the amplifier and FET characteristics as well as the input resistor, R_{IN}. Using a smaller R_{IN} will allow the output current to increase more quickly, decreasing the response time at the output. This will also have the effect of increasing the maximum output current. Using a larger R_{OUT} will also decrease the response time, since $V_{OUT} = I_{OUT} \bullet R_{OUT}$. Reducing R_{IN} and increasing R_{OUT} will both have the effect of increasing the voltage gain of the circuit.

Bandwidth

For applications that require higher bandwidth from the LTC6102, care must be taken in choosing R_{IN}. For a general-purpose op-amp, the gain-bandwidth product is used to determine the speed at a given gain. Gain is determined by external resistors, and the gain-bandwidth product is an intrinsic property of the amplifier. The same is true for the LTC6102, except that the feedback resistance is determined by an internal FET characteristic. The feedback impedance is approximately $1/g_m$ of the internal MOSFET. The impedance is reduced as current into –INF is increased. At 1mA, the impedance of the MOSFET is on the order of 10kΩ. R_{IN} sets the closed-loop gain of the internal loop as $1/(R_{IN} \bullet g_m)$. The bandwidth is then limited to GBW • $(R_{IN} \bullet g_m)$, with a maximum bandwidth of around 2MHz. This is illustrated in the characteristic curves, where gain vs frequency for two input conditions is shown. The exact impedance of the MOSFET is difficult to determine, as it is a function of input current, process, and capacitance, and has a very different characteristic for low currents vs high currents. However, it is clear that smaller values of R_{IN} and smaller values of I_{OUT} will generally result in lower closed-loop bandwidth. V_{SENSE} and R_{IN} should be chosen to maximize both I_{OUT} and closed-loop gain for highest speed. Theoretically, maximum bandwidth would be achieved for the case where V_{IN} = 10VDC and R_{IN} = 10k, giving I_{OUT} = 1mA and a closed-loop gain near 1. However, this may not be possible in a practical application. Note that the MOSFET g_m is determined by the average or DC value of I_{OUT}, not the peak value. Adding DC current to a small AC input will help increase the bandwidth.

V_{REG} Bypassing

The LTC6102 has an internally regulated supply near V+ for internal bias. It is not intended for use as a supply or bias pin for external circuitry. A 0.1µF capacitor should be connected between the V_{REG} and V^+ pins. This capacitor should be located very near to the LTC6102 for the best performance. In applications which have large supply transients, a 6.8V zener diode may be used in parallel with this bypass capacitor for additional transient suppression.

Enable Pin Operation

The LTC6102-1 includes an enable pin which can place the part into a low power disable state. The enable pin is a logic input pin referenced to $V^–$ and accepts standard TTL logic levels regardless of the V^+ voltage. When the enable pin is driven high, the part is active. When the enable pin is floating or pulled low, then the part is disabled and draws very little supply current. When driven high, the enable pin draws a few microamps of input bias current.

If there is no external logic supply available, the enable pin can be pulled to the V^+ supply through a large value resistor. The voltage at the enable pin will be clamped by the built-in ESD protection structure (which acts like a zener diode). The resistor should be sized so that the current through the resistor is a few milliamps or less to prevent any reduction in long-term reliability. For practical purposes, the current through the resistor should be minimized to save power. The resistor value is limited by the input bias current requirements of the enable

APPLICATIONS INFORMATION

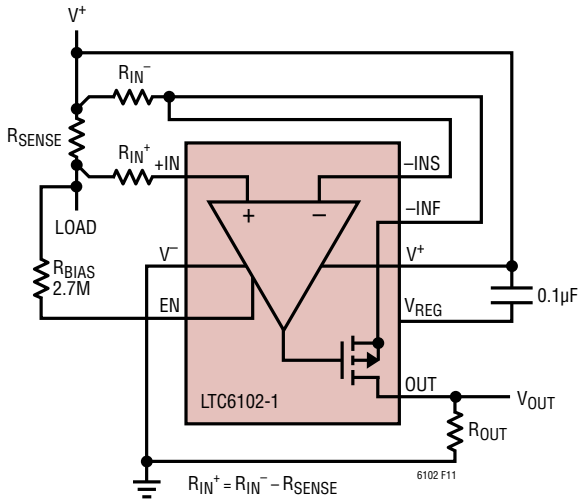


Figure 11

pin. Figure 11 shows the LTC6102-1 with a 2.7M pull-up resistor to limit the current to less than 20µA with a 60V supply, which is enough to satisfy the input bias current requirement.

Start-Up Current

The start-up current of the LTC6102 when the part is powered on or enabled (LTC6102-1) consists of three parts: the first is the current necessary to charge the V_{REG} bypass capacitor, which is nominally 0.1µF. Since the V_{REG} voltage charges to approximately 4.5V below the V^+ voltage, this can require a significant amount of start-up current. The second source is the active supply current of the LTC6102 amplifier, which is not significantly greater during start-up than during normal operation. The third source is the output current of the LTC6102, which upon start-up may temporarily drive the output high. This could cause milliamps of output current (limited mostly by the input resistor R_{IN}) to flow into the output resistor and/or the output limiting ESD structure in the LTC6102. This is a temporary condition which will cease when the LTC6102 amplifier settles into normal closed-loop operation.

When the LTC6102-1 is disabled, the internal amplifier is also shut down, which means that the discharge rate of the 0.1µF capacitor is very low. This is significant when the LTC6102-1 is disabled to save power, because the recharging of the 0.1µF capacitor is a significant portion of the overall power consumed in startup. Figure 12 shows the discharge rate of the 0.1µF capacitor after the LTC6102-1 is shut down at room temperature.

In a system where the LTC6102-1 is disabled for short periods, the start-up power (and therefore the average power) can be reduced since the V_{REG} bypass capacitor is never significantly discharged. The time required to charge the V_{REG} capacitor will also be reduced, allowing the LTC6102-1 to start-up more quickly.

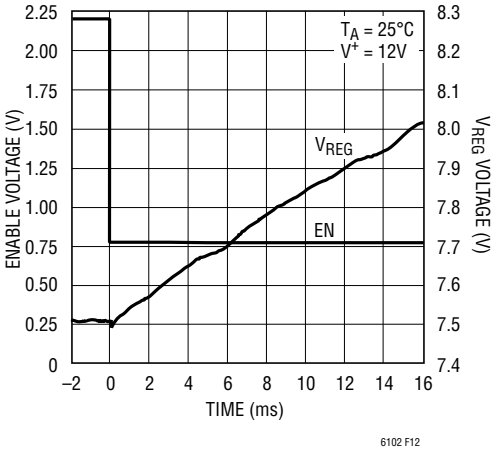
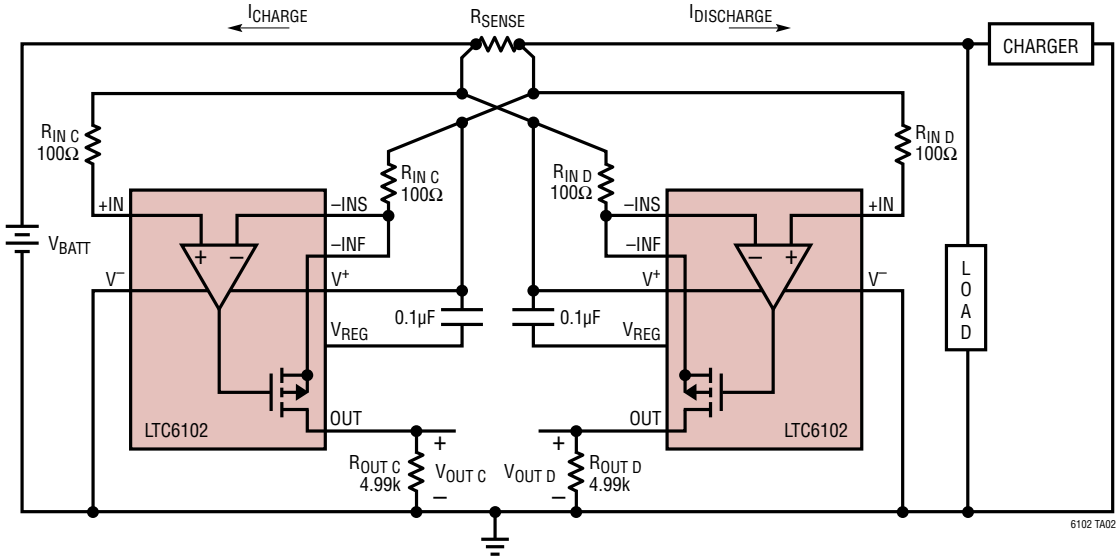


Figure 12. LTC6102-1 V_{REG} Voltage During Bypass Capacitor Discharge when Disabled

TYPICAL APPLICATIONS

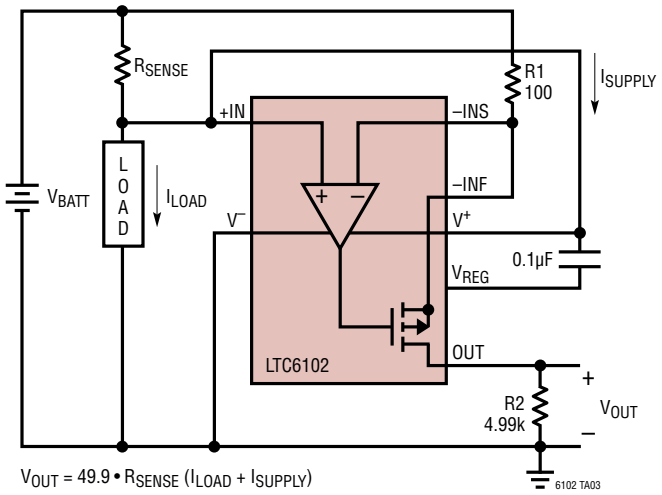
Bidirectional Current Sense Circuit with Separate Charge/Discharge Output



DISCHARGING: $V_{OUT\ D} = I_{DISCHARGE} \bullet R_{SENSE} \left(\frac{R_{OUT\ D}}{R_{IN\ D}}\right)$ WHEN $I_{DISCHARGE} \geq 0$

CHARGING: $V_{OUT\ C} = I_{CHARGE} \bullet R_{SENSE} \left(\frac{R_{OUT\ C}}{R_{IN\ C}}\right)$ WHEN $I_{CHARGE} \geq 0$

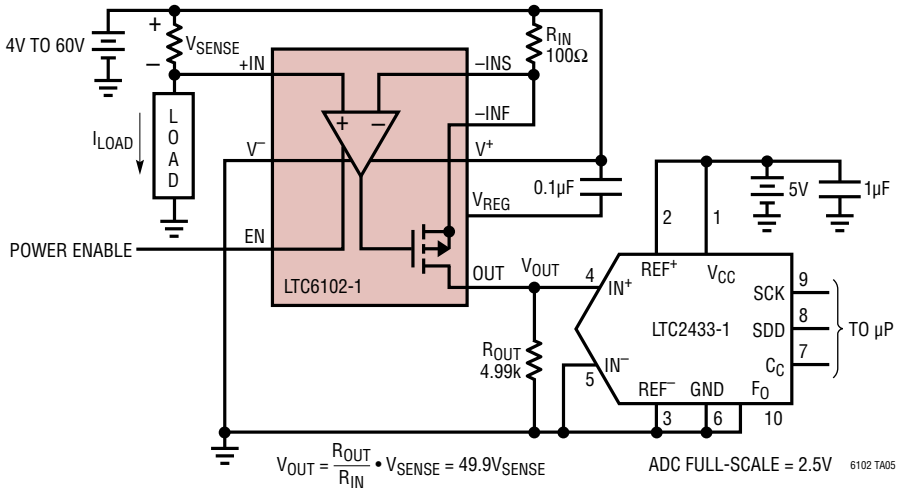
LTC6102 Monitors Its Own Supply Current



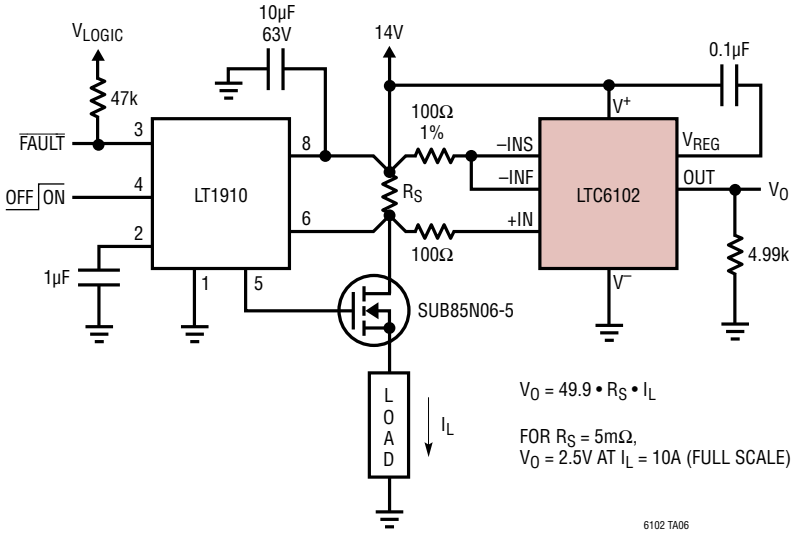
$V_{OUT} = 49.9 \bullet R_{SENSE} (I_{LOAD} + I_{SUPPLY})$

TYPICAL APPLICATIONS

16-Bit Resolution Unidirectional Output into LTC2433 ADC

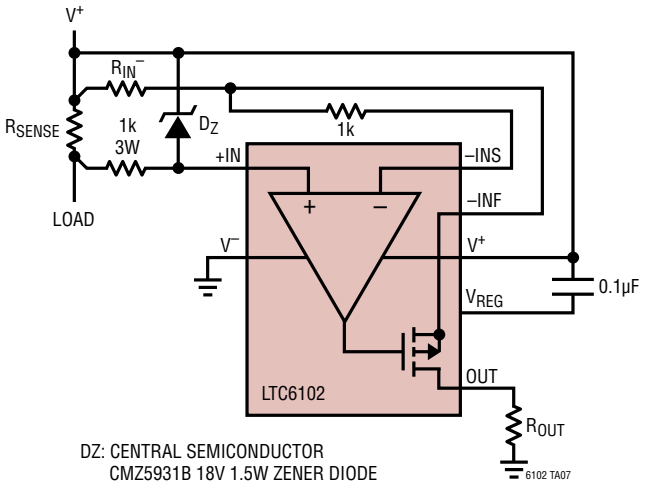


Intelligent High-Side Switch with Current Monitor



TYPICAL APPLICATIONS

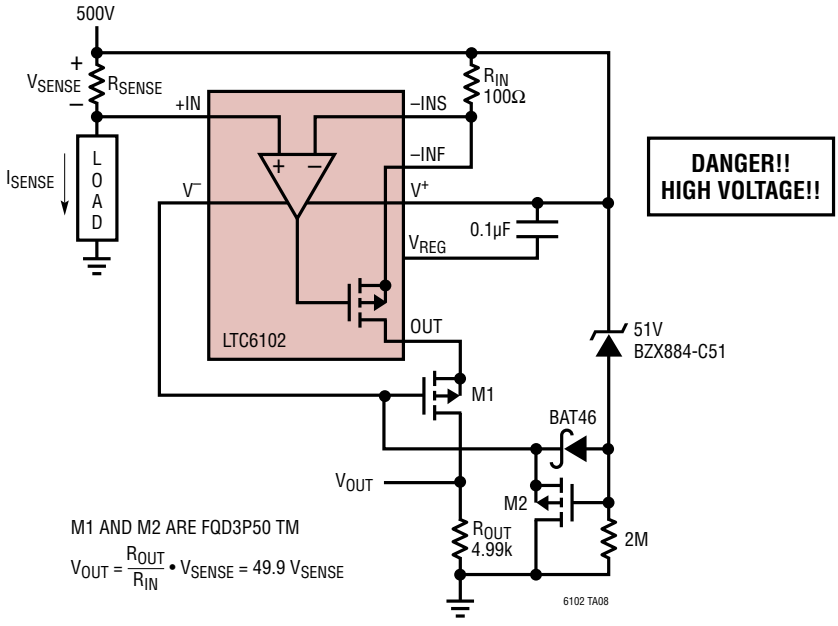
Input Overvoltage Protection



DZ: CENTRAL SEMICONDUCTOR
CMZ5931B 18V 1.5W ZENER DIODE

Simple 500V Current Monitor

DANGER! Lethal Potentials Present — Use Caution

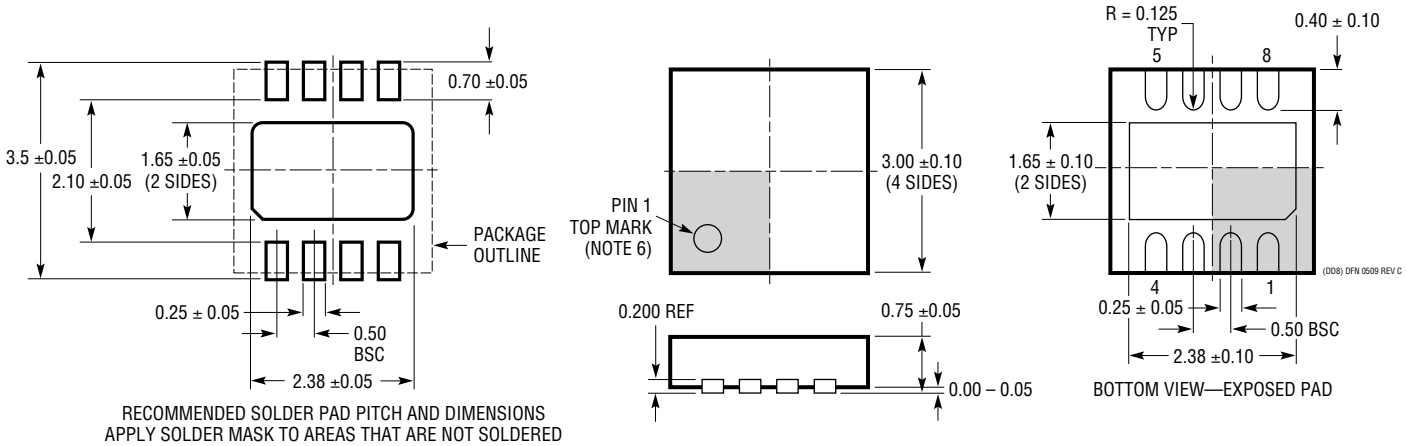


M1 AND M2 ARE FQD3P50 TM

$V_{OUT} = \frac{R_{OUT}}{R_{IN}} \bullet V_{SENSE} = 49.9\ V_{SENSE}$

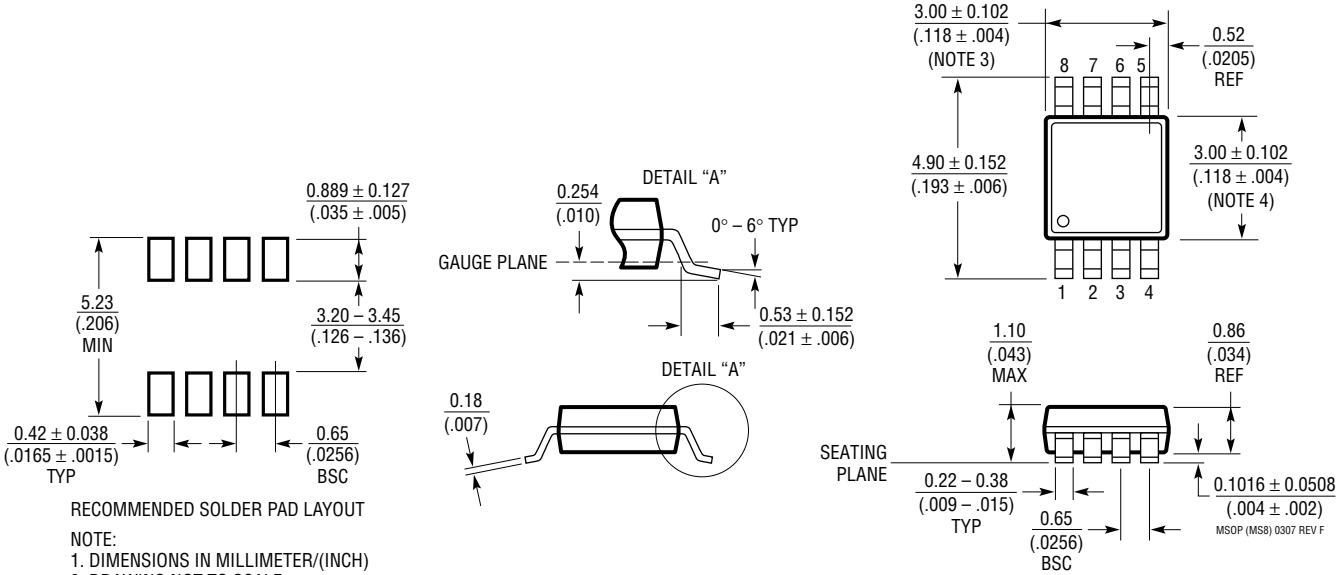
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	8/10	Updated graph 21	8
E	6/14	Web Links Added	All
		Correction to Output Current Absolute Maximum Ratings, (–1mA, +10mA) instead of (+1mA, –10mA)	2
		Correction to Supply Current at V^+=60V. Specification does not apply over the full operating temperature range	4