# 0.88nV/√Hz 730MHz, 500V/µs, Low Distortion Rail-to-Rail Output Op Amps with Shutdown

## FEATURES

- **Ultra Low Voltage Noise: 0.88nV/√Hz**
- **Low Distortion at High Speeds: HD2/HD3 < –100dBc (Av = +1, 4V$_{P-P}$, 2MHz, R$_L$ = 1kΩ)**
- **High Slew Rate: 500V/µs**
- **GBW = 890MHz**
- **–3dB Frequency (A$_V$ = +1): 730MHz**
- Input Offset Voltage: 250µV Max Across Temperature
- Offset Drift :0.4µV/°C
- Input Common Mode Range Includes Negative Rail
- Output Swings Rail-to-Rail
- Supply Current: 16mA/Channel Typ
- Shutdown Supply Current = 500µA
- Operating Supply Range: 2.8V to 11.75V
- Large Output Current: 80mA Min
- Very High Open Loop Gain: 5.6V/µV (135dB), R$_L$ = 1kΩ
- Operating Temp Range: –40°C to 125°C
- Singles in 8-Lead SOIC, TSOT-23, DC-6, Duals in DD10, MS8

## APPLICATIONS

- Optical Electronics: Fast Transimpedance Amplifiers
- Driving High Dynamic Range A/D Converters
- Active Filters
- Video Amplifiers
- High Speed Differential to Single-Ended Conversion
- Low Voltage Hi-Fi Amplification



## DESCRIPTION

The LTC®6228/LTC6229 are single/dual very fast, low noise rail-to-rail output, unity gain stable op amps. They have a gain-bandwidth product of 890MHz and a slew rate of 500V/µs. The low input referred voltage noise of only 0.88nV/√Hz and low distortion performance of better than –100dB at 4V$_{P-P}$ even for signals as fast as 2MHz make them ideal for applications that require high dynamic range and deal with high slew rate signals, such as driving A/D converters. Additional features include Shutdown and the ability to enable/disable internal bias current cancellation to optimize noise performance.

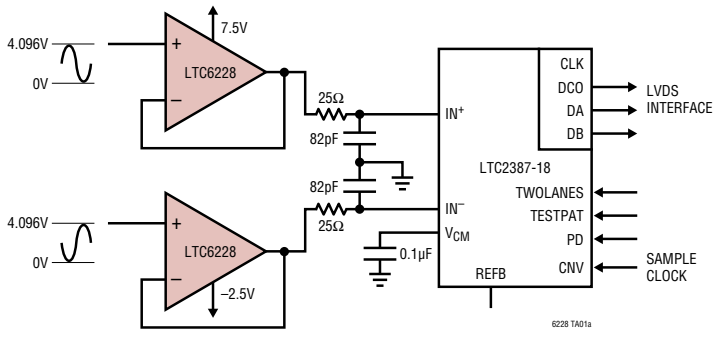
The combination of low offset, low offset drift, high gain and high CMRR make the LTC6228 family the superior choice for wide dynamic range applications.

The LTC6228 family maintains excellent performance for supply voltages of 2.8V to 11.75V and the devices are specified at supplies of 3V, 5V and 10V(±5V). With an input range extending to the negative rail and an output range that encompasses the entire supply range, the operational amplifier can accommodate wide swinging signals, and single supply operation.

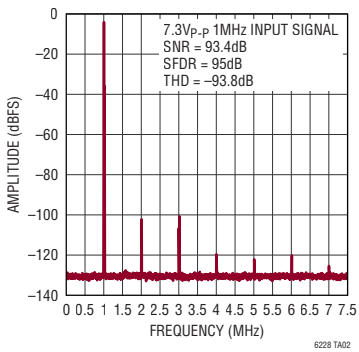
For space constrained PCB layouts, the LTC6228 is available in a 2mm × 2mm DFN and the LTC6229 is available in a 3mm × 3mm DFN. The amplifiers are also available in conventional leaded packages. These amplifiers can be used as improved replacements for many high speed op amps to improve speed, noise, distortion and dynamic range.

## TYPICAL APPLICATION

**LTC6228 Based Driver for the LTC2387-18 SAR ADC**




**System Performance: 2 x LTC6228 Driving LTC2387-18**
**8192 Point FFT, –1dBFS**
**f$_{SMPL}$ = 15Msps, f$_{IN}$ = 1MHz**




Rev. B

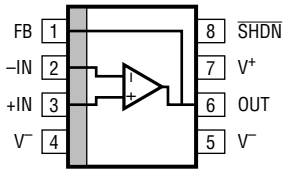
## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($V^-$ to $V^+$) ..... 12V
Input Voltage (–IN, +IN, $\overline{SHDN}$)....$V^-$ – 0.3V to $V^+$ + 0.3V
Input Current (–IN, +IN, $\overline{SHDN}$) (Note 2)..... ±10mA
Operating Temperature Range
LTC6228I/LTC6229I (Note 4).....–40°C to 85°C
LTC6228H/LTC6229H (Note 4) .....–40°C to 125°C
Specified Temperature Range
LTC6228I/LTC6229I (Note 4).....–40°C to 85°C
LTC6228H/LTC6229H (Note 4) .....–40°C to 125°C

Output Current (OUT, FB)(Note 3) ..... ±100mA
Output Short-Circuit Duration .....Thermally Limited
Storage Temperature Range ..... –65°C to 150°C
Maximum Junction Temperature ..... 150°C
Lead Temperature (Soldering 10s)
(MSOP/S8/TSOT Only) ..... 300°C

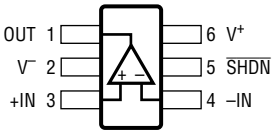
## PIN CONFIGURATION

TOP VIEW



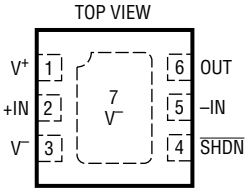

S8 PACKAGE
8-LEAD PLASTIC SO
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 120°C/W (NOTE 7)

TOP VIEW



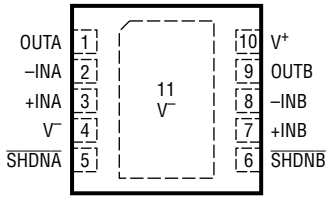

S6 PACKAGE
6-LEAD PLASTIC TSOT-23
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 192°C/W (NOTE 7)

TOP VIEW



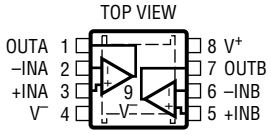

DC PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 80°C/W (NOTE 7)
EXPOSED PAD (PIN 7) IS $V^-$, MUST BE SOLDERED TO PCB

TOP VIEW




DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W (NOTE 2)
EXPOSED PAD (PIN 11) IS $V^-$, MUST BE SOLDERED TO PCB

TOP VIEW




MSE PACKAGE
8-LEAD PLASTIC MSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 35°C/W (NOTE 8)
EXPOSED PAD (PIN 9) IS $V^-$, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6228IS6#TRMPBF | LTC6228IS6#TRPBF | LTHGB | 6-Lead TSOT-23 | –40°C to 85°C |
| LTC6228HS6#TRMPBF | LTC6228HS6#TRPBF | LTHGB | 6-Lead TSOT-23 | –40°C to 125°C |
| LTC6228IDC#TRMPBF | LTC6228IDC#TRPBF | LHGC | 6-Lead 2mm × 2mm DFN | –40°C to 85°C |
| LTC6228HDC#TRMPBF | LTC6228HDC#TRPBF | LHGC | 6-Lead 2mm × 2mm DFN | –40°C to 125°C |
| LTC6228IS8#TRMPBF | LTC6228IS8#TRPBF | 6228 | 8-Lead SOIC-8 | –40°C to 85°C |
| LTC6228HS8#TRMPBF | LTC6228HS8#TRPBF | 6228 | 8-Lead SOIC-8 | –40°C to 125°C |
| LTC6229IMS8E#PBF | LTC6229IMS8E#TRPBF | LTGHD | 8-Lead MSOP | –40°C to 85°C |
| LTC6229HMS8E#PBF | LTC6229HMS8E#TRPBF | LTGHD | 8-Lead MSOP | –40°C to 125°C |
| LTC6229IDD#PBF | LTC6229IDD#TRPBF | LHGF | 10-Lead 3mm × 3mm DFN | –40°C to 85°C |
| LTC6229HDD#PBF | LTC6229HDD#TRPBF | LHGF | 10-Lead 3mm × 3mm DFN | –40°C to 125°C |

Consult ADI Marketing for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS ($V_S$ = ±5V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±5V, $V_{CM}$ = 0V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | –95 | 20 | 95 | µV |
| | | | ● | –250 | | 250 | µV |
| $\Delta V_{OS}$ | Input Offset Voltage Match (LTC6229) | | | –140 | 18 | 140 | µV |
| | | | ● | –400 | | 400 | µV |
| $T_{CVOS}$ | Input Offset Voltage Drift | | ● | | 0.4 | | µV/°C |
| $I_B$ | Input Bias Current (Note 6) | Bias Cancellation Disabled | | –40 | –16 | | µA |
| | | | ● | –44 | | | µA |
| | | Bias Cancellation Enabled | | –2.5 | 0.6 | 2.5 | µA |
| | | | ● | –4.1 | | 4.1 | µA |
| $\Delta I_B$ | Input Bias Current Match (LTC6229) | Bias Cancellation Disabled | | –2 | 0.3 | 2 | µA |
| | | | ● | –3 | | 3 | µA |
| | | Bias Cancellation Enabled | | –3 | 0.3 | 3 | µA |
| | | | ● | –4 | | 4 | µA |
| $I_{OS}$ | Input Offset Current | Bias Cancellation Disabled | | –0.55 | 0.1 | 0.55 | µA |
| | | | ● | –0.8 | | 0.8 | µA |
| | | Bias Cancellation Enabled | | –0.9 | 0.1 | 0.9 | µA |
| | | | ● | –1 | | 1 | µA |
| $\Delta I_{OS}$ | Input Offset Current Match (LTC6229) | Bias Cancellation Disabled | | –1 | 0.15 | 1 | µA |
| | | | ● | –1.4 | | 1.4 | µA |
| | | Bias Cancellation Enabled | | –1.3 | 0.25 | 1.3 | µA |
| | | | ● | –1.6 | | 1.6 | µA |
| $e_n$ | Input Noise Voltage Spectral Density | f = 1MHz | | | 0.88 | | nV/√Hz |
| | Integrated 1/f Noise | 0.1Hz to 10Hz | | | 0.94 | | $\mu V_{P-P}$ |
| $i_n$ | Input Current Noise Spectral Density | f = 1MHz Bias Cancellation Disabled | | | 3 | | pA/√Hz |
| | | f = 1MHz Bias Cancellation Enabled | | | 6.3 | | pA/√Hz |
| $C_{IN}$ | Input Capacitance | Differential Mode | | | 3.5 | | pF |
| | | Common Mode | | | 1.5 | | pF |
| $R_{IN}$ | Input Resistance | Differential Mode | | | 2.6 | | kΩ |
| | | Common Mode | | | 4 | | MΩ |

## ELECTRICAL CHARACTERISTICS ($V_S$ = ±5V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±5V, $V_{CM}$ = 0V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L$ = 1kΩ to Half Supply $V_{OUT}$ = ±4V | ●<br>● | 120<br>113 | 135 | | dB<br>dB |
| | | $R_L$ = 100Ω to Half Supply $V_{OUT}$ = ±3V | ●<br>● | 100<br>92 | 120 | | dB<br>dB |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = $V^-$ – 0.1 to $V^+$ – 1.2V | ●<br>● | 100<br>94 | 110 | | dB<br>dB |
| $V_{CMR}$ | Input Common Mode Range | | ● | $V^-$ – 0.1 | | $V^+$ – 1.2 | V |
| $PSRR^+$ | Positive Power Supply Rejection Ratio | $V^-$ = –1V, $V^+$ = 1.8V to 10.75V | ●<br>● | 100<br>95 | 110 | | dB<br>dB |
| $PSRR^-$ | Negative Power Supply Rejection Ratio | $V^+$ = 1.5V, $V^-$ = –1.3V to –10.25V | ●<br>● | 101<br>99 | 126 | | dB<br>dB |
| | Supply Voltage Range ($V^+$ – $V^-$) (Note 5) | | ● | 2.8 | | 11.75 | V |
| $V_{OL}$ | Output Swing Low ($V_{OUT}$ – $V^-$) | No Load | ●<br>● | | 8 | 16<br>20 | mV<br>mV |
| | | $I_{SINK}$ = 5mA | ●<br>● | | 46 | 70<br>85 | mV<br>mV |
| | | $I_{SINK}$ = 25mA | ●<br>● | | 140 | 220<br>280 | mV<br>mV |
| $V_{OH}$ | Output Swing High ($V^+$ – $V_{OUT}$) | No Load | ●<br>● | | 27 | 50<br>60 | mV<br>mV |
| | | $I_{SINK}$ = 5mA | ●<br>● | | 90 | 140<br>180 | mV<br>mV |
| | | $I_{SOURCE}$ = 25mA | ●<br>● | | 250 | 340<br>450 | mV<br>mV |
| $I_{SC}$ | Output Short-Circuit Current | Sourcing | ●<br>● | | –130 | –80<br>–65 | mA<br>mA |
| | | Sinking | ●<br>● | 80<br>60 | 140 | | mA<br>mA |
| $I_S$ | Supply Current per Channel | | ●<br>● | | 16 | 16.9<br>19.8 | mA<br>mA |
| $I_{SD}$ | Disable Supply Current per Channel, Amplifier Off | $V_{\overline{SHDN}}$ = $V^+$ – 2.75V | ●<br>● | | 500 | 610<br>770 | µA<br>µA |
| $V_{L\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Voltage Low, Disable Amplifier | | ● | | | $V^+$ – 2.75 | V |
| $V_{H\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Voltage High, Enable Amplifier | | ● | $V^+$ – 1.6 | | | V |
| $V_{L\_IBIAS}$ | $\overline{SHDN}$ Pin Input Voltage Low, Disable Bias Cancellation | | ● | | | $V^+$ – 1 | V |
| $V_{H\_IBIAS}$ | $\overline{SHDN}$ Pin Input Voltage Low, Enable Bias Cancellation | | ● | $V^+$ – 0.35 | | | V |
| $I_{L\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Current, Disable Amplifier | $V_{\overline{SHDN}}$ = $V^+$ – 2.75V | ● | –10 | –2.5 | 10 | µA |
| $I_{H\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Current, Enable Amplifier | $V_{\overline{SHDN}}$ = $V^+$ – 1.6V | ● | –10 | –0.3 | 10 | µA |
| $I_{L\_IBIAS}$ | $\overline{SHDN}$ Pin Input Current Low, Disable Bias Cancellation | $V_{\overline{SHDN}}$ = $V^+$ – 1V | ● | –10 | 0.265 | 10 | µA |
| $I_{H\_IBIAS}$ | $\overline{SHDN}$ Pin Input Current Low, Enable Bias Cancellation | $V_{\overline{SHDN}}$ = $V^+$ – 0.35V | ● | –10 | 1 | 10 | µA |
| $I_{OSD}$ | Output Leakage Current in Shutdown | $V_{\overline{SHDN}}$ = $V^+$ – 2.75V, OUT Shorted to $V^+$ or $V^-$ | | | 100 | | nA |
| BW | –3dB Closed Loop Bandwidth | $A_V$ = 1, $R_L$ = 1kΩ to Half Supply | | | 730 | | MHz |
| GBW | Gain-Bandwidth Product | f = 5MHz, $R_L$ = 1kΩ to Half Supply | ●<br>● | 700<br>650 | 890 | | MHz<br>MHz |
| $t_{ON}$ | Turn-On Time | $V_{\overline{SHDN}}$ = $V^+$ – 2.75V to $V^+$ – 1.6V | | | 900 | | ns |

## ELECTRICAL CHARACTERISTICS ($V_S$ = ±5V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±5V, $V_{CM}$ = 0V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{OFF}$ | Turn-Off Time | $V_{\overline{SHDN}}$ = V⁺ – 1.6V to V⁺ – 2.75V | | | 500 | | ns |
| $t_{S\_0.1}$ | Settling Time to 0.1% | $A_V$ = 1, 2V Output Step, $R_L$ = 1kΩ | | | 26 | | ns |
| | | $A_V$ = 1, 4V Output Step, $R_L$ = 1kΩ | | | 34 | | ns |
| $t_{S\_0.01}$ | Settling Time to 0.01% | $A_V$ = 1, 6V Output Step, $R_L$ = 1kΩ | | | 53 | | ns |
| SR | Slew Rate | $A_V$ = +4, 8V Output Step (Note 8) | | 320 | 500 | | V/µs |
| | | | ● | 250 | | | V/µs |
| FPBW | Full Power Bandwidth | $V_{OUT}$ = $8V_{P-P}$, $A_V$ = +2, THD < –40dBc | | | 12.5 | | MHz |
| HD2/HD3 | Harmonic Distortion, $R_L$ = 1kΩ to Half Supply, $A_V$ = +1 | $f_C$ = 100kHz, $V_O$ = $4V_{P-P}$ | | | –113/–119 | | dBc |
| | | $f_C$ = 100kHz, $V_O$ = $2V_{P-P}$ | | | –126/–131 | | dBc |
| | | $f_C$ = 1MHz, $V_O$ = $4V_{P-P}$ | | | –107/–114 | | dBc |
| | | $f_C$ = 1MHz, $V_O$ = $2V_{P-P}$ | | | –119/–132 | | dBc |
| | | $f_C$ = 5MHz, $V_O$ = $4V_{P-P}$ | | | –83/–96 | | dBc |
| | | $f_C$ = 5MHz, $V_O$ = $2V_{P-P}$ | | | –90/–113 | | dBc |
| | | $f_C$ = 10MHz, $V_O$ = $2V_{P-P}$ | | | –74/–89 | | dBc |
| | Harmonic Distortion, $R_L$ = 100Ω to Half Supply, $A_V$ = +1 | $f_C$ = 100kHz, $V_O$ = $4V_{P-P}$ | | | –105/–106 | | dBc |
| | | $f_C$ = 100kHz, $V_O$ = $4V_{P-P}$ | | | –118/–124 | | dBc |
| | | $f_C$ = 1MHz, $V_O$ = $4V_{P-P}$ | | | –97/–107 | | dBc |
| | | $f_C$ = 1MHz, $V_O$ = $2V_{P-P}$ | | | –100/–114 | | dBc |
| | | $f_C$ = 5MHz, $V_O$ = $4V_{P-P}$ | | | –79/–75 | | dBc |
| | | $f_C$ = 5MHz, $V_O$ = $2V_{P-P}$ | | | –83/–82 | | dBc |
| | | $f_C$ = 10MHz, $V_O$ = $2V_{P-P}$ | | | –72/–68 | | dBc |
| ΔG | Differential Gain (NTSC) | $A_V$ = 2, $R_L$ = 150Ω | | | 0.008 | | % |
| | | $A_V$ = +1, $R_L$ = 1kΩ | | | 0.001 | | % |
| Δθ | Differential Phase (NTSC) | $A_V$ = 2, $R_L$ = 150Ω | | | 0.004 | | Deg |
| | | $A_V$ = +1, $R_L$ = 1kΩ | | | 0.09 | | Deg |

## ELECTRICAL CHARACTERISTICS ($V_S$ = 5V, 0V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 5V, 0V, $V_{CM}$ = $V_{OUT}$ = 2.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | –105 | 20 | 105 | µV |
| | | | ● | –290 | | 290 | µV |
| $\Delta V_{OS}$ | Input Offset Voltage Match (LTC6229) | | | –140 | 18 | 140 | µV |
| | | | ● | –400 | | 400 | µV |
| $T_{CVOS}$ | Input Offset Voltage Drift | | ● | | 0.4 | | µV/°C |
| $I_B$ | Input Bias Current (Note 6) | Bias Cancellation Disabled | | –40 | –16 | | µA |
| | | | ● | –44 | | | µA |
| | | Bias Cancellation Enabled | | –3 | 1 | 3 | µA |
| | | | ● | –4.4 | | 4.4 | µA |
| $\Delta I_B$ | Input Bias Current Match (LTC6229) | Bias Cancellation Disabled | | –2 | 0.3 | 2 | µA |
| | | | ● | –3 | | 3 | µA |
| | | Bias Cancellation Enabled | | –3 | 0.3 | 3 | µA |
| | | | ● | –4 | | 4 | µA |
| $I_{OS}$ | Input Offset Current | Bias Cancellation Disabled | | –0.55 | 0.1 | 0.55 | µA |
| | | | ● | –0.8 | | 0.8 | µA |
| | | Bias Cancellation Enabled | | –0.9 | 0.15 | 0.9 | µA |
| | | | ● | –1 | | 1 | µA |
| $\Delta I_{OS}$ | Input Offset Current Match (LTC6229) | Bias Cancellation Disabled | | –1 | 0.15 | 1 | µA |
| | | | ● | –1.4 | | 1.4 | µA |
| | | Bias Cancellation Enabled | | –1.3 | 0.25 | 1.3 | µA |
| | | | ● | –1.6 | | 1.6 | µA |

## ELECTRICAL CHARACTERISTICS ($V_S$ = 5V, 0V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 5V, 0V, $V_{CM}$ = $V_{OUT}$ = 2.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $e_n$ | Input Noise Voltage Spectral Density | f = 1MHz | | | 0.88 | | nV/√Hz |
| | Integrated 1/f Noise | 0.1Hz to 10Hz | | | 0.94 | | $\mu V_{P-P}$ |
| $i_n$ | Input Current Noise Spectral Density | f = 1MHz Bias Cancellation Disabled<br>f = 1MHz Bias Cancellation Enabled | | | 3<br>6.3 | | pA/√Hz<br>pA/√Hz |
| $C_{IN}$ | Input Capacitance | Differential Mode<br>Common Mode | | | 3.5<br>1.5 | | pF<br>pF |
| $R_{IN}$ | Input Resistance | Differential Mode<br>Common Mode | | | 2.6<br>4 | | kΩ<br>MΩ |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L$ = 1kΩ to Half Supply, $V_{OUT}$ = $V_{CM}$ ±2 | ●<br>● | 120<br>115 | 140 | | dB<br>dB |
| | | $R_L$ = 100Ω to Half Supply, $V_{OUT}$ = $V_{CM}$ ±2 | ●<br>● | 106<br>100 | 120 | | dB<br>dB |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = $V^-$ – 0.1 to $V^+$ – 1.2V | ●<br>● | 97<br>92 | 110 | | dB<br>dB |
| $V_{CMR}$ | Input Common Mode Range | | ● | $V^-$ – 0.1 | | $V^+$ – 1.2 | V |
| $PSRR^+$ | Positive Power Supply Rejection Ratio | $V^-$ = –1V, $V^+$ = 1.8V to 10.75V | ●<br>● | 100<br>95 | 110 | | dB<br>dB |
| $PSRR^-$ | Negative Power Supply Rejection Ratio | $V^+$ = 1.5V, $V^-$ = –1.3V to –10.25V | ●<br>● | 103<br>100 | 126 | | dB<br>dB |
| | Supply Voltage Range ($V^+$ – $V^-$) (Note 5) | | ● | 2.8 | | 11.75 | V |
| $V_{OL}$ | Output Swing Low ($V_{OUT}$ – $V^-$) | No Load | ●<br>● | | 7 | 18<br>32 | mV<br>mV |
| | | $I_{SINK}$ = 5mA | ●<br>● | | 40 | 70<br>90 | mV<br>mV |
| | | $I_{SINK}$ = 25mA | ●<br>● | | 150 | 220<br>300 | mV<br>mV |
| $V_{OH}$ | Output Swing High ($V_{CC}$ – $V^+$) | No Load | ●<br>● | | 26 | 48<br>58 | mV<br>mV |
| | | $I_{SINK}$ = 5mA | ●<br>● | | 93 | 144<br>185 | mV<br>mV |
| | | $I_{SOURCE}$ = 25mA | ●<br>● | | 255 | 347<br>459 | mV<br>mV |
| $I_{SC}$ | Output Short-Circuit Current | Sourcing | ●<br>● | | –110 | –65<br>–52 | mA<br>mA |
| | | Sinking | ●<br>● | 70<br>45 | 110 | | mA<br>mA |
| $I_S$ | Supply Current per Channel | | ●<br>● | | 16.5 | 17.8<br>19.6 | mA<br>mA |
| $I_{SD}$ | Disable Supply Current per Channel, Amplifier Off | $V_{\overline{SHDN}}$ = $V^+$ – 2.65V | ●<br>● | | 300 | 380<br>430 | µA<br>µA |
| $V_{L\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Voltage Low, Disable Amplifier | | ● | | | $V^+$ – 2.65 | V |
| $V_{H\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Voltage High, Enable Amplifier | | ● | $V^+$ – 1.6 | | | V |
| $V_{L\_IBIAS}$ | $\overline{SHDN}$ Pin Input Voltage Low, Disable Bias Cancellation | | ● | | | $V^+$ – 1 | V |
| $V_{H\_IBIAS}$ | $\overline{SHDN}$ Pin Input Voltage Low, Enable Bias Cancellation | | ● | $V^+$ – 0.35 | | | V |
| $I_{L\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Current, Disable Amplifier | $V_{\overline{SHDN}}$ = $V^+$ – 2.65V | ● | –10 | –2.5 | 10 | µA |

## ELECTRICAL CHARACTERISTICS ($V_S$ = 5V, 0V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 5V, 0V, $V_{CM}$ = $V_{OUT}$ = 2.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{H\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Current, Enable Amplifier | $V_{\overline{SHDN}}$ = $V^+$ – 1.6V | ● | –10 | –0.3 | 10 | µA |
| $I_{L\_IBIAS}$ | $\overline{SHDN}$ Pin Input Current Low, Disable Bias Cancellation | $V_{\overline{SHDN}}$ = $V^+$ – 1V | ● | –10 | 0.265 | 10 | µA |
| $I_{H\_IBIAS}$ | $\overline{SHDN}$ Pin Input Current Low, Enable Bias Cancellation | $V_{\overline{SHDN}}$ = $V^+$ – 0.35V | ● | –10 | 1 | 10 | µA |
| $I_{OSD}$ | Output Leakage Current in Shutdown | $V_{\overline{SHDN}}$ = $V^+$ – 2.65V, OUT Shorted to $V^+$ or $V^–$ | | | 100 | | nA |
| BW | –3dB Closed Loop Bandwidth | $A_V$ = 1, $R_L$ = 1kΩ to Half Supply | | | 800 | | MHz |
| GBW | Gain-Bandwidth Product | f = 5MHz, $R_L$ = 1kΩ to Half Supply | <br>● | 700<br>600 | 865 | | MHz<br>MHz |
| $t_{ON}$ | Turn-On Time | $V_{\overline{SHDN}}$ = $V^+$ – 2.65V to $V^+$ – 1.6V | | | 900 | | ns |
| $t_{OFF}$ | Turn-Off Time | $V_{\overline{SHDN}}$ = $V^+$ – 1.6V to $V^+$ – 2.65V | | | 500 | | ns |
| $t_{S\_0.1}$ | Settling Time to 0.1% | $A_V$ = 1, 2V Output Step, $R_L$ = 1kΩ | | | 26 | | ns |
| SR | Slew Rate | $A_V$ = +4, 4V Output Step (Note 8) | | | 350 | | V/µs |
| FPBW | Full Power Bandwidth | $V_{OUT}$ = $4V_{P-P}$, $A_V$ = +2, THD < –40dBc | | | 18 | | MHz |
| HD2/HD3 | Harmonic Distortion, $R_L$ = 1kΩ to Half Supply | $f_C$ = 100kHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 1MHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 5MHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 10MHz, $V_O$ = $2V_{P-P}$ | | | –106/–130<br>–95/–105<br>–88/–114<br>–78/–90 | | dBc<br>dBc<br>dBc<br>dBc |
| | Harmonic Distortion, $R_L$ = 100Ω to Half Supply | $f_C$ = 100kHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 1MHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 5MHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 10MHz, $V_O$ = $2V_{P-P}$ | | | –112/–115<br>–99/–120<br>–83/–88<br>–70/–73 | | dBc<br>dBc<br>dBc<br>dBc |
| ΔG | Differential Gain (NTSC) | $A_V$ = 2, $R_L$ = 150Ω<br>$A_V$ = +1, $R_L$ = 1kΩ | | | 0.005<br>0.002 | | %<br>% |
| Δθ | Differential Phase (NTSC) | $A_V$ = 2, $R_L$ = 150Ω<br>$A_V$ = +1, $R_L$ = 1kΩ | | | 0.007<br>0.018 | | Deg<br>Deg |

## ELECTRICAL CHARACTERISTICS ($V_S$ = 3V, 0V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 3V, 0V, $V_{CM}$ = 1.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | <br>● | –110<br>–300 | 24 | 110<br>300 | µV<br>µV |
| $\Delta V_{OS}$ | Input Offset Voltage Match (LTC6229) | | <br>● | –140<br>–400 | 18 | 140<br>400 | µV<br>µV |
| $T_{CVOS}$ | Input Offset Voltage Drift | | ● | | 0.4 | | µV/°C |
| $I_B$ | Input Bias Current (Note 6) | Bias Cancellation Disabled | <br>● | –38<br>–44 | –16 | | µA<br>µA |
| | | Bias Cancellation Enabled | <br>● | –3.5<br>–4.3 | 1.5 | 3.5<br>4.1 | µA<br>µA |
| $\Delta I_B$ | Input Bias Current Match (LTC6229) | Bias Cancellation Disabled | <br>● | –2<br>–3 | 0.3 | 2<br>3 | µA<br>µA |
| | | Bias Cancellation Enabled | <br>● | –3<br>–4 | 0.3 | 3<br>4 | µA<br>µA |

## ELECTRICAL CHARACTERISTICS ($V_S$ = 3V, 0V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 3V, 0V, $V_{CM}$ = 1.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{OS}$ | Input Offset Current | Bias Cancellation Disabled | | –0.55 | 0.1 | 0.55 | µA |
| | | | ● | –0.8 | | 0.8 | µA |
| | | Bias Cancellation Enabled | | –0.9 | 0.15 | 0.9 | µA |
| | | | ● | –1 | | 1 | µA |
| $\Delta I_{OS}$ | Input Offset Current Match (LTC6229) | Bias Cancellation Disabled | | –1 | 0.15 | 1 | µA |
| | | | ● | –1.4 | | 1.4 | µA |
| | | Bias Cancellation Enabled | | –1.3 | 0.25 | 1.3 | µA |
| | | | ● | –1.6 | | 1.6 | µA |
| $e_n$ | Input Noise Voltage Spectral Density | f = 1MHz | | | 0.88 | | nV/√Hz |
| | Integrated 1/f Noise | 0.1Hz to 10Hz | | | 0.94 | | $\mu V_{P-P}$ |
| $i_n$ | Input Current Noise Spectral Density | f = 1MHz Bias Cancellation Disabled | | | 3 | | pA/√Hz |
| | | f = 1MHz Bias Cancellation Enabled | | | 6.3 | | pA/√Hz |
| $C_{IN}$ | Input Capacitance | Differential Mode | | | 3.5 | | pF |
| | | Common Mode | | | 1.5 | | pF |
| $R_{IN}$ | Input Resistance | Differential Mode | | | 2.6 | | kΩ |
| | | Common Mode | | | 4 | | MΩ |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L$ = 1kΩ to Half Supply, ($V_{OUT}$ = $V_{CM}$ ±1V) | | 118 | 130 | | dB |
| | | | ● | 113 | | | dB |
| | | $R_L$ = 100Ω to Half Supply, ($V_{OUT}$ = $V_{CM}$ ±1V) | | | 120 | | dB |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = $V^-$ to $V^+$ – 1.2V | | 95 | 110 | | dB |
| | | | ● | 91 | | | dB |
| $V_{CMR}$ | Input Common Mode Range | | ● | $V^-$ – 0.1 | | $V^+$ – 1.2 | V |
| $PSRR^+$ | Positive Power Supply Rejection Ratio | $V^-$ = –1V, $V^+$ = 1.8V to 10.75V | | 100 | 110 | | dB |
| | | | ● | 95 | | | dB |
| $PSRR^-$ | Negative Power Supply Rejection Ratio | $V^+$ = 1.5V, $V^-$ = –1.3V to –10.25V | | 101 | 126 | | dB |
| | | | ● | 99 | | | dB |
| | Supply Voltage Range ($V^+$ – $V^-$) (Note 5) | | ● | 2.8 | | 11.75 | V |
| $V_{OL}$ | Output Swing Low ($V_{OUT}$ – $V^-$) | No Load | | | 7 | 10 | mV |
| | | | ● | | | 18 | mV |
| | | $I_{SINK}$ = 5mA | | | 48 | 74 | mV |
| | | | ● | | | 100 | mV |
| | | $I_{SINK}$ = 25mA | | | 165 | 320 | mV |
| | | | ● | | | 430 | mV |
| $V_{OH}$ | Output Swing High ($V_{CC}$ – $V^+$) | No Load | | | 27 | 49 | mV |
| | | | ● | | | 59 | mV |
| | | $I_{SINK}$ = 5mA | | | 106 | 166 | mV |
| | | | ● | | | 213 | mV |
| | | $I_{SOURCE}$ = 25mA | | | 290 | 520 | mV |
| | | | ● | | | 580 | mV |
| $I_{SC}$ | Output Short-Circuit Current | Sourcing | | | –67 | | mA |
| | | Sinking | | | 84 | | mA |
| $I_S$ | Supply Current per Channel | | | | 16.4 | 17.6 | mA |
| | | | ● | | | 19 | mA |
| $I_{SD}$ | Disable Supply Current per Channel, Amplifier Off | $V_{\overline{SHDN}}$ = $V^+$ – 2.65V | | | 260 | 305 | µA |
| | | | ● | | | 350 | µA |

## ELECTRICAL CHARACTERISTICS ($V_S$ = 3V, 0V)

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = 3V, 0V, $V_{CM}$ = 1.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{L\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Voltage Low, Disable Amplifier | | ● | | | $V^+ – 2.65$ | V |
| $V_{H\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Voltage High, Enable Amplifier | | ● | $V^+ – 1.6$ | | | V |
| $V_{L\_IBIAS}$ | $\overline{SHDN}$ Pin Input Voltage Low, Disable Bias Cancellation | | ● | | | $V^+ – 1$ | V |
| $V_{H\_IBIAS}$ | $\overline{SHDN}$ Pin Input Voltage Low, Enable Bias Cancellation | | ● | $V^+ – 0.35$ | | | V |
| $I_{L\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Current, Disable Amplifier | $V_{\overline{SHDN}} = V^+ – 2.65V$ | ● | –10 | –2.5 | 10 | µA |
| $I_{H\_\overline{SHDN}}$ | $\overline{SHDN}$ Pin Input Current, Enable Amplifier | $V_{\overline{SHDN}} = V^+ – 1.6V$ | ● | –10 | –0.3 | 10 | µA |
| $I_{L\_IBIAS}$ | $\overline{SHDN}$ Pin Input Current Low, Disable Bias Cancellation | $V_{\overline{SHDN}} = V^+ – 1V$ | ● | –10 | 0.265 | 10 | µA |
| $I_{H\_IBIAS}$ | $\overline{SHDN}$ Pin Input Current Low, Enable Bias Cancellation | $V_{\overline{SHDN}} = V^+ – 0.35V$ | ● | –10 | 1 | 10 | µA |
| $I_{OSD}$ | Output Leakage Current in Shutdown | $V_{\overline{SHDN}} = V^+ – 2.65V$, OUT Shorted to $V^+$ or $V^–$ | | | 100 | | nA |
| BW | –3dB Closed Loop Bandwidth | $A_V$ = 1, $R_L$ = 1kΩ to Half Supply | | | 763 | | MHz |
| GBW | Gain-Bandwidth Product | f = 5MHz, $R_L$ = 1kΩ to Half Supply | <br>● | 700<br>560 | 845 | | MHz<br>MHz |
| $t_{ON}$ | Turn-On Time | $V_{\overline{SHDN}} = V^+ – 2.65V$ to $V^+ – 1.6V$ | | | 900 | | ns |
| $t_{OFF}$ | Turn-Off Time | $V_{\overline{SHDN}} = V^+ – 1.6V$ to $V^+ – 2.65V$ | | | 500 | | ns |
| $t_{S\_0.1}$ | Settling Time to 0.1% | $A_V$ = 1, $V_{CM}$ = 1V, 1V Output Step, $R_L$ = 1kΩ | | | 31 | | ns |
| SR | Slew Rate | $A_V$ = +4, 2V Output Step | | | 200 | | V/µs |
| FPBW | Full Power Bandwidth | $V_{OUT} = 2V_{P-P}$, $V_{CM}$ = 1V, $A_V$ = –1, THD < –40dBc | | | 22 | | MHz |
| HD2/HD3 | Harmonic Distortion, $R_L$ = 1kΩ to $V_{CM}$, $V_{OUT} = 1_{VP-P}$, $V_{CM}$ = 1.25V | $f_C$ = 100kHz<br>$f_C$ = 1MHz<br>$f_C$ = 5MHz<br>$f_C$ = 10MHz | | | –106/–127<br>–110/–128<br>–82/–105<br>–77/–96 | | dBc<br>dBc<br>dBc<br>dBc |
| | Harmonic Distortion, $R_L$ = 100Ω to $V_{CM}$, $V_{OUT} = 1_{VP-P}$, $V_{CM}$ = 1.25V | $f_C$ = 100kHz<br>$f_C$ = 1MHz<br>$f_C$ = 5MHz<br>$f_C$ = 10MHz | | | –116/–123<br>–105/–132<br>–89/–98<br>–77/–86 | | dBc<br>dBc<br>dBc<br>dBc |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The inputs are protected by back-to-back diodes. If any of the input or shutdown pins goes 300mV beyond either supply or the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output current is high.

**Note 4:** The LTC6228I/LTC6229I is guaranteed functional and specified over the temperature range of –40°C to 85°C. The LTC6228H/LTC6229H is guaranteed functional and specified over the temperature range of –40°C to 125°C.

**Note 5:** Supply range voltage is guaranteed by power supply rejection ratio test.

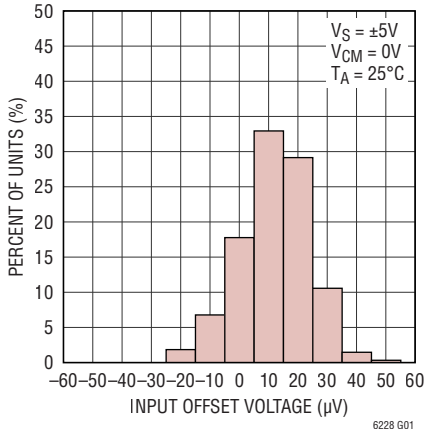
**Note 6:** The input bias current is the average of the currents through the non-inverting and inverting input pins.

**Note 7:** Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are with short traces connected to the leads with minimal metal area.

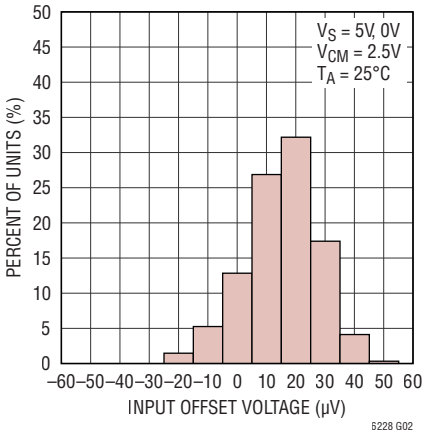
**Note 8:** Middle 2/3 of the output waveform is observed. $R_L$ = 1kΩ at half supply.

## TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

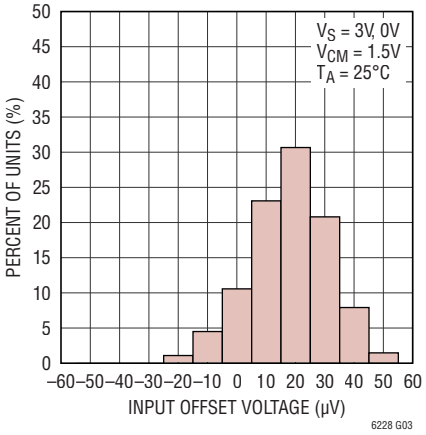
### Offset Distribution



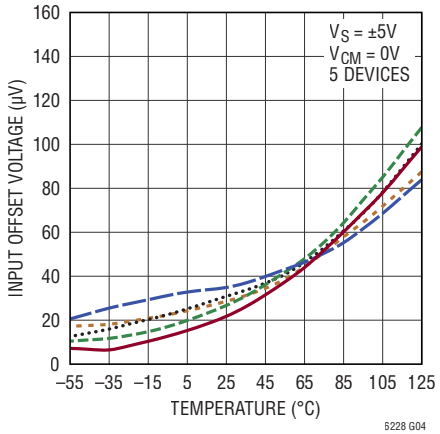

### Offset Distribution



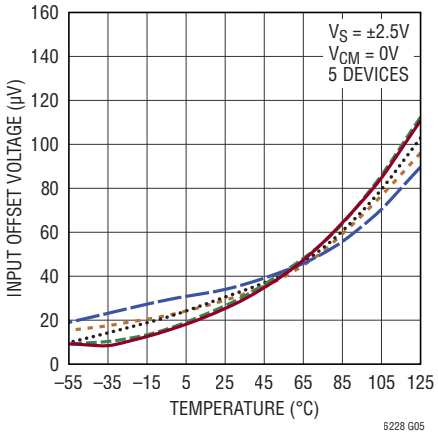

### Offset Distribution



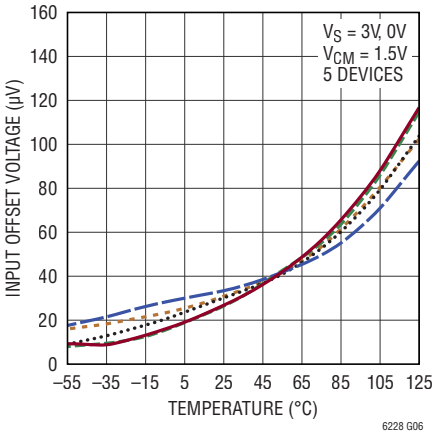

### $V_{OS}$ vs Temperature, 10V Supply



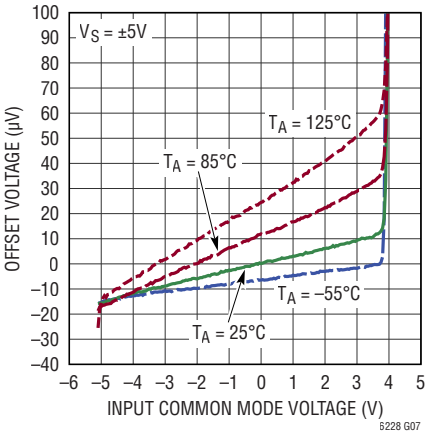

### $V_{OS}$ vs Temperature, 5V Supply



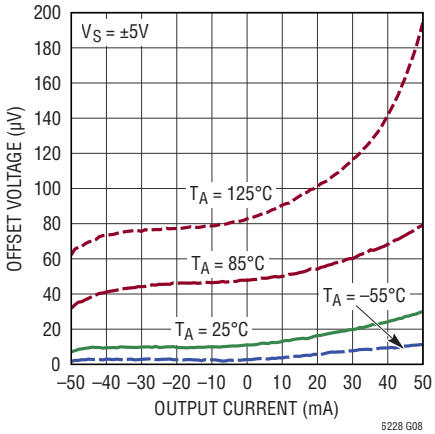

### $V_{OS}$ vs Temperature, 3V Supply



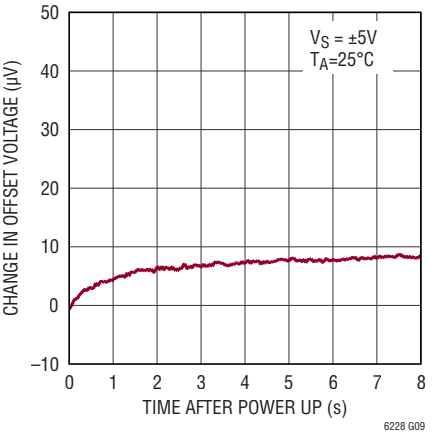

### Offset Voltage vs Input Common Mode Voltage




### Offset Voltage vs Output Current



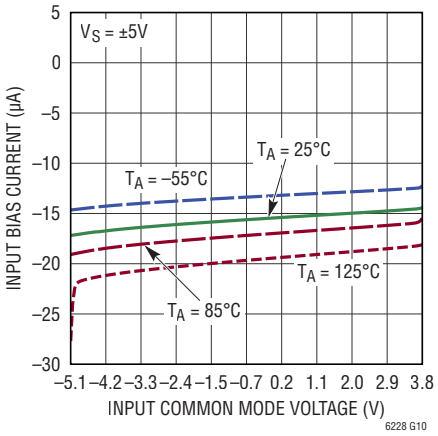

### Warm Up Drift vs Time



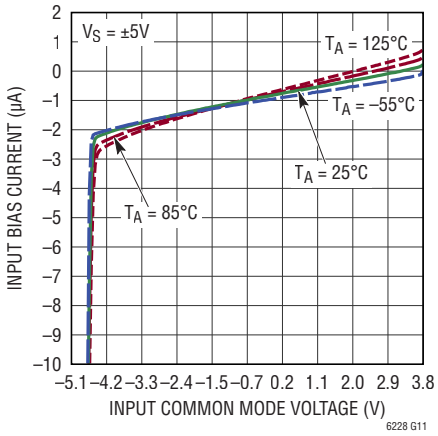

Rev. B

## TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

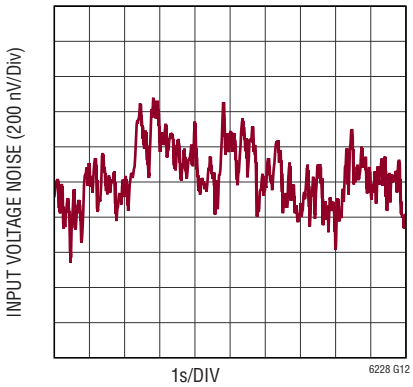
### Input Bias Current vs Input Common Voltage, Bias Cancellation Disabled



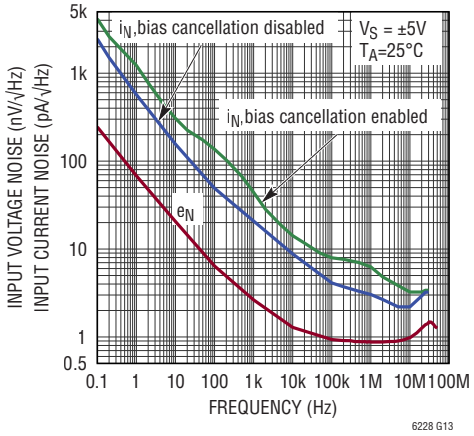

### Input Bias Current vs Input Common Mode Voltage, Bias Cancellation Enabled



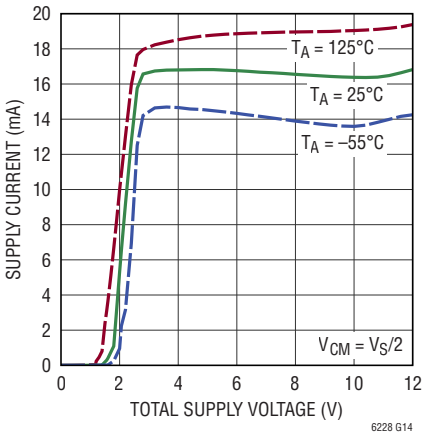

### 0.1Hz to 10Hz Voltage Noise



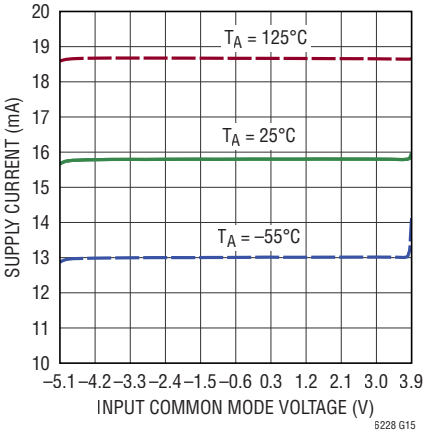

### Input Voltage Noise and Current Noise Spectral Densities vs Frequency



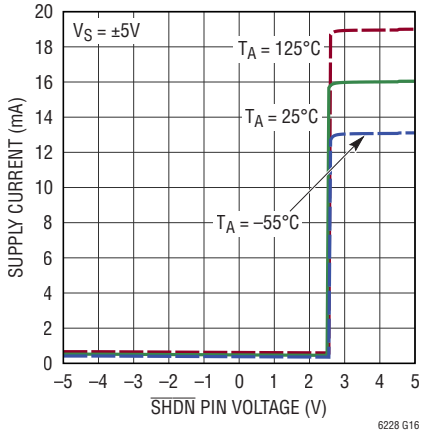

### Supply Current vs Supply Voltage



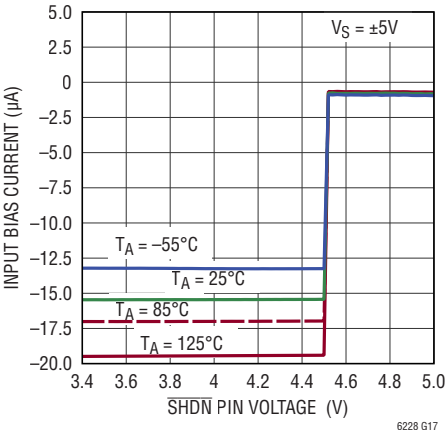

### Supply Current vs Input Common Mode Voltage



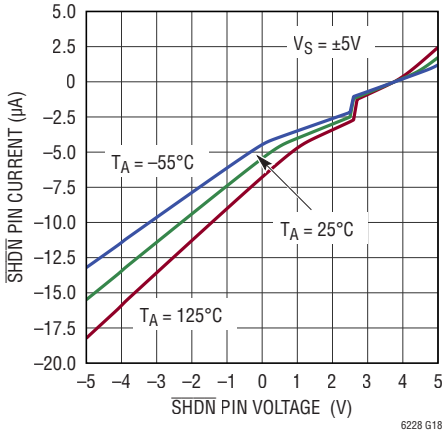

### Supply Current vs $\overline{SHDN}$ Pin Voltage




### Input Bias Current vs $\overline{SHDN}$ Pin Voltage



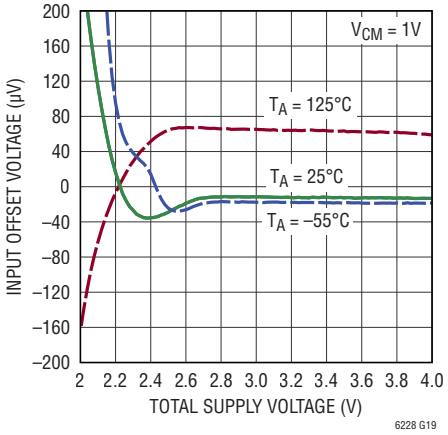

### $\overline{SHDN}$ Pin Current vs $\overline{SHDN}$ Pin Voltage



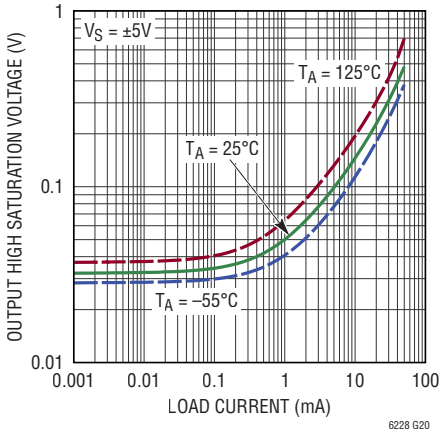
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_S$ = ±5V, $V_{CM}$ = 0V, $T_A$ = 25°C, unless otherwise noted.

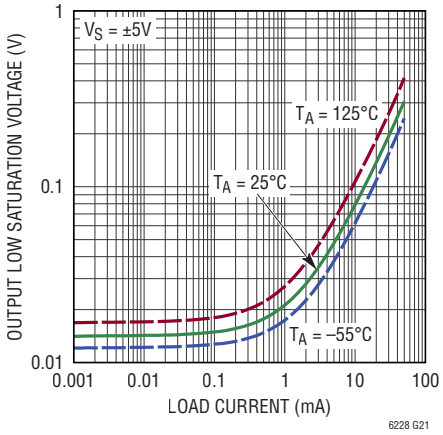
### Minimum Supply Voltage



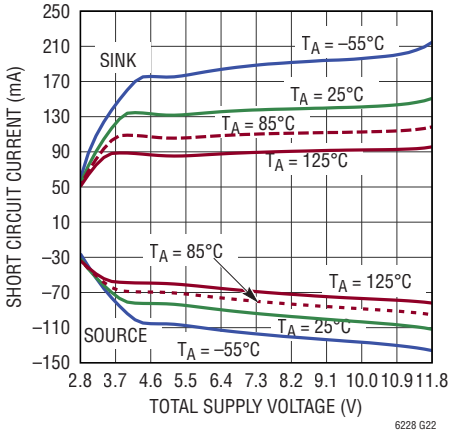

### Output Saturation Voltage vs Load Current (Output High)



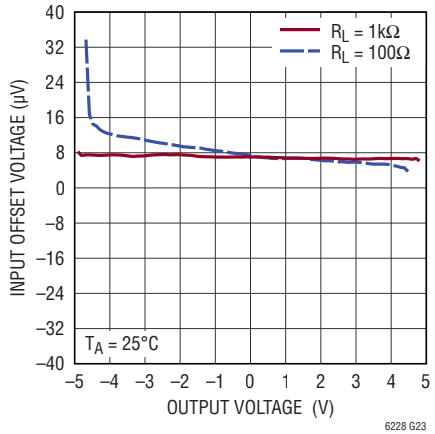

### Output Saturation Voltage vs Load Current (Output Low)



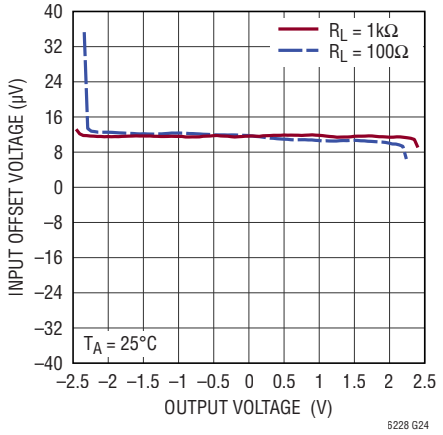

### Output Short Circuit vs Supply Voltage



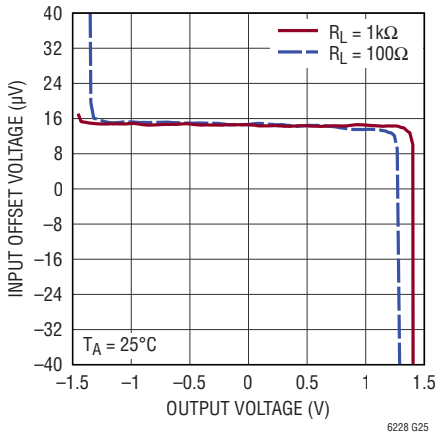

### Open Loop Gain, $V_S$ = ±5V



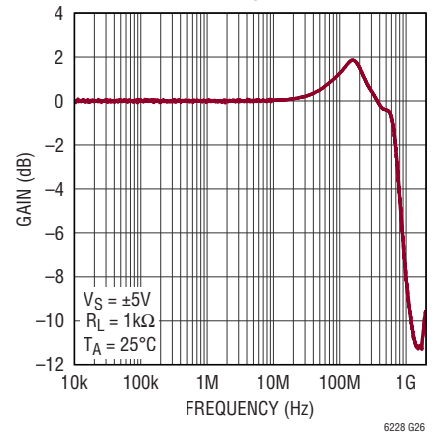

### Open Loop Gain, $V_S$ = ±2.5V



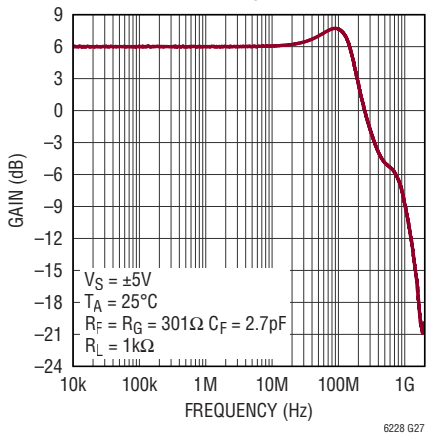

### Open Loop Gain, $V_S$ = ±1.5V




### Gain vs Frequency, $A_V$ = 1




### Gain vs Frequency, $A_V$ = 2

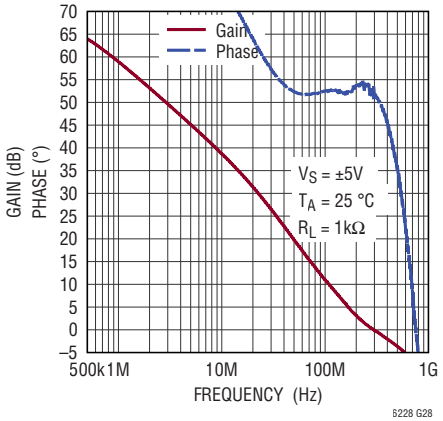



Rev. B

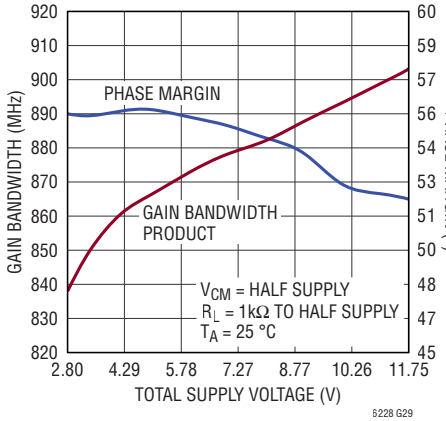
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 5V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

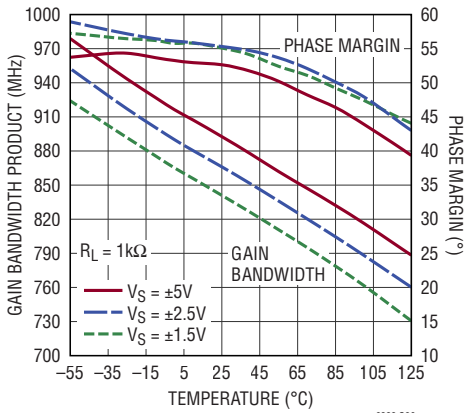
### Open Loop Gain and Phase vs Frequency



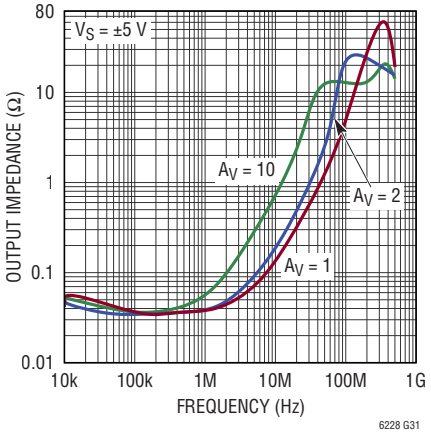

### Gain Bandwidth and Phase Margin vs Supply Voltage



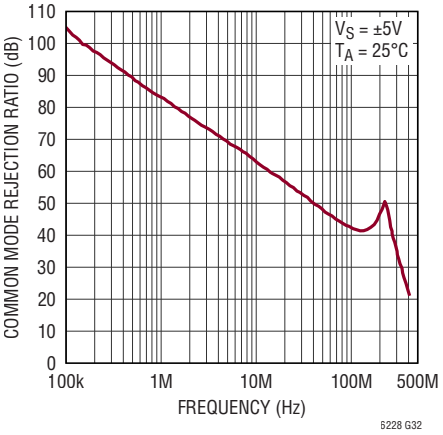

### Gain Bandwidth and Phase Margin vs Temperature



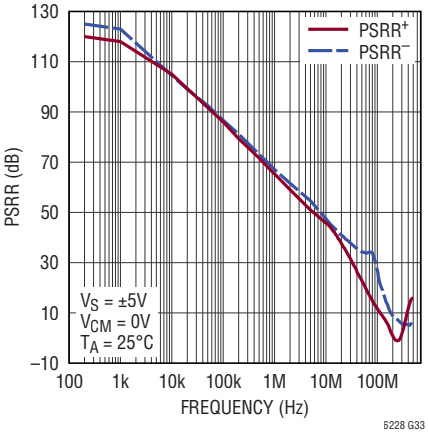

### Output Impedance vs Frequency



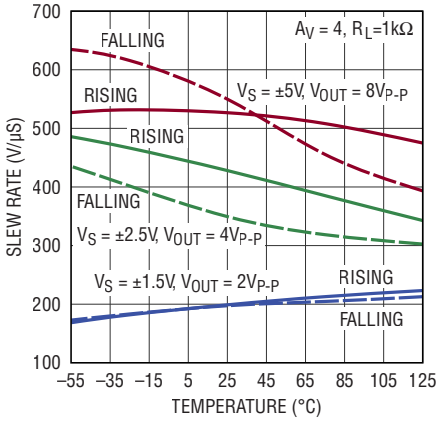

### Common Mode Rejection Ratio vs Frequency




### Power Supply Rejection Ratio vs Frequency

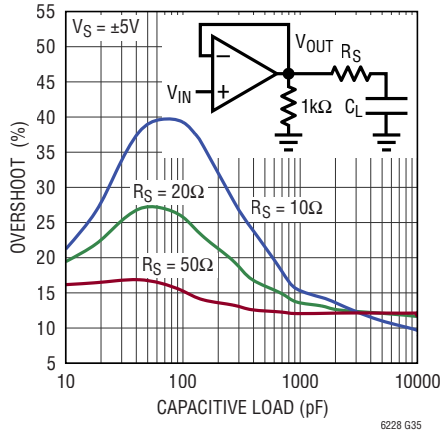



### Slew Rate vs Temperature

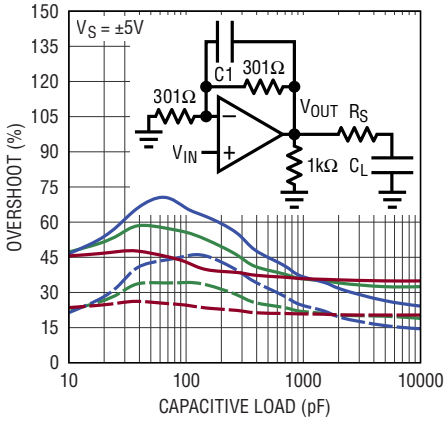



SLEW RATE MEASURED AT MIDDLE 2/3 OF OUTPUT

### Series Output Resistor vs Capacitive Load, $A_V = 1$

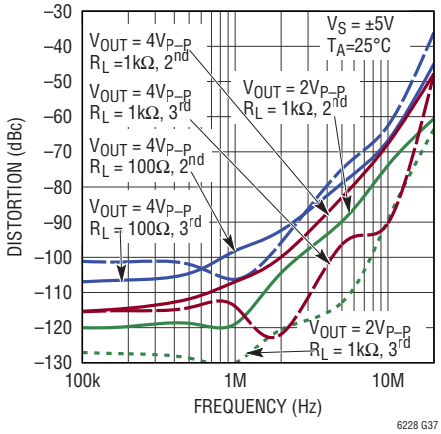



### Series Output Resistor vs Capacitive Load, $A_V = 2$

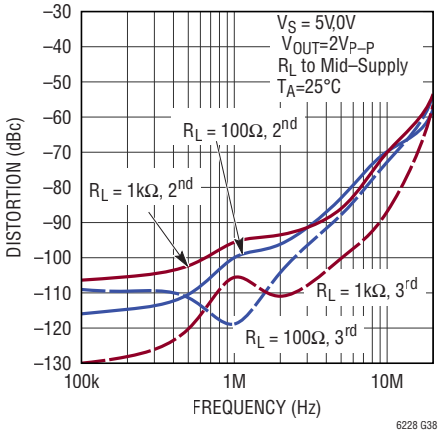


## TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

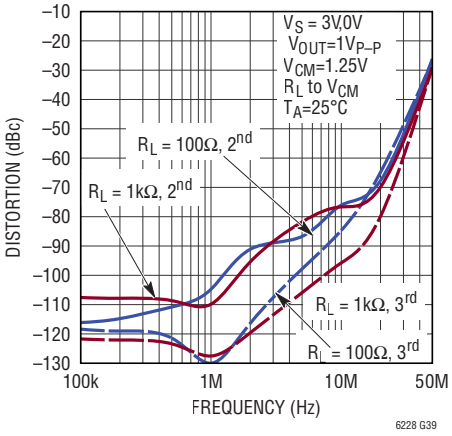
### Distortion vs Frequency, $A_V = 1$, ±5V Supply



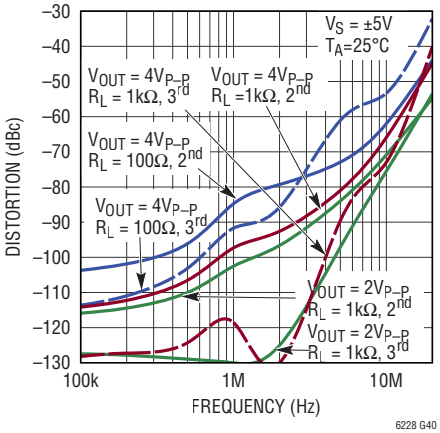

### Distortion vs Frequency, $A_V = 1$, 5V Supply



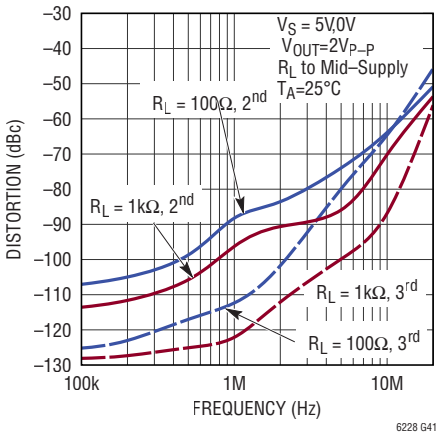

### Distortion vs Frequency, $A_V = 1$, 3V Supply



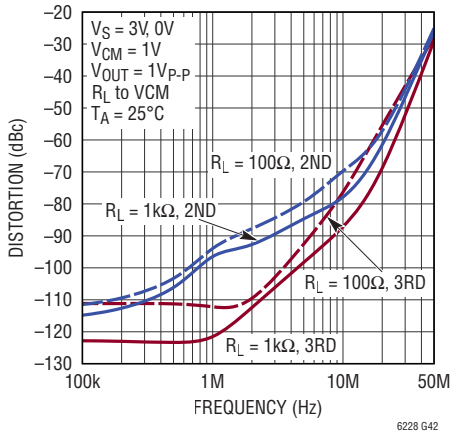

### Distortion vs Frequency, $A_V = 2$, ±5V Supply



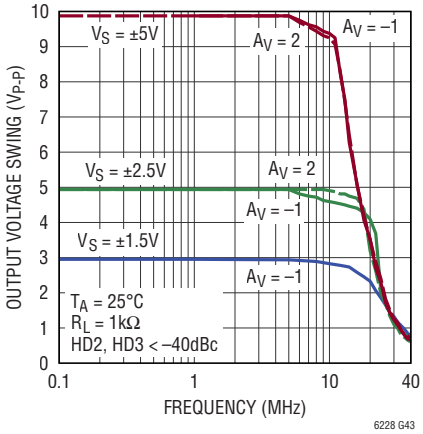

### Distortion vs Frequency, $A_V = 2$, 5V Supply



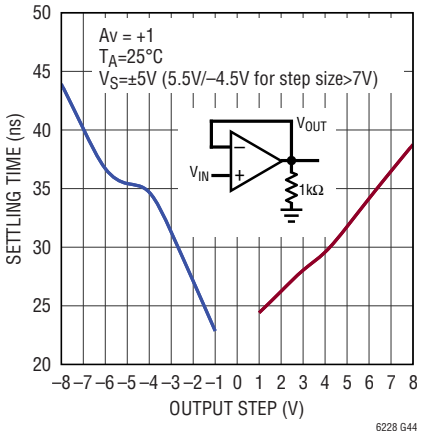

### Distortion vs Frequency, $A_V = 2$, 3V Supply



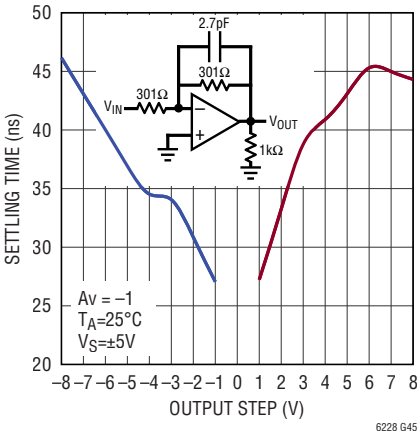

### Maximum Undistorted Output Signal vs Frequency




### 0.1% Settling Time vs Output Step (Non-Inverting)




### 0.1% Settling Time vs Output Step (Inverting)

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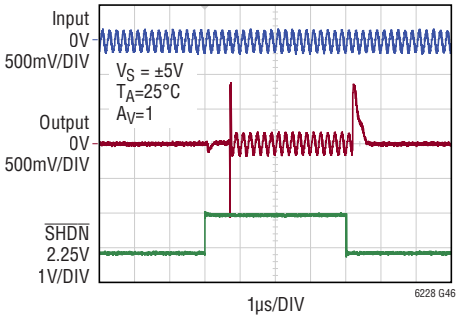
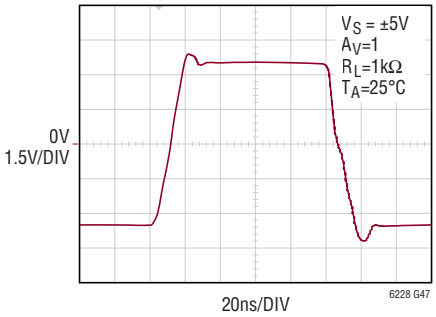
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_S$ = ±5V, $V_{CM}$ = 0V, $T_A$ = 25°C, unless otherwise noted.

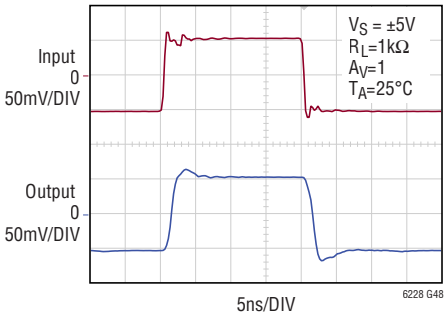
### $\overline{SHDN}$ Pin Response Time



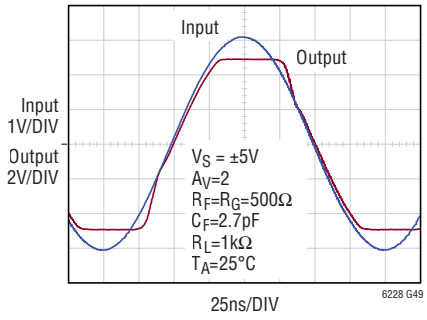

### Large Signal Response




### Small Signal Response




### Output Overdrive Recovery



## PIN FUNCTIONS

**FB (SOIC-8 Only):** Feedback Pin. Internally connected to OUT.

**+IN:** Non-Inverting Input of Amplifier. Valid input range is from $V^-$ to $V^+ – 1.2V$

**–IN:** Inverting Input of Amplifier. Valid input range is from $V^-$ to $V^+ – 1.2V$

**OUT:** Output of the Amplifier. Swings rail to rail and can typically source/sink more than 90mA of current.

**$\overline{SHDN}$:** Shutdown Pin (Active Low). Referenced to $V^+$. When taken 2.75V below $V^+$, the amplifier shuts down and enters low power mode, with the outputs in a high impedance state. When taken to within 350mV of $V^+$, bias current cancellation is enabled. When left floating, the amplifier is on but bias cancellation is not enabled.

**$V^+$:** Positive Supply to Amplifier. Valid range is from 2.8V to 11.75V when $V^-$ is 0V.

**$V^-$:** Negative Supply to Amplifier. Typically 0V. This can be made a negative voltage as long as $2.8V \leq (V^+ – V^-) \leq 11.75V$

# APPLICATIONS INFORMATION

## Circuit Description

The LTC6228/LTC6229 have an input signal range that extends from the negative power supply to 1.2V below the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage consists of PNP transistors Q1 and Q2. At the input stage, devices Q18 and Q19 act to cancel the bias current of the input pair when bias cancellation is enabled. Bootstrap transistor Q13 and R5 match the collector and emitter voltages of Q11 and Q12, thus enhancing gain by improving output impedance. By making the collector current of Q13 twice that of Q11 and Q12, the base currents of Q11 and Q12 do not contribute towards mismatch between the collector currents of Q9 and Q8. This improves DC accuracy. A pair of complementary common emitter stages, Q15 and Q14, enables the output to swing to either rail. The $\overline{SHDN}$ Interface block translates the $\overline{SHDN}$ signal into 2 signals, pwr_dn for powering down the device (by deactivating current sources I1 - I4) and putting the output in a high impedance state (by shorting the bases of Q15/Q14 to the supplies via M2 and M1), and disable_bias, which disables the input bias cancellation circuit, by shorting the base of Q19 to $V^-$ through M3.

## Input Bias Current

The LTC6228 family has an input bias current of approximately 16µA. For the LTC6228 and the LTC6229DD10, the input bias current can be reduced to under 2.5µA at room temperature when the $\overline{SHDN}$ pin voltage is taken to within 350mV of the positive power supply. This capability enables the input bias current cancellation circuitry, allowing the amplifiers to be used in DC applications involving source impedances.

When input bias current cancellation is enabled and the input common mode voltage is within approximately 500mV of $V^-$, the bias cancellation is no longer effective, because transistors Q18 and Q19 in Figure 1 enter saturation. The input bias current can then exceed 50µA or higher, which is more than the input bias current

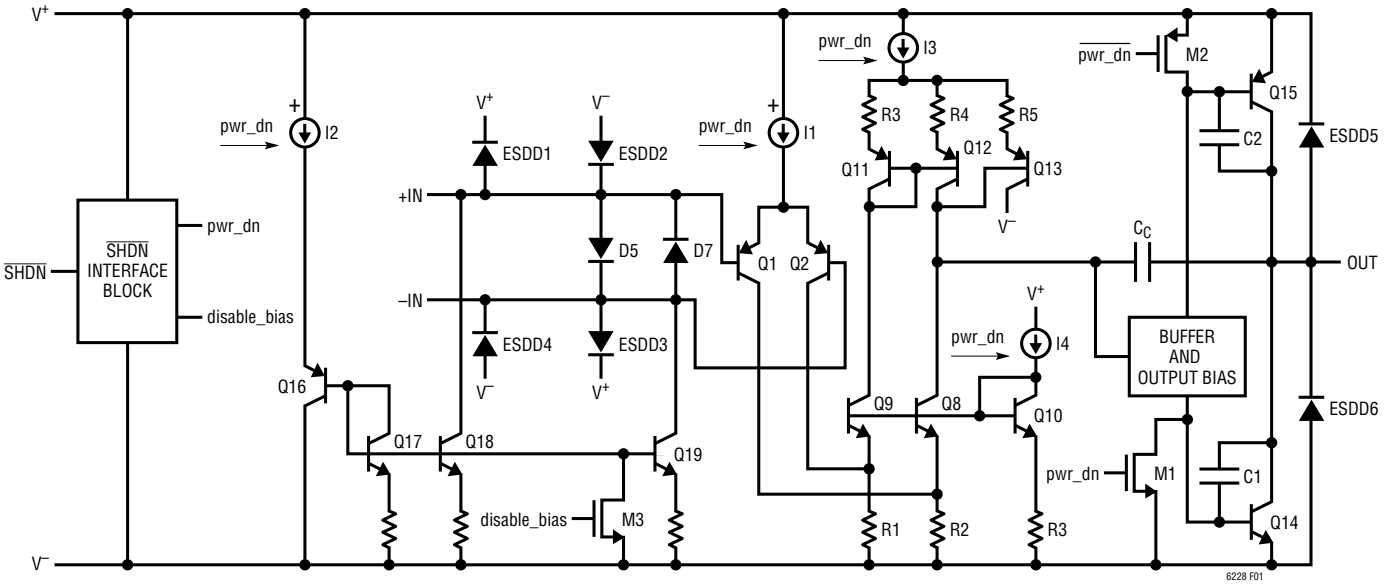



**Figure 1. LTC6228 Simplified Schematic Diagram**

## APPLICATIONS INFORMATION

without input bias cancellation. Additionally when input bias current cancellation is enabled, the current noise increases. The decision to use input bias cancellation should be made with the end application's specifications and conditions in mind.

If the $\overline{SHDN}$ pin is left floating, input bias cancellation is not enabled, which may be suitable for many applications.

### Output

The LTC6228 family has excellent output drive capability. The amplifiers can typically deliver more than 90mA of output current at a total supply of 10V, and can typically swing to within 320mV of the supply with load currents as high as 25mA. As the supply voltage to the amplifier decreases, the output current capability also decreases. Attention must be paid to keep the junction temperature of the IC below 150°C (refer to Power Dissipation section) when the output is in continuous short-circuit. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, extremely high currents will flow through those diodes, which may result in damage to the device.

### Input Protection

The LTC6228 has a pair of back to back diodes (D5 and D7) to prevent the emitter base breakdown of the input transistors and limit the differential input to ±700mV. Unlike many other high performance amplifiers, the bases of the input pair transistors Q1 and Q2 are not connected to the pins through internal resistors to limit input current, since doing so would cause the noise to increase. For instance, a 100Ω resistor in series with each input generates 1.8nV/$\sqrt{Hz}$ of noise, and the total amplifier noise voltage would rise from 0.88nV/$\sqrt{Hz}$ to 2nV/$\sqrt{Hz}$. If the input differential voltage exceeds ±0.7V, current conducted though the protection diodes D5 and D7 should be limited to under 10mA. This implies 25Ω of protection resistance per quarter volt (250mV) of overdrive beyond ±0.7V. In addition, the input and shutdown pins have reverse biased diodes connected to the supplies. The current in these diodes must be limited to under 10mA. The amplifiers should not be used as comparators or in other open loop applications.

### ESD

The LTC6228 family has reverse biased ESD protection diodes on all inputs as shown in Figure 1. There is an additional clamp between the positive and negative supplies that further protects the device during ESD strikes.

Hot plugging of the device into a powered socket should be avoided since this can trigger the clamp resulting in larger currents flowing between the supply pins.

### Capacitive Loads

Because the LTC6228/LTC6229 is designed for high bandwidth applications, the output has not been designed to drive capacitive loads directly. Load capacitance at the output creates a non-dominant pole in the open loop frequency response, worsening the phase margin. When driving capacitive loads, a resistor of 10Ω to 100Ω should be connected between the amplifier output and the capacitive load to avoid ringing or oscillation. The feedback should be taken directly from the amplifier output. Higher voltage gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth. The graphs titled Series Output Resistor vs Capacitive Load demonstrate the transient response of the amplifier when driving capacitive loads with various series resistors.

### Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the non-dominant pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example if the amplifier is set up in a gain of +2 configuration with gain and feedback resistors of 1k, a parasitic capacitance of 7pF (device + PC board) at the amplifier's

## APPLICATIONS INFORMATION

inverting input will cause the part to oscillate, due to the pole formed at 45MHz. Adding a capacitor of 7pF across the feedback resistor as shown in Figure 2 will eliminate any ringing or oscillation. In general, if the resistive feedback network results in a pole whose frequency lies within the closed loop bandwidth of the amplifier, a capacitor can be added in parallel with the feedback resistor to introduce a zero whose frequency is close to the frequency of the pole, improving stability.

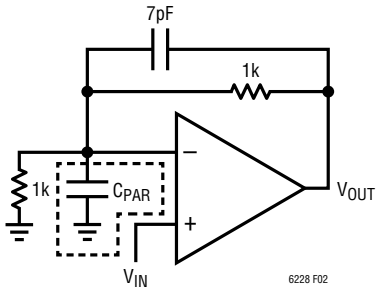



**Figure 2. 7pF Feedback Cancels Parasitic Pole**

For high speed designs, minimizing parasitic inductance is important. The use of capacitors where the electrodes are terminated on the long side instead of the short side (for example the use of 0306 instead of 0603 components) can help in this regard.

### Shutdown

The LTC6228/LTC6229 have shutdown pins ($\overline{SHDN}$), which disable the amplifiers and reduce the quiescent current per channel to approximately 500µA. The $\overline{SHDN}$ pin needs to be driven at least 2.75V below $V^+$ to disable amplifier operation. For total supply voltages of 5V and or less, the amplifier can be disabled at a pin voltage of $V^+$ – 2.65V. During shutdown, the output transistors Q15 and Q14 in Figure 1 are placed into a high impedance state. If $\overline{SHDN}$ is left floating, the pin is internally biased to 1.2V below the positive supply, and the amplifier remains on.

### Power Dissipation

Care must be taken to ensure that the junction temperature of the die does not exceed 150°C.

The junction temperature, $T_J$, is calculated from the ambient temperature, $T_A$, power dissipation, $P_D$, and thermal resistance, $\theta_{JA}$:

$$T_J = T_A + (P_D \bullet \theta_{JA}).$$

The power dissipation in the IC is a function of the supply voltage, output voltage and load resistance. For a given supply voltage with output load connected to mid supply, the worst-case power dissipation $P_{D(MAX)}$ occurs when the supply current is maximum and the output voltage at half of either supply voltage for a given load resistance. $P_{D(MAX)}$ is approximately (since $I_S$ actually changes with output load current) given by:

$$P_{D(MAX)} = (2 \bullet V_S \bullet I_{S(MAX)}) + (V_S/2)^2/R_L$$

Example: For an LTC6228 in a 6-lead DC package operating on ±5V supplies and driving a 500Ω load to ground, the worst-case power dissipation is approximately given by $P_{D(MAX)}/Amp = (10 \bullet 19mA) + (5)^2/500 = 240mW$.

At the Absolute Maximum ambient operating temperature, the junction temperature under these conditions will be:

$$T_J = T_A + (P_D \bullet \theta_{JA}) = 125 + 0.24 \bullet 80 = 144.2°C$$

which is slightly less than the absolute maximum junction temperature for the LTC6228/LTC6229.

Refer to the Pin Configuration section for thermal resistances of various packages

### Board Layout and Bypass Capacitors

High speed and RF board layout techniques should be used due to the very high speeds of the signals involved. For the LTC6228 SOIC-8 package option, the feedback should be taken from the FB pin rather than from the output pin, to reduce signal trace length.

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Stray capacitances at the –IN and +IN pins should be made as low as possible to reduce stability degradation. For example, ground or supply planes on a PCB should not encompass the areas just beneath the input pins.

For single supply applications, it is recommended that high quality 0.1µF||1000pF ceramic bypass capacitors be placed directly between each $V^+$ pin and its closest $V^–$ pin with short connections. The $V^–$ pins (including the Exposed Pad) should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that additional high quality 0.1µF||1000pF ceramic capacitors be used to bypass $V^+$ pins to ground and $V^–$ pins to ground, again with minimal routing.

### Noise Considerations

The ultralow input referred voltage noise of 0.88nV/$\sqrt{Hz}$ is equivalent to that of a 47Ω resistor at room temperature. As with all BJT input amplifiers, lowering input referred voltage noise is achieved by increasing the collector current of the input differential pair, which increases the input referred current noise.

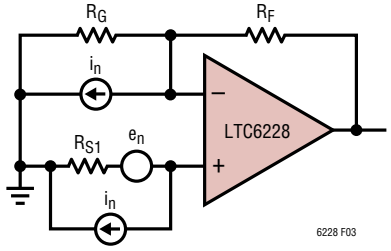



**Figure 3.**

Figure 3 shows the LTC6228 in a typical gain configuration.

As can be seen, the input referred noise spectral density of the gain stage ($e_T$) can be calculated by the following equations:

$$e_T^2 = \underbrace{e_n^2}_{\substack{\text{opamp}\\ \text{voltage}\\ \text{noise}}} + \underbrace{i_n^2 R_{EQ}^2}_{\substack{\text{opamp}\\ \text{current}\\ \text{noise}}} + \underbrace{4KTR_{EQ}}_{\substack{\text{resistor}\\ \text{thermal}\\ \text{noise}}}$$

Where

$$R_{EQ} = R_{S1} + R_G||R_F$$

Op amp input referred noise dominates the input referred noise of the gain stage when

$$R_{EQ} << e_n^2/4KT$$

Resistor noise dominates the input referred noise of the gain stage when

$$R_{EQ} >> e_n^2/4KT \text{ and } R_{EQ} << 4KT/i_n^2$$

Op amp input referred current noise dominates the input referred noise when

$$R_{EQ} >> 4kT/i_n^2$$

To summarize, initially $e_n$ dominates for low resistance values. As the resistance increased, resistor noise starts to dominate, then on further increase current noise dominates.

With an input referred voltage noise spectral density of 0.88nV/Hz and an input referred current noise of 3pA/Hz (bias cancellation disabled), it is easy to see that the gain stage's input referred noise is dominated by op amp voltage noise when $R_{EQ}$ << 47Ω and by resistor noise when

$$55Ω << R_{EQ} << 1.8kΩ.$$

Above an $R_{EQ}$ of 1.8kΩ, input referred current noise dominates.

### Distortion/Noise Trade-Off

As evident from the previous section, gain stage noise can be reduced by reducing $R_{EQ}$. However, reducing $R_{EQ}$, by reducing $R_F$ and $R_G$, has its disadvantages. In addition to increasing power dissipation in the presence of large output signals, the use of smaller resistors for a given gain results in increased distortion, because the internal nonlinearities of the op amp worsen with increasing load current. In addition, smaller resistors decrease op amp gain and hence can affect bandwidth. The disadvantage, however of making the resistors too large is that parasitic capacitance can start to affect the gain at high frequencies. Hence when designing a system using the LTC6228, it is recommended that the resistor values be limited only by the system noise requirements, with the caveat that the effect of the impedances parasitic capacitances shouldn't affect the gain below the intended bandwidth. For example, for a feedback resistor of 5k, a parasitic capacitor of 400fF will impact gain at frequencies above 79MHz.

# TYPICAL APPLICATIONS

### 18-Bit High Speed ADC Driver

The ultralow noise and distortion performance of the LTC6228 makes it an excellent candidate for driving high speed high resolution ADCs with fast, large amplitude signals. Figure 4 shows a pair of LTC6228s driven by a differential input, driving an LTC2387-18, a 15Msps, 18-bit ADC. Figure 5 shows an FFT obtained with a –1dBFS, 1MHz input signal. The obtained SNR is 93.4dB, better than the LTC2387-18's guaranteed SNR of 93dB, and close to its typical value of 95.7dB. Spurious free dynamic range is an excellent 95dB, close to the LTC2387-18's guaranteed SFDR of 97dB.

### High Speed Low Voltage Low Noise Instrumentation Amplifier

Figure 6 shows a three op amp instrumentation amplifier with a gain of 41V/V which can operate on a wide range of supply voltage. An RC snubber is used at the common terminal of the 30Ω gain setting resistors to reduce the effects of any board induced layout coupling from the output of one amplifier to the negative input of the other. Figure 7 shows the measured frequency response of the instrumentation amplifier for a load of 1kΩ. Figure 8 shows the measured CMRR of the instrumentation amplifier, and Figure 9 shows the transient response for a 50mV$_{P-P}$ input square wave applied to the positive input, with the negative input grounded. The total supply voltage was 3.3V. The extremely low offset voltage and low 1/f noise at the LTC6229 inputs allow for wide band instrumentation amplifier operation, down to DC. Note, the bias currents of the LTC6229 are higher than might appear in a traditional low speed instrumentation amplifier. High speed instrumentation such as in Figure 6 assume a correspondingly low enough impedance excitation.

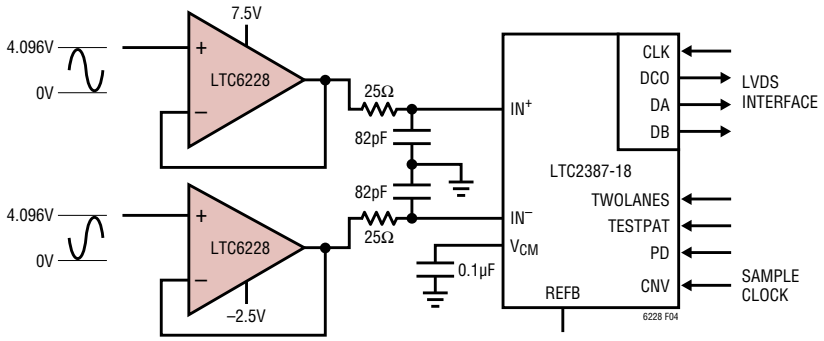



**Figure 4. High Speed Driver for 18-Bit ADC**

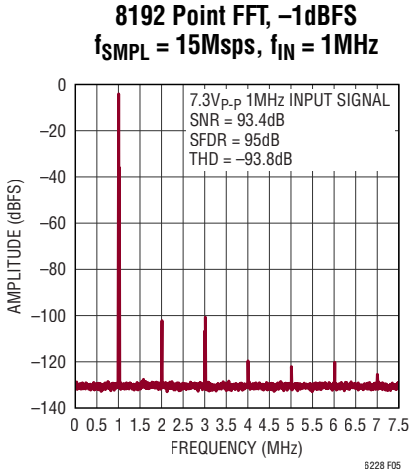



**Figure 5. Measured Performance of LTC6228 Based Driver Driving the LTC2387-18**

## TYPICAL APPLICATIONS

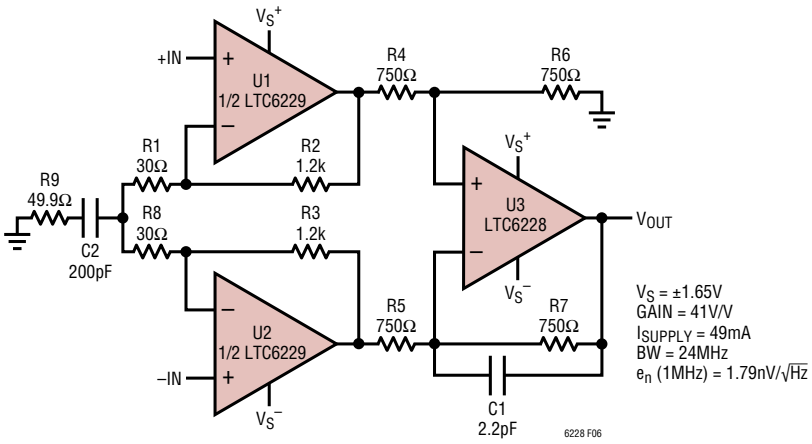



**Figure 6. High Speed Low Voltage Low Noise Instrumentation Amplifier**

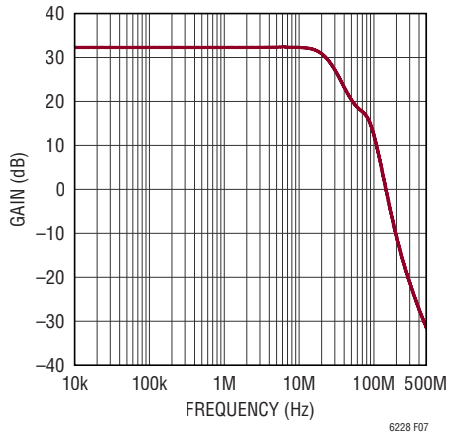



**Figure 7. Instrumentation Amplifier Frequency Response**

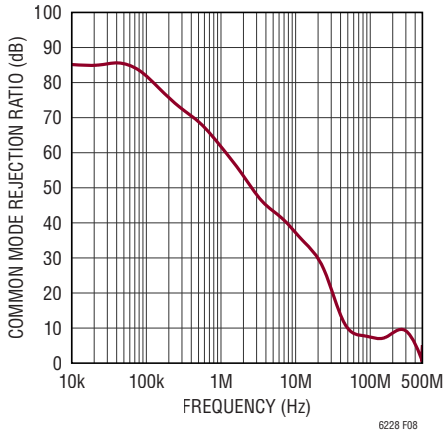



**Figure 8. Instrumentation Amplifier CMRR**

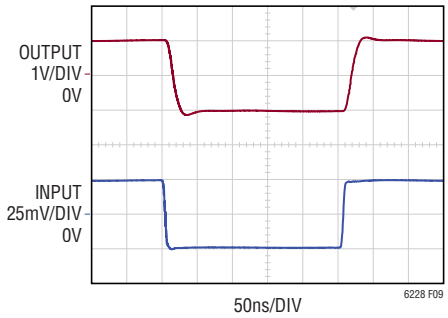



**Figure 9. Transient Response**

# TYPICAL APPLICATIONS

### Wideband Differential to Single-Ended Converter

The combination of high slew rate and bandwidth enables the LTC6228 to be used as a translator for large signals at high frequencies.

Figure 10 shows the implementation of a wide band, differential to single-ended converter with a gain of –6dB using just one LTC6228. Figure 11 shows the frequency response of the circuit for a differential input of $2V_{P-P}$. The bandwidth obtained was 50MHz. The common mode gain of the driver is shown in Figure 12, and is limited by the matching between the resistors in the circuit. Figure 13 shows the response of the driver to a $1V_{P-P}$ differential square wave signal.

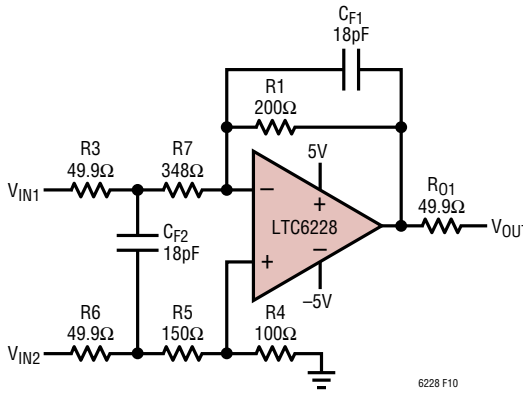



**Figure 10. Wideband Differential to Single-Ended Converter**

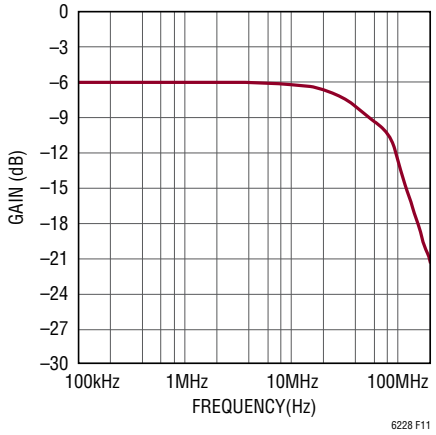



**Figure 11. Frequency Response of Differential to Single-Ended Converter**

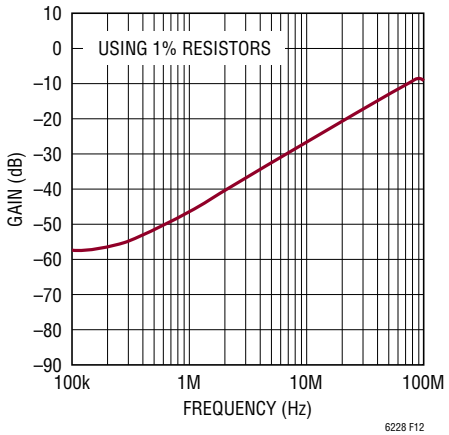



**Figure 12. Common Mode Gain vs Frequency**

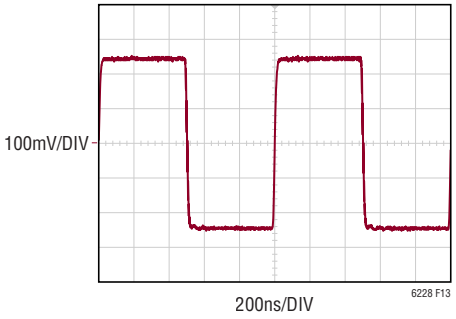
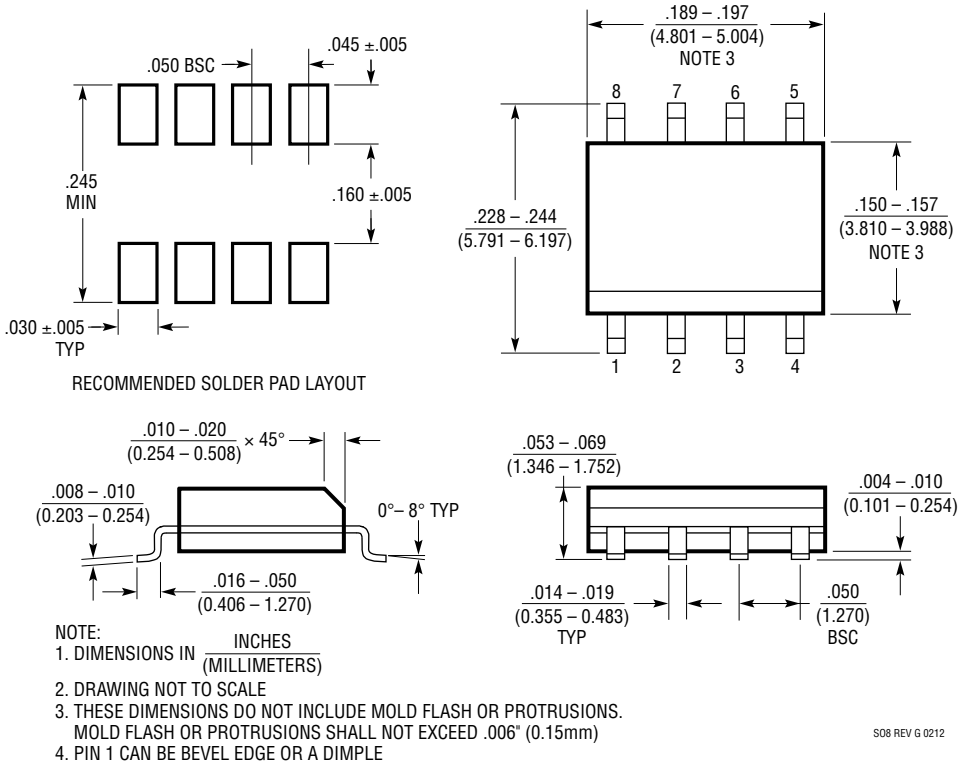



**Figure 13. Pulse Response of the Differential to Single-Ended Converter**

# PACKAGE DESCRIPTION

**S8 Package**
**8-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610 Rev G)

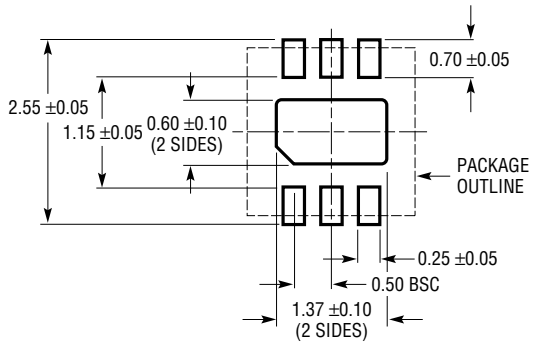



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

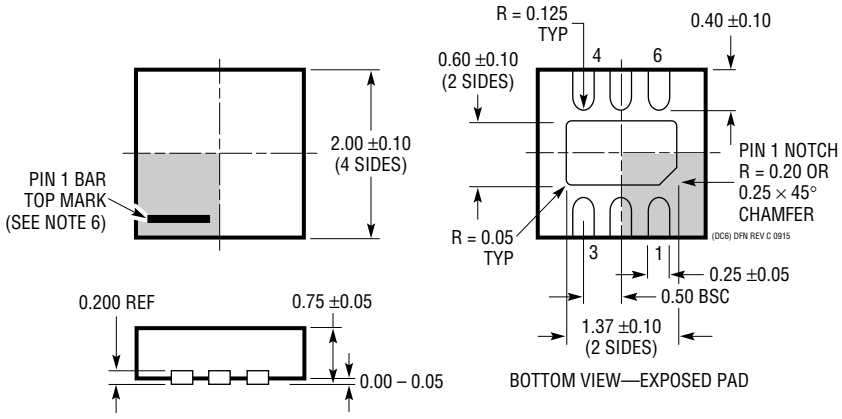
S08 REV G 0212

# PACKAGE DESCRIPTION

**DC6 Package**
**6-Lead Plastic DFN (2mm × 2mm)**
(Reference LTC DWG # 05-08-1703 Rev C)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

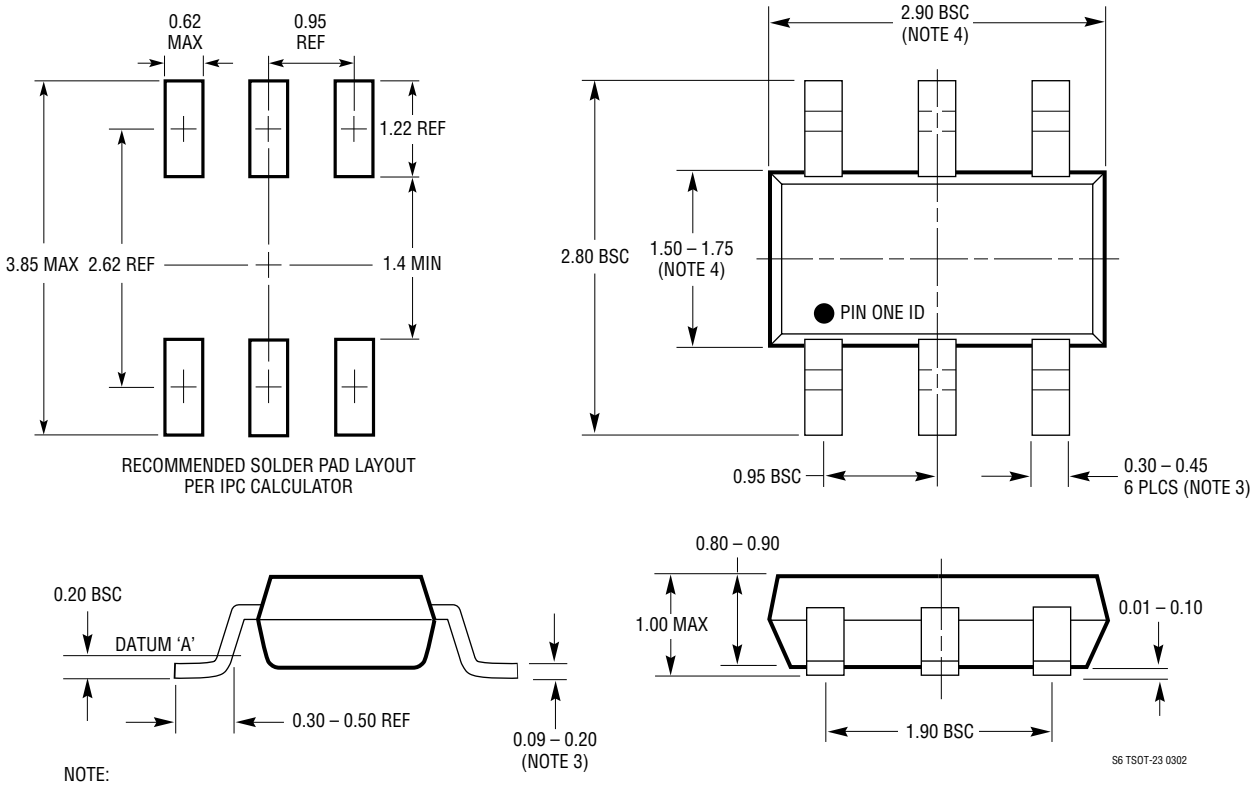



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

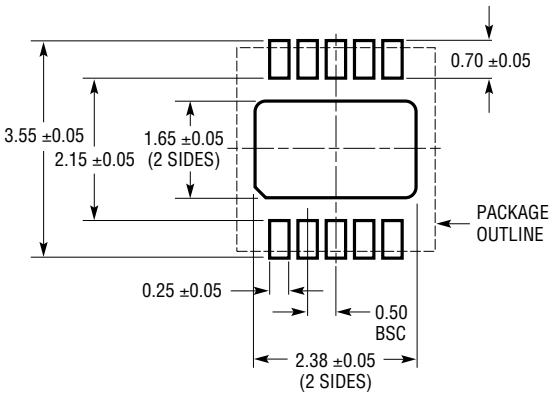
**S6 Package**
**6-Lead Plastic TSOT-23**
(Reference LTC DWG # 05-08-1636)



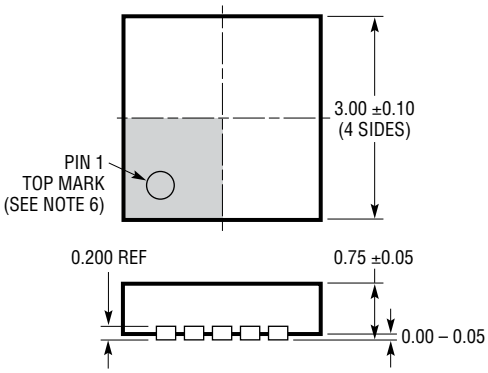

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

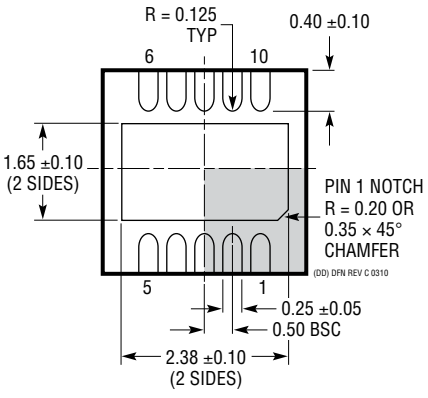
# PACKAGE DESCRIPTION

**DD Package**
**10-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1699 Rev C)




**RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS



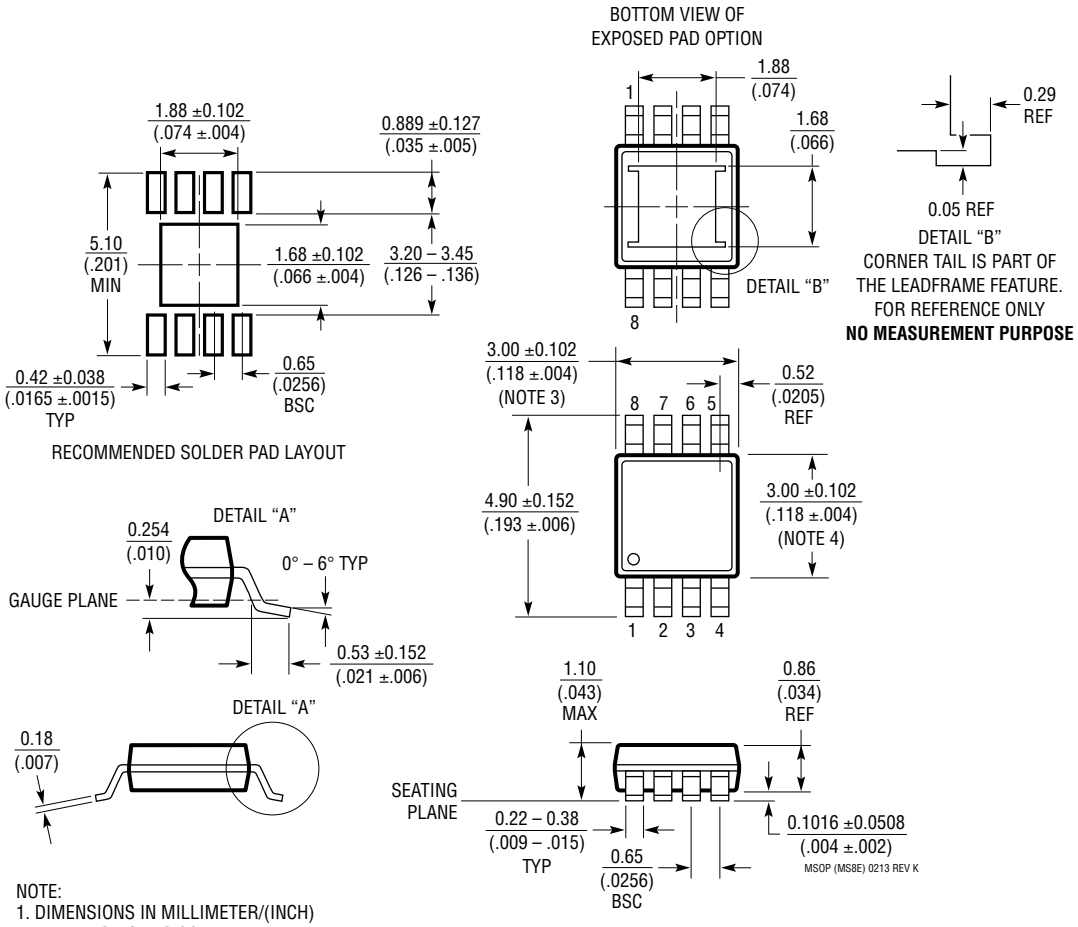




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**MS8E Package**
**8-Lead Plastic MSOP, Exposed Die Pad**
(Reference LTC DWG # 05-08-1662 Rev K)




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 09/19 | Added LTC6229 to data sheet. | All |
| B | 03/20 | Corrected wording and values on various pages. | 1, 9, 17, 20, 30 |