Dual 50MHz, Low Noise, Rail-to-Rail, CMOS Op Amp

FEATURES

- **Input Bias Current: 1pA (Typ at 25°C)**
- **Low Offset Voltage: 100µV Max**
- **Low Offset Drift: 2.5µV/°C Max**
- 0.1Hz to 10Hz Noise: 1.5µV$_{P-P}$
- Slew Rate: 40V/µs
- Gain Bandwidth Product: 50MHz
- Output Swings Rail-to-Rail
- Supply Operation:
  - 2.8V to 6V LTC6244
  - 2.8V to ±5.25V LTC6244HV
- Low Input Capacitance: 2.1pF
- Available in 8-Pin MSOP and Tiny DFN Packages

APPLICATIONS

- Photodiode Amplifiers
- Charge Coupled Amplifiers
- Low Noise Signal Processing
- Active Filters
- Medical Instrumentation
- High Impedance Transducer Amplifier

DESCRIPTION

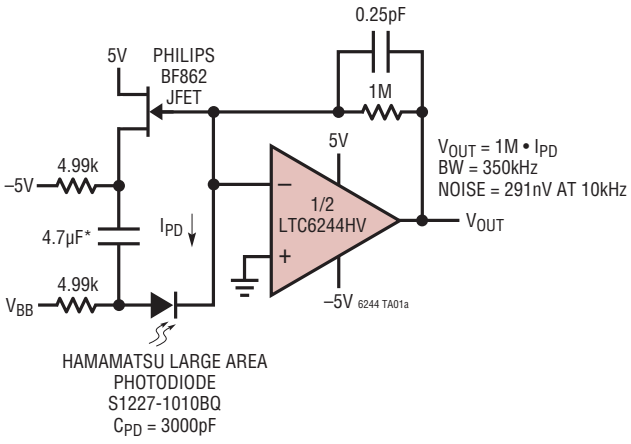
The LTC®6244 is a dual high speed, unity-gain stable CMOS op amp that features a 50MHz gain bandwidth, 40V/µs slew rate, 1pA of input bias current, low input capacitance and rail-to-rail output swing. The 0.1Hz to 10Hz noise is just 1.5µV$_{P-P}$ and 1kHz noise is guaranteed to be less than 12nV/$\sqrt{Hz}$. This excellent AC and noise performance is combined with wide supply range operation, a maximum offset voltage of just 100µV and drift of only 2.5µV/°C, making it suitable for use in many fast signal processing applications, such as photodiode amplifiers.

This op amp has an output stage that swings within 35mV of either supply rail to maximize the signal dynamic range in low supply applications. The input common mode range extends to the negative supply. It is fully specified on 3V and 5V, and an HV version guarantees operation on supplies of ±5V.

The LTC6244 is available in the 8-pin MSOP, and for compact designs, it is packaged in the tiny dual fine pitch lead free (DFN) package.

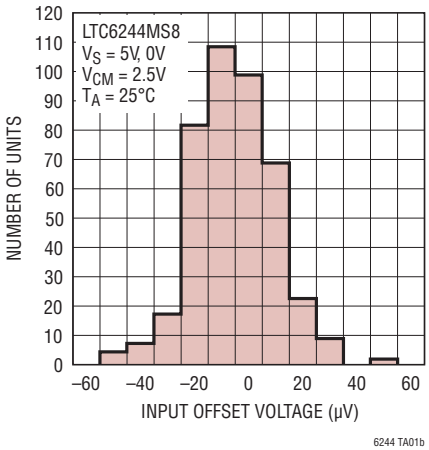
TYPICAL APPLICATION

Very Low Noise Large Area Photodiode



* CAN BE MICROPHONIC, FILM, X7R, IF NEEDED.

V_{OS} Distribution



ABSOLUTE MAXIMUM RATINGS (Note 1)

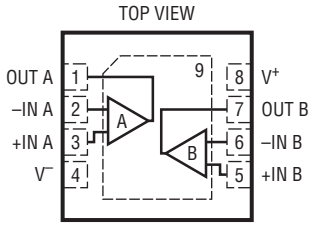
Total Supply Voltage (V^+ to V^-)
- LTC6244 ..... 7V
- LTC6244HV 12V

Input Voltage ..... (V^+ + 0.3V) to (V^- – 0.3V)
Input Current ..... ±10mA
Output Short Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range
- LTC6244C ..... –40°C to 85°C
- LTC6244I ..... –40°C to 85°C
- LTC6244H ..... –40°C to 125°C

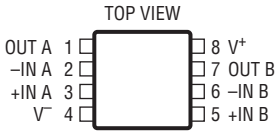
Specified Temperature Range (Note 3)
- LTC6244C ..... 0°C to 70°C
- LTC6244I ..... –40°C to 85°C
- LTC6244H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) CONNEECTED TO V^-
(PCB CONNECTION OPTIONAL)



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6244CDD#PBF	LTC6244CDD#TRPBF	LCCF	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6244HVCDD#PBF	LTC6244HVCDD#TRPBF	LCGD	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6244IDD#PBF	LTC6244IDD#TRPBF	LCCF	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6244HVIDD#PBF	LTC6244HVIDD#TRPBF	LCGD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6244HDD#PBF	LTC6244HDD#TRPBF	LCCF	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6244HVHDD#PBF	LTC6244HVHDD#TRPBF	LCGD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6244CMS8#PBF	LTC6244CMS8#TRPBF	LTCCM	8-Lead Plastic MSOP	0°C to 70°C
LTC6244HVCMS8#PBF	LTC6244HVCMS8#TRPBF	LTCGF	8-Lead Plastic MSOP	0°C to 70°C
LTC6244IMS8#PBF	LTC6244IMS8#TRPBF	LTCCM	8-Lead Plastic MSOP	–40°C to 85°C
LTC6244HVIMS8#PBF	LTC6244HVIMS8#TRPBF	LTCGF	8-Lead Plastic MSOP	–40°C to 85°C
LTC6244HMS8#PBF	LTC6244HMS8#TRPBF	LTCCM	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

(LTC6244C/I, LTC6244HVC/I) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	MS8 Package			40	100	µV
		0°C to 70°C	●			225	µV
		–40°C to 85°C	●			300	µV
		DD Package			100	650	µV
		0°C to 70°C	●			800	µV
		–40°C to 85°C	●			950	µV
	V_{OS} Match Channel-to-Channel (Note 5)	MS8 Package			40	160	µV
		0°C to 70°C	●			275	µV
		–40°C to 85°C	●			325	µV
		DD Package			150	800	µV
		0°C to 70°C	●			900	µV
		–40°C to 85°C	●			1.1	mV
TC V_{OS}	Input Offset Voltage Drift, MS8 (Note 6)		●		0.7	2.5	µV/°C
I_B	Input Bias Current (Notes 4, 7)				1		pA
			●			75	pA
I_{OS}	Input Offset Current (Notes 4, 7)				0.5		pA
			●			75	pA
	Input Noise Voltage	0.1Hz to 10Hz			1.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			8	12	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density (Note 8)				0.56		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode			10^{12}		Ω
C_{IN}	Input Capacitance	f = 100kHz					
	Differential Mode				3.5		pF
	Common Mode				2.1		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	0		3.5	V
CMRR	Common Mode Rejection	0V ≤ V_{CM} ≤ 3.5V	●	74	105		dB
	CMRR Match Channel-to-Channel (Note 5)		●	72	100		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 4V					
		R_L = 10k to V_S/2		1000	2500		V/mV
		0°C to 70°C	●	600			V/mV
		–40°C to 85°C	●	450			V/mV
		V_O = 1.5V to 3.5V					
		R_L = 1k to V_S/2		300	1000		V/mV
		0°C to 70°C	●	200			V/mV
		–40°C to 85°C	●	150			V/mV
V_{OL}	Output Voltage Swing Low (Note 9)	No Load	●		15	35	mV
		I_{SINK} = 1mA	●		40	75	mV
		I_{SINK} = 5mA	●		150	300	mV
V_{OH}	Output Voltage Swing High (Note 9)	No Load	●		15	35	mV
		I_{SOURCE} = 1mA	●		45	75	mV
		I_{SOURCE} = 5mA	●		175	325	mV
PSRR	Power Supply Rejection	V_S = 2.8V to 6V, V_{CM} = 0.2V	●	75	105		dB
	PSRR Match Channel-to-Channel (Note 5)		●	73	100		dB
	Minimum Supply Voltage (Note 10)		●	2.8			V
I_{SC}	Short-Circuit Current		●	25	35		mA
I_S	Supply Current per Amplifier		●		6.25	7.4	mA

ELECTRICAL CHARACTERISTICS

(LTC6244C/I, LTC6244HVC/I) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GBW	Gain Bandwidth Product	Frequency = 100kHz, R_L = 1kΩ	●	35	50		MHz
SR	Slew Rate (Note 11)	A_V = –2, R_L = 1kΩ	●	18	35		V/µs
FPBW	Full Power Bandwidth (Note 12)	V_{OUT} = $3V_{P-P}$, R_L = 1kΩ	●	1.9	3.7		MHz
t_s	Settling Time	V_{STEP} = 2V, A_V = –1, R_L = 1kΩ, 0.1%			535		ns

(LTC6244C/I, LTC6244HVC/I) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V, V_{CM} = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	MS8 Package			40	175	µV
		0°C to 70°C	●			250	µV
		–40°C to 85°C	●			325	µV
		DD Package			100	650	µV
		0°C to 70°C	●			800	µV
		–40°C to 85°C	●			950	µV
	V_{OS} Match Channel-to-Channel (Note 5)	MS8 Package			40	200	µV
		0°C to 70°C	●			300	µV
		–40°C to 85°C	●			350	µV
		DD Package			150	800	µV
		0°C to 70°C	●			900	µV
		–40°C to 85°C	●			1.1	mV
I_B	Input Bias Current (Notes 4, 7)				1		pA
			●			75	pA
I_{OS}	Input Offset Current (Notes 4, 7)				0.5		pA
			●			75	pA
	Input Noise Voltage	0.1Hz to 10Hz			1.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			8	12	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density (Note 8)				0.56		$fA/\sqrt{Hz}$
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	0		1.5	V
CMRR	Common Mode Rejection	0V ≤ V_{CM} ≤ 1.5V	●	70	105		dB
	CMRR Match Channel-to-Channel (Note 5)		●	68	100		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 2V					
		R_L = 10k to V_S/2		200	800		V/mV
		0°C to 70°C	●	100			V/mV
		–40°C to 85°C	●	85			V/mV
V_{OL}	Output Voltage Swing Low (Note 9)	No Load	●		12	30	mV
		I_{SINK} = 1mA	●		45	110	mV
V_{OH}	Output Voltage Swing High (Note 9)	No Load	●		12	30	mV
		I_{SOURCE} = 1mA	●		50	110	mV
PSRR	Power Supply Rejection	V_S = 2.8V to 6V, V_{CM} = 0.2V	●	75	105		dB
	PSRR Match Channel-to-Channel (Note 5)		●	73	100		dB
	Minimum Supply Voltage (Note 10)		●	2.8			V
I_{SC}	Short-Circuit Current		●	8	15		mA

ELECTRICAL CHARACTERISTICS

(LTC6244C/I, LTC6244HVC/I) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V, V_{CM} = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current per Amplifier		●		4.8	5.8	mA
GBW	Gain Bandwidth Product	Frequency = 100kHz, R_L = 1kΩ	●	35	50		MHz

(LTC6244HVC/I) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, 0V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	MS8 Package			50	220	µV
		0°C to 70°C	●			275	µV
		–40°C to 85°C	●			375	µV
		DD Package			100	700	µV
		0°C to 70°C	●			800	µV
		–40°C to 85°C	●			1050	µV
	V_{OS} Match Channel-to-Channel (Note 5)	MS8 Package			50	250	µV
		0°C to 70°C	●			325	µV
		–40°C to 85°C	●			400	µV
		DD Package			150	900	µV
		0°C to 70°C	●			1000	µV
		–40°C to 85°C	●			1100	µV
TC V_{OS}	Input Offset Voltage Drift, MS8 (Note 6)		●		0.7	2.5	µV/°C
I_B	Input Bias Current (Notes 4, 7)				1		pA
			●			75	pA
I_{OS}	Input Offset Current (Notes 4, 7)				0.5		pA
			●			75	pA
	Input Noise Voltage	0.1Hz to 10Hz			1.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			8	12	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density (Note 8)				0.56		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode			10^{12}		Ω
C_{IN}	Input Capacitance	f = 100kHz					
	Differential Mode				3.5		pF
	Common Mode				2.1		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–5		3.5	V
CMRR	Common Mode Rejection	–5V ≤ V_{CM} ≤ 3.5V	●	80	105		dB
	CMRR Match Channel-to-Channel (Note 5)		●	78	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = –3.5V to 3.5V					
		R_L = 10k		2500	6000		V/mV
		0°C to 70°C	●	1500			V/mV
		–40°C to 85°C	●	1200			V/mV
		R_L = 1k		700	3500		V/mV
		0°C to 70°C	●	400			V/mV
		–40°C to 85°C	●	300			V/mV
V_{OL}	Output Voltage Swing Low (Note 9)	No Load	●		15	40	mV
		I_{SINK} = 1mA	●		45	75	mV
		I_{SINK} = 10mA	●		360	550	mV
V_{OH}	Output Voltage Swing High (Note 9)	No Load	●		15	40	mV
		I_{SOURCE} = 1mA	●		45	75	mV
		I_{SOURCE} = 10mA	●		360	550	mV

ELECTRICAL CHARACTERISTICS

(LTC6244HVC/I) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, 0V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection	V_S = 2.8V to 10.5V, V_{CM} = 0.2V	●	75	110		dB
	PSRR Match Channel-to-Channel (Note 5)		●	73	106		dB
	Minimum Supply Voltage (Note 10)		●	2.8			V
I_{SC}	Short-Circuit Current		●	40	55		mA
I_S	Supply Current per Amplifier		●		7	8.8	mA
GBW	Gain Bandwidth Product	Frequency = 100kHz, R_L = 1kΩ	●	35	50		MHz
SR	Slew Rate (Note 11)	A_V = –2, R_L = 1kΩ	●	18	40		V/µs
FPBW	Full Power Bandwidth (Note 12)	V_{OUT} = $3V_{P-P}$, R_L = 1kΩ	●	1.9	4.25		MHz
t_s	Settling Time	V_{STEP} = 2V, A_V = –1, R_L = 1kΩ, 0.1%			330		ns

(LTC6244H) The ● denotes the specifications which apply from –40°C to 125°C, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	MS8 Package	 ●		40	125 400	µV µV
		DD8 Package	 ●		100	650 950	µV µV
	V_{OS} Match Channel-to-Channel (Note 5)	MS8 Package	 ●		40	160 400	µV µV
		DD8 Package –40°C to 125°C	 ●		150	800 1160	µV µV
TC V_{OS}	Input Offset Voltage Drift, MS8 (Note 6)		●		0.7	2.5	µV/°C
I_B	Input Bias Current (Notes 4, 7)		 ●		1	 2	pA nA
I_{OS}	Input Offset Current (Notes 4, 7)		 ●		0.5	 250	pA pA
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	0		3.5	V
CMRR	Common Mode Rejection	0V ≤ V_{CM} ≤ 3.5V	●	74			dB
	CMRR Match Channel-to-Channel (Note 5)		●	72			dB
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 4V R_L = 10k to V_S/2	●	350			V/mV
		V_O = 1.5V to 3.5V R_L = 1k to V_S/2	●	125			V/mV
V_{OL}	Output Voltage Swing Low (Note 9)	No Load I_{SINK} = 1mA I_{SINK} = 5mA	● ● ●			40 85 325	mV mV mV
V_{OH}	Output Voltage Swing High (Note 9)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 5mA	● ● ●			40 85 325	mV mV mV

ELECTRICAL CHARACTERISTICS

(LTC6244H) The ● denotes the specifications which apply from –40°C to 125°C, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection	V_S = 2.8V to 6V, V_{CM} = 0.2V	●	75			dB
	PSRR Match Channel-to-Channel (Note 5)		●	73			dB
	Minimum Supply Voltage (Note 10)		●	2.8			V
I_{SC}	Short-Circuit Current		●	20			mA
I_S	Supply Current per Amplifier		●		6.25	7.4	mA
GBW	Gain Bandwidth Product	Frequency = 100kHz, R_L = 1kΩ	●	30			MHz
SR	Slew Rate (Note 11)	A_V = –2, R_L = 1kΩ	●	17			V/µs
FPBW	Full Power Bandwidth (Note 12)	V_{OUT} = $3V_{P-P}$, R_L = 1kΩ	●	1.8			MHz

(LTC6244H) The ● denotes the specifications which apply from –40°C to 125°C, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V, V_{CM} = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	MS8 Package	 ●		40	175 400	µV µV
		DD8 Package	 ●		100	650 950	µV µV
	V_{OS} Match Channel-to-Channel (Note 5)	MS8 Package	 ●		40	160 400	µV µV
		DD8 Package	 ●		150	800 1200	µV µV
I_B	Input Bias Current (Notes 4, 7)		 ●		1	 2	pA nA
I_{OS}	Input Offset Current (Notes 4, 7)		 ●		0.5	 250	pA pA
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	0		1.5	V
CMRR	Common Mode Rejection	0V ≤ V_{CM} ≤ 1.5V	●	70			dB
	CMRR Match Channel-to-Channel (Note 5)		●	68			dB
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 2V R_L = 10k to V_S/2	 ●	 75			 V/mV
V_{OL}	Output Voltage Swing Low (Note 9)	No Load I_{SINK} = 1mA	● ●			30 110	mV mV
V_{OH}	Output Voltage Swing High (Note 9)	No Load I_{SOURCE} = 1mA	● ●			30 110	mV mV
PSRR	Power Supply Rejection	V_S = 2.8V to 6V, V_{CM} = 0.2V	●	75			dB
	PSRR Match Channel-to-Channel (Note 5)		●	73			dB
	Minimum Supply Voltage (Note 10)		●	2.8			V
I_{SC}	Short-Circuit Current		●	5			mA
I_S	Supply Current per Amplifier		●		4.8	5.8	mA
GBW	Gain Bandwidth Product	Frequency = 100kHz, R_L = 1kΩ	●	28			MHz

ELECTRICAL CHARACTERISTICS

(LTC6244HVH) The ● denotes the specifications which apply from –40°C to 125°C, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 4)	DD8 Package	 ●		100	700 1050	µV µV
	V_{OS} Match Channel-to-Channel (Note 5)	DD8 Package	 ●		150	900 1165	µV µV
TC V_{OS}	Input Offset Voltage Drift, MS8 (Note 6)		●		0.7	2.5	µV/°C
I_B	Input Bias Current (Notes 4, 7)		 ●		1	 2	pA nA
I_{OS}	Input Offset Current (Notes 4, 7)		 ●		0.5	 250	pA nA
	Input Noise Voltage	0.1Hz to 10Hz			1.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			8	12	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density (Note 8)				0.56		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode			10^{12}		Ω
C_{IN}	Input Capacitance Differential Mode Common Mode	f = 100kHz			 3.5 2.1		 pF pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–5		3.5	V
CMRR	Common Mode Rejection	$-5V \le V_{CM} \le 3.5V$	●	80	105		dB
	CMRR Match Channel-to-Channel (Note 5)		 ●	 78	 95		 dB
A_{VOL}	Large Signal Voltage Gain	V_O = –3.5V to 3.5V R_L = 10k	 ●	2500 1000	6000		V/mV V/mV
		R_L = 1k	 ●	700 170	3500		V/mV V/mV
V_{OL}	Output Voltage Swing Low (Note 9)	No Load I_{SINK} = 1mA I_{SINK} = 10mA	● ● ●		15 45 360	40 75 550	mV mV mV
V_{OH}	Output Voltage Swing High (Note 9)	No Load I_{SOURCE} = 1mA I_{SINK} = 10mA	● ● ●		15 45 360	40 75 550	mV mV mV
PSRR	Power Supply Rejection	V_S = 2.8V to 10.5V, V_{CM} = 0.2V	●	75	110		dB
	PSRR Match Channel-to-Channel (Note 5)		 ●	 73	 106		 dB
	Minimum Supply Voltage (Note 10)		●	2.8			V
I_{SC}	Short-Circuit Current		●	40	55		mA
I_S	Supply Current per Amplifier		●			9.3	mA
GBW	Gain Bandwidth Product	Frequency = 100kHz, R_L = 1kΩ	●	35	50		MHz
SR	Slew Rate (Note 11)	A_V = –2, R_L = 1kΩ	●	18	40		V/µs
FPBW	Full Power Bandwidth (Note 12)	V_{OUT} = $3V_{P-P}$, R_L = 1kΩ	●	1.9	4.3		MHz
t_s	Settling Time	V_{OUT} = 2V, A_V = –1 , R_L =1kΩ	●		330		ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 3: The LTC6244C/LTC6244HVC are guaranteed to meet specified performance from 0°C to 70°C. They are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LTC6244I/LTC6244HVI, are guaranteed to meet specified performance from –40°C to 85°C. The LTC6244H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: ESD (Electrostatic Discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6244; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 5: Matching parameters are the difference between the two amplifiers of the LTC6244. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in µV/V on the amplifiers. The difference is calculated between the sides in µV/V. The result is converted to dB.

Note 6: This parameter is not 100% tested.

Note 7: This specification is limited by high speed automated test capability. See Typical Characteristics curves for actual typical performance.

Note 8: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$ where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 50GΩ dominates the contribution of current noise. See also Typical Characteristics curve Noise Current vs Frequency.

Note 9: Output voltage swings are measured between the output and power supply rails.

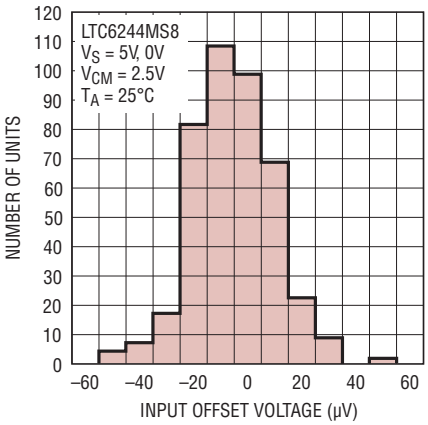
Note 10: Minimum supply voltage is guaranteed by the power supply rejection ratio test.

Note 11: Slew rate is measured in a gain of –2 with R_F = 1k and R_G = 500Ω. V_{IN} is ±1V and V_{OUT} slew rate is measured between –1V and +1V. On the LTC6244HV/LTC6245HV, V_{IN} is ±2V and V_{OUT} slew rate is measured between –2V and +2V.

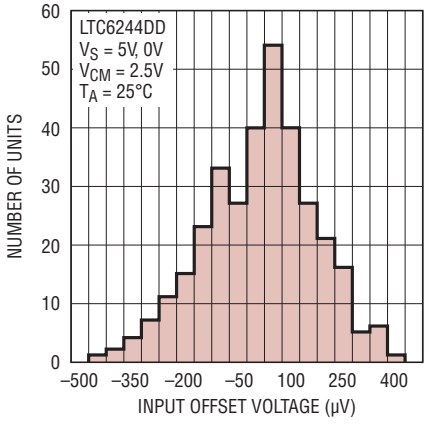
Note 12: Full-power bandwidth is calculated from the slew rate: $FPBW = SR/2\pi V_P$.

TYPICAL PERFORMANCE CHARACTERISTICS

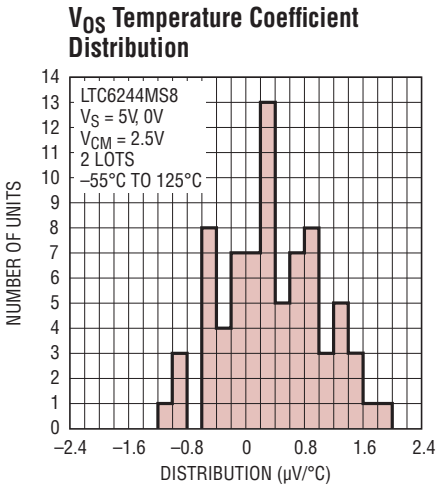
V_{OS} Distribution



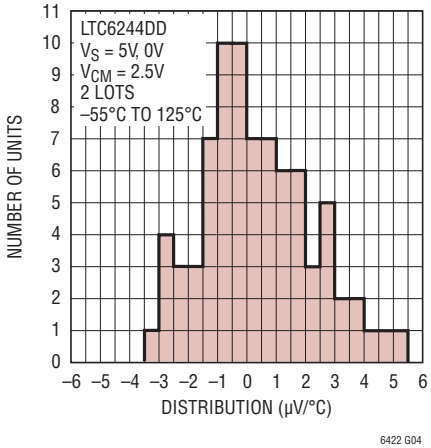
V_{OS} Distribution



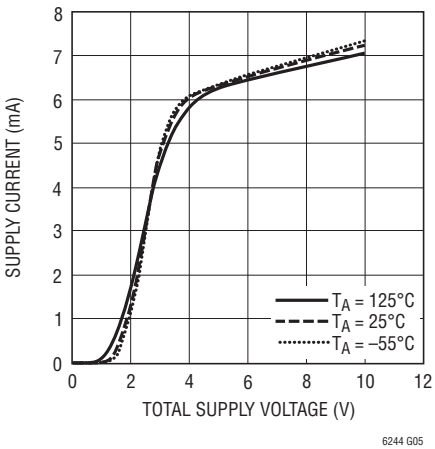
V_{OS} Temperature Coefficient Distribution



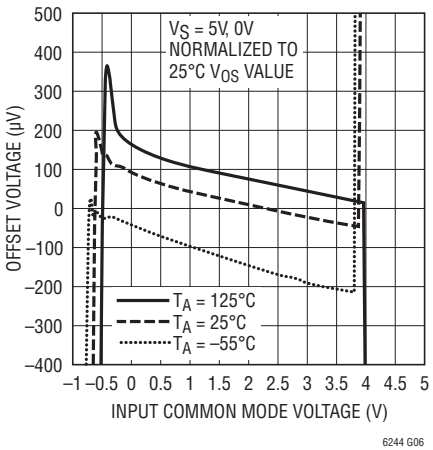
V_{OS} Temperature Coefficient Distribution



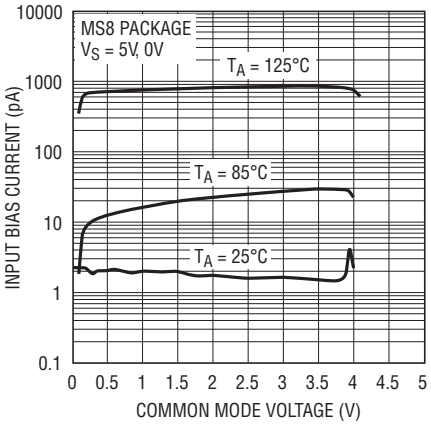
Supply Current vs Supply Voltage (Per Amplifier)



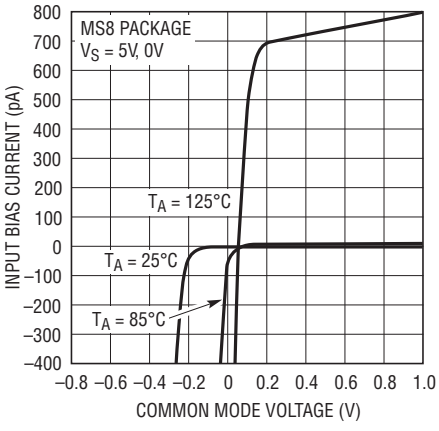
Offset Voltage vs Input Common Mode Voltage



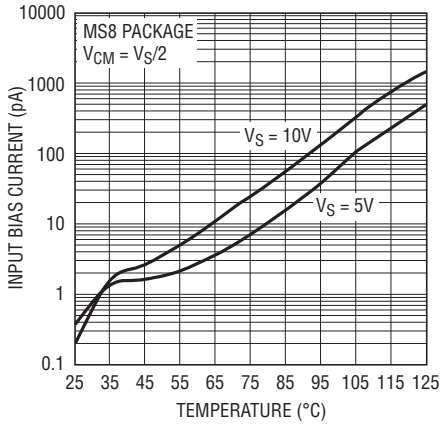
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Common Mode Voltage

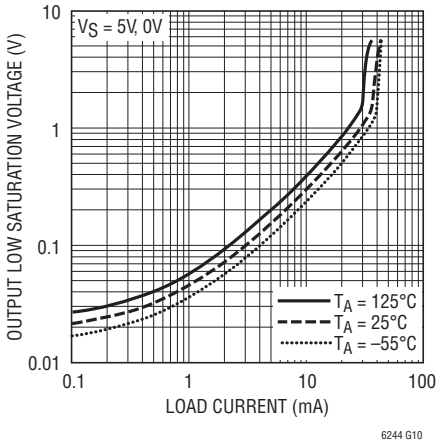


Input Bias Current vs Temperature

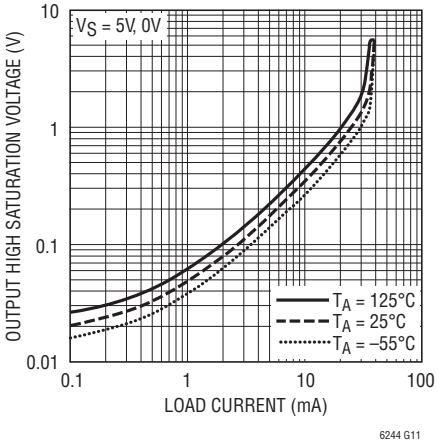


TYPICAL PERFORMANCE CHARACTERISTICS

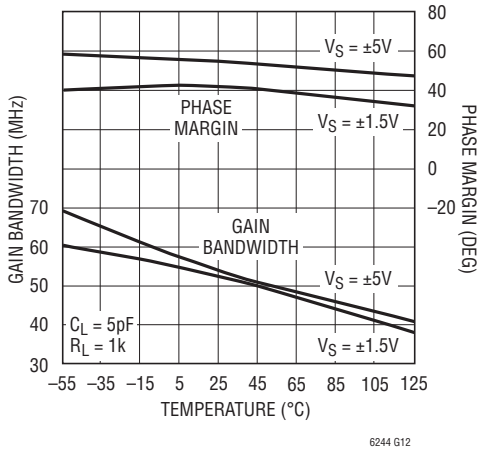
Output Saturation Voltage vs Load Current (Output Low)



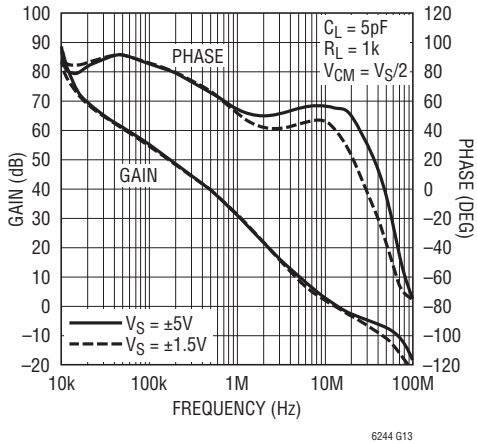
Output Saturation Voltage vs Load Current (Output High)



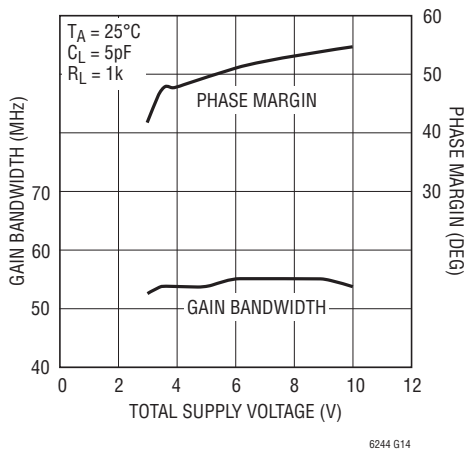
Gain Bandwidth and Phase Margin vs Temperature



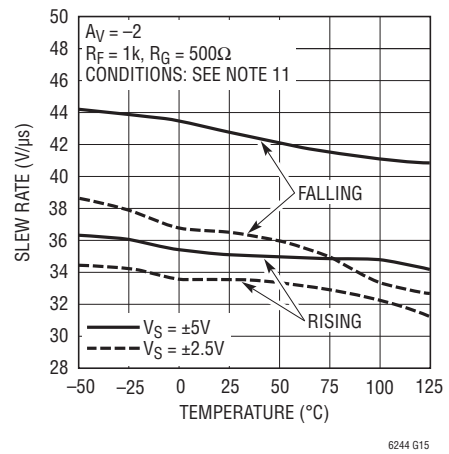
Open Loop Gain vs Frequency



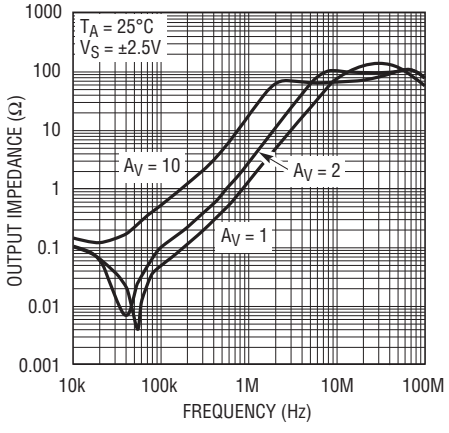
Gain Bandwidth and Phase Margin vs Supply Voltage



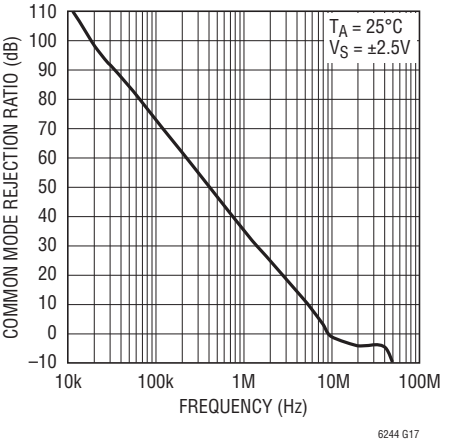
Slew Rate vs Temperature



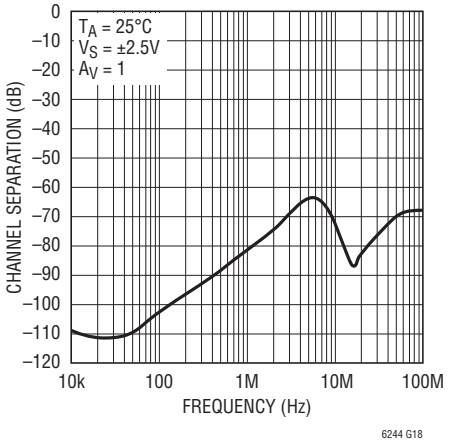
Output Impedance vs Frequency



Common Mode Rejection Ratio vs Frequency

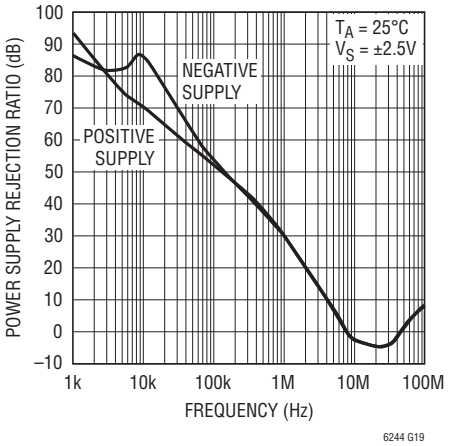


Channel Separation vs Frequency

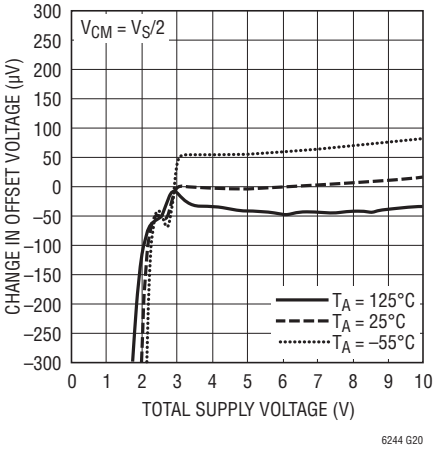


TYPICAL PERFORMANCE CHARACTERISTICS

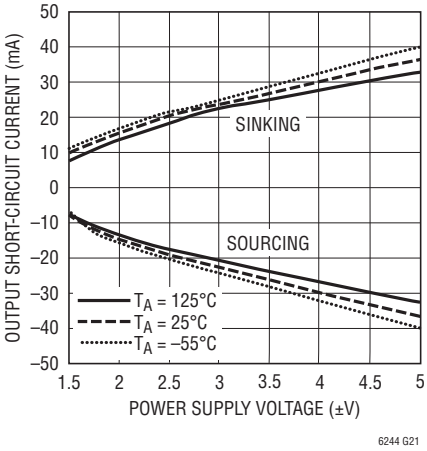
Power Supply Rejection Ratio vs Frequency



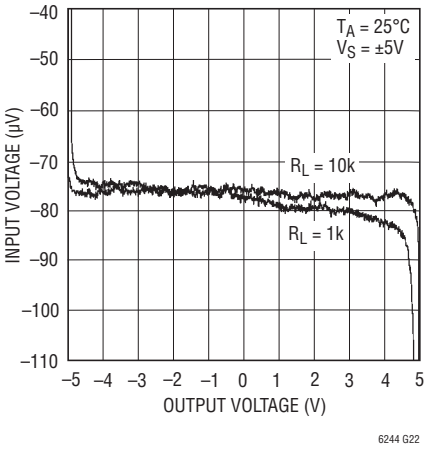
Minimum Supply Voltage



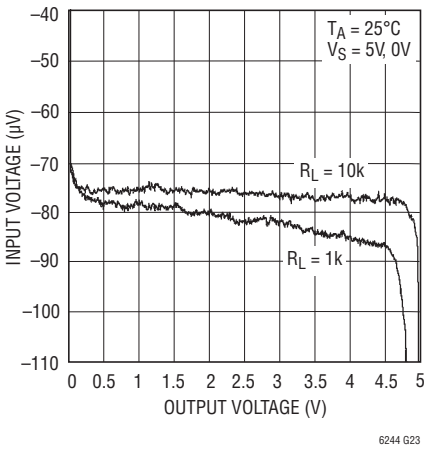
Output Short-Circuit Current vs Power Supply Voltage



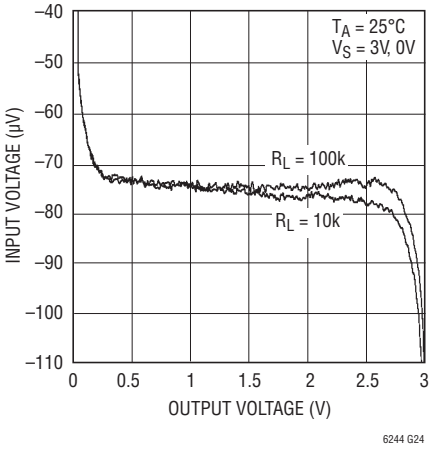
Open-Loop Gain



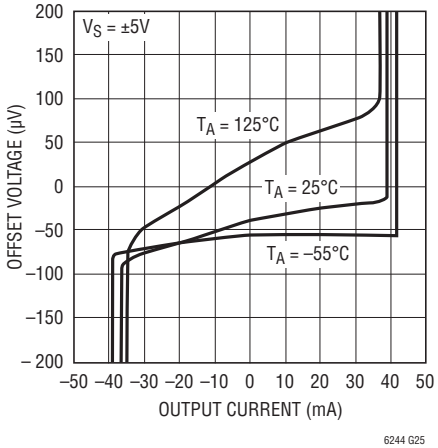
Open-Loop Gain



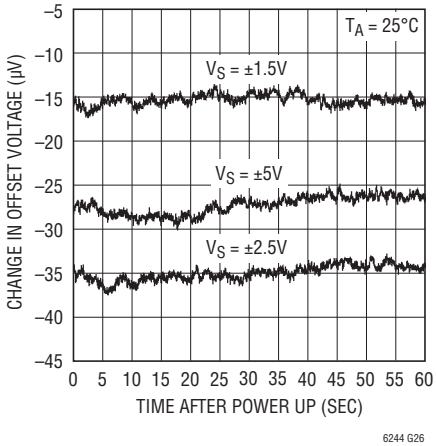
Open-Loop Gain



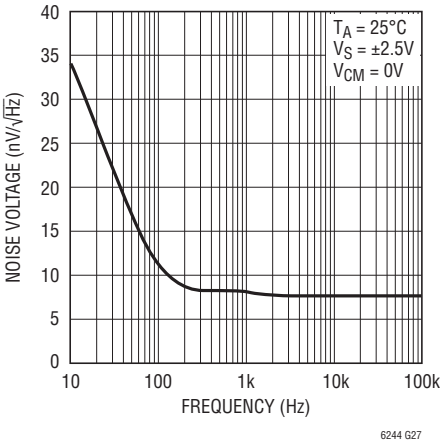
Offset Voltage vs Output Current



Warm-Up Drift vs Time

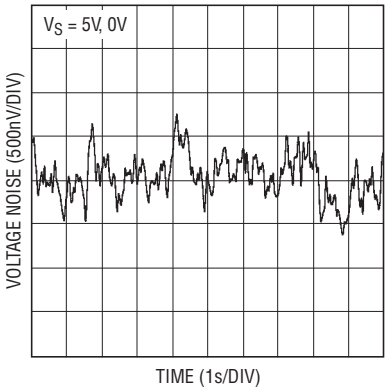


Noise Voltage vs Frequency



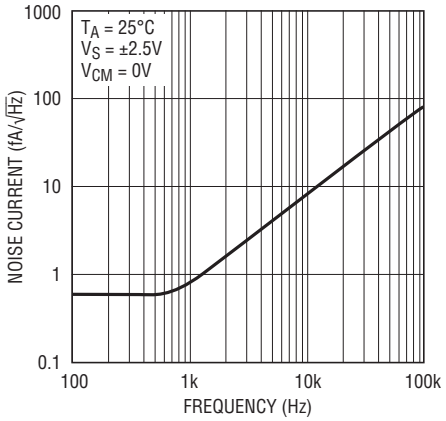
TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 10Hz Voltage Noise



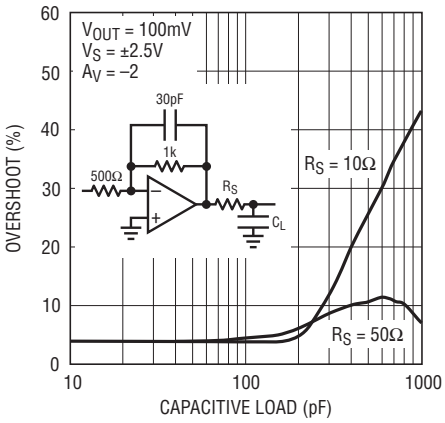
6244 G28

Noise Current vs Frequency



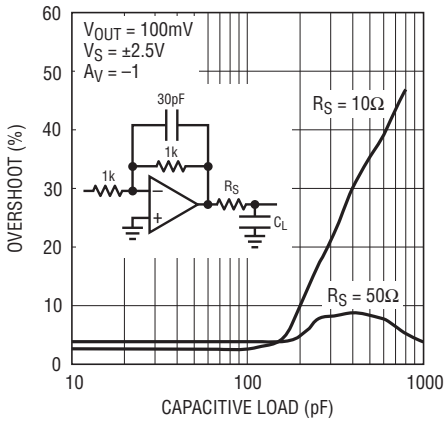
6244 G29

Series Output Resistance and Overshoot vs Capacitive Load



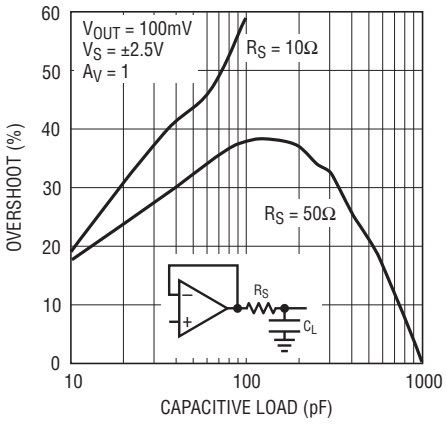
6244 G30

Series Output Resistance and Overshoot vs Capacitive Load



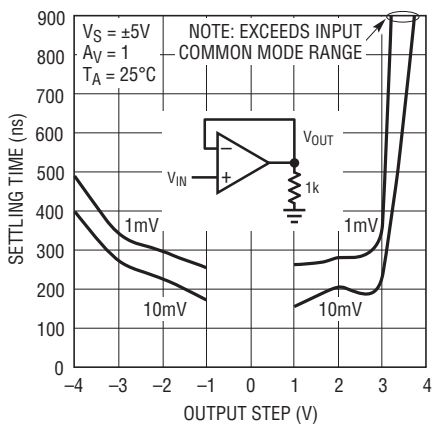
6244 G31

Series Output Resistance and Overshoot vs Capacitive Load



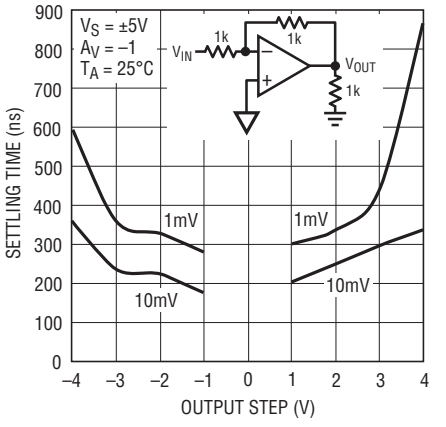
6244 G32

Settling Time vs Output Step (Noninverting)



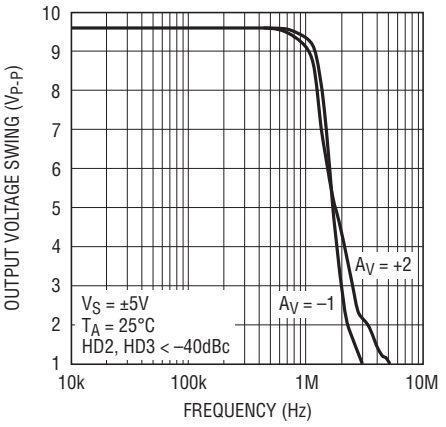
6244 G33

Settling Time vs Output Step (Inverting)



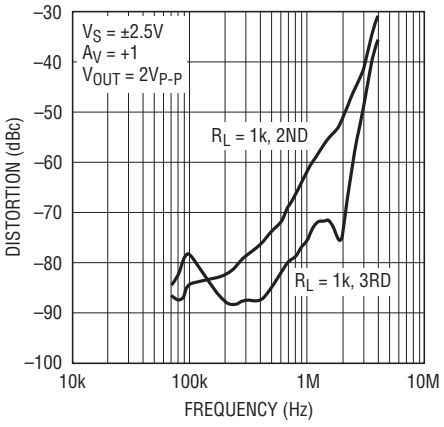
6244 G34

Maximum Undistorted Output Signal vs Frequency



6244 G35

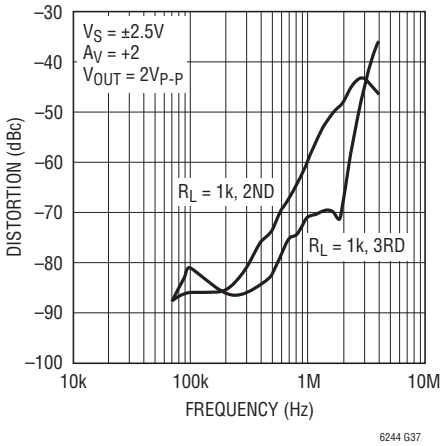
Distortion vs Frequency



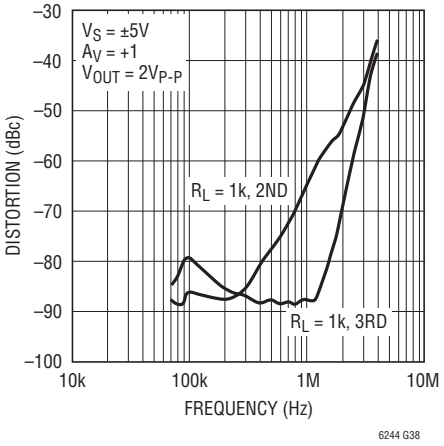
6244 G36

TYPICAL PERFORMANCE CHARACTERISTICS

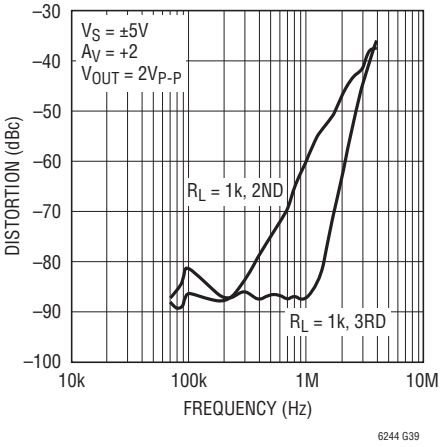
Distortion vs Frequency



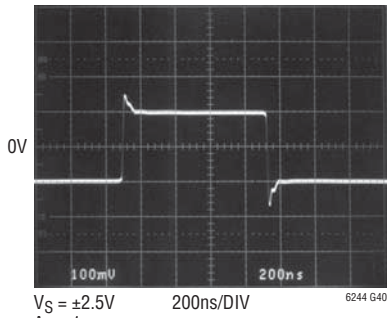
Distortion vs Frequency



Distortion vs Frequency

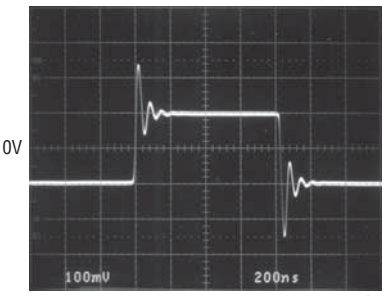


Small-Signal Response



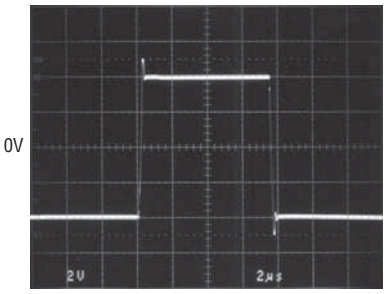
VS = ±2.5V 200ns/DIV
AV = 1
RL = ∞

Small-Signal Response



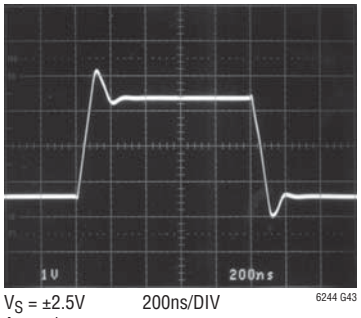
VS = ±2.5V 200ns/DIV
AV = 1
RL = ∞
CL = 75pF

Large-Signal Response



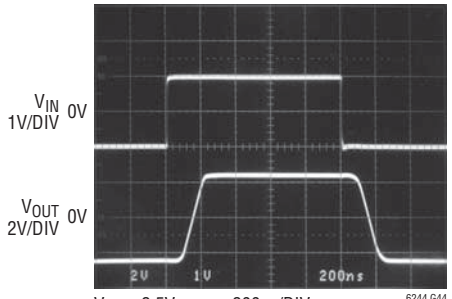
VS = ±5V 2µs/DIV
AV = 1
RL = ∞

Large-Signal Response



VS = ±2.5V 200ns/DIV
AV = –1
RL = 1k

Output Overdrive Recovery



VS = ±2.5V 200ns/DIV
AV = 3
RL = 3k

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 1 is a simplified schematic of the LTC6244, which has a pair of low noise input transistors M1 and M2. A simple folded cascode Q1, Q2 and R1, R2 allow the input stage to swing to the negative rail, while performing level shift to the Differential Drive Generator. Low offset voltage is accomplished by laser trimming the input stage.

Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. Capacitor C_M sets the overall amplifier gain bandwidth. The differential drive generator supplies signals to transistors M3 and M4 that swing the output from rail-to-rail.

The photo of Figure 2 shows the output response to an input overdrive with the amplifier connected as a voltage follower. If the negative going input signal is less than a diode drop below $V^–$, no phase inversion occurs. For input signals greater than a diode drop below $V^–$, limit the current to 3mA with a series resistor R_S to avoid phase inversion.

The input common mode voltage range extends from $V^–$ to $V^+ – 1.5V$. In unity gain voltage follower applications, exceeding this range by applying a signal that reaches 1V from the positive supply rail can create a low level instability at the output. Loading the amplifier with several hundred micro-amps will reduce or eliminate the instability.

ESD

The LTC6244 has reverse-biased ESD protection diodes on all input and outputs as shown in Figure 1. These diodes protect the amplifier for ESD strikes to 4kV. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current transient is less than 1 second and limited to one hundred milliamps or less, no damage to the device will occur.

The amplifier input bias current is the leakage current of these ESD diodes. This leakage is a function of the temperature and common mode voltage of the amplifier, as shown in the Typical Performance Chacteristics.

Noise

The LTC6244 exhibits low 1/f noise in the 0.1Hz to 10Hz region. This $1.5\mu V_{P-P}$ noise allows these op amps to be used in a wide variety of high impedance low frequency applications, where Zero-Drift amplifiers might be inappropriate due to their input sampling characteristic.

In the frequency region above 1kHz the LTC6244 also shows good noise voltage performance. In this frequency region, noise can easily be dominated by the total source

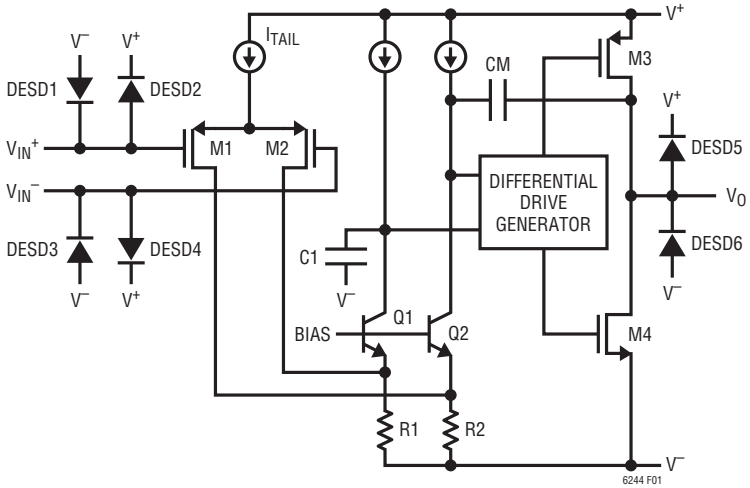
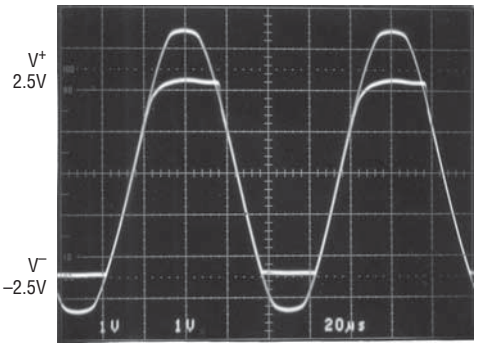


Figure 1. Simplified Schematic



V_{OUT} AND V_{IN} OF FOLLOWER WITH LARGE INPUT OVERDRIVE

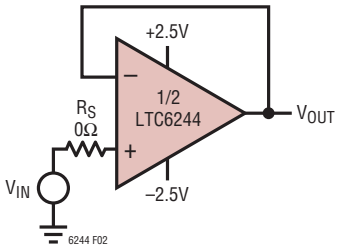


Figure 2. Unity Gain Follower Test Circuit

APPLICATIONS INFORMATION

resistance of the particular application. Specifically, these amplifiers exhibit the noise of a 4k resistor, meaning it is desirable to keep the source and feedback resistance at or below this value, i.e., $R_S + R_G||R_{FB} \leq 4k$. Above this total source impedance, the noise voltage is not dominated by the amplifier.

Noise current can be estimated from the expression $i_n = \sqrt{2qI_B}$, where $q = 1.6 \bullet 10^{-19}$ coulombs. Equating $\sqrt{4kTR\Delta f}$ and $R_S\sqrt{2qI_B\Delta f}$ shows that for source resistors below 50GΩ the amplifier noise is dominated by the source resistance. See the Typical Characteristics curve Noise Current vs Frequency.

Proprietary design techniques are used to obtain simultaneous low 1/f noise and low input capacitance. Low input capacitance is important when the amplifier is used with high source and feedback resistors. High frequency noise from the amplifier tail current source, I_{TAIL} in Figure 1, couples through the input capacitance and appears across these large source and feedback resistors.

Stability

The good noise performance of these op amps can be attributed to large input devices in the differential pair. Above several hundred kilohertz, the input capacitance can cause amplifier stability problems if left unchecked. When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance, source capacitance (R_S, C_S), and the amplifier input capacitance. In low gain configurations and with R_F and R_S in even the kilohm range (Figure 3), this pole can create excess phase shift and possibly oscillation. A small capacitor C_F in parallel with R_F eliminates this problem.

Achieving Low Input Bias Current

The DD package is leadless and makes contact to the PCB beneath the package. Solder flux used during the attachment of the part to the PCB can create leakage current paths and can degrade the input bias current performance of the part. All inputs are susceptible because the backside paddle is connected to V^- internally. As the input voltage changes or if V^- changes, a leakage path can be formed and alter the observed input bias current. For lowest bias current, use the LTC6244 in the MS8 package.

Photodiode Amplifiers

Photodiodes can be broken into two categories: large area photodiodes with their attendant high capacitance (30pF to 3000pF) and smaller area photodiodes with relatively low capacitance (10pF or less). For optimal signal-to-noise performance, a transimpedance amplifier consisting of an inverting op amp and a feedback resistor is most commonly used to convert the photodiode current into voltage. In low noise amplifier design, large area photodiode amplifiers require more attention to reducing op amp input voltage noise, while small area photodiode amplifiers require more attention to reducing op amp input current noise and parasitic capacitances.

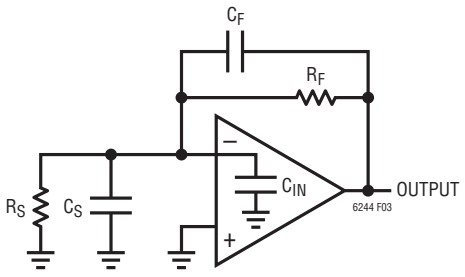


Figure 3. Compensating Input Capacitance

APPLICATIONS INFORMATION

Large Area Photodiode Amplifiers

A simple large area photodiode amplifier is shown in Figure 4a. The capacitance of the photodiode is 3650pF (nominally 3000pF), and this has a significant effect on the noise performance of the circuit. For example, the photodiode capacitance at 10kHz equates to an impedance of 4.36kΩ, so the op amp circuit with 1MΩ feedback has a noise gain of NG = 1 + 1M/4.36k = 230 at that frequency. Therefore, the LTC6244 input voltage noise gets to the output as NG • 7.8nV/√Hz = 1800nV/√Hz, and this can clearly be seen in the circuit's output noise spectrum in Figure 4b. Note that we have not yet accounted for the op amp current noise, or for the 130nV/√Hz of the gain resistor, but these are obviously trivial compared to the op amp voltage noise and the noise gain. For reference, the DC output offset of this circuit is about 100µV, bandwidth is 52kHz, and the total noise was measured at 1.7mV_{RMS} on a 100kHz measurement bandwidth.

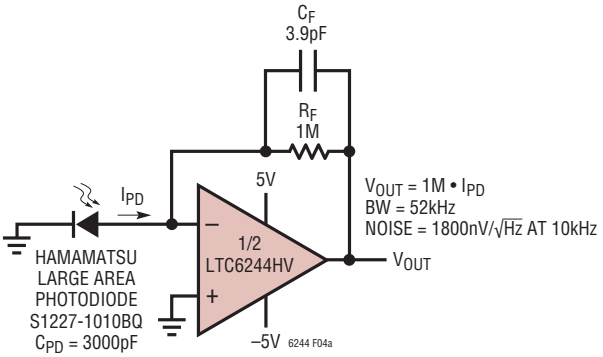


Figure 4a. Large Area Photodiode Transimpedance Amplifier

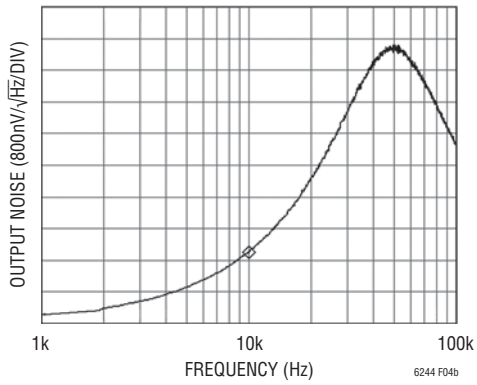


Figure 4b. Output Noise Spectral Density of the Circuit of Figure 4a. At 10kHz, the 1800nV/√Hz Output Noise is Due Almost Entirely to the 7.8nV Voltage Noise of the LTC6244 and the High Noise Gain of the 1M Feedback Resistor Looking Into the High Photodiode Capacitance

An improvement to this circuit is shown in Figure 5a, where the large diode capacitance is bootstrapped by a 1nV/√Hz JFET. This depletion JFET has a V_{GS} of about –0.5V, so that R_{BIAS} forces it to operate at just over 1mA of drain current. Connected as shown, the photodiode has a reverse bias of one V_{GS}, so its capacitance will be slightly lower than in the previous case (measured 2640pF), but the most drastic effects are due to the bootstrapping. Figure 5b shows the output noise of the new circuit. Noise at 10kHz is now 220nV/√Hz, and the 130nV/√Hz noise thermal noise floor of the 1M feedback resistor is discernible at low frequencies. What has happened is that the 7.8nV/√Hz of the op amp has been effectively replaced by the 1nV/√Hz of the JFET. This is because the 1M feedback resistor is no longer "looking back" into the large photodiode capacitance. It is instead looking back into a JFET gate capacitance, an op amp input capacitance, and some parasitics, approximately 10pF total. The large photodiode capacitance is across the gate-source voltage of the low noise JFET. Doing a sample calculation at 10kHz as before, the photodiode capacitance looks like 6kΩ, so the 1nV/√Hz of the JFET creates a current noise of 1nV/6k = 167fA/√Hz. This current noise necessarily flows through the 1M feedback resistor, and so appears as 167nV/√Hz at the output. Adding the 130nV/√Hz of the resistor (RMS wise) gives a total calculated noise density of 210nV/√Hz, agreeing well with the measured noise of Figure 5b. Another drastic improvement is in bandwidth, now over 350kHz, as the bootstrap enabled a reduction of the compensating feedback capacitance. Note that the bootstrap does not affect the DC accuracy of the amplifier, except by adding a few picoamps of gate current.

There is one drawback to this circuit. Most photodiode circuits require the ability to set the amount of applied reverse bias, whether it's 0V, 5V, or 200V. This circuit has a fixed reverse bias of about 0.5V, dictated by the JFET.

APPLICATIONS INFORMATION

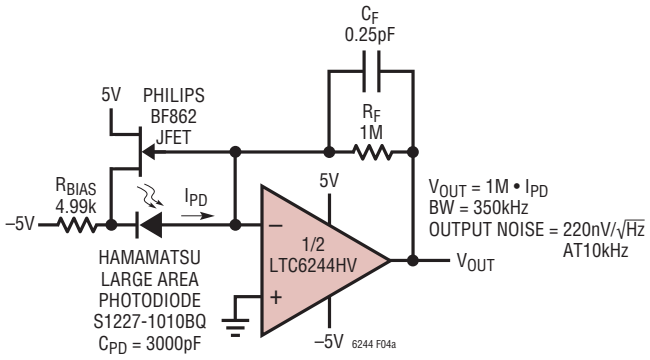


Figure 5a. Large Area Diode Bootstrapping

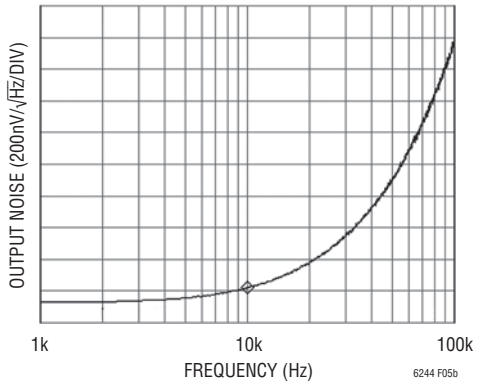


Figure 5b: Output Noise Spectral Density of Figure 5a. The Simple JFET Bootstrap Improves Noise (and Bandwidth) Drastically. Noise Density at 10kHz is Now 220nV/√Hz, About a 8.2x Reduction. This is Mostly Due to the Bootstrap Effect of Swapping the 1nV/√Hz of the JFET for the 7.8nV/√Hz of the Op Amp

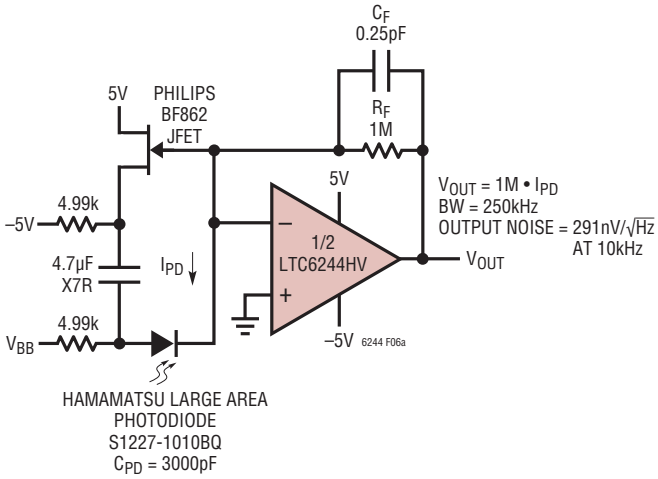


Figure 6a. The Addition of a Capacitor and Resistor Enable the Benefit of Bootstrapping While Applying Arbitrary Photodiode Bias Voltage V_{BB}

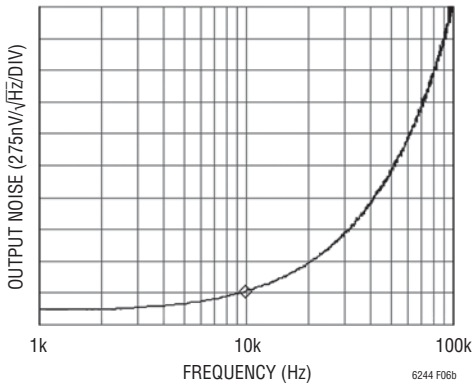


Figure 6b: Output Spectrum of Circuit of Figure 6a, with Photodiode Bias at 0V. Photodiode Capacitance is Back Up, as in the Original Circuit of Figure 4a. However, it can be Reduced Arbitrarily by Providing Reverse Bias. This Plot Shows that Bootstrapping Alone Reduced the 10kHz Noise Density by a Factor of 6.2, from 1800nV/√Hz to 291nV/√Hz

The solution is as shown in the circuit of Figure 6a, which uses a capacitor-resistor pair to enable the AC benefits of bootstrapping while allowing a different reverse DC voltage on the photodiode. The JFET is still running at the same current, but an arbitrary reverse bias may be applied to the photodiode. The output noise spectrum of the circuit with 0V of photodiode reverse bias is shown in Figure 6b. Photodiode capacitance is again 3650pF, as in the original circuit of Figure 4a. This noise plot with 0V bias shows that bootstrapping alone was responsible for a factor of 6.2 noise reduction, from 1800nV/√Hz to 291nV/√Hz at 10kHz, independent of photodiode capacitance. However, photodiode capacitance can now can be reduced arbitrarily by providing reverse bias, and the photodiode can also be reversed to support either cathode or anode connections for positive or negative going outputs.

The circuit on the last page of this data sheet shows further reduction in noise by paralleling four JFETs to attain 152nV/√Hz at 10kHz, a noise of 12 times less than the basic photodiode circuit of Figure 4a.

APPLICATIONS INFORMATION

Small Area Photodiode Amplifiers

Small area photodiodes have very low capacitance, typically under 10pF and some even below 1pF. Their low capacitance makes them more approximate current sources to higher frequencies than large area photodiodes. One of the challenges of small area photodiode amplifier design is to maintain low input capacitance so that voltage noise does not become an issue and current noise dominates. A simple small area photodiode amplifier using the LTC6244 is shown in Figure 7. The input capacitance of the amplifier consists of C_{DM} and one C_{CM} (because the +input is grounded), or about 6pF total. The small photodiode has 1.8pF, so the input capacitance of the amplifier is dominating the capacitance. The small feedback capacitor is an actual component (AVX Accu-F series), but it is also in parallel with the op amp lead, resistor and parasitic capacitances, so the total real feedback capacitance is probably about 0.4pF. The reason this is important is that this sets the compensation of the circuit and, with op amp gain bandwidth, the circuit bandwidth. The circuit as shown has a bandwidth of 350kHz, with an output noise of 120µV_{RMS} measured over that bandwidth.

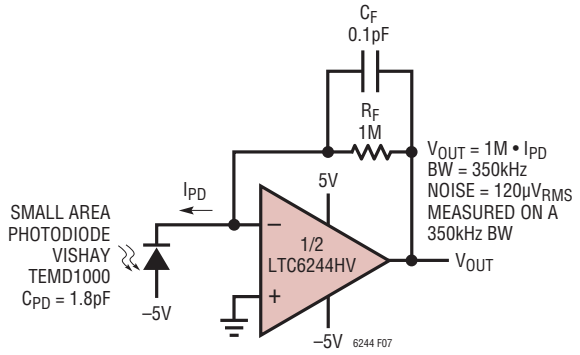


Figure 7. LTC6244 in a Normal TIA Configuration

The circuit of Figure 8a makes some slight improvements. Operation is still transimpedance mode, with R_F setting the gain to 1MΩ. However, a noninverting input stage A1 with a gain of 3 has been inserted, followed by the usual inverting stage performed by A2. Note what this achieves. The amplifier input capacitance is bootstrapped by the feedback of R2:R1, eliminating the effect of A1's input C_{DM} (3.5pF), and leaving only one C_{CM} (2.1pF). The op amp at Pins 5, 6 and 7 was chosen for the input amplifier to eliminate extra pin-to-pin capacitance on the (+) input. The lead capacitance on the corner of an MSOP package is only about 0.15pF. By using this noninverting configuration, input capacitance is minimized.

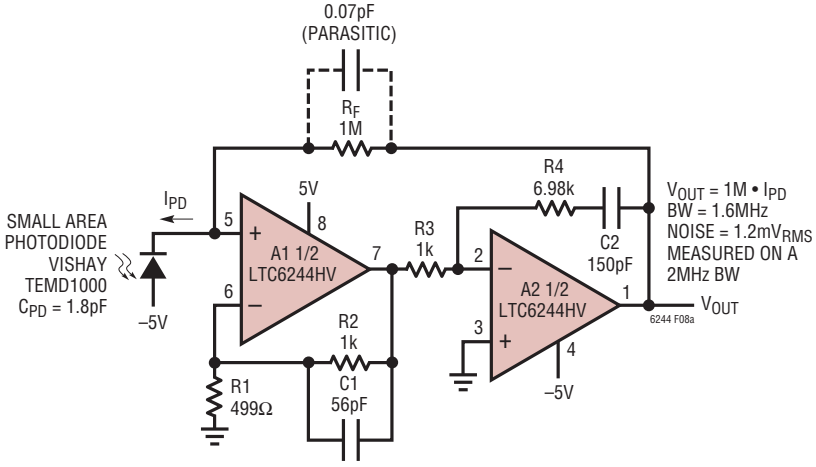


Figure 8a: Using Both Op Amps for Higher Bandwidth. A1 Provides a Gain of 3 Within the Loop, Increasing the Gain Bandwidth Product. This Bootstraps the C_{DM} Accross A1's Inputs, Reducing Amplifier Input Capacitance. Inversion is Provided by A2, so that the Photodiode Looks Into a Noninverting Input. Pin 5 was Selected Because it is in the Corner, Removing One Lead Capacitance

APPLICATIONS INFORMATION

Total capacitance at the amplifier's input is now one C_{CM} (2.1pF) plus the photodiode capacitance C_{PD} (1.8pF), or about 4pF accounting for parasitics. The shunt impedance at 1MHz, for example, is $X_C = 1/(2\pi fC) = 39.8k\Omega$, and therefore, the noise gain at 1MHz is $NG = 1+Rf/X_C = 26$. The input voltage noise of this amplifier is about $15nV/\sqrt{Hz}$, after accounting for the effects of R1 through R3, the noise of the second stage and the fact that voltage noise does rise with frequency. Multiplying the noise gain by the input voltage noise gives an output noise density due to voltage noise of $26 \bullet 15nV/\sqrt{Hz} = 390nV/\sqrt{Hz}$. But the noise spectral density plot of Figure 8b shows an output noise of $782nV/\sqrt{Hz}$ at 1MHz. The extra output noise is due to input current noise, multiplied by the feedback impedance. So while the circuit of Figure 8a does increase bandwidth, it does not offer a noise advantage. Note, however, that the $1.2mV_{RMS}$ of noise is now measured in a 2MHz bandwidth, instead of over a 350kHz bandwidth of the previous example.

A Low Noise Fully Differential Buffer/Amplifier

In differential signal conditioning circuits, there is often a need to monitor a differential source without loading or adding appreciable noise to the circuit. In addition, adding gain to low level signals over appreciable bandwidth is extremely useful. A typical application for a low noise, high impedance, differential amplifier is in the baseband circuit of an RFID (radio frequency identification) receiver. The baseband signal of a UHF RFID receiver is typically a low level differential signal at the output of a demodulator with differential output impedance in the range of 100Ω to 400Ω. The bandwidth of this signal is 1MHz or less.

The circuit of Figure 9a uses an LTC6244 to make a low noise fully differential amplifier. The amplifier's gain, input impedance and –3dB bandwidth can be specified independently. Knowing the desired gain, input impedance and –3dB bandwidth, R_G, C_F and C_{IN} can be calculated from the equations shown in Figure 9b. The common mode gain of this amplifier is equal to one ($V_{OUTCM} = V_{INCM}$) and is independent of resistor matching. The component values in the Figure 9a circuit implement a 970kHz, gain = 5, differential amplifier with 4k input impedance. The output differential DC offset is typically less than 500µV. The differential input referred noise voltage density is shown in Figure 10. The total input referred noise in a 1MHz bandwidth is $16\mu V_{RMS}$.

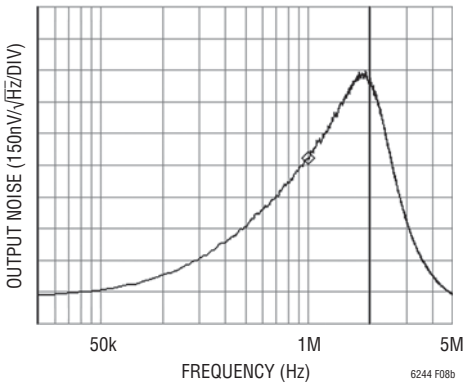


Figure 8b: Output Noise Spectrum of the Circuit in Figure 8a. Noise at 1MHz is $782nV/\sqrt{Hz}$, Due Mostly to the Input Current Noise Rising with Frequency

APPLICATIONS INFORMATION

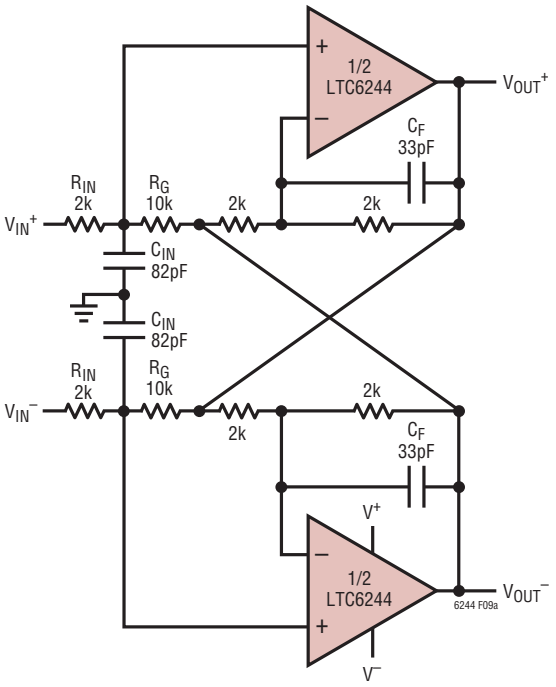


Figure 9a. Low Noise Fully Differential Buffer/Amplifier (f_{-3dB} = 970kHz, Gain = 5, R_{IN} = 4k)

$$\text{Input Impedance} = 2 \bullet R_{IN}$$

$$\text{Gain} = \frac{V_{OUT}^{+} - V_{OUT}^{-}}{V_{IN}^{+} - V_{IN}^{-}} = \frac{R_G}{R_{IN}}$$

$$\text{Maximum Gain} = \frac{5\text{MHz}}{f_{3dB}}$$

$$C_F = \frac{1}{4398 \bullet f_{3dB} \bullet (\text{Gain} + 2)}$$

$$C_{IN} = \frac{\text{Gain} + 2}{8.977 \bullet \text{Gain} \bullet R_{IN} \bullet f_{3dB}}$$

$$f_{3dB} = \frac{1}{\sqrt{4000 \bullet \pi^2 \bullet R_G \bullet C_F \bullet C_{IN}}}$$

Figure 9b. Design Equations for Figure 9a Circuit

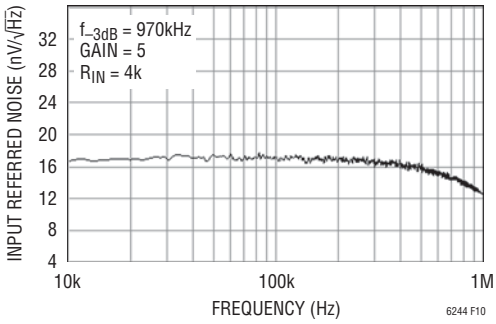


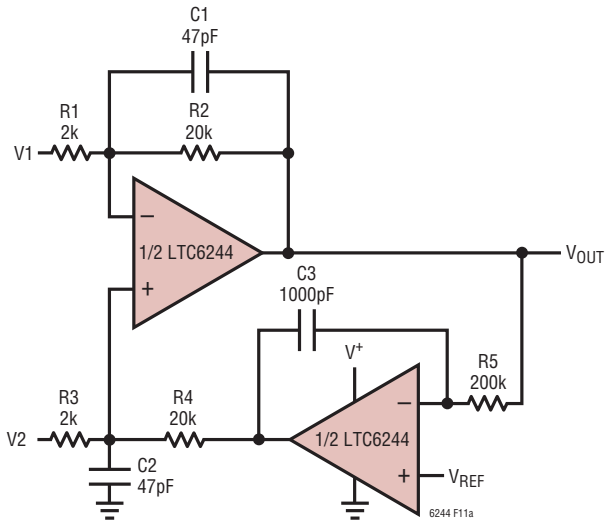
Figure 10. Differential Input Referred Noise

A Low Noise AC Difference Amplifier

In the signal conditioning of wideband sensors and transducers, a low noise amplifier is often used to provide gain for low level AC difference signals in the frequency range of a few Hertz to hundreds of kilo-Hertz. In addition, the amplifier must reject common mode AC signals and its input impedance should be higher than the differential source impedance. Typical applications are piezoelectric sensors used in sonar, sound and ultrasound systems and LVDT (linear variable differential transformers) for displacement measurements in process control and robotics.

The Figure 11a circuit is a low noise, single supply AC difference amplifier. The amplifier's low frequency –3dB bandwidth is set with resistor R5 and capacitor C3, while the upper –3dB bandwidth is set with R2 and C1. The input common mode DC voltage can vary from ground to V^+ and the output DC voltage is equal to the V_{REF} voltage. The amplifier's gain is the ratio of resistors R2 to R1 (R4 = R2 and R3 = R1). The component values in the circuit of Figure 11a implement an 800Hz to 160kHz AC amplifier with a gain equal to 10 and 12nV/$\sqrt{\text{Hz}}$ input referred voltage noise density shown in Figure 11b. The total input referred wideband noise is 4.5µV_{RMS}, in the bandwidth of 500Hz to 200kHz.

APPLICATIONS INFORMATION



$$V_{OUT} = GAIN \bullet (V2 - V1) + V_{REF}$$

$$GAIN = \frac{R2}{R1}\ R3 = R1,\ R4 = R2,\ C1 = C2$$

$$BANDWIDTH = f_{HI} - f_{LO}$$

$$f_{HI} = \frac{1}{2 \bullet \pi \bullet R2 \bullet C1},\ f_{LO} = \frac{1}{2 \bullet \pi \bullet R5 \bullet C3}$$

Figure 11a. Low Noise AC Difference Amplifier (Bandwidth 800Hz to 160kHz, Gain = 10)

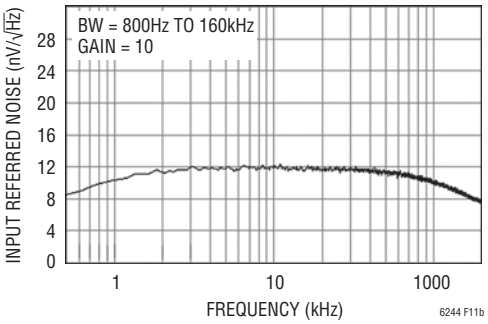
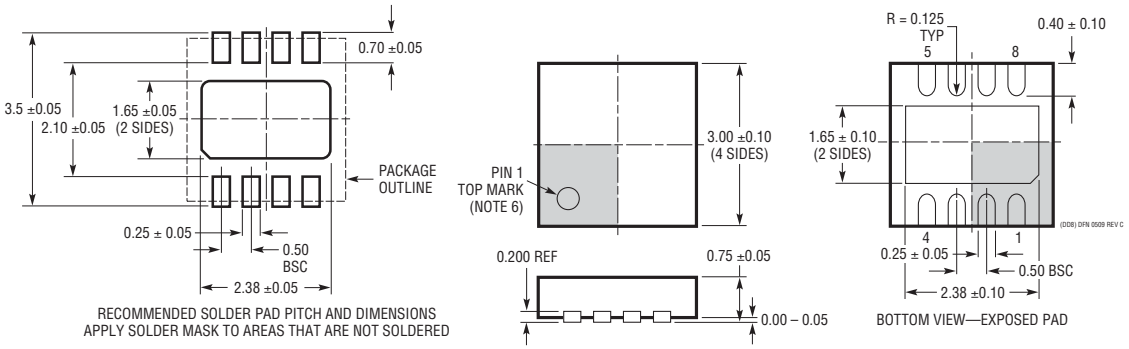


Figure 11b. Input Referred Noise

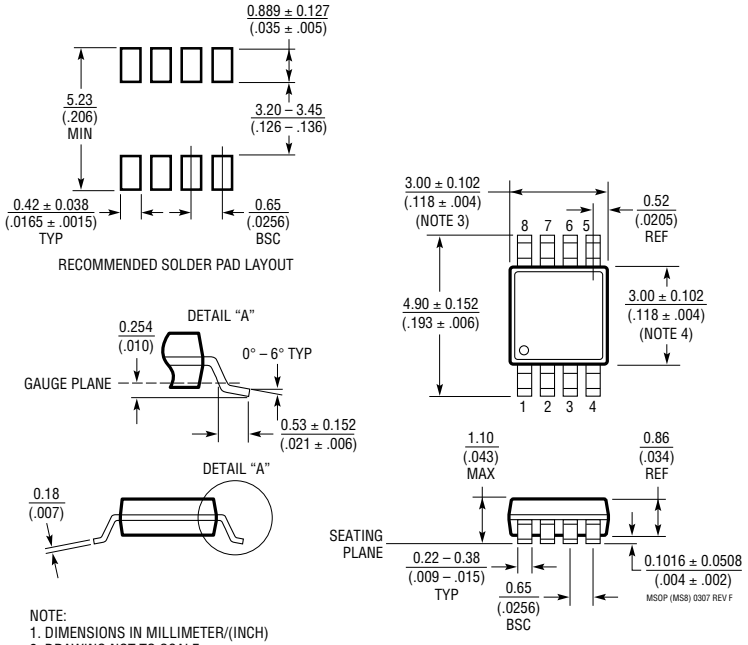
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	12/09	Change to Figure 2	15