1.3MHz, 20µA Power Efficient Rail-to-Rail I/O Op Amps

FEATURES

- **Gain Bandwidth Product: 1.3MHz**
- **Low Quiescent Current: 20µA**
- **C-Load™ Op Amp Drives all Capacitive Loads**
- **Offset Voltage: 400µV Maximum**
- **Rail-to-Rail Input and Output**
- **Supply Voltage Range: 1.8V to 5.25V**
- **EMI Rejection Ratio: 45dB at 1GHz**
- Input Bias Current: 75nA Maximum
- CMRR/PSRR: 95dB/90dB
- Shutdown Current: 7µA Maximum
- Operating Temperature Range: –40°C to 125°C
- Single in 6-Lead TSOT-23, 2mm × 2mm DFN Packages
- Dual in 8-Lead MS8, MS10, TSOT-23, 2mm × 2mm DFN Packages
- Quad in MS16 Package

APPLICATIONS

- Micropower Active Filters
- Portable Instrumentation
- Battery or Solar Powered Systems
- Automotive Electronics

DESCRIPTION

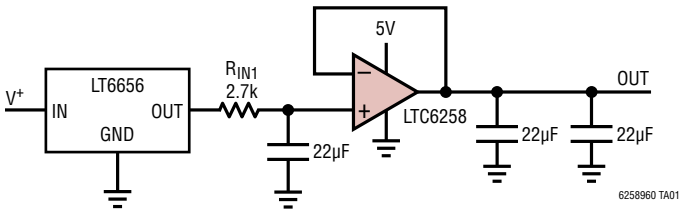
The LTC®6258/LTC6259/LTC6260 are single/dual/quad operational amplifiers with low noise, low power, low supply voltage, and rail-to-rail inputs and outputs. They are unity gain stable with or without capacitive loads. They feature 1.3MHz gain-bandwidth product, 0.24V/µs slew rate while consuming only 20µA of supply current per amplifier operating on supply voltages ranging from 1.8V to 5.25V. The combination of low supply current, low supply voltage, high gain bandwidth product and low noise makes the LTC6258 family unique among rail-to-rail input/output op amps with similar supply current. These operational amplifiers are ideal for power efficient applications.

For applications that require power-down, the LTC6258 in 2mm × 2mm DFN and LTC6259 MS10 packages respectively offer shutdown which reduces the current consumption to 7µA maximum.

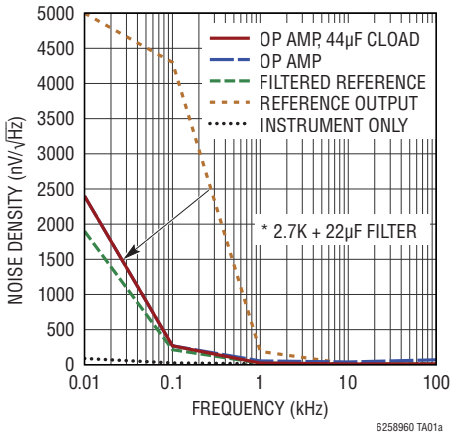
The LTC6258 family can be used as plug-in replacements for many commercially available op amps to reduce power and improve input/output range and performance.

TYPICAL APPLICATION

Low Noise Reference



Reference Buffer Noise Density



ABSOLUTE MAXIMUM RATINGS

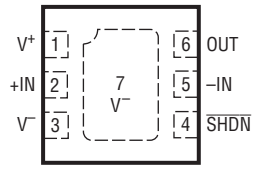
(Note 1)

Supply Voltage: $V^+ – V^–$ 5.5V
Input Voltage ..... $V^–$ – 0.2 to V^+ + 0.2
Input Current: +IN, –IN, $\overline{SHDN}$ (Note 2) ..... ±10mA
Output Current: OUT ..... ±20mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4).....–40°C to 125°C

Specified Temperature Range (Note 5)
LTC6258I/LTC6259I/LTC6260I .....–40°C to 85°C
LTC6258H/LTC6259H/LTC6260H .....–40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TS8, MS8, MS only.....300°C

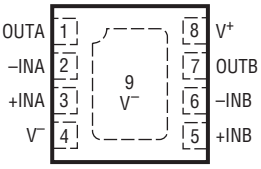
PIN CONFIGURATION

TOP VIEW



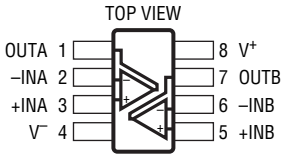
DC PACKAGE
6-LEAD (2mm × 2mm × 0.8mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (NOTE 6)
EXPOSED PAD (PIN 7) IS $V^–$, MUST BE SOLDERED TO PCB

TOP VIEW



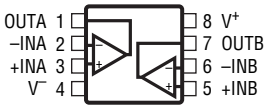
DC PACKAGE
8-LEAD (2mm × 2mm × 0.8mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (NOTE 6)
EXPOSED PAD (PIN 9) IS $V^–$, MUST BE SOLDERED TO PCB

TOP VIEW



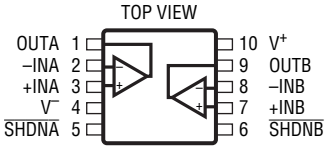
TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 195°C/W (NOTE 6)

TOP VIEW



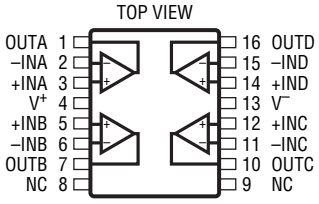
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W (NOTE 6)

TOP VIEW



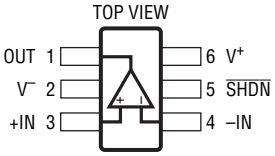
MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 160°C/W (NOTE 6)

TOP VIEW



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 125°C/W (NOTE 6)

TOP VIEW



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 192°C/W (NOTE 6)

ORDER INFORMATION

http://www.linear.com/product/LTC6258#orderinfo

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6258IS6#TRMPBF	LTC6258IS6#TRPBF	LTGWD	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6258HS6#TRMPBF	LTC6258HS6#TRPBF	LTGWD	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6258IDC#TRMPBF	LTC6258IDC#TRPBF	LGZS	6-Lead Plastic DFN (2mm × 2mm × 0.8mm)	–40°C to 85°C
LTC6258HDC#TRMPBF	LTC6258HDC#TRPBF	LGZS	6-Lead Plastic DFN (2mm × 2mm × 0.8mm)	–40°C to 125°C
LTC6259ITS8#TRMPBF	LTC6259ITS8#TRPBF	LTGWX	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC6259HTS8#TRMPBF	LTC6259HTS8#TRPBF	LTGWX	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC6259IDC#TRMPBF	LTC6259IDC#TRPBF	LGWT	8-Lead (2mm × 2mm × 0.8mm) Plastic DFN	–40°C to 85°C
LTC6259HDC#TRMPBF	LTC6259HDC#TRPBF	LGWT	8-Lead (2mm × 2mm × 0.8mm) Plastic DFN	–40°C to 125°C
TUBE				
LTC6259IMS8#PBF	LTC6259IMS8#TRPBF	LTGWW	8-Lead Plastic MSOP	–40°C to 85°C
LTC6259HMS8#PBF	LTC6259HMS8#TRPBF	LTGWW	8-Lead Plastic MSOP	–40°C to 125°C
LTC6259IMS#PBF	LTC6259IMS8#TRPBF	LTGWY	10-Lead Plastic MSOP	–40°C to 85°C
LTC6259HMS#PBF	LTC6259HMS8#TRPBF	LTGWY	10-Lead Plastic MSOP	–40°C to 125°C
LTC6260IMS#PBF	LTC6260IMS#TRPBF	6260	16-Lead Plastic MSOP	–40°C to 85°C
LTC6260HMS#PBF	LTC6260HMS#TRPBF	6260	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Parts ending with PBF are RoHS and WEEE Compliant.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/.

5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{SUPPLY} = 5V, V_{CM} = V_{OUT} = V_{SUPPLY}/2, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^- + 0.3V	 ●	–400 –1000	100	400 1000	µV µV
		V_{CM} = V^+ – 0.3V	 ●	–400 –1000	100	400 1000	µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	V_{CM} = V^- + 0.3V, V^+ – 0.3V			1.5		µV/°C
I_B	Input Bias Current (Note 7)	V_{CM} = V^- + 0.3V	●	–75	–5	75	nA
		V_{CM} = V^+ – 0.3V	●	–75	0	75	nA
I_{OS}	Input Offset Current	V_{CM} = V^- + 0.3V	●	–75	–1	75	nA
		V_{CM} = V^+ – 0.3V	●	–75	–1	75	nA
e_n	Input Voltage Noise Density	f = 1kHz			38		nV/√Hz
	Input Noise Voltage	f = 0.1Hz to 10Hz			2		μV_{P-P}
i_n	Input Current Noise Density	f = 1kHz, V_{CM} = 0V to 4V f = 1kHz, V_{CM} = 4V to 5V			500 500		fA/√Hz fA/√Hz
R_{IN}	Input Resistance	Differential Common Mode		1 10			MΩ MΩ

5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{SUPPLY} = 5V, V_{CM} = V_{OUT} = V_{SUPPLY}/2, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	Differential Common Mode			0.65 1.2		pF pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.3V to 3.5V V_{CM} = –0.1V to 5.1V	● ●	66 64	95 95		dB dB
IVR	Input Voltage Range		●	–0.1		5.1	V
PSRR	Power Supply Rejection Ratio	V_{CM} = 0.4V, V_S = 1.8V to 5.25V	 ●	78 68	90		dB dB
	Supply Voltage Range		●	1.8		5.25	V
A_V	Large Signal Gain	V_{OUT} = 0.5V to 4.5V, R_{LOAD} = 100k	 ●	14 2.8	40		V/mV V/mV
		V_{OUT} = 0.5V to 4.5V, R_{LOAD} = 10k	 ●	3.5 0.5	10		V/mV V/mV
V_{OL}	Output Swing Low (Input Overdrive 30mV). Measured from V^-	No Load	 ●		12	40 50	mV mV
		I_{SINK} = 100µA	 ●		80	105 120	mV mV
		I_{SINK} = 1mA	 ●		145	180 250	mV mV
V_{OH}	Output Swing High (Input Overdrive 30mV). Measured from V^+	No Load	 ●		25	40 65	mV mV
		I_{SOURCE} = 100µA	 ●		35	55 100	mV mV
		I_{SOURCE} = 1mA	 ●		100	140 350	mV mV
I_{SC}	Output Short-Circuit Current		 ●	4 1	10		mA mA
I_S	Supply Current per Amplifier		 ●	16 11	20	23 25	µA µA
	Supply Current in Shutdown		 ●		4	5 7	µA µA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.6V $V_{\overline{SHDN}}$ = 1.5V	● ●		60 0	200 15	nA nA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable	●			0.6	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable	●	1.5			V
t_{ON}	Turn-On Time	$\overline{SHDN}$ Toggle from 0V to 5V			152		µs
t_{OFF}	Turn-Off Time	$\overline{SHDN}$ Toggle from 5V to 0V			7		µs
GBW	Gain-Bandwidth Product	f = 10kHz	 ●	1.0 0.4	1.3		MHz MHz
t_S	Settling Time, 0.5V to 4.5V, Unity Gain	0.1% 0.01%			14 18		µs µs
SR	Slew Rate	A_V = –1, V_{OUT} = 0.5V to 4.5V, C_{LOAD} = 10pF, R_F = R_G = 10kΩ	 ●	0.2 0.1	0.24		V/µs V/µs
FPBW	Full Power Bandwidth (Note 8)	$4V_{P-P}$			20		kHz
THD+N	Total Harmonic Distortion and Noise	f = 500Hz, A_V = 2, R_L = 4kΩ, V_{OUTP-P} = 1V V_{IN} = 2.25V to 2.75V			0.025 72		% dB
I_{LEAK}	Output Leakage Current in Shutdown	$V_{\overline{SHDN}}$ = 0V, V_{OUT} = 0V $V_{\overline{SHDN}}$ = 0V, V_{OUT} = 5V	● ●		100 100		nA nA
%MP	Large Signal Overshoot	V_{IN} = 0.5V to 4.5V, A_V = 1, C_L = 100nF			2.7		%
EMIRR	Electromagnetic Interference Rejection Ratio	Input Power –10dB to Input Pins at 1GHz			45		dB

1.8V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{SUPPLY} = 1.8V, V_{CM} = V_{OUT} = 0.4V, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^- + 0.3V	 ●	–400 –1000	100	400 1000	µV µV
		V_{CM} = V^+ – 0.3V	 ●	–400 –1000	100	400 1000	µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	V_{CM} = V^- + 0.3V, V^+ – 0.3V			1.5		µV/°C
I_B	Input Bias Current (Note 7)	V_{CM} = V^- + 0.3V	●	–75	2	75	nA
		V_{CM} = V^+ – 0.3V	●	–75	5	75	nA
I_{OS}	Input Offset Current	V_{CM} = V^- + 0.3V	●	–75	2	75	nA
		V_{CM} = V^+ – 0.3V	●	–75	2	75	nA
e_n	Input Voltage Noise Density	f = 1kHz, V_{CM} = 0.4V			38		nV/√Hz
	Input Noise Voltage	f = 0.1Hz to 10Hz			2		μV_{P-P}
i_n	Input Current Noise Density	f = 1kHz, V_{CM} = 0V to 0.8V f = 1kHz, V_{CM} = 1V to 1.8V			500 500		fA/√Hz fA/√Hz
R_{IN}	Input Resistance	Differential Common Mode		1 10			MΩ MΩ
C_{IN}	Input Capacitance	Differential Common Mode			0.65 1.2		pF pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.2V to 1.6V	 ●	70 61	90		dB dB
IVR	Input Voltage Range		●	–0.1		1.9	V
PSRR	Power Supply Rejection Ratio	V_{CM} = 0.4V, V_S = 1.8V to 5.25V	 ●	78 68	90		dB dB
A_V	Large Signal Gain	V_{OUT} = 0.5V to 1.3V, R_{LOAD} = 100k	 ●	15 1.6	50		V/mV V/mV
		V_{OUT} = 0.5V to 1.3V, R_{LOAD} = 10k	 ●	4 0.4	10		V/mV V/mV
V_{OL}	Output Swing Low (Input Overdrive 30mV), Measured from V^-	No Load	 ●		15	30 50	mV mV
		I_{SINK} = 100µA	 ●		80	110 130	mV mV
		I_{SINK} = 1mA	 ●		150	200 230	mV mV

1.8V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{SUPPLY} = 1.8V, V_{CM} = V_{OUT} = 0.4V, C_L = 10pF, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output Swing High (Input Overdrive 30mV), Measured from V^+	No Load	 ●		25	40 50	mV mV
		I_{SOURCE} = 100µA	 ●		35	60 100	mV mV
		I_{SOURCE} = 1mA	 ●		95	140 300	mV mV
I_{SC}	Output Short-Circuit Current		 ●	4 1	10		mA mA
I_S	Supply Current per Amplifier		 ●	17 10	20	21 23	µA µA
	Supply Current in Shutdown		 ●		1.0	1.5 2	µA µA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.5V $V_{\overline{SHDN}}$ = 1.5V	● ●		50 0	80 10	nA nA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable	●			0.5	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable	●	1.5			V
t_{ON}	Turn-On Time	$\overline{SHDN}$ Toggle From 0V to 1.8V			47		µs
t_{OFF}	Turn-Off Time	$\overline{SHDN}$ Toggle From 1.8V to 0V			17		µs
GBW	Gain-Bandwidth Product	f = 10kHz	 ●	1.0 0.4	1.3		MHz MHz
T_S	Settling Time, 0.3V to 1.5V, Unity Gain	0.1% 0.01%			7 12		µs µs
SR	Slew Rate	A_V = –1, V_{OUT} = 0.3V to 1.5V, C_{LOAD} = 10pF R_F = R_G = 10kΩ	 ●	0.16 0.1	0.22		V/µs V/µs
FPBW	Full Power Bandwidth (Note 8)	$1.2V_{P-P}$			58		kHz
THD+N	Total Harmonic Distortion and Noise	f = 500Hz, A_V = 2, R_L = 4kΩ, V_{OUTP-P} = 1V V_{IN} = 0.65V to 0.15V			0.04 68		% dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes as well as ESD protection diodes to each power supply. If the differential input voltage exceeds 1.4V or the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: LTC6258I/LTC6259I/LTC6260I and LTC6258H/LTC6259H/LTC6260H are guaranteed functional over the temperature range of –40°C to 125°C.

Note 5: The LTC6258I/LTC6259I/LTC6260I are guaranteed to meet specified performance from –40°C to 85°C. The LTC6258H/LTC6259H/LTC6260H are guaranteed to meet specified performance from –40°C to 125°C.

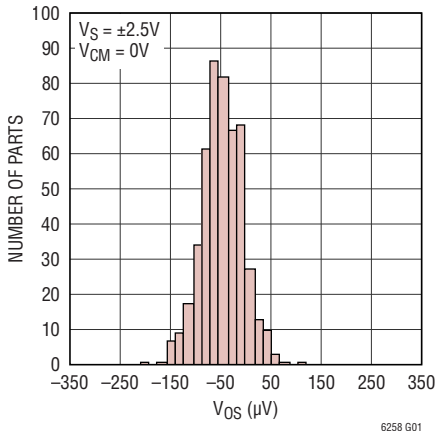
Note 6: Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

Note 7: The input bias current is the average of the currents into the positive and negative input pins.

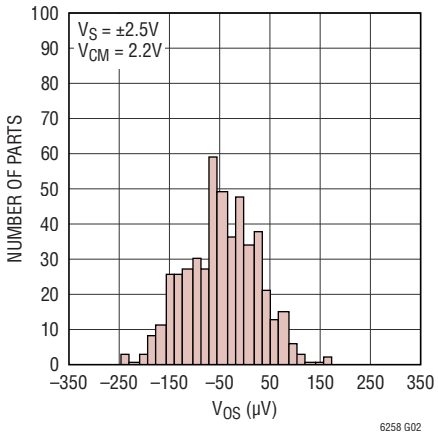
Note 8: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}.

TYPICAL PERFORMANCE CHARACTERISTICS

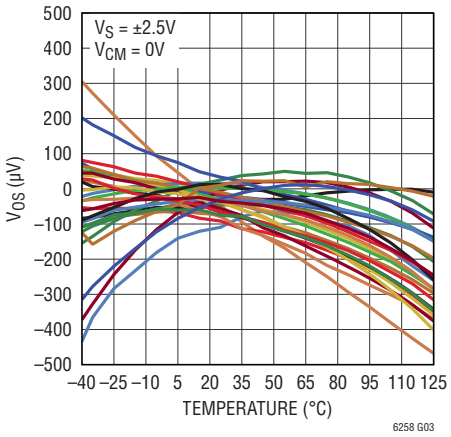
Input V_{OS} Histogram



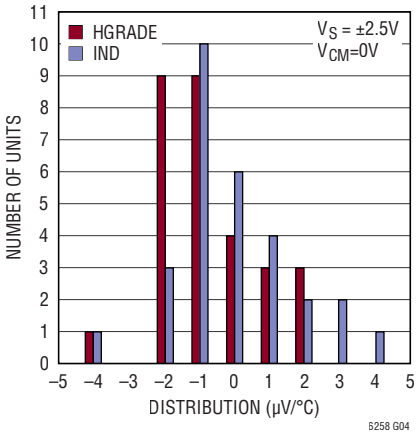
Input V_{OS} Histogram



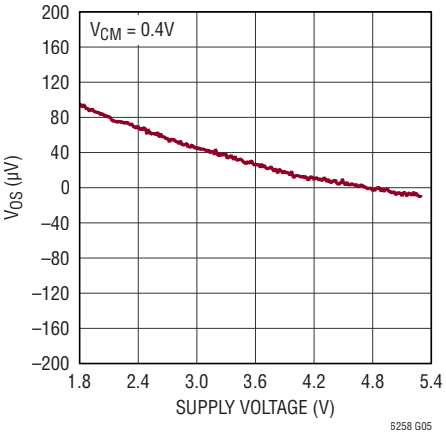
V_{OS} vs Temperature



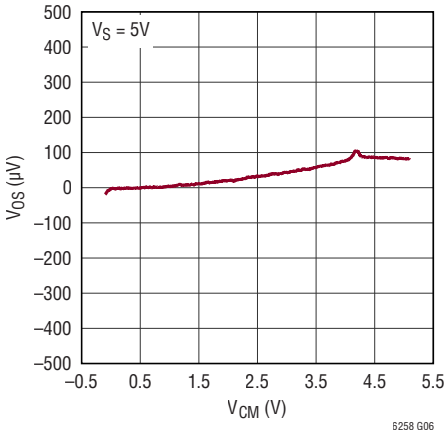
Input Offset Drift Distribution



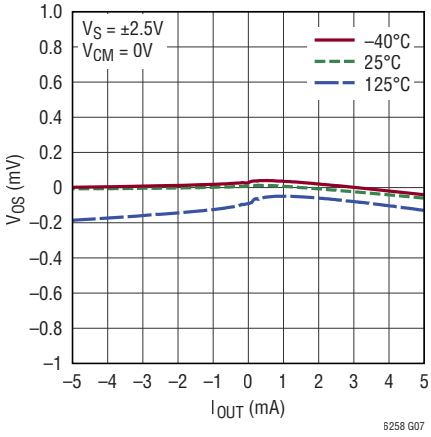
V_{OS} vs Supply Voltage (25°C)



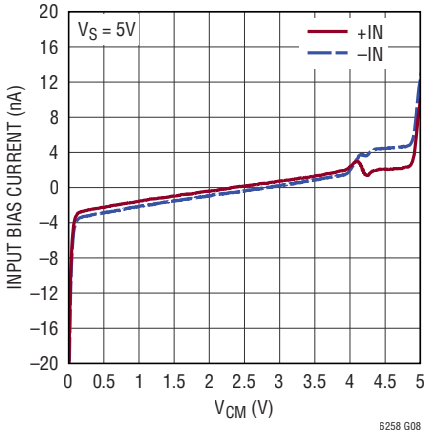
V_{OS} vs Common Mode Voltage



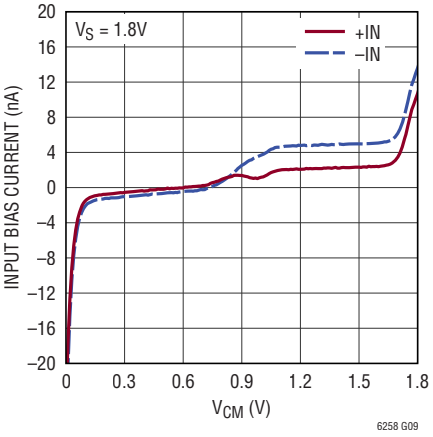
V_{OS} vs I_{OUT}



Input Bias Current vs Common Mode Voltage

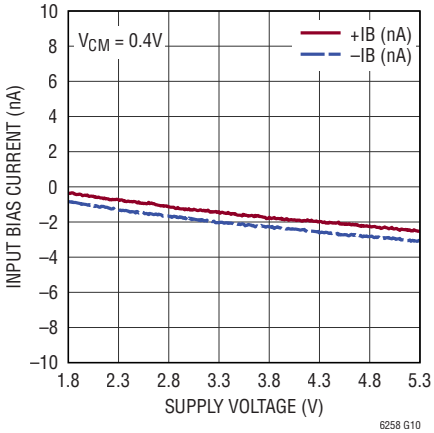


Input Bias Current vs Common Mode Voltage

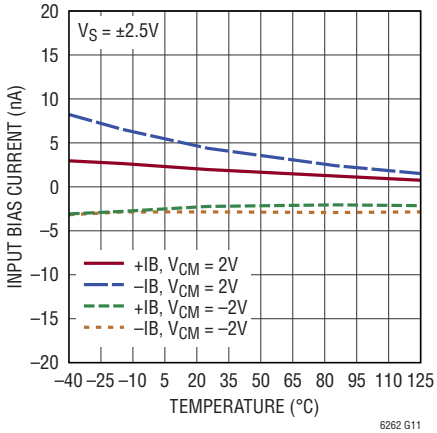


TYPICAL PERFORMANCE CHARACTERISTICS

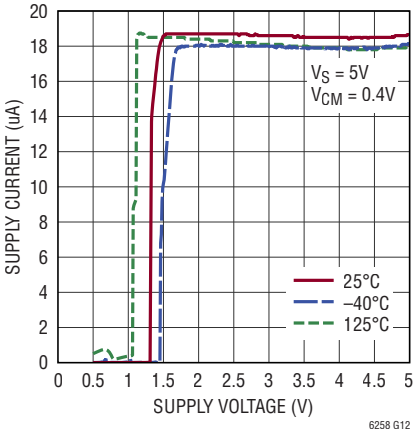
Input Bias Current vs Supply Voltage



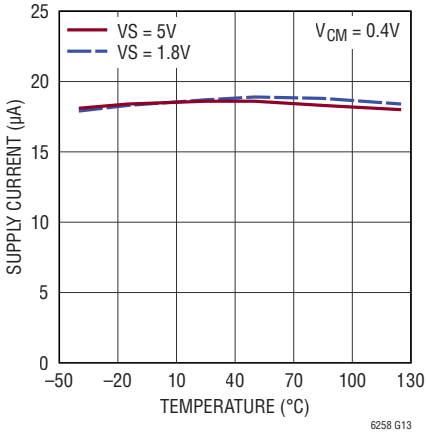
Input Bias Current vs Temperature



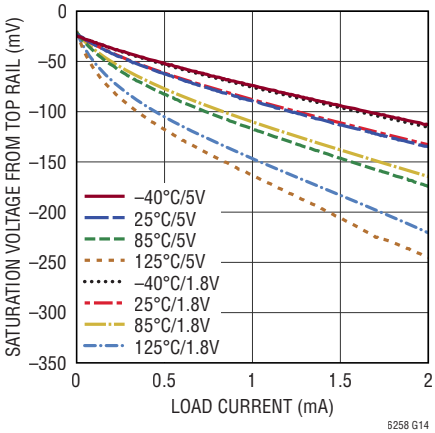
Supply Current vs Supply Voltage per Channel



Supply Current vs Temperature Per Channel



Output Saturation Voltage vs Load Current



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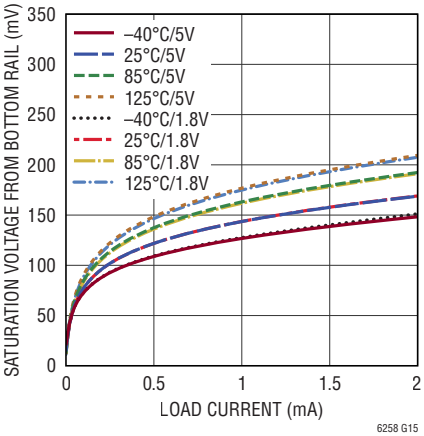
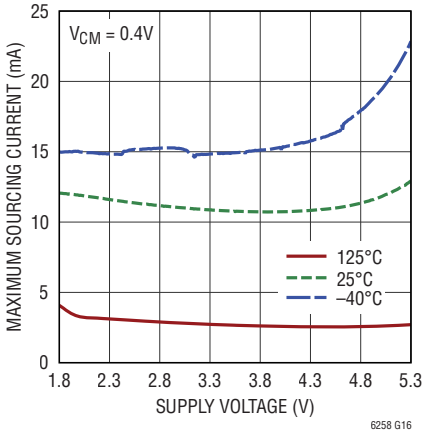
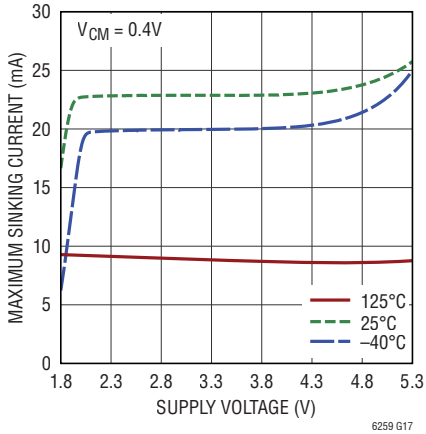


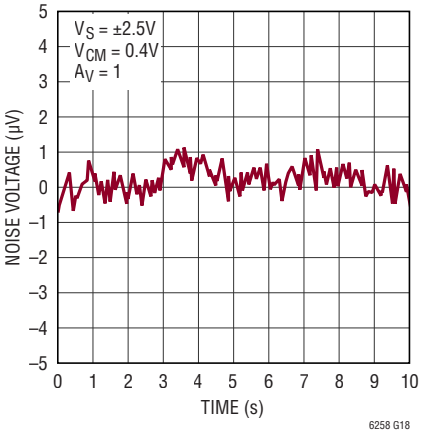
Output Short-Circuit Current vs Supply Voltage (Sourcing)



Output Short-Circuit Current vs Supply Voltage (Sinking)

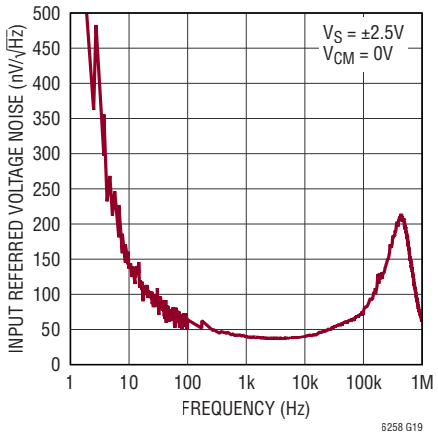


0.1Hz to 10Hz Output Voltage Noise

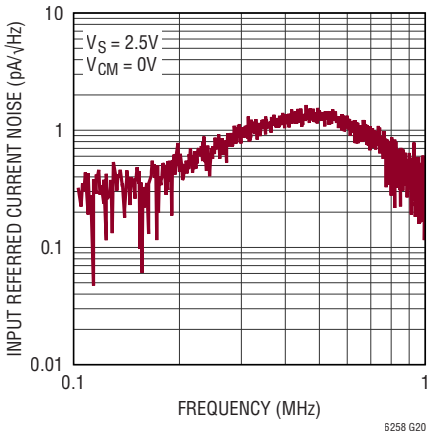


TYPICAL PERFORMANCE CHARACTERISTICS

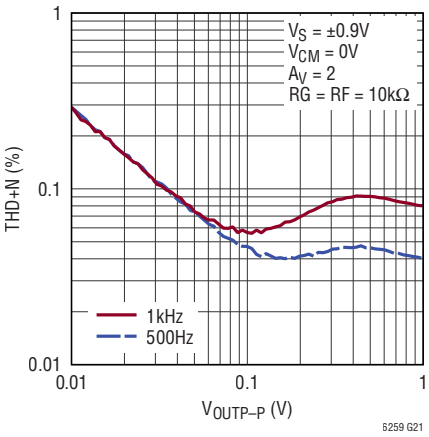
Noise Voltage Density vs Frequency



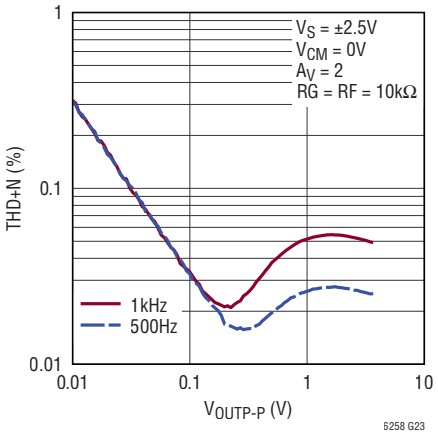
Input Referred Current Noise vs Frequency



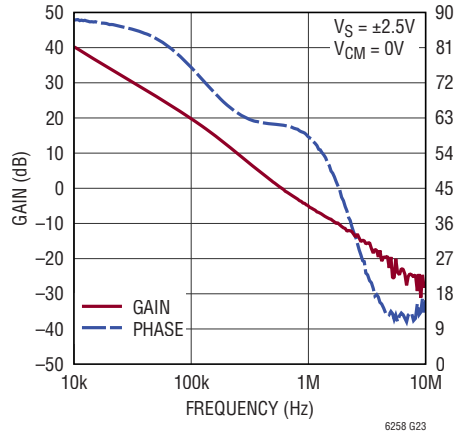
Total Harmonic Distortion and Noise



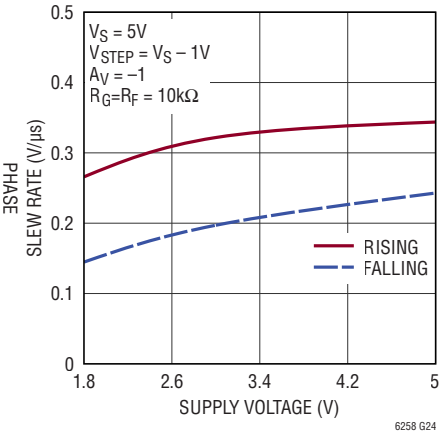
Total Harmonic Distortion and Noise



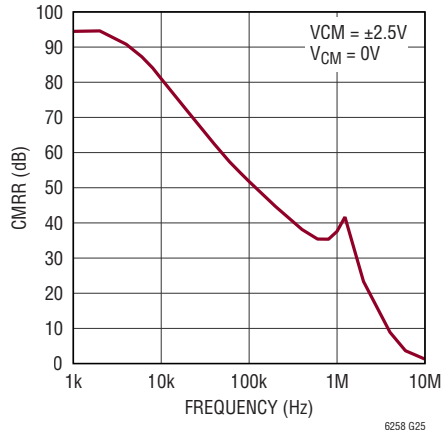
Gain and Phase vs Frequency



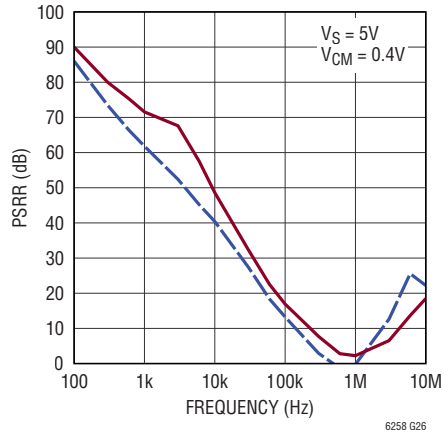
Slew Rate vs Supply Voltage



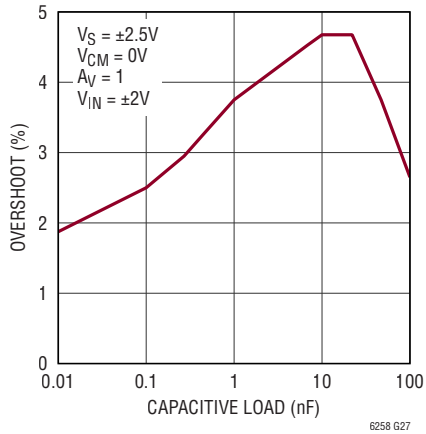
Common Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency

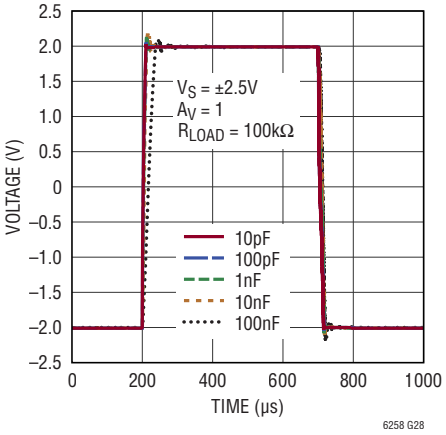


Capacitive Load Handling Overshoot vs Capacitive Load

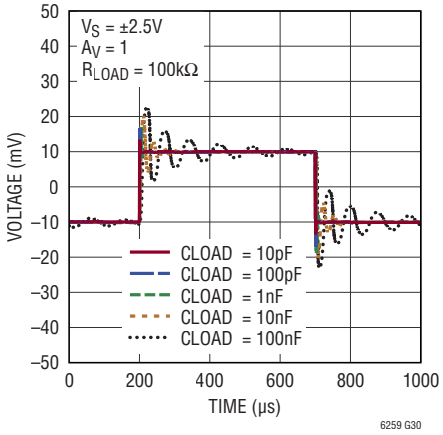


TYPICAL PERFORMANCE CHARACTERISTICS

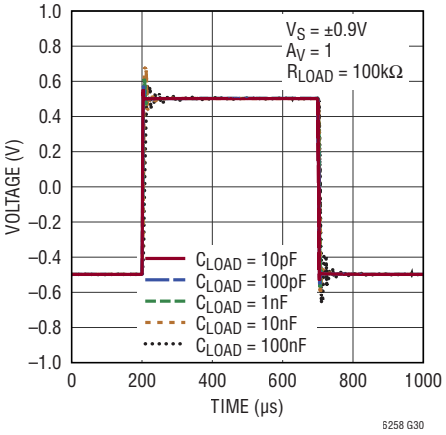
Large-Signal Response



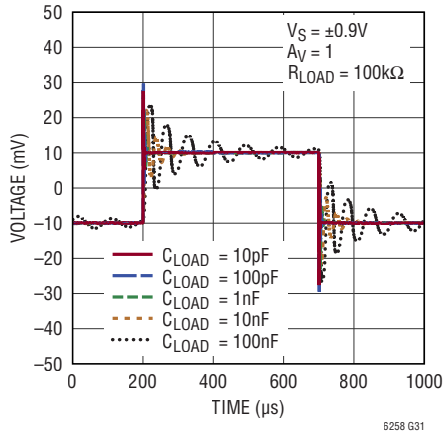
Small-Signal Response



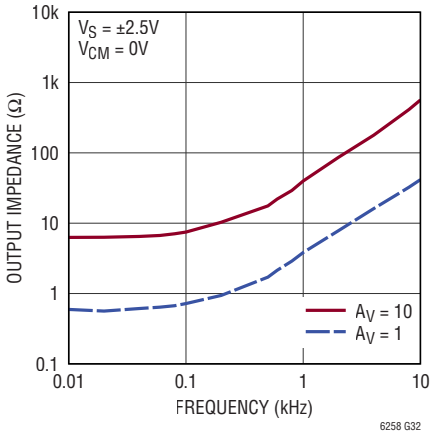
Large-Signal Response



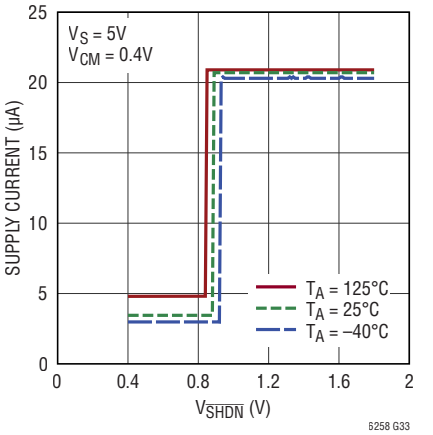
Small-Signal Response



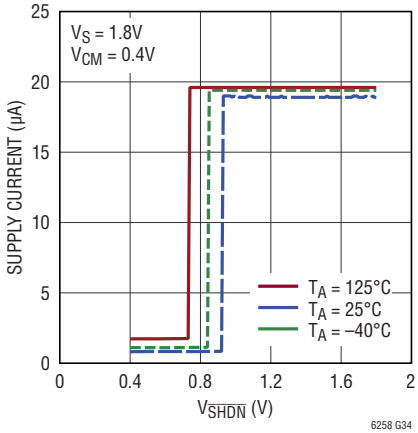
Output Impedance vs Frequency



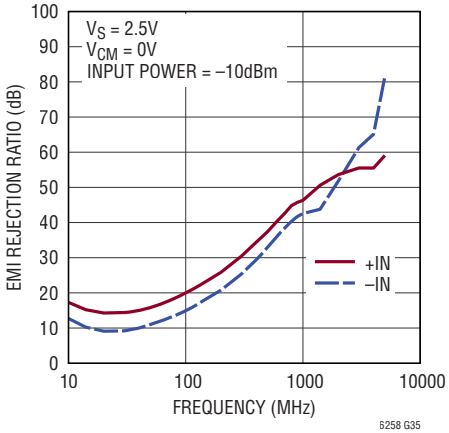
Supply Current vs $\overline{SHDN}$ Pin Voltage



Supply Current vs $\overline{SHDN}$ Pin Voltage



Electromagnetic Interference Rejection Ratio



PIN FUNCTIONS

–IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- – 0.1V to V^+ + 0.1V.

+IN: Noninverting Input of Amplifier. This pin has the same voltage range as –IN.

V^+: Positive Power Supply. Typically the voltage is from 1.8V to 5.25V. Split supplies are possible as long as the voltage between V^+ and V^- is between 1.8V and 5.25V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^-: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 1.8V to 5.25V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

$\overline{\text{SHDN}}$: Active Low Shutdown. Shutdown threshold is 0.6V above negative rail. If left unconnected, the amplifier will be on.

OUT: Amplifier Output. Rail-to rail amplifier output capable of delivering 4mA.

SIMPLIFIED SCHEMATIC

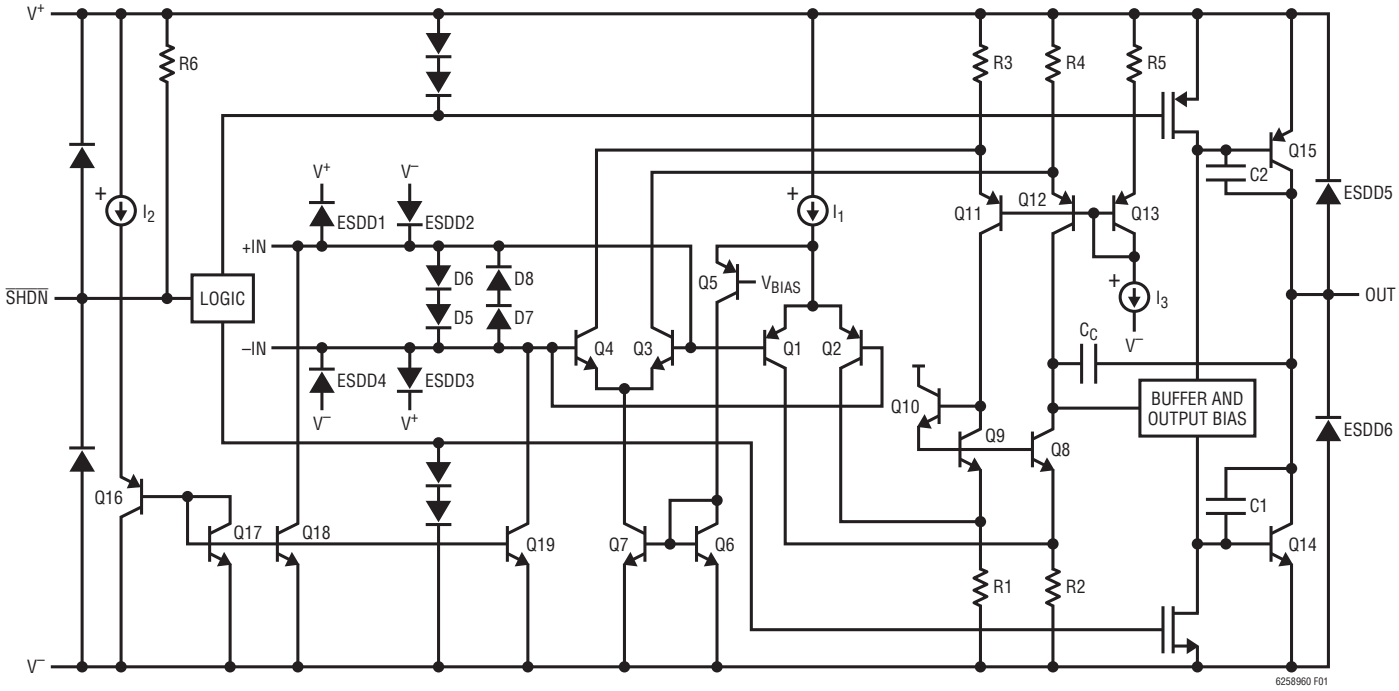


Figure 1. LTC6258/LTC6259/LTC6260 Simplified Schematic

OPERATION

The LTC6258 family input signal range extends beyond the negative and positive power supplies. Figure 1 depicts a Simplified Schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage Q1/Q2 and NPN stage Q3/Q4 that are active over different ranges of common mode input voltage. The PNP stage is active between the negative power supply to approximately 1V below the positive supply. As the input voltage approaches the positive supply, transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the remaining input common mode range. Also for the input stage, devices Q17, Q18 and Q19 act to cancel the bias current of the PNP input pair. When Q1/Q2 is active, the current in Q16 is controlled to be the same as the current Q1/Q2. Thus, the base current of Q16 is normally equal to the base current of the input devices of Q1/Q2. Similar circuitry (not shown) is used to cancel the base current of Q3/Q4. The buffer and output bias stage uses a special compensation technique to take full advantage of the process technology to drive high capacitive loads. The common emitter topology of Q14/Q15 enables the output to swing from rail to rail.

APPLICATIONS INFORMATION

Low Supply Voltage and Low Power Consumption

The LTC6258 family of operational amplifiers can operate with power supply voltages from 1.8V to 5.25V. Each amplifier draws 20µA. The low supply voltage capability and low supply current are ideal for portable applications.

High Capacitive Load Driving Capability and Wide Bandwidth

The LTC6258 family is optimized for wide bandwidth low power applications. They have a high gain-bandwidth to power ratio and are unity gain stable. When the load capacitance increases, the increased capacitance at the output pushes the non-dominant pole to lower frequency in the open loop frequency response, worsening the phase and gain margin. The LTC6258 family are designed to directly drive up to 100nF of capacitive load in unity gain configuration (see Typical Performance Characteristics, Capacitive Load Handling).

Low Input Referred Noise

The LTC6258 family provides a low input referred noise of 38nV/$\sqrt{Hz}$ at 1kHz. The average noise voltage density over a 100kHz bandwidth is less than 80nV/$\sqrt{Hz}$. The LTC6258 family is ideal for low noise and low power signal processing applications.

Low Input Offset Voltage

The LTC6258 family has a low offset voltage of 400µV, which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage over the entire common mode voltage range.

Low Input Bias Current

The LTC6258 family uses a bias current cancellation circuit to compensate for the base current of the input transistors. When the input common mode voltage is within 200mV of either rail, the bias cancellation circuit is no longer active. For common mode voltages ranging from 0.2V above the negative supply to 0.2V below the positive supply, the low input bias current allows the amplifiers to be used in applications with high resistance sources.

Ground Sensing and Rail to Rail Output

The LTC6258 family delivers over 4mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 300mV of either rail. If output swing to the negative rail is required, an external pull down resistor to a negative supply can be added. For 5V/0V op amp supplies, a pull down resistor of 10k to –2V will allow a 'true zero' output swing. In this case, the output can swing all the way to the bottom rail while maintaining 45dB of open loop gain. Since the inputs can go 100mV beyond either rail, the op amp can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the maximum output current also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

EMI Rejection

Electromagnetic interference (EMI) rejection is built into the LTC6258 op amp family. Rejection is measured by injecting 200mV$_{P-P}$ (–10dBm) RF signal into the pins and measuring the offset change (delta_VOS). The rejection ratio is calculated as 20log (100mV/delta_VOS).

Input Protection and Output Overdrive

To prevent breakdown of the input transistors, the input stages are protected against a large differential input voltage by two pairs of back-to-back diodes, D5 to D8. If the differential input voltage exceeds 1.4V, the current in these diodes must be limited to less than 10mA. These amplifiers are not intended for open loop applications such as comparators. When the output stage is overdriven, internal limiting circuitry is activated to improve overdrive recovery. In some applications, this circuitry may draw as much as 1mA supply current.

APPLICATIONS INFORMATION

ESD

The LTC6258 family has reverse-biased ESD protection diodes on all inputs and output as shown in Figure 1.

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

Feedback Components

Care must be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration with gain and feedback resistors of 100k, a poorly designed circuit board layout with parasitic capacitance of 5pF (part +PC board) at the amplifier's inverting input will cause the amplifier to oscillate due to a pole formed at 640kHz. An additional capacitor of 4.7pF across the feedback resistor as shown in Figure 2 will eliminate any ringing or oscillation.

Shutdown

The single and dual versions have package options with $\overline{SHDN}$ pins that can shut down the amplifier to less than 7µA supply current. The $\overline{SHDN}$ pin voltage needs to be within 0.6V of V^- for the amplifier to shut down. During shutdown, the output is in a high output impedance state. When left floating, the $\overline{SHDN}$ pin is internally pulled up to the positive supply and the amplifier remains enabled.

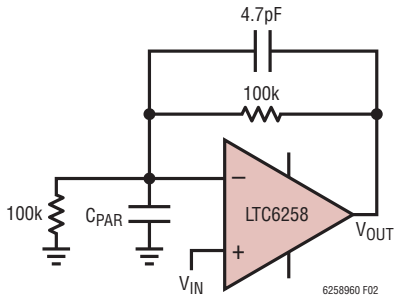


Figure 2.

Active Filter

The bandpass filter Figure 3a is AC-coupled to an input. As a result, LTC6259 input does not place a burden on the previous stage to develop an absolute common mode voltage. A simple resistor divider with RA1 and RA2 provides biasing for the LTC6259 inputs. Pegging the op amp inputs to a fixed voltage helps to reduce distortion that might arise with moving common mode. This filter is centered at 10kHz. The exact resistance and capacitance values can be tweaked upwards or downwards, depending on whether lowest resistor noise or lowest total supply current is more important.

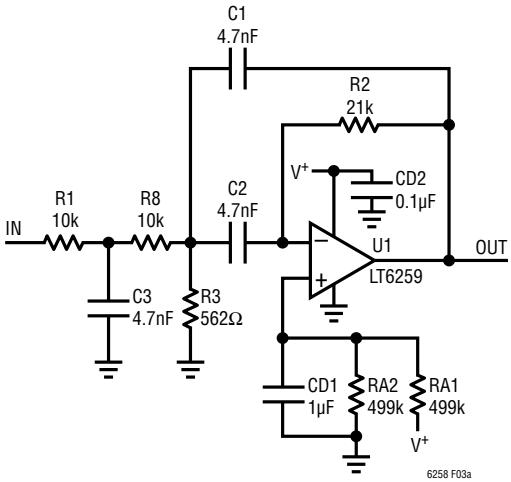


Figure 3a. 10kHz Bandpass Filter

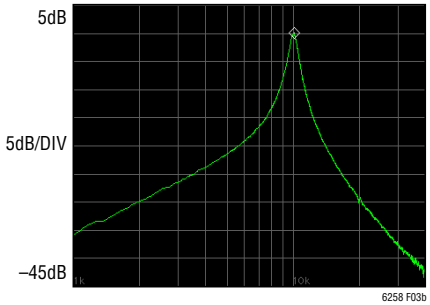


Figure 3b. Frequency Response of 10kHz Bandpass Filter of Figure 3a

APPLICATIONS INFORMATION

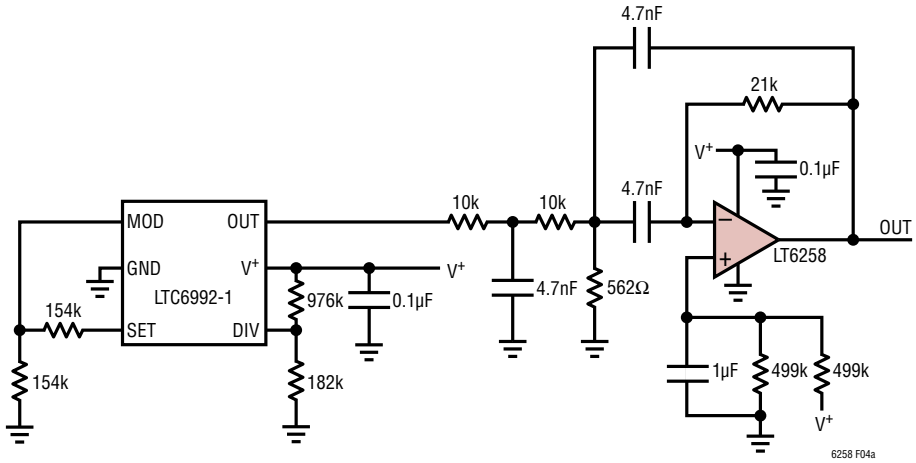


Figure 4a. Low Power Squarewave - Sinewave Oscillator

Low Power Sine Wave Generator

A low power sine wave generator can be derived by driving a square wave into the bandpass filter. A complete schematic is shown in Figure 4a. The LTC6992-1 easily configures as a 50% duty cycle 10kHz square wave, and can drive the relatively benign loading seen in the bandpass filter.

Figures 4b and 4c show the LTC6992-1 output and bandpass filter output. THD of the sine wave is –30.5 dBc. Note, even harmonics that appear in the distortion products of the filtered output already appear in the source square wave.

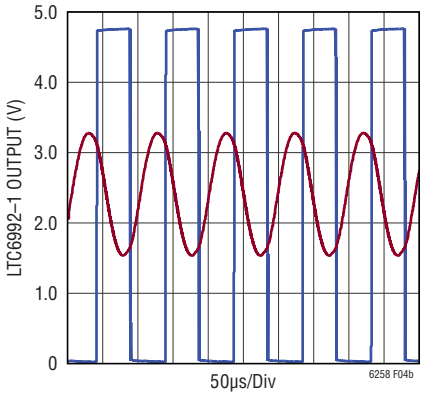


Figure 4b. Low Power Sine Generator

Low Noise Reference

The LT6656 is a 1µA precision series voltage reference. Yet with low power comes low drive current capability and higher noise. The LTC6259 can be used as a buffer that follows a filter to enhance the utilization of the LT6656 in low power applications. Figure 5a shows such a configuration. First a very low cutoff frequency follows the LT6656 output (R_{IN1} and C_{IN1}, lower than 5Hz cutoff). Choice of filter resistor R_{IN1} is such that the bias current in the LTC6259, multiplied by the resistance value, is lower than the nominal offset voltage of the op amp. C_{IN1} can be larger or smaller, with more or less filtering accordingly. The voltage withstanding requirement of C_{IN1} is low, resulting in large capacitance in a small volume.

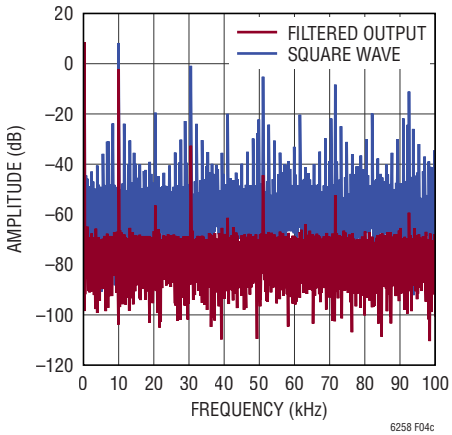


Figure 4c. FFT

APPLICATIONS INFORMATION

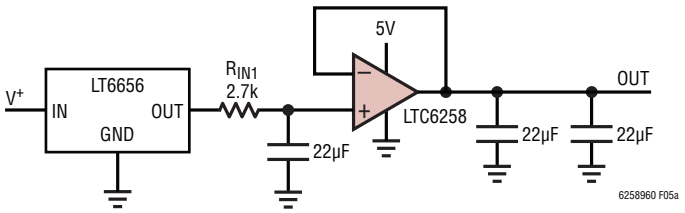


Figure 5a. Low Noise Reference Use LT6656 for a Low Current Starting Reference

This circuit takes advantage of the ability of the LTC6259 to drive large capacitive loads. Use of a large output capacitor attached to the LT6659 enables significant bypassing of follow-on circuits that use the reference voltage. In total, the combination of LT6656 and LTC6259, in this configuration, develops a reference voltage, with low noise, at low power, and with appreciably large available bypass capacitance.

Voltage spectral noise densities are shown in Figure 5b. Larger noise from the reference below 10kHz noticeably drops down once a filter (R_{IN1} and C_{IN1}) follow the reference. The op amp, configured in unity gain, with a large 44µF load, remains stable and contributes only a small amount of low frequency noise. Figure 5c shows the transient response of the combination of R_{IN1}-C_{IN1} filter and op amp circuit, with and without the 44µF output capacitor.

Figure 5c shows the time domain response of the reference buffer.

The total measured supply current consumption is 21µA.

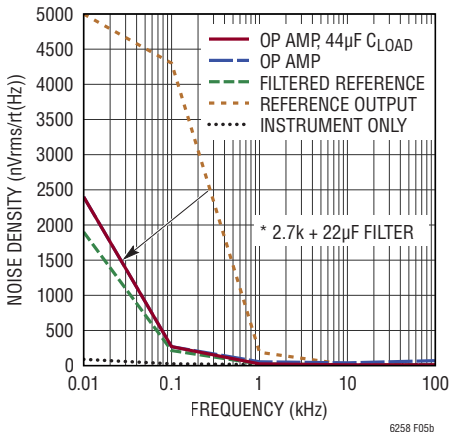


Figure 5b. Noise Density, Reference Buffer

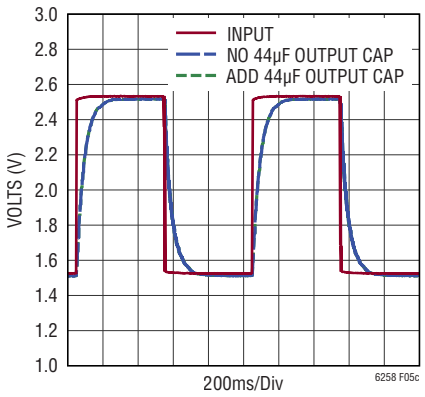


Figure 5c. Reference Buffer Transient Response

Analog LED Control

Figure 6a shows a voltage controlled LED drive circuit. When V_{IN} is at 0V, the op amp supply current is nominally 20µA. The offset, for example, could be 450µV, appears across R1, inducing a 0.45mA current in the LED. Some applications want a guaranteed zero LED current at V_{IN} = 0, and this is the purpose of R5. R5 forces 2.5µA current through R7, creating a negative 0.6mV sense offset. This offset guarantees a zero LED current.

APPLICATIONS INFORMATION

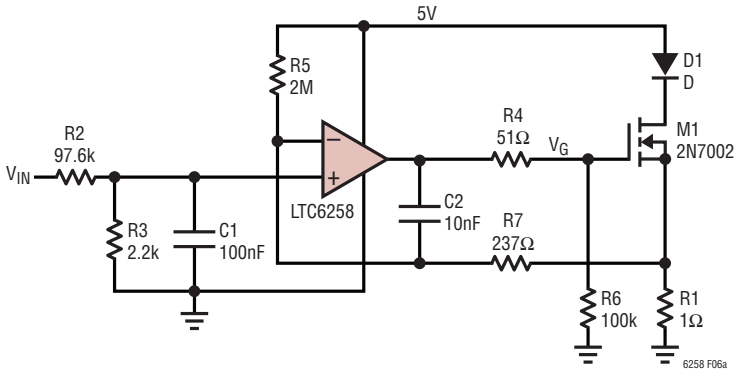


Figure 6a. Lower Power LED Driver with Voltage Command

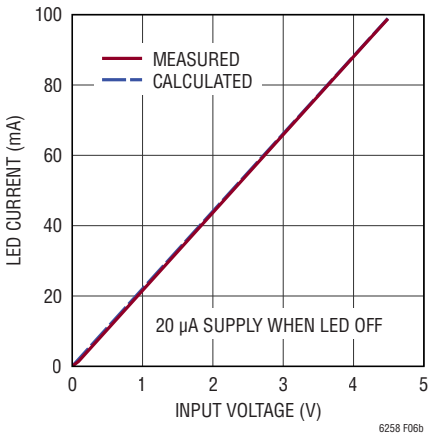


Figure 6b. LED Current

Indeed, the circuit works nicely. Once the input voltage is near 0, the LED current output is 0 and the total supply current is 20µA. Gain from the input voltage to LED current is 0.022A/V, as can be taken from the R2/R3 voltage divider and the sense resistor value.

$$\text{LED Current} = \frac{V_{IN}}{R1} \bullet \frac{R3}{R2+R3}$$

Self-Oscillating LED Driver

Taking the circuit of the above application a step further, the circuit of Figure 7a combines edge detection with use of the shutdown pin of the LTC6259. R2 and R3 bring in a divided down copy of the supply voltage as a reference into the positive terminal. The op amp forces this voltage on the sense resistor R_{SENSE} in "LED ON" operation. In that sense this circuit is similar to the one above.

However, whereas the previous circuit assumes an always-on operation mode, this new circuit hijacks the shutdown pin. C2 can AC couple fast action signals into the signal V_C. Hence when the gate voltage V_G increases when "LED ON" begins, V_C will suddenly rise. V_C connects to the shutdown pin; a rising edge on the shutdown pin enables the LTC6259, which is already active, to stay on. However, M3 is also on while M1 is on, and as a result will work with R9 to charge C2 slowly until V_C falls below the shutdown threshold. At that moment, the active low shutdown kicks in, and the LTC6259 turns off. A negative falling V_G voltage again feeds through C2, and a falling V_C and hence a falling shutdown pin voltage keeps the circuit in an "LED OFF" state for some time. M3 turns off, and C2 discharges until V_C is high enough to reactivate the LTC6259.

It may seem a bit odd to develop such a circuit when a microprocessor or a LTC6992 can provide on-off capability in combination with a single MOSFET and resistor. The problem with those circuits, however, is the lack of control over the LED current. In the circuit of this application, a voltage is controlled across a sense resistor. There is no dependence on the LED voltage in how much current drives the LED. And generation of the on-off, or blinking, comes with the addition of only a handful of low cost components.

APPLICATIONS INFORMATION

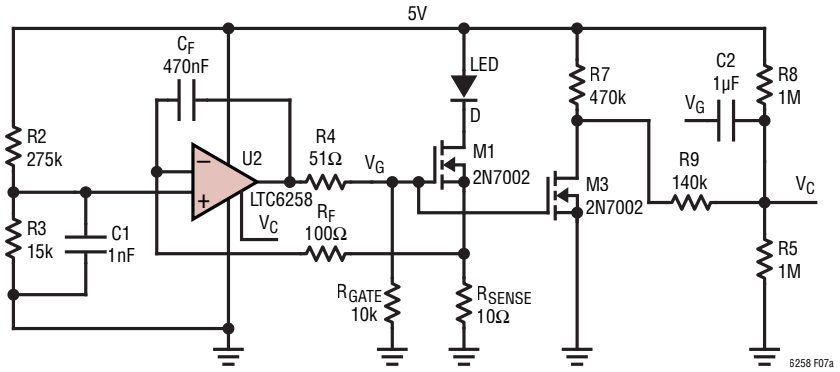


Figure 7a. LED Driver with Self-Oscillation

It is interesting to note that the LED current depends on the supply in this implementation in as much as the supply feeds through R2 and R3 to create a reference. The supply also figures into the time of the on and off cycle since the supply powers the edge detection and relaxation part of the circuitry. When the supply falls, the LED current drops and the cycle time increases. This change of behavior can help in battery powered LED blinking applications to predict end of life.

The figure shows the sense resistor voltage (red) and the shutdown pin voltage (blue). The shutdown voltage is tied to V_C; the gate drive couples through C2 as already described.

Components R_F and C_F may apparently slow edges down greatly. Adding this much delay is not essential, but it can help to smooth out any hiccups that occur when the part goes through a startup sequence after the shutdown pin goes inactive. 47µs as a time constant is insignificant in the time scale of the blinking (10's or 100's of ms). The 47µs is much smaller than any time constant associated with C2 and its resistors.

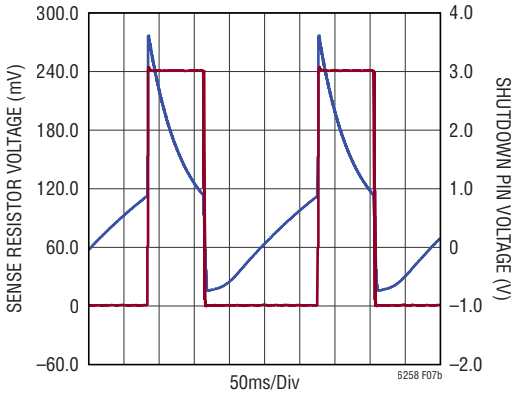
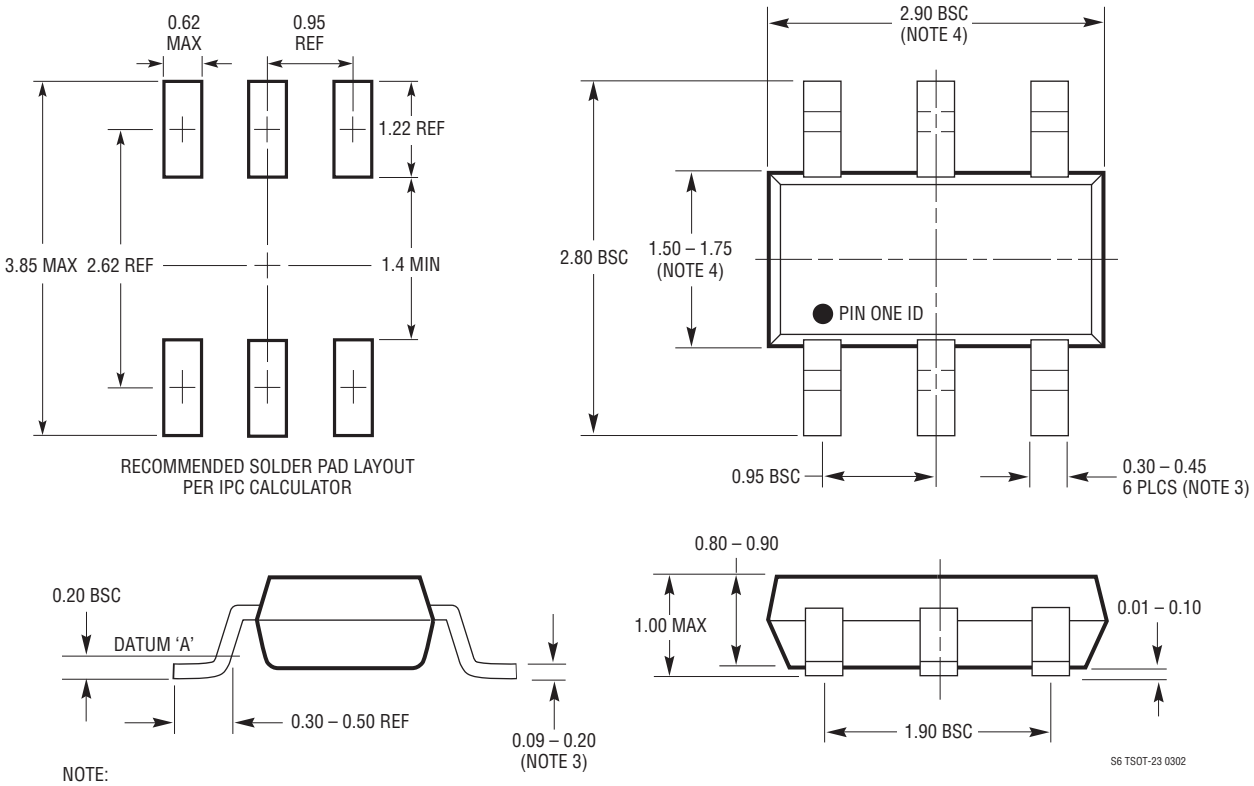


Figure 7b. LED Blinker Circuit

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTCLTC6258#packaging for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

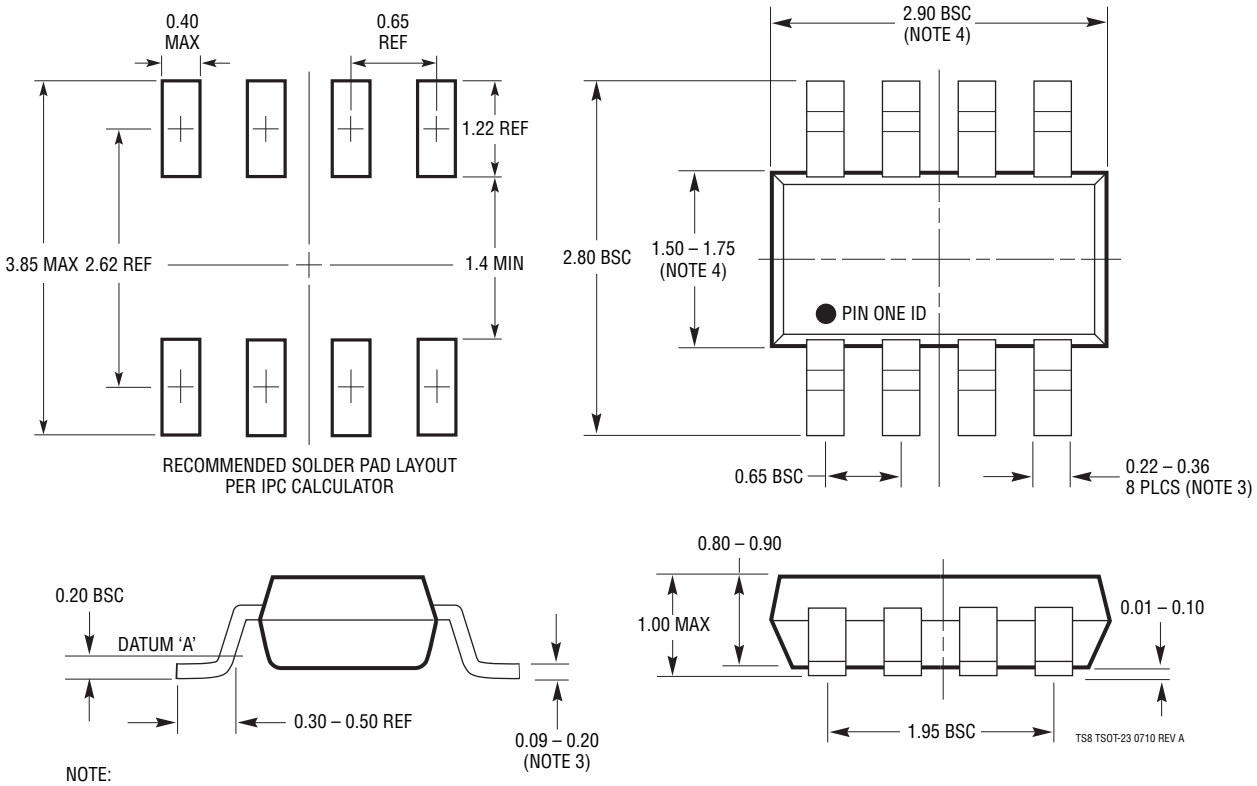


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6259#packaging for the most recent package drawings.

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)

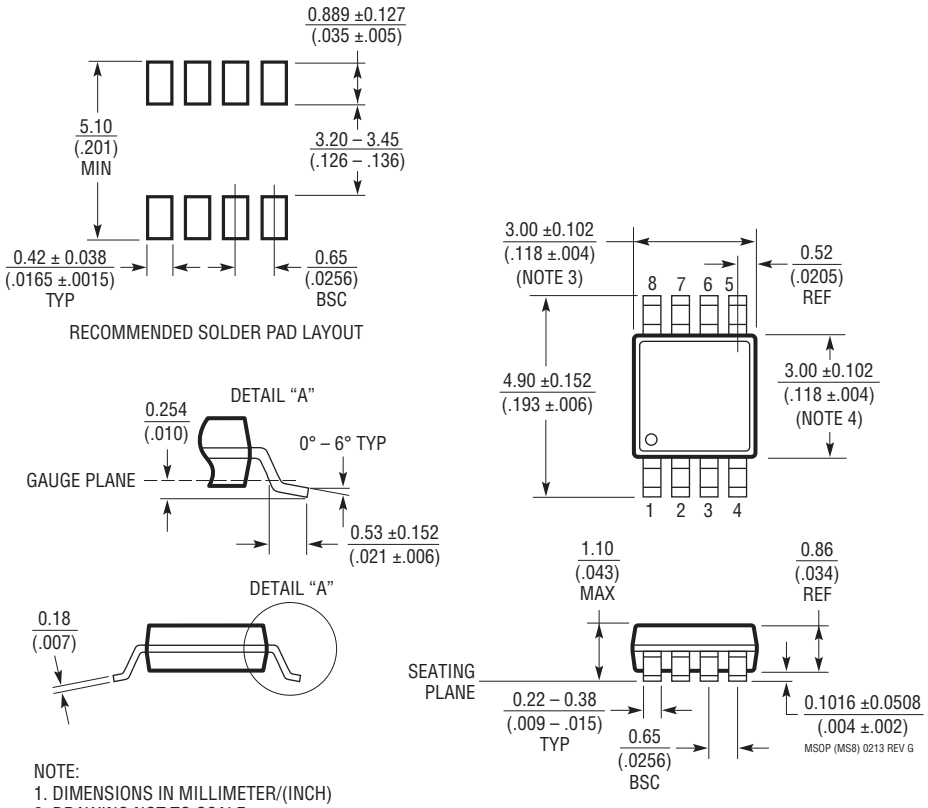


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6259#packaging for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

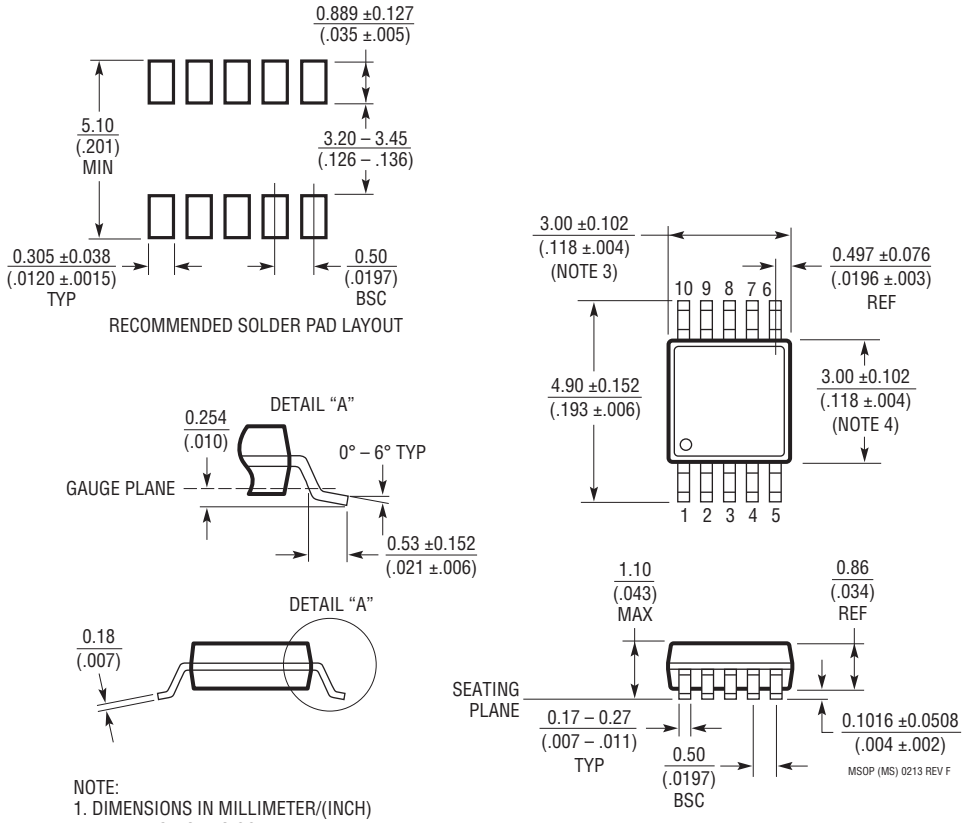


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6259#packaging for the most recent package drawings.

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)

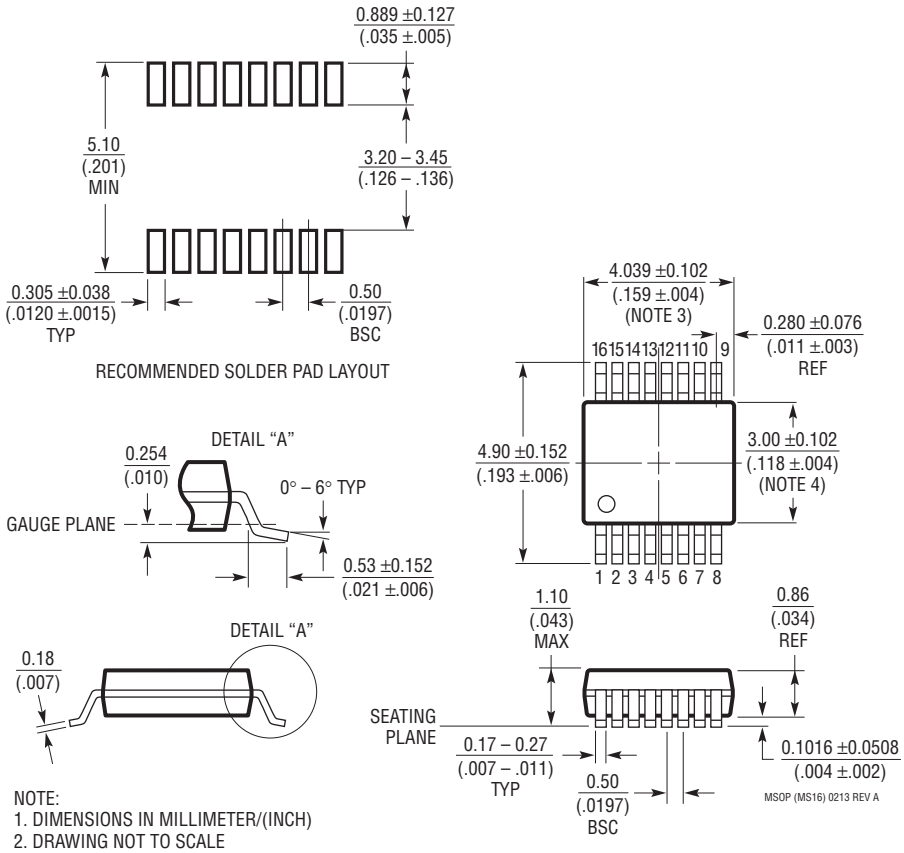


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6260#packaging for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev A)

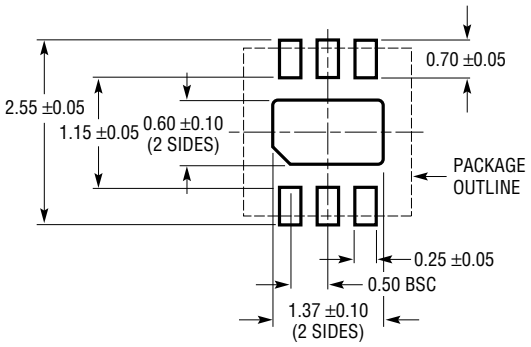


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

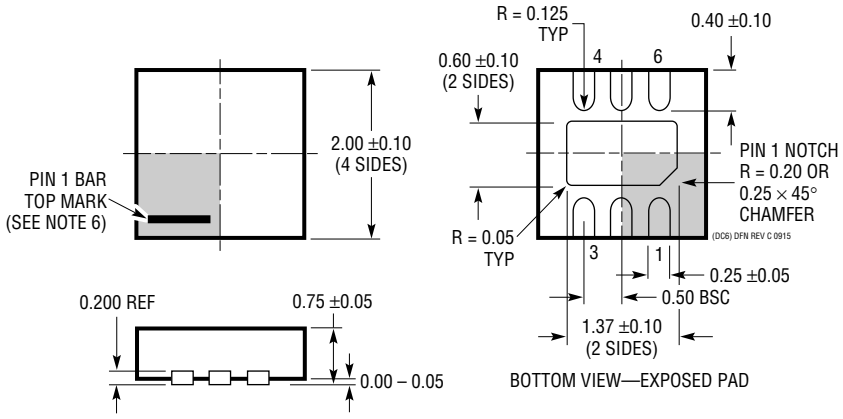
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6258#packaging for the most recent package drawings.

DC6 Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



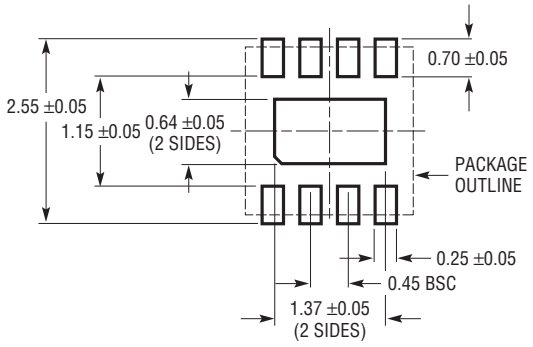
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

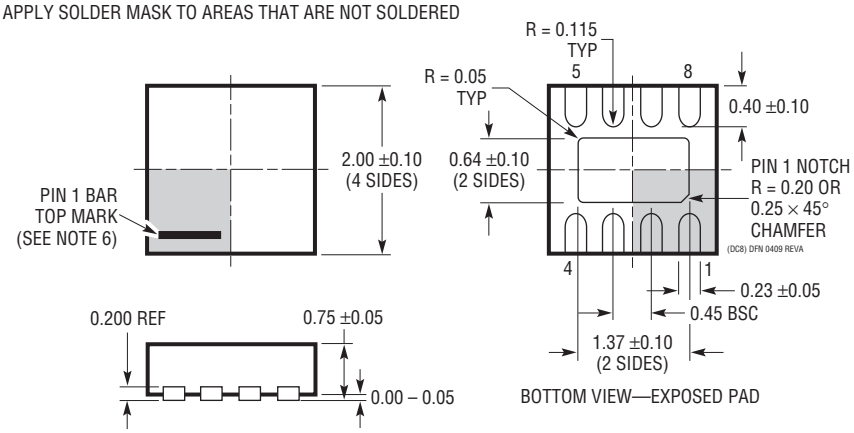
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6259#packaging for the most recent package drawings.

DC8 Package
8-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1719 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/17	Added SOT-23 package.	1, 2, 3, 20