LTC6373

36V Fully-Differential Programmable-Gain Instrumentation Amplifier with 25pA Input Bias Current

FEATURES

- Pin-Programmable Gains:
  G = 0.25, 0.5, 1, 2, 4, 8, 16V/V + Shutdown
- Fully Differential Outputs
- Gain Error: 0.012% (Max)
- Gain Error Drift: 1ppm/°C (Max)
- CMRR: 103dB (Min), G = 16
- Input Bias Current: 25pA (Max)
- Input Offset Voltage: 92µV (Max), G = 16
- Input Offset Voltage Drift: 1.7µV/°C (Max), G = 16
- –3dB Bandwidth: 4MHz, G = 16
- Input Noise Density: 8nV/√Hz, G = 16
- Slew Rate: 12V/µs, G = 16
- Adjustable Output Common Mode Voltage
- Quiescent Supply Current: 4.4mA
- Supply Voltage Range: ±4.5V to ±18V
- –40°C to 125°C Specified Temperature Range
- Small 12-Lead 4mm × 4mm DFN (LFCSP) Package

APPLICATIONS

- Data Acquisition Systems
- Biomedical Instrumentation
- Test and Measurement Equipment
- Differential ADC Drivers
- Single-Ended-to-Differential Conversion
- Multiplexed Applications

DESCRIPTION

The LTC®6373 is a precision instrumentation amplifier with fully differential outputs which includes a closely-matched internal resistor network to achieve excellent CMRR, offset voltage, gain error, gain drift, and gain non-linearity. The user can easily program the gain to one of seven available settings through a 3-bit parallel interface (A2 to A0). The 8th state puts the part in shutdown which reduces the current consumption to 220µA. Unlike a conventional voltage feedback amplifier, the LTC6373 maintains nearly the same bandwidth across all its gain settings.

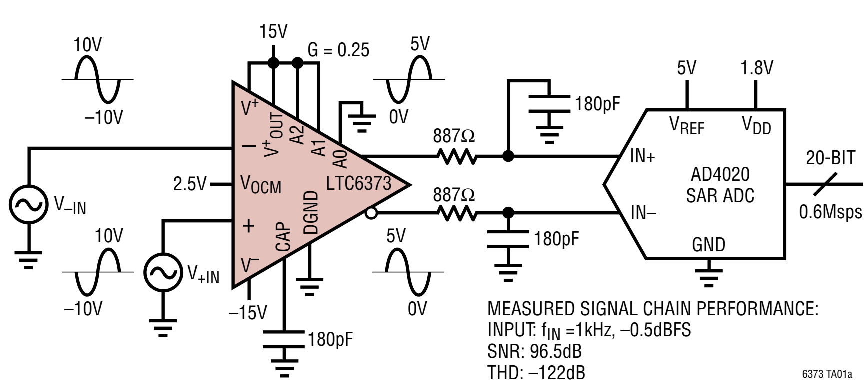
The LTC6373 features fully differential outputs to drive high performance, differential-input ADCs. The output common mode voltage is independently adjustable via the V_{OCM} pin. The combination of high impedance inputs, DC precision, low noise, low distortion, and high-speed differential ADC drive makes the LTC6373 an ideal candidate for optimizing data acquisition systems.

The LTC6373 is available in a 12-lead 4mm × 4mm DFN (LFCSP) package and is fully specified over the –40°C to 125°C temperature range.

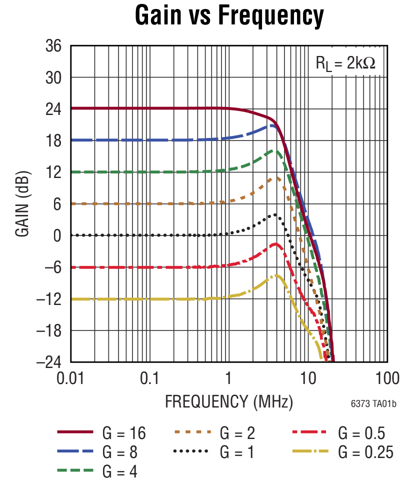
All registered trademarks and trademarks are the property of their respective owners.

TYPICAL APPLICATION

Interfacing a 40V_{P-P} Ground-Referenced Differential Input Signal to a 5V ADC



Gain vs Frequency



Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

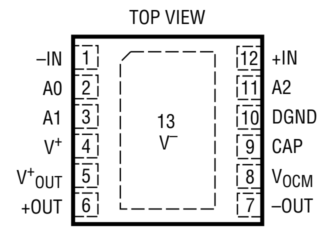
Supply Voltages
- V^+ .... V^- to (V^- + 40V)
- V^+_{OUT} .... V^- to (V^+ + 0.3V)

V_{OCM} .... (V^- – 0.3V) to (V^+_{OUT} + 0.3V)
A0, A1, A2, DGND .... (V^- – 0.3V) to (V^+ + 0.3V)
+IN, –IN
- Common Mode .... (V^- – 0.3V) to (V^+ + 0.3V)
- Differential .... ±20V

Output Current (+OUT, –OUT) (Note 2) .... $40mA_{RMS}$
Output Short-Circuit Duration (+OUT, –OUT) (Note 3) .... Thermally Limited
Operating and Specified Temperature Range (Notes 4, 5)
- LTC6373I .... –40°C to 85°C
- LTC6373H .... –40°C to 125°C

Maximum Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C

PIN CONFIGURATION



DFM PACKAGE
12-LEAD (4mm × 4mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 13) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6373IDFM#PBF	LTC6373IDFM#TRPBF	6373	12-Lead (4mm × 4mm) Plastic DFN, Side Solderable	–40°C to 85°C
LTC6373HDFM#PBF	LTC6373HDFM#TRPBF	6373	12-Lead (4mm × 4mm) Plastic DFN, Side Solderable	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and all typical values are at $T_A = 25°C$. $V^+ = V^+_{OUT} = 15V$, $V^- = –15V$, $V_{ICM} = V_{OCM} = DGND = 0V$, G = 1 (A2 = 5V, A1 = A0 = 0V). V_S is defined as $(V^+ – V^-)$. V_{ICM} is defined as $(V_{+IN} + V_{–IN})/2$. V_{OUTCM} is defined as $(V_{+OUT} + V_{–OUT})/2$. $V_{OUTDIFF}$ is defined as $(V_{+OUT} – V_{–OUT})$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G_{DIFF}	Differential Gain Range	G = 16, 8, 4, 2, 1, 0.5, 0.25		0.25		16	V/V
ΔG_{DIFF}	Differential Gain Error (Note 11)	G = 4, 2, 1, 0.5, 0.25 G = 4, 2, 1, 0.5, 0.25	 ●		0.002	0.012 0.02	% %
		G = 16, 8 G = 16, 8	 ●		0.003	0.015 0.023	% %
$\Delta G_{DIFF}/\Delta T$	Differential Gain Drift (Note 6)		●		0.25	1	ppm/°C
GNL	Differential Gain Nonlinearity (Note 11)	$V_{OUTDIFF} = 40V_{P-P}$	 ●		1	3 10	ppm ppm
V_{OSDIFF}	Differential Offset Voltage (Input Referred) (Note 7)	G = 16, 8, 4, 2, 1, 0.5, 0.25 T_A = –40°C to 85°C T_A = –40°C to 125°C	 ● ●		10 + 40/G	80 + 192/G 250 + 400/G 1120 + 1120/G	µV µV µV
$\Delta V_{OSDIFF}/\Delta T$	Differential Offset Voltage Drift (Input Referred) (Note 6)	G = 16, 8, 4, 2, 1, 0.5, 0.25 T_A = –40°C to 85°C T_A = –40°C to 125°C	 ● ●		 0.3 + 0.5/G 2 + 1.5/G	 1.5 + 2.5/G 5 + 5.5/G	 µV/°C µV/°C
	Differential Offset Voltage Hysteresis (Input Referred) (Note 12)	G = 16, 8, 4, 2, 1, 0.5, 0.25	●		10 + 15/G		µV
I_B	Input Bias Current (Notes 7, 8)	Active T_A = –40°C to 85°C T_A = –40°C to 125°C	 ● ●		2	25 50 500	pA pA pA
		Shutdown (A2 = A1 = A0 = 5V)			20		pA
I_{OS}	Input Offset Current (Notes 7, 8)	Active T_A = –40°C to 85°C T_A = –40°C to 125°C	 ● ●		2	25 40 100	pA pA pA
		Shutdown (A2 = A1 = A0 = 5V)			5		pA
e_n	Differential Input Voltage Noise Density	f = 10kHz G = 16 G = 8 G = 4 G = 2 G = 1 G = 0.5 G = 0.25			 8 8.4 9.5 12.2 18.7 26.4 41		 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Differential Input Voltage Noise	0.1Hz to10Hz G = 16 G = 8 G = 4 G = 2 G = 1 G = 0.5 G = 0.25			 1.1 1.2 1.3 1.5 1.8 2.4 4.2		 $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$
i_n	Input Current Noise Density	f = 10kHz			1		$fA/\sqrt{Hz}$
	Input Current Noise	0.1Hz to 10Hz			100		fA_{P-P}
e_{nVOCM}	Common Mode Voltage Noise Density	f = 10kHz			24		$nV/\sqrt{Hz}$
R_{IN}	Input Resistance	Differential Mode Common Mode			5×10^{12} 5×10^{12}		Ω Ω
C_{IN}	Input Capacitance				15		pF
V_{INR}	Input Voltage Range		 ●	$V^- + 3$ $V^- + 3.25$		$V^+ – 3$ $V^+ – 3$	V V

Rev. 0

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and all typical values are at T_A = 25°C. $V^+ = V^+_{OUT}$ = 15V, V^- = –15V, $V_{ICM} = V_{OCM}$ = DGND = 0V, G = 1 (A2 = 5V, A1 = A0 = 0V). V_S is defined as ($V^+ – V^-$). V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR (Note 9)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	DC to 60Hz, 1kΩ Source Imbalance, V_{ICM} = ±10V					
		G = 16		103	119		dB
		G = 16	●	98			dB
		G = 8		100	113		dB
		G = 8	●	98			dB
		G = 4		94	107		dB
		G = 4	●	92			dB
		G = 2		88	101		dB
		G = 2	●	86			dB
		G = 1		82	95		dB
		G = 1	●	80			dB
		G = 0.5		83	95		dB
		G = 0.5	●	80			dB
		G = 0.25		80	95		dB
		G = 0.25	●	75			dB
CMRRIO (Note 9)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_{OCM} = ±13V	●	75	95		dB
PSRR (Note 10)	Differential Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = ±4.5V to ±18V					
		G = 16	●	105	142		dB
		G = 8	●	102	139		dB
		G = 4	●	102	136		dB
		G = 2	●	100	133		dB
		G = 1	●	98	130		dB
		G = 0.5	●	95	125		dB
		G = 0.25	●	92	120		dB
PSRRCM (Note 10)	Output Common Mode Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OSCM}$)	V_S = ±4.5V to ±18V	●	110	135		dB
V_{OUT}	Output Voltage, High, Either Output Pin	I_L = 0mA, V_S = ±4.5V	●	V^+_{OUT} – 0.6	V^+_{OUT} – 0.3		V
		I_L = –5mA, V_S = ±4.5V	●	V^+_{OUT} –1.1	V^+_{OUT} – 0.7		V
		I_L = 0mA, V_S = ±15V	●	V^+_{OUT} – 1.8	V^+_{OUT} – 1.1		V
		I_L = –5mA, V_S = ±15V	●	V^+_{OUT} – 1.9	V^+_{OUT} – 1.3		V
	Output Voltage, Low, Either Output Pin	I_L = 0mA, V_S = ±4.5V	●		V^- + 0.3	V^- + 0.6	V
		I_L = 5mA, V_S = ±4.5V	●		V^- + 0.6	V^- + 1	V
		I_L = 0mA, V_S = ±15V	●		V^- + 1.1	V^- + 1.8	V
		I_L = 5mA, V_S = ±15V	●		V^- + 1.2	V^- + 1.9	V
I_{SC}	Output Short-Circuit Current, Either Output Pin, Sinking	V_S = ±4.5V	●	27	39		mA
		V_S = ±15V	●	35	47		mA
	Output Short-Circuit Current, Either Output Pin, Sourcing	V_S = ±4.5V	●	23	33		mA
		V_S = ±15V	●	29	38		mA
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = ±4.5V, V_{OCM} = ±3V	●		1		V/V
		V_S = ±15V, V_{OCM} = ±13V	●		1		V/V
ΔG_{CM}	Common Mode Gain Error 100 × (G_{CM} – 1)	V_S = ±4.5V, V_{OCM} = ±3V	●		0.05	0.1	%
		V_S = ±15V, V_{OCM} = ±13V	●		0.05	0.1	%
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$V_{OUTDIFF}$ = ±10V					
		Single-Ended Input	●		–80	–70	dB
		Differential Input	●		–90	–75	dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} – V_{OCM}$)				1	40	mV
			●			50	mV

Rev. 0

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and all typical values are at T_A = 25°C. $V^+ = V^+_{OUT}$ = 15V, V^- = –15V, $V_{ICM} = V_{OCM}$ = DGND = 0V, G = 1 (A2 = 5V, A1 = A0 = 0V). V_S is defined as $(V^+ – V^-)$. V_{ICM} is defined as $(V_{+IN} + V_{–IN})/2$. V_{OUTCM} is defined as $(V_{+OUT} + V_{–OUT})/2$. $V_{OUTDIFF}$ is defined as $(V_{+OUT} – V_{–OUT})$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUTCMR}	Voltage Range for the V_{OCM} Pin (Guaranteed by ΔG_{CM})	V_S = ±4.5V V_S = ±15V	● ●	V^- + 1.5 V^- + 2		V^+_{OUT} – 1.5 V^+_{OUT} – 2	V V
V_{OCM}	Self-Biased Voltage at the V_{OCM} Pin	V_{OCM} Not Connected	●	$(V^+_{OUT} + V^-)/2 – 0.1$	$(V^+_{OUT} + V^-)/2$	$(V^+_{OUT} + V^-)/2 + 0.1$	V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	1.9	2.3	2.7	MΩ
V_{DGND}	Voltage Range for the DGND Pin		●	V^-	0	V^+ – 2.5	V
I_{DGND}	DGND Pin Current	DGND = 5V, A2 = A1 = A0 = 15V	●	–7	–4	–1	µA
V_{IL}	Digital Input (A2/A1/A0) Logic Low	Referred to DGND	●	DGND		DGND + 0.6	V
V_{IH}	Digital Input (A2/A1/A0) Logic High	Referred to DGND	●	DGND + 1.5		V^+	V
$I_{A2/A1/A0}$	Digital Input (A2/A1/A0) Pin Current	A2/A1/A0 = 5V	●		8	12	µA
$f_{–3dB}$	–3dB Bandwidth	G = 16 G = 8 G = 4 G = 2 G = 1 G = 0.5 G = 0.25			4 5.5 6 6.5 6.5 7 7.5		MHz MHz MHz MHz MHz MHz MHz
SR	Slew Rate	G = 16, $V_{OUTDIFF}$ = 40V_{P-P} Step, R_L = 2kΩ	●	7.5	12		V/µs
t_s	Settling Time	G = 16, $V_{OUTDIFF}$ = 8V_{P-P} Step, R_L = 1kΩ 0.1% 0.01% 0.0015% (16-Bit) 4ppm (18-Bit)			 2.1 2.25 2.4 2.7		 µs µs µs µs
THD	Total Harmonic Distortion	G = 1, $V_{OUTDIFF}$ = 10V_{P-P}, R_L = 2kΩ f = 1kHz f = 10kHz			 –115 –110		 dB dB
t_{ON}	Turn-On Time				10		µs
t_{OFF}	Turn-Off Time				5		µs
	Gain Switching Time				5		µs
V_S	Supply Voltage Range	Guaranteed by PSRR	●	9		36	V
I_S	Supply Current	Active	 ●		4.4	4.75 5.25	mA mA
		Shutdown (A2 = A1 = A0 = 5V)	●		220	600	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6373 is capable of producing peak output currents in excess of 40mA. Current density limitations within the IC require the continuous RMS current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 40mA (Absolute Maximum).

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LTC6373I is guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6373H is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 5: The LTC6373I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6373H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Guaranteed by design.

Note 7: ESD (Electrostatic Discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6373; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 8: Input bias current is defined as the maximum of the input currents flowing into either of the input pins (–IN and +IN). Input Offset current is defined as the difference between the input currents ($I_{OS} = I_B^+ – I_B^–$).

Note 9: Input CMRR (CMRR) is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred offset voltage. Output CMRR (CMRRIO) is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred offset voltage.

Note 10: Differential power supply rejection ratio (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred offset voltage. Common mode power supply rejection ratio (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset voltage.

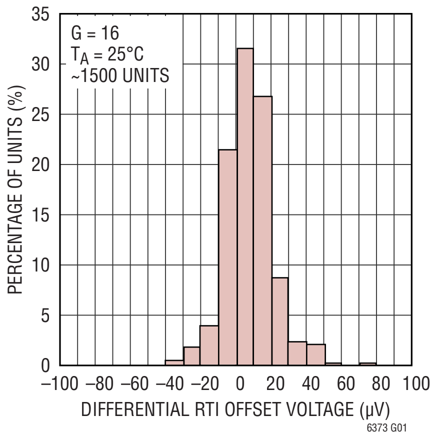
Note 11: This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects are dependent on the package used, PCB layout, heat sinking and air flow conditions.

Note 12: Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. For instruments that are stored in well controlled temperatures (within 20 or 30 degrees of operational temperature), hysteresis is usually not a significant error source. Typical Hysteresis is the worst case of differential offset measured between 25°C to -40°C to 25°C thermal cycle and 25°C to 125°C to 25°C thermal cycle.

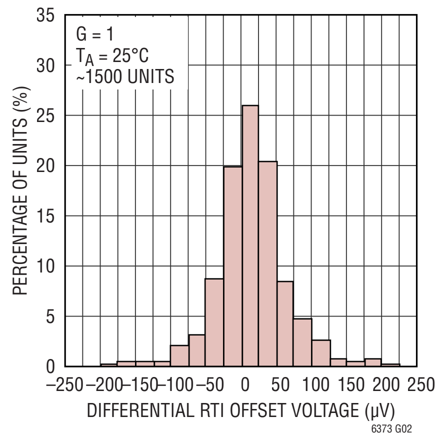
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = -15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

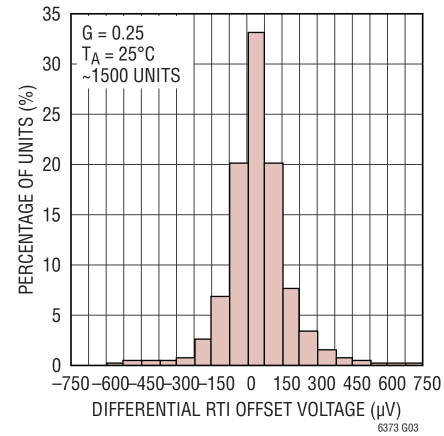
Typical Distribution of Differential RTI Offset Voltage



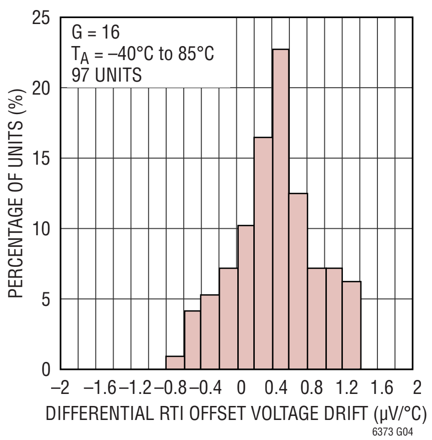
Typical Distribution of Differential RTI Offset Voltage



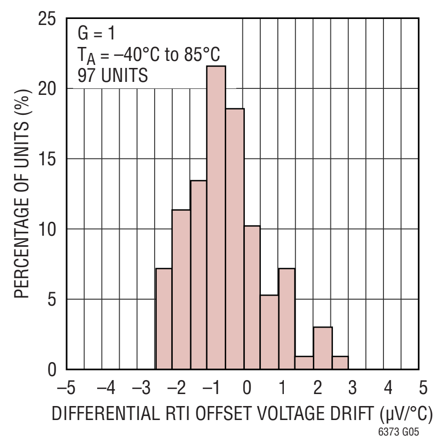
Typical Distribution of Differential RTI Offset Voltage



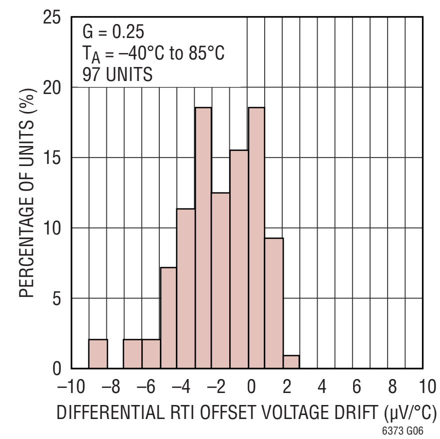
Typical Distribution of Differential RTI Offset Voltage Drift



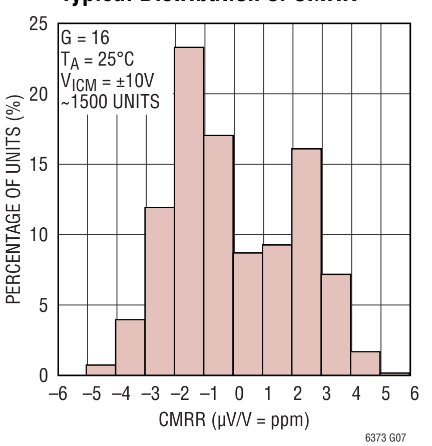
Typical Distribution of Differential RTI Offset Voltage Drift



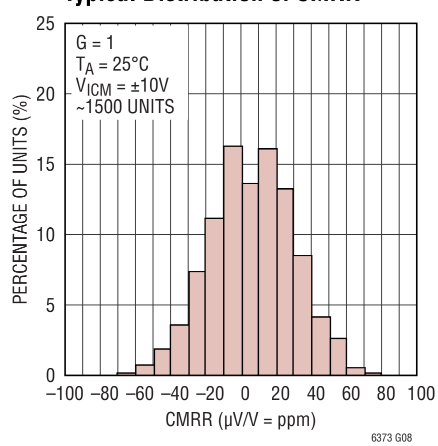
Typical Distribution of Differential RTI Offset Voltage Drift



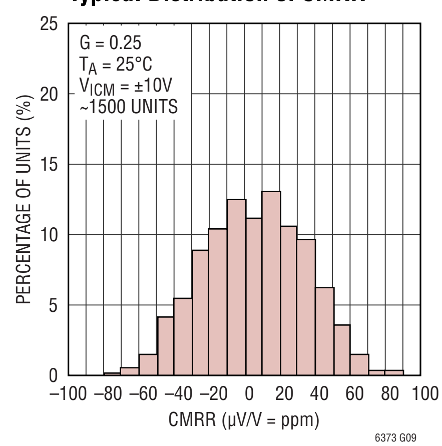
Typical Distribution of CMRR



Typical Distribution of CMRR



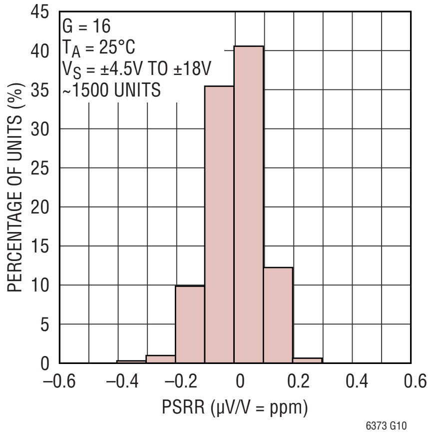
Typical Distribution of CMRR



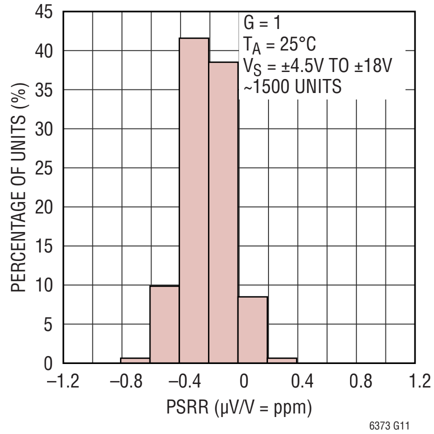
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = –15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

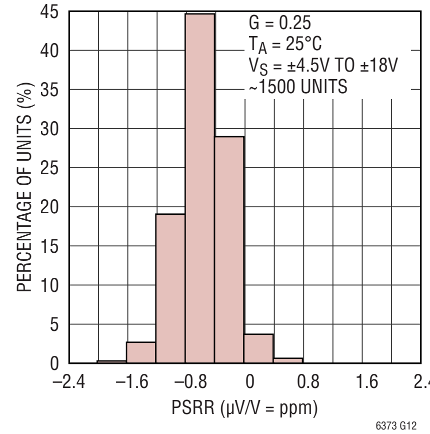
Typical Distribution of Differential PSRR



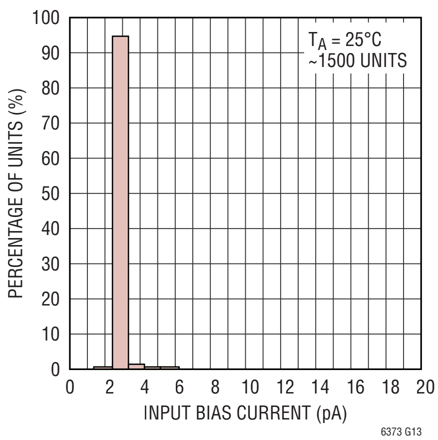
Typical Distribution of Differential PSRR



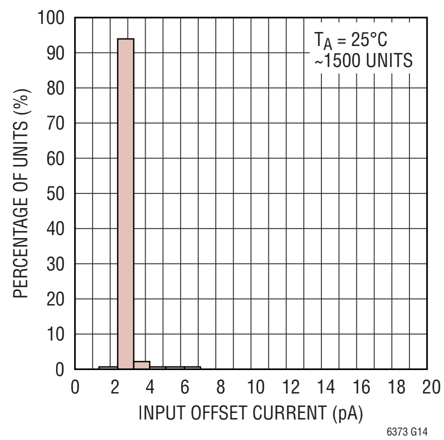
Typical Distribution of Differential PSRR



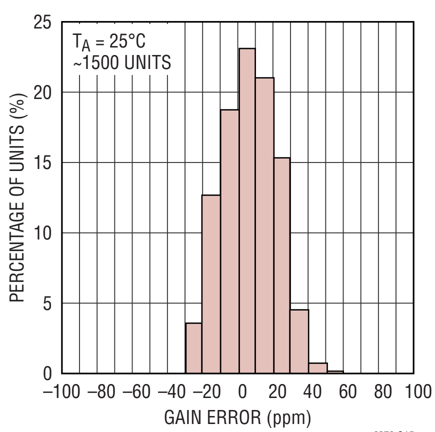
Typical Distribution of Input Bias Current



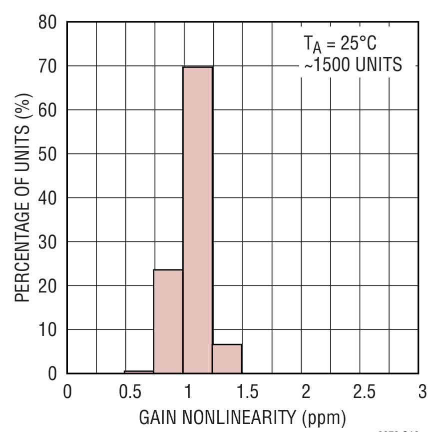
Typical Distribution of Input Offset Current



Typical Distribution of Differential Gain Error



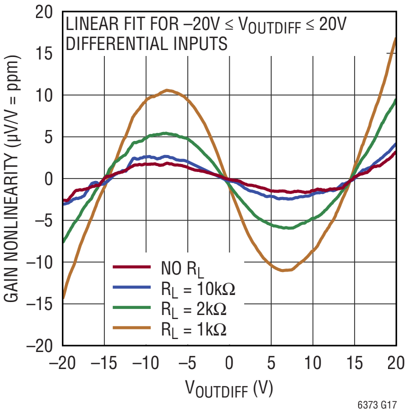
Typical Distribution of Differential Gain Nonlinearity



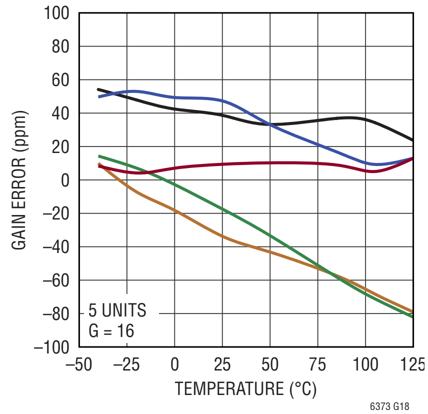
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = -15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

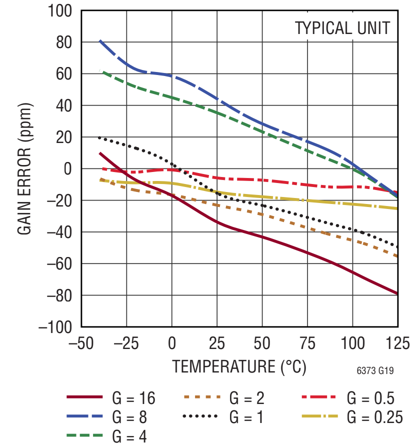
Differential Gain Nonlinearity vs Output Voltage



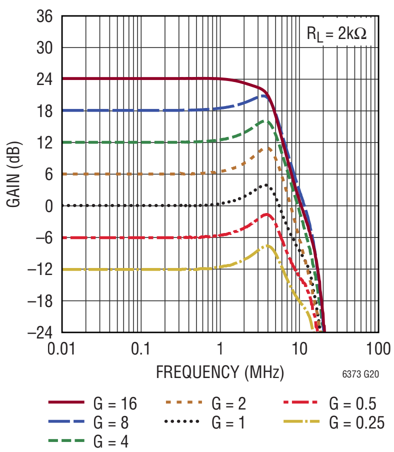
Differential Gain Error vs Temperature



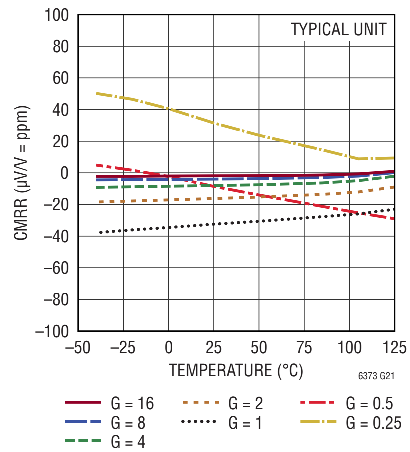
Differential Gain Error vs Temperature



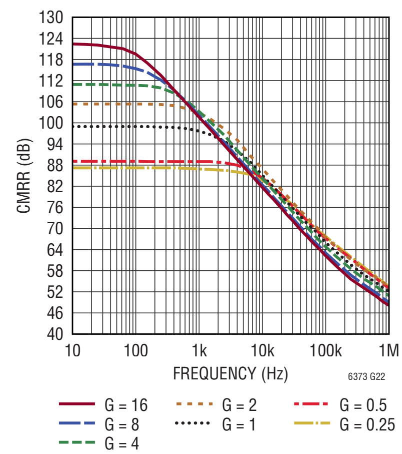
Gain vs Frequency



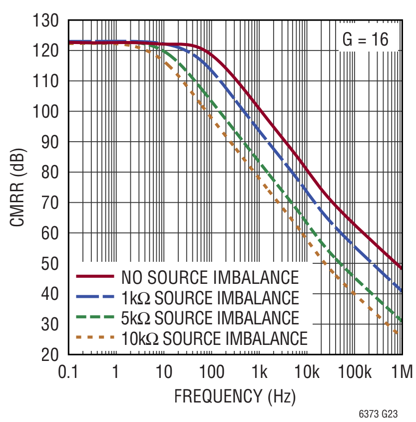
CMRR vs Temperature



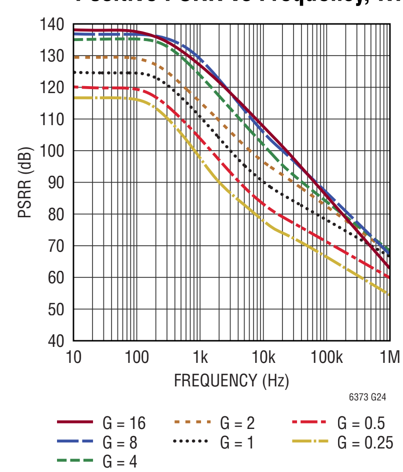
CMRR vs Frequency



CMRR vs Frequency With Source Imbalance



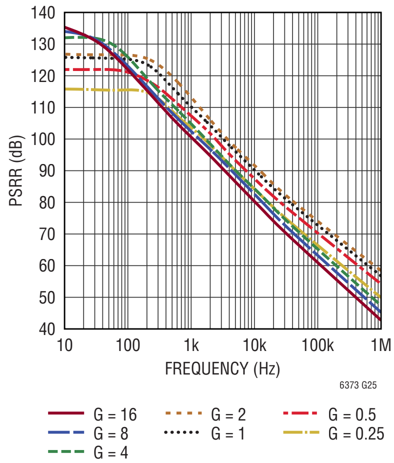
Positive PSRR vs Frequency, RTI



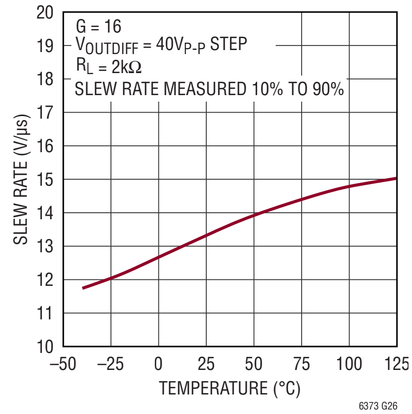
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = -15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

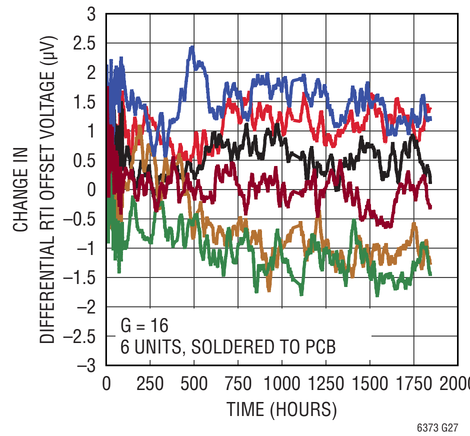
Negative PSRR vs Frequency, RTI



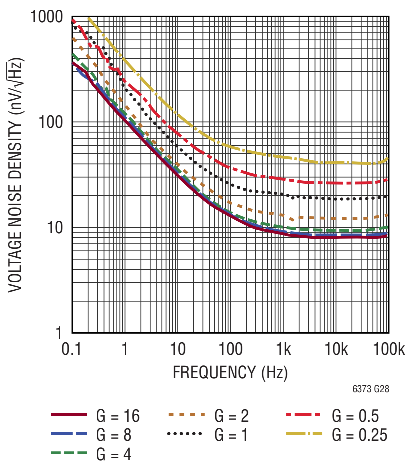
Slew Rate vs Temperature



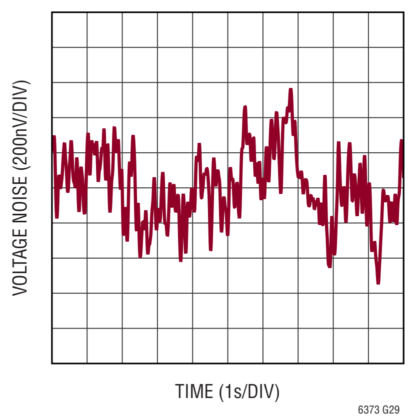
Long Term Differential RTI Offset Voltage Drift



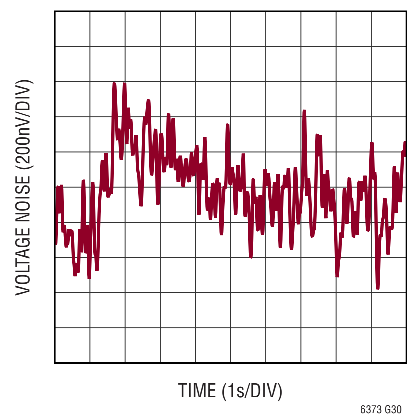
Input Referred Voltage Noise Density vs Frequency



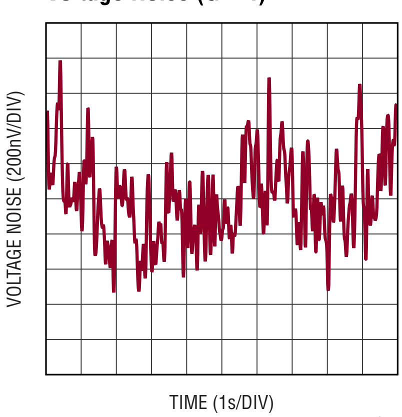
Input Referred 0.1Hz to 10Hz Voltage Noise (G = 16)



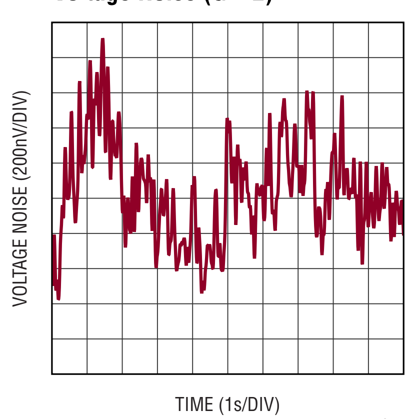
Input Referred 0.1Hz to 10Hz Voltage Noise (G = 8)



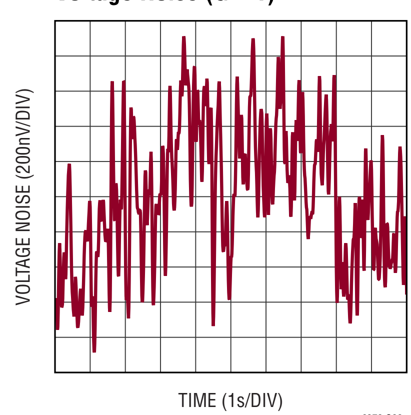
Input Referred 0.1Hz to 10Hz Voltage Noise (G = 4)



Input Referred 0.1Hz to 10Hz Voltage Noise (G = 2)



Input Referred 0.1Hz to 10Hz Voltage Noise (G = 1)

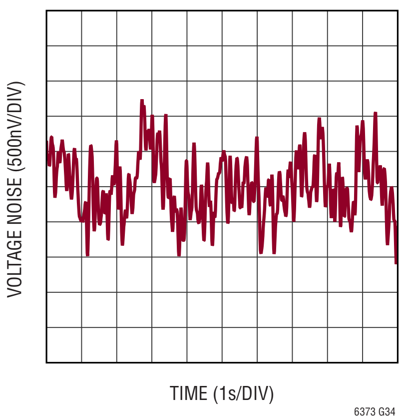


Rev. 0

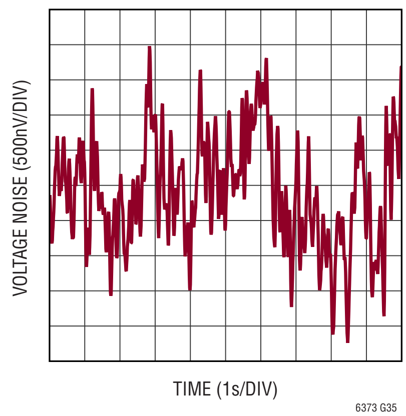
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = -15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

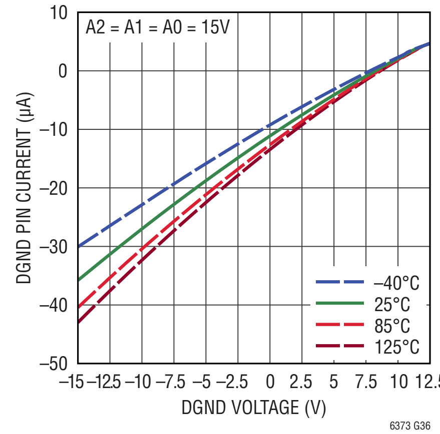
Input Referred 0.1Hz to 10Hz Voltage Noise (G = 0.5)



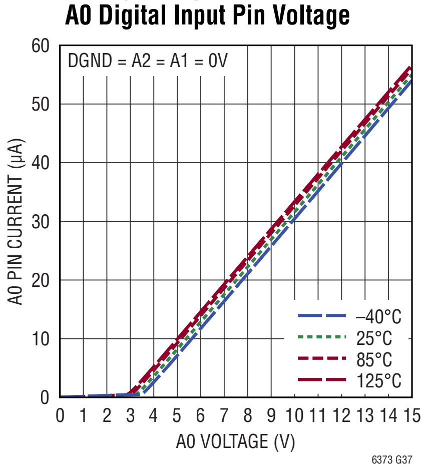
Input Referred 0.1Hz to 10Hz Voltage Noise (G = 0.25)



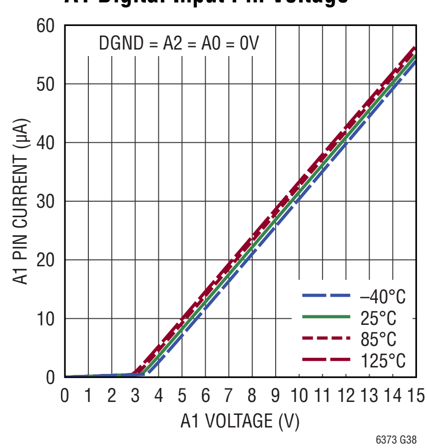
DGND Pin Current vs DGND Pin Voltage



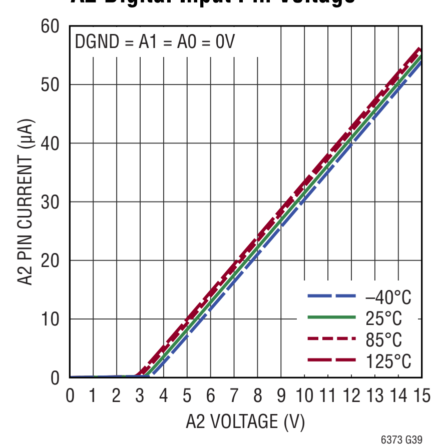
A0 Digital Input Pin Current vs A0 Digital Input Pin Voltage



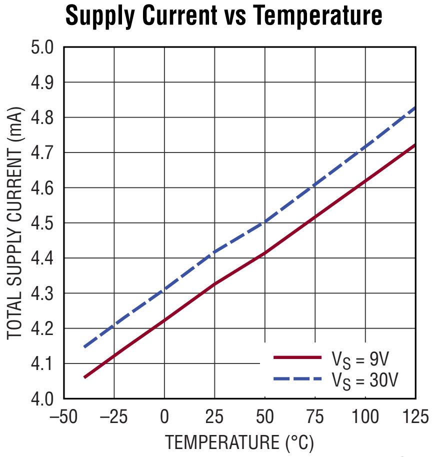
A1 Digital Input Pin Current vs A1 Digital Input Pin Voltage



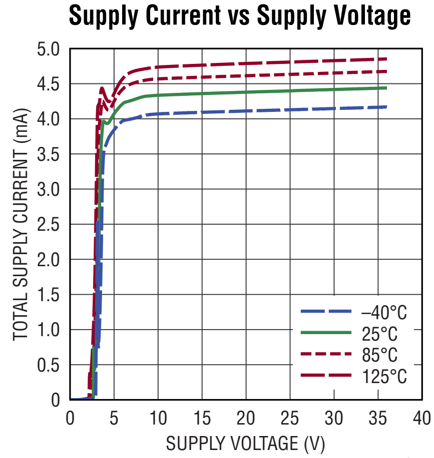
A2 Digital Input Pin Current vs A2 Digital Input Pin Voltage



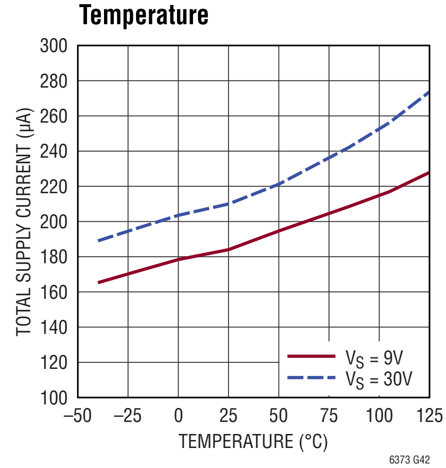
Supply Current vs Temperature



Supply Current vs Supply Voltage



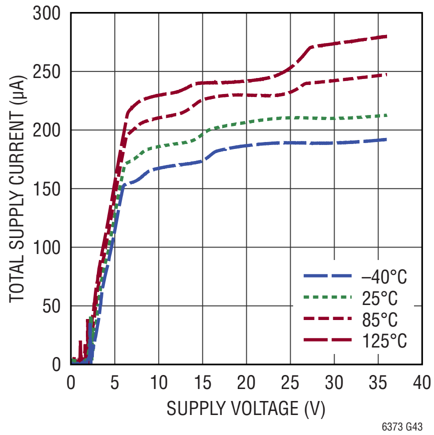
Shutdown Supply Current vs Temperature



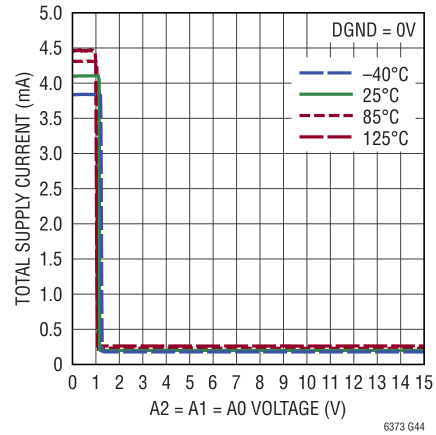
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = –15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

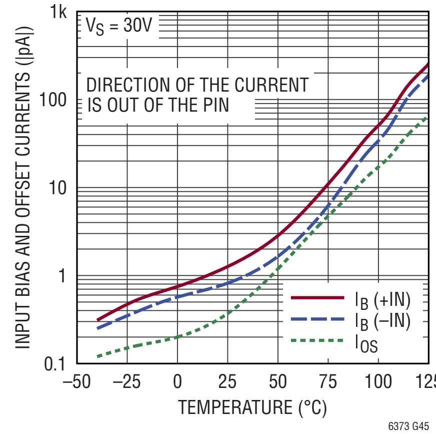
Shutdown Supply Current vs Supply Voltage



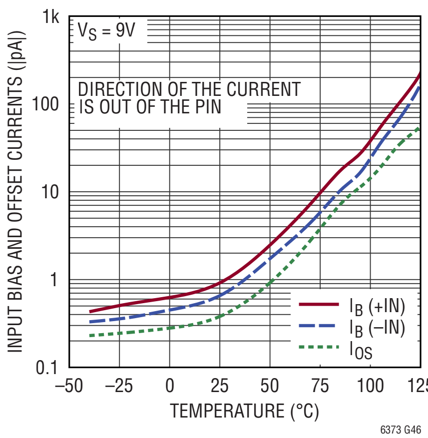
Supply Current vs Digital Input (A2/A1/A0) Pin Voltage



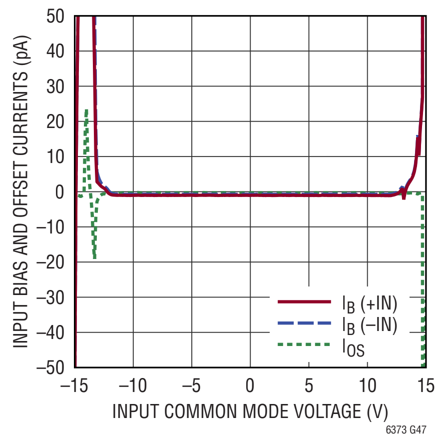
Input Bias Current and Offset Current vs Temperature



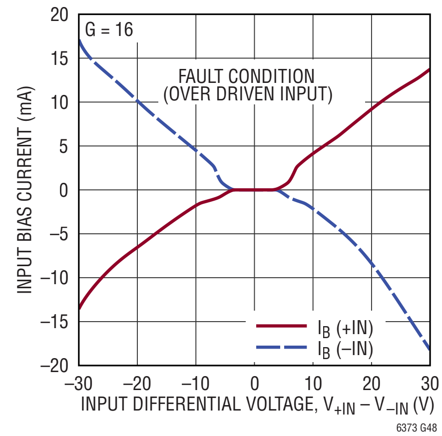
Input Bias Current and Offset Current vs Temperature



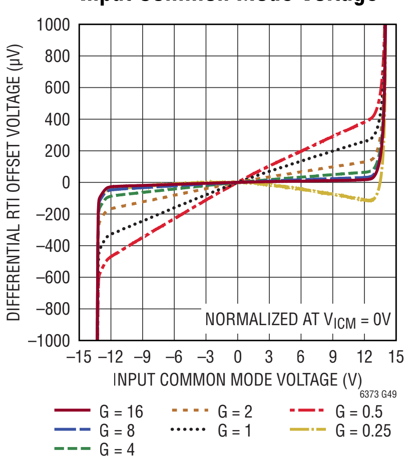
Input Bias Current and Offset Current vs Input Common Mode Voltage



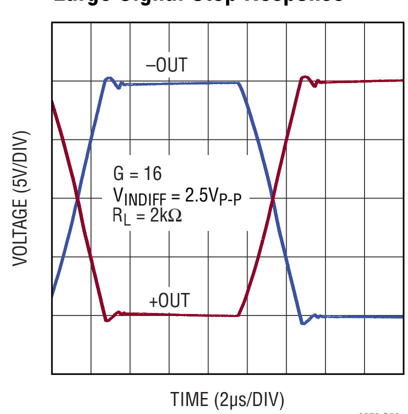
Input Bias Current vs Input Differential Voltage



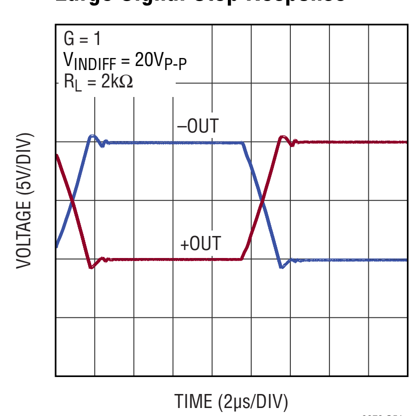
Differential RTI Offset Voltage vs Input Common Mode Voltage



Large Signal Step Response



Large Signal Step Response

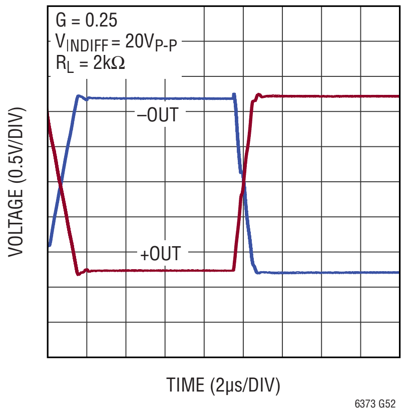


Rev. 0

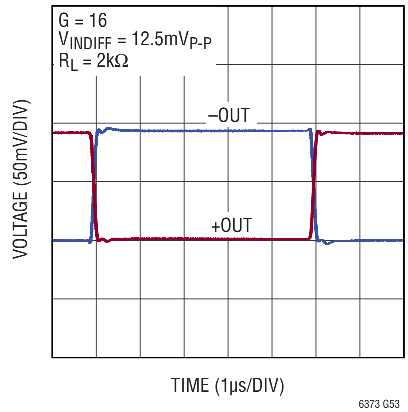
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = -15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

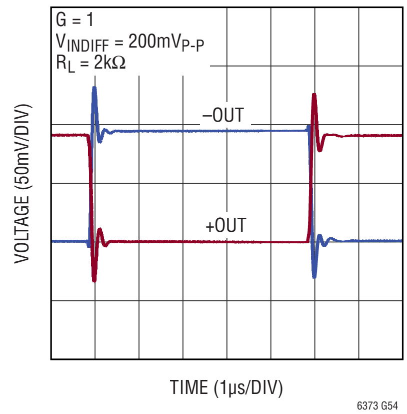
Large Signal Step Response



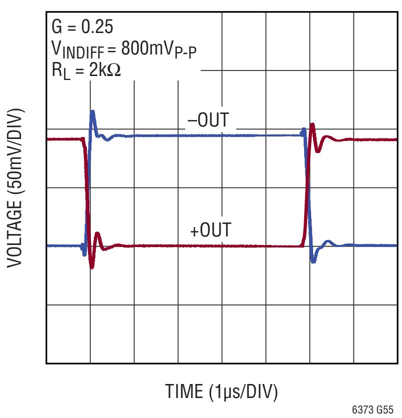
Small Signal Step Response



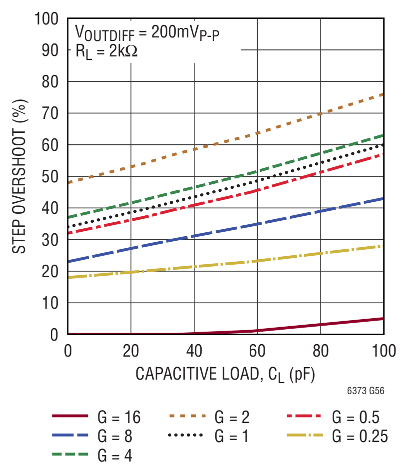
Small Signal Step Response



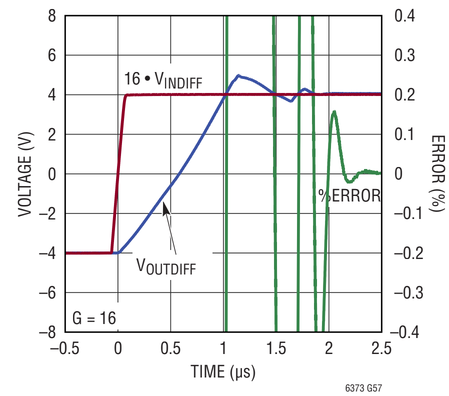
Small Signal Step Response



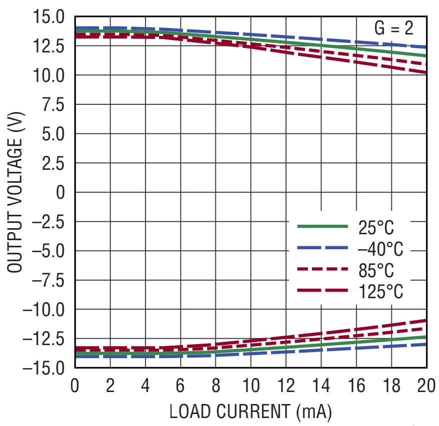
Small Signal Step Overshoot vs Load Capacitance



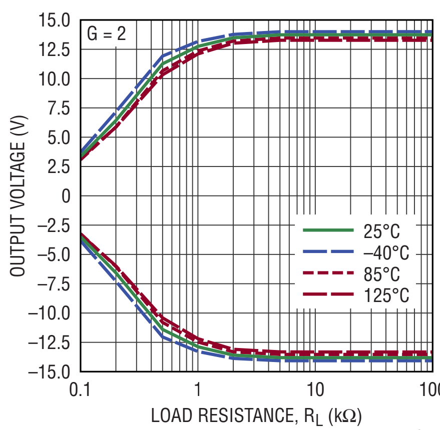
Settling Time to 8VP-P Output Step



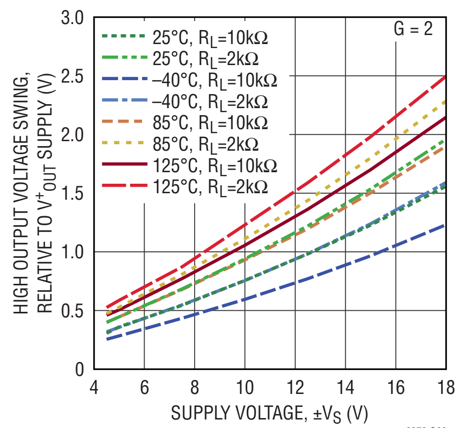
Output Voltage Swing vs Load Current



Output Voltage Swing vs Load Resistance



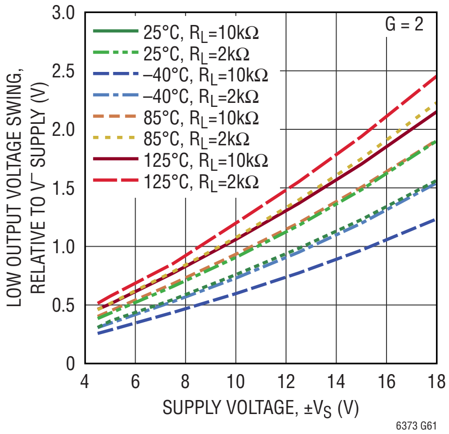
High Output Voltage Swing vs Supply Voltage



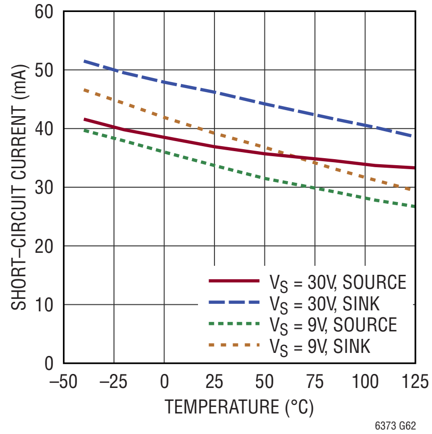
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = -15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

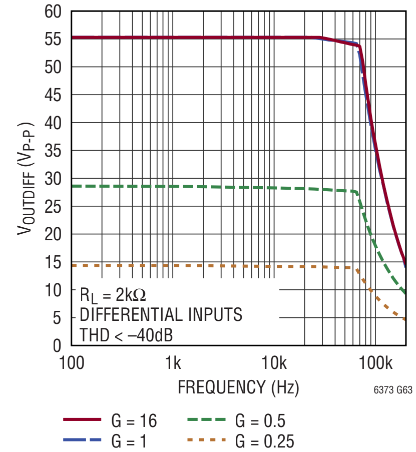
Low Output Voltage Swing vs Supply Voltage



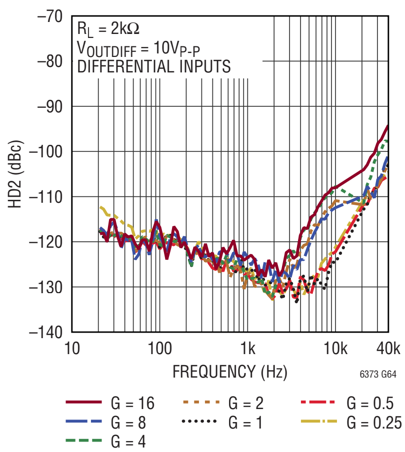
Output Short-Circuit Current vs Temperature



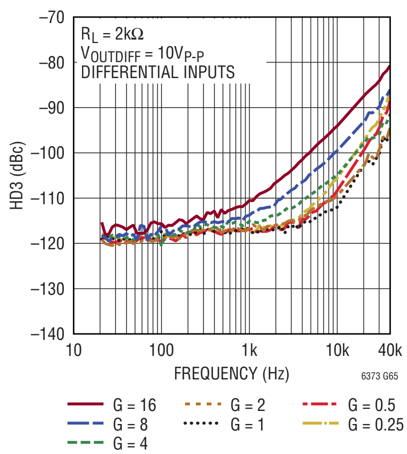
Maximum Undistorted Output Swing vs Frequency



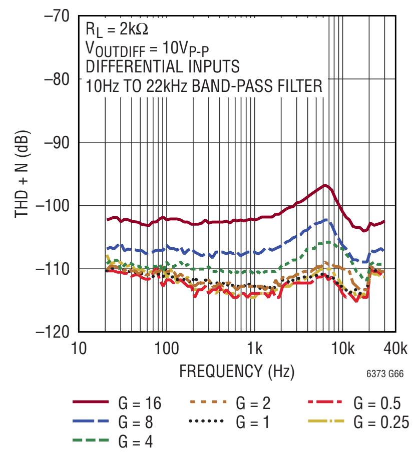
2nd Harmonic Distortion vs Frequency



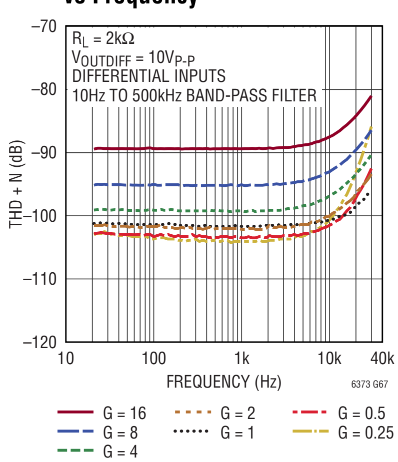
3rd Harmonic Distortion vs Frequency



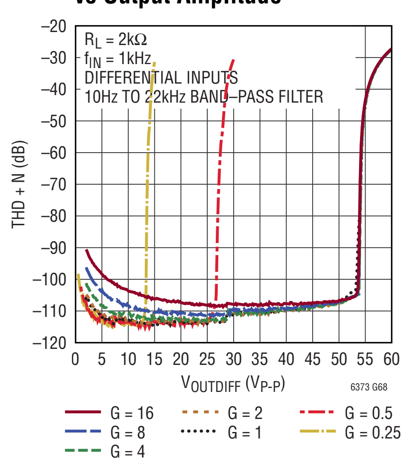
Total Harmonic Distortion + Noise vs Frequency



Total Harmonic Distortion + Noise vs Frequency



Total Harmonic Distortion + Noise vs Output Amplitude

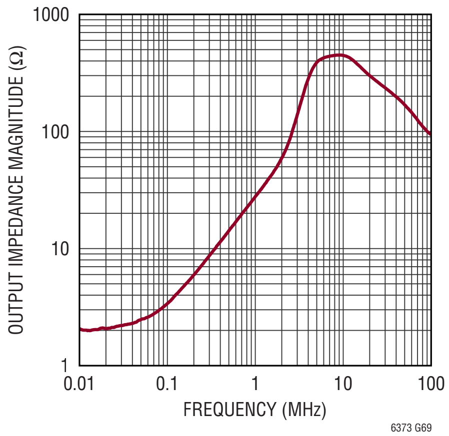


Rev. 0

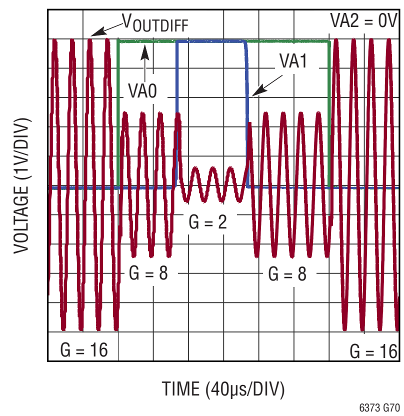
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V^+_{OUT} = 15V$, $V^- = -15V$, $V_{ICM} = V_{OCM} = 0V$, $T_A = 25°C$, G = 1, unless otherwise noted.

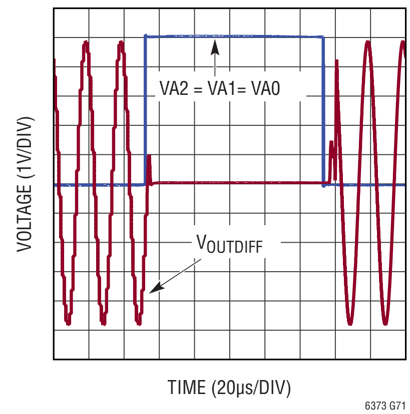
Differential Output Impedance vs Frequency



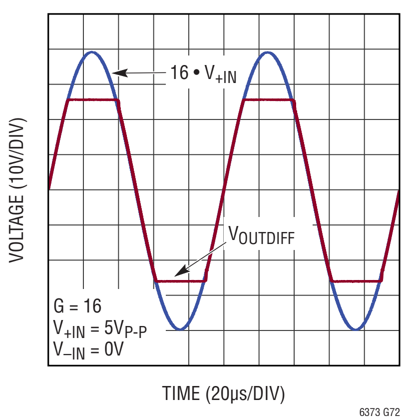
Gain Switching Transient Response



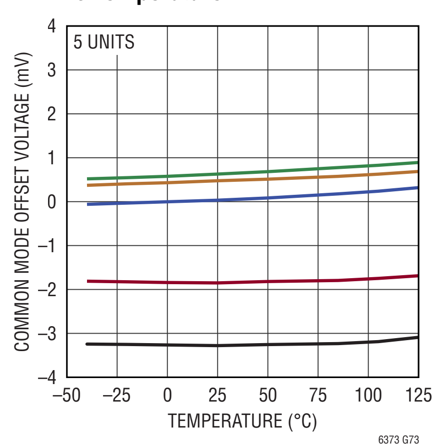
Turn-On and Turn-Off Transient Response



Output Overdrive Recovery



Common Mode Offset Voltage vs Temperature



PIN FUNCTIONS

–IN (Pin 1): Inverting Input of Instrumentation Amplifier. Input voltage range is between V^- + 3V and V^+ – 3V.

A0 (Pin 2): Digital Gain Programming Pin 0. In combination with A2 and A1, the user can choose the desired gain setting for the LTC6373 (refer to Gain Selection section of this data sheet). The logic threshold for the A0 pin is specified with respect to the voltage on the DGND pin (logic low = any voltage between DGND and DGND + 0.6V; logic high = any voltage between DGND + 1.5V and V^+). If the A0 pin is left floating, an internal resistor pulls its voltage close to the DGND pin, resulting in a default logic low state for this programming pin.

A1 (Pin 3): Digital Gain Programming Pin 1. In combination with A2 and A0, the user can choose the desired gain setting for the LTC6373 (refer to Gain Selection section of this data sheet). The logic threshold for the A1 pin is specified with respect to the voltage on the DGND pin (logic low = any voltage between DGND and DGND + 0.6V; logic high = any voltage between DGND + 1.5V and V^+). If the A1 pin is left floating, an internal resistor pulls its voltage close to the DGND pin, resulting in a default logic low state for this programming pin.

V^+ (Pin 4): Positive Power Supply. The operating voltage range for V^+ is $(V^- + 9V) \le V^+ \le (V^- + 36V)$.

V^+_{OUT} (Pin 5): Positive Power Supply for the Output Differential Amplifier inside the LTC6373 (the amplifier marked as A3 in Figure 1 of this data sheet). V^+_{OUT} pin is normally tied to V^+ pin, however the user may also choose a lower voltage for V^+_{OUT} to save power dissipation or to help protect ADC inputs. The voltage on V^+_{OUT} pin should never be higher than V^+ pin. The operating voltage range for V^+_{OUT} is $(V^- + 9V) \le V^+_{OUT} \le V^+$.

+OUT (Pin 6): Positive Output Pin of Instrumentation Amplifier.

–OUT (Pin 7): Negative Output Pin of Instrumentation Amplifier.

V_{OCM} (Pin 8): Output Common Mode Reference Voltage. Voltage applied to this pin sets the output common mode voltage level. If the V_{OCM} pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+_{OUT} and V^-. The V_{OCM} pin should be decoupled to ground with a minimum of 0.1µF bypass capacitor.

CAP (Pin 9): Bypass Capacitor Pin. The CAP pin should be decoupled to ground with a 180pF bypass capacitor.

DGND (Pin 10): Reference for Digital Gain Programming Pins (A2/A1/A0). DGND is normally tied to ground, however any voltage between V^- and V^+ – 2.5V may also be chosen. If the DGND pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+ and V^-. The logic threshold for A2/A1/A0 pins is specified with respect to the DGND pin.

A2 (Pin 11): Digital Gain Programming Pin 2. In combination with A1 and A0, the user can choose the desired gain setting for the LTC6373 (refer to Gain Selection section of this data sheet). The logic threshold for the A2 pin is specified with respect to the voltage on the DGND pin (logic low = any voltage between DGND and DGND + 0.6V; logic high = any voltage between DGND + 1.5V and V^+). If the A2 pin is left floating, an internal resistor pulls its voltage close to the DGND pin, resulting in a default logic low state for this programming pin.

+IN (Pin 12): Noninverting Input of Instrumentation Amplifier. Input voltage range is between V^- + 3V and V^+ – 3V.

V^- (Exposed Pad Pin 13): Negative Power Supply. The exposed pad must be soldered to PCB and connected to V^-.

SIMPLIFIED BLOCK DIAGRAM

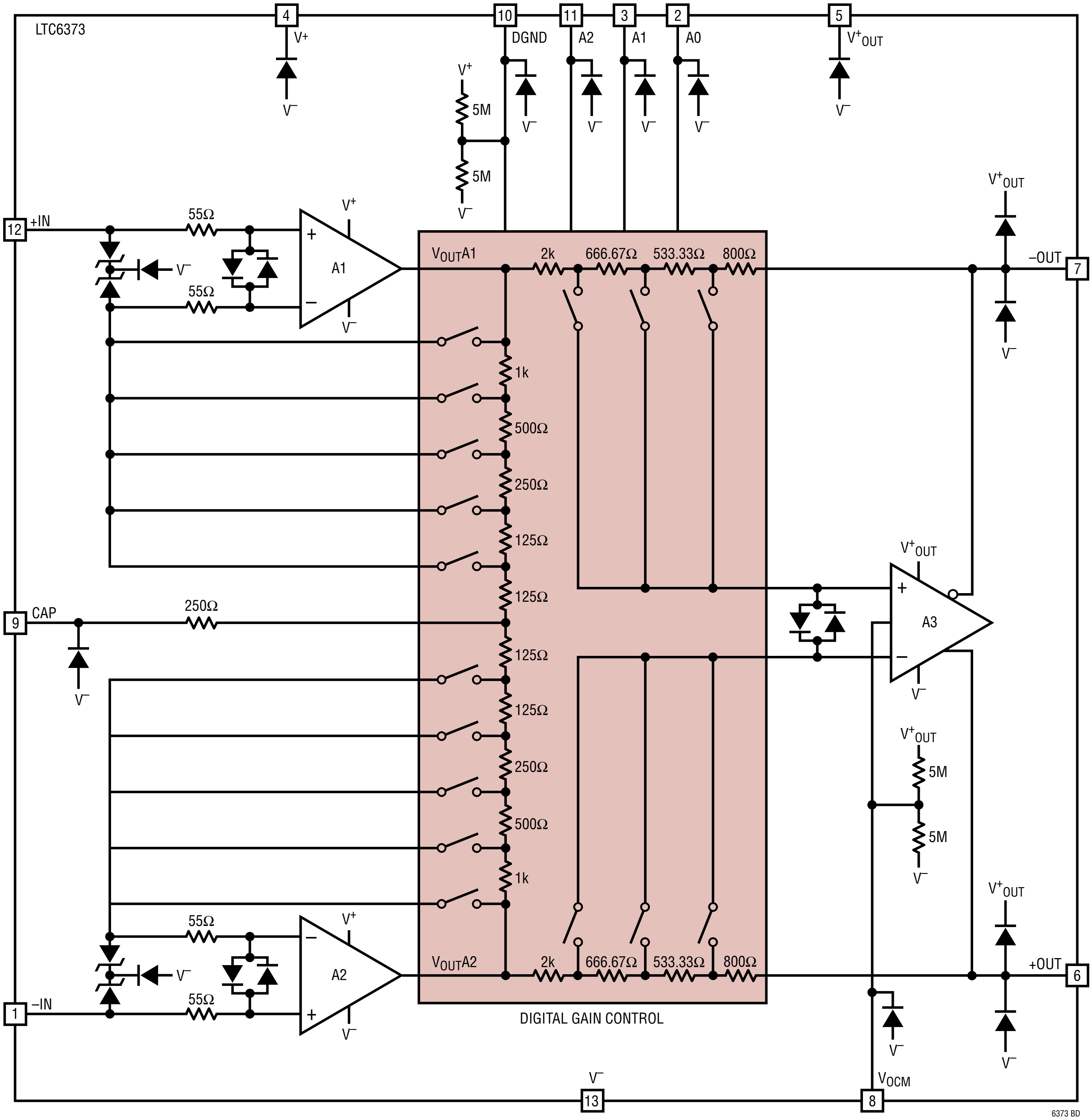


Figure 1. Simplified Block Diagram

APPLICATIONS INFORMATION

Functional Description

The LTC6373 is a monolithic instrumentation amplifier based on the classic 3-op-amp topology, as shown in the Block Diagram of Figure 1. A parallel interface allows users to digitally program gains to one of the seven available settings (G = 0.25, 0.5, 1, 2, 4, 8, and 16V/V) while the 8th state puts the part in shutdown mode (which reduces the current drawn from the supplies to 220µA). Gain control is achieved by switching resistors in an internal, precision resistor array (as shown in Figure 1). Although the LTC6373 has a voltage feedback topology, the gain-bandwidth product increases at higher gain settings because each gain has its own frequency compensation, resulting in increased bandwidth at higher gains and minimum phase variation across all gains.

The LTC6373 is optimized to convert a fully differential or single-ended input signal to a low impedance, balanced differential output suitable for driving high performance, analog-to-digital converters (ADCs). The balanced differential nature of the amplifier provides even-order harmonic distortion cancellation, and low susceptibility to common mode noise (like power supply noise). Load capacitances above 50pF to ground or 25pF differentially should be decoupled with 10Ω to 50Ω of series resistance from each output to prevent oscillation or ringing.

Overall, the LTC6373 simplifies signal chain design by offering:

- High impedance buffering (due to using CMOS technology and the resulting pA input bias current)
- Signal amplification (G>1) and attenuation (G<1) together in one socket at nearly the same bandwidth
- Digital gain programming (which enables changing gain settings easily and rapidly)
- Superior matching specs (due to trimmed, precision internal resistors)
- The ability to drive ADCs directly (due to attributes such as fully differential outputs, good DC precision, low noise, low distortion, and high bandwidth)
- Level shifting (achieved by using V_{OCM} pin to independently adjust the output common mode voltage to match it to the desired input level of the next stage of the signal chain).

The LTC6373 accommodates all the above features in a small 12-lead 4mm × 4mm DFN (LFCSP) package, making it an excellent solution for applications where size and packing density are important considerations.

Gain Selection

The gain of the LTC6373 can be programmed to its desired setting using a digital interface consisting of a digital reference pin DGND and three parallel gain programming pins A2, A1, and A0. The logic threshold for A2/A1/A0 pins is specified with respect to the voltage on the DGND pin. Any voltage between DGND and DGND + 0.6V on A2 or A1 or A0 pins will generate a logic low (L) state for that pin; any voltage between DGND + 1.5V and V^+ on A2 or A1 or A0 pins will generate a logic high (H) state for that pin. The gain for the LTC6373 is programmed according to the truth table below:

Table 1. Gain Selection Table for LTC6373

A2	A1	A0	G = GAIN SETTING (V/V)
L	L	L	16
L	L	H	8
L	H	L	4
L	H	H	2
H	L	L	1
H	L	H	0.5
H	H	L	0.25
H	H	H	Shutdown

The permissible voltage range for DGND is between V^- and V^+ – 2.5V. However, typically DGND is tied to ground (0V) and A2/A1/A0 pins can be connected to 0V or 5V to generate logic low (L) and logic high (H) states, respectively.

If the DGND pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+ and V^-. Additionally, if A2 or A1 or A0 pins are left floating, internal resistors pull the voltage on each of these pins close to the DGND pin, resulting in a default logic low (L) state for that programming pin. As a result, if A2 and A1 and A0 pins are left floating all at the same time, the LTC6373 will have a gain setting of G = 16. When these pins are left open, care should be taken to control leakage currents at these pins to prevent inadvertently putting the LTC6373 into an undesired gain setting.

APPLICATIONS INFORMATION

Keep in mind that any change in voltages applied to A2 or A1 or A0 pins from logic low to logic high (or vice versa) immediately results in a gain setting change for LTC6373 (transparent mode).

Valid Input and Output Range

Instrumentation amplifiers traditionally specify a valid input common mode range and an output swing range. This however often fails to identify swing limitations associated with internal nodes, as they experience a combination of gained differential signal and common mode signal. Referring to the Simplified Block Diagram of Figure 1, the output swing of amplifiers A1, A2, and A3 as well as the common mode input range of the output differential amplifier A3 impose limitations on the valid operating range. The graphs in Figure 2 show the maximum input common mode voltage limits where a valid output is produced for each gain setting of LTC6373.

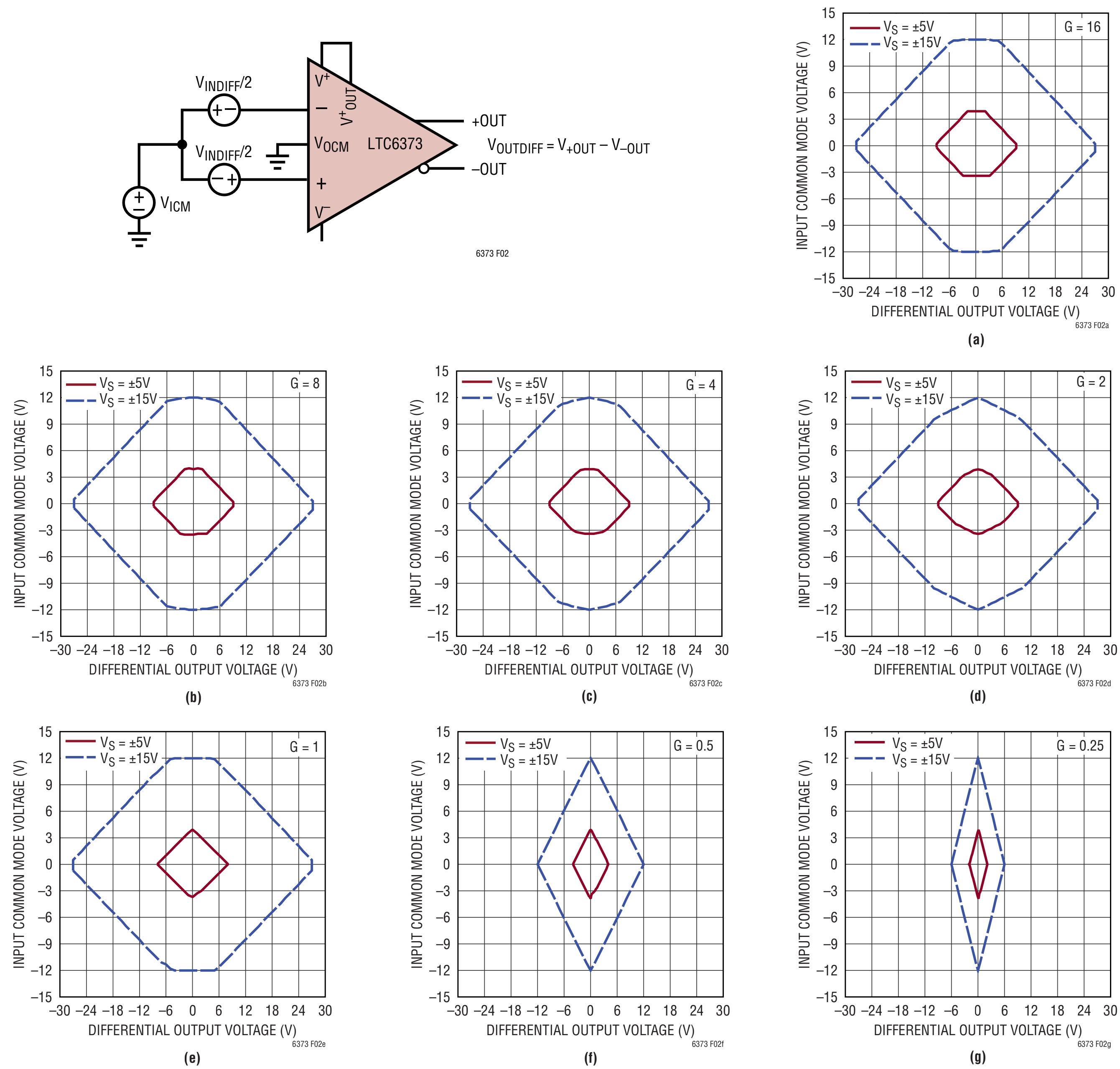


Figure 2. Input Common Mode Range vs Differential Output Voltage for Each Gain Setting of LTC6373 with No Load

APPLICATIONS INFORMATION

Diamond Plot Interpretation

Diamond plots can be used to determine the valid input common mode voltage (V_{ICM}) operating range for instrumentation amplifiers such as LTC6373. The valid region of operation is where all signals, input or output, are not clipped.

Subplots (a)-(g) of Figure 2 show the input common mode voltage (V_{ICM}) range allowed for a given differential output voltage ($V_{OUTDIFF}$), under various combinations of gain (G) and supply (V_S) settings. In each plot, the output stage positive supply pin V^+_{OUT} is tied to the main positive supply pin V^+, V_{OCM} = 0V (mid-rail) and there is no load.

To identify the valid V_{ICM} range for a specific application: First, identify the gain and supply conditions that the LTC6373 will be operated under. Then, identify the range of valid differential output voltages ($V_{OUTDIFF}$) desired. For example, this could be the full-scale signal that is optimal for the subsequent ADC's SNR.

This combination of settings and output range implies a specific differential input signal (V_{INDIFF}) range, since $V_{INDIFF} = V_{OUTDIFF}/G$.

While the input signal's V_{INDIFF} is fixed when specific $V_{OUTDIFF}$ and G are chosen, the input signal's common mode voltage V_{ICM} is not, because the same V_{INDIFF} can be superimposed on many different V_{ICM} values.

The valid V_{ICM} range can be set by the swing limits on +IN and/or –IN, since V_{ICM} is the average of +IN and –IN. It can also be set by internal node swing limits, since the internal nodes are also operating with common mode voltage V_{ICM}, and these nodes must also be able to swing enough away from V_{ICM} to produce the gained-up output.

On a diamond plot, this valid region of operation for V_{ICM} for a specific output $V_{OUTDIFF}$ is indicated by the portion of the vertical line going straight up from $V_{OUTDIFF}$ that falls inside the diamond borders, as shown in Figure 3.

If the part's input common mode voltage is within the V_{ICM} borders of the diamond, there should be no problems with clipping. If the differential input signal is shifted by a V_{ICM} value that is outside of the diamond, either +IN or –IN (or internal nodes) will be clipped, or the output itself will hit the rails, and thus result in a clipped output.

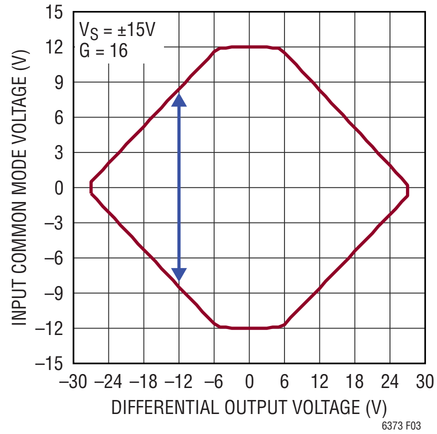


Figure 3. The Blue Arrow Indicates the Range of Valid V_{ICM} Values for $V_{OUTDIFF}$ = –12V, Where No Signals are Clipped, for the V_S = ±15V, G = 16 Case

The following example shows how a diamond plot point is determined. For the specific case of $V_{OUTDIFF}$ = –12V as shown in Figure 3, the upper limit of V_{ICM} is 8V, and the lower limit is –8V.

For V_{ICM} = 8V, if the gained-up input (aka output) is –12V, the maximum negative internal node swing is 6V above V_{ICM}. Referenced to ground, this internal node reaches 8V + 6V = 14V, which is roughly the output high limit of LTC6373 with ±15V supplies. If V_{ICM} were any higher than 8V, the internal node would run into the output high limit, and the output would clip.

For V_{ICM} = –8V, with –12V output, the minimum positive internal node swing is –6V below V_{ICM}. Referenced to ground, this internal node can hit a minimum of –6V + (–8V) = –14V, which is roughly the output low limit of LTC6373 with ±15V supplies. If V_{ICM} were any lower than –8V, this internal node would run into the output low limit, and the output would clip.

APPLICATIONS INFORMATION

Output Common Mode and V_{OCM} Pin

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = (V_{+OUT} + V_{-OUT})/2 = V_{OCM}$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the V_{OCM} pin, by means of an internal common mode feedback loop. If the V_{OCM} pin is left floating, an internal resistor divider creates a default voltage approximately halfway between V^+_{OUT} and V^-. The V_{OCM} pin can be overdriven to another voltage if desired for greater accuracy or flexibility. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the V_{OCM} pin, as long as the ADC is capable of driving the 2.3MΩ input resistance presented by the V_{OCM} pin. The Electrical Characteristics table specifies the valid range that can be applied to the V_{OCM} pin (V_{OUTCMR}).

Input Pin Protection

To prevent damage, the LTC6373 has a comprehensive protection scheme, especially on the input pins, as illustrated in the Simplified Block Diagram of Figure 1. The input current applied to the LTC6373's input pins should be kept under ±10mA. To achieve additional input protection, external series resistors and/or low leakage clamp diodes should be used.

Reducing Board-Related Leakage Effects

Leakage currents can have a significant impact on system accuracy, particularly in high temperature and high voltage applications. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

Leakage into the input pins reacts with the source resistance, creating an error directly at the input. As shown in Figure 4, this leakage can be minimized by enclosing the input connections with guard rings operated at a potential very close to that of the input pins. For the lowest leakage, amplifiers can be used to drive the guard rings. These buffers must have very low input bias current since that current will now be a leakage current.

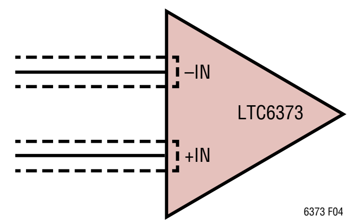


Figure 4. Guard Rings Can Be Used to Minimize Leakage into the Input Pins

Input Bias Current Return Path

The low input bias current (25pA max) and high input impedance (5000GΩ) of the LTC6373 allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a DC path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path, the inputs will float to either rail and exceed the input voltage range of the LTC6373, resulting in a saturated input amplifier. Figure 5 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both DC and AC common mode rejection as well as DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

APPLICATIONS INFORMATION

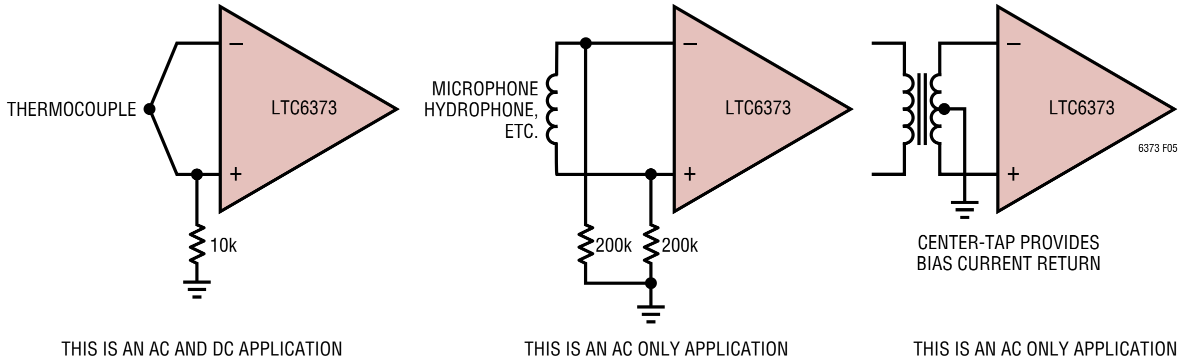


Figure 5. Providing an Input Common Mode Current Path

RF Interference

In many industrial and data acquisition applications, the LTC6373 will be used to process small signals accurately in the presence of large common mode voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry using shielded or unshielded twisted-pair cabling, the cabling may act as an antenna, conveying very high frequency interference directly into the input stage of the LTC6373.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing an unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively, or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

To help minimize this effect, high frequency signals can be filtered with a low pass RC network placed at the input of the LTC6373, as illustrated in Figure 6. The filter limits the input signal bandwidth according to the following formulas:

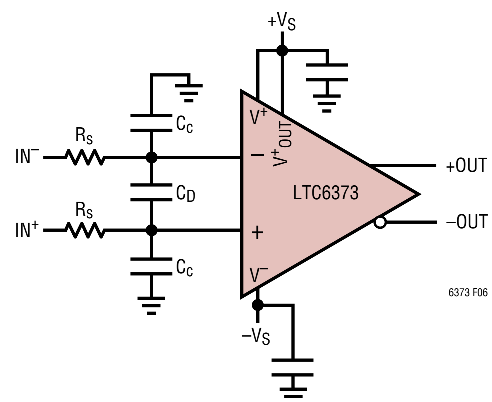


Figure 6. Adding a Simple External RC Filter at the Inputs of the LTC6373 Is Effective in Suppressing RF Interference.

$$FilterFreq_{DIFF} = 1/[2 \bullet \pi \bullet R_S \bullet (C_C + 2C_D)]$$

$$FilterFreq_{CM} = 1/[2 \bullet \pi \bullet R_S \bullet C_C]$$

Setting the filter frequencies requires knowledge of the frequency (or frequencies) of the RF interference. Once the interference frequency is known, the common mode filter frequency can be set (low enough to filter out the interference frequency) followed by the differential mode filter frequency. To avoid any possibility of inadvertently affecting the differential signal of interest, set the common mode filter frequency an order of magnitude (or more) higher than the differential mode filter frequency. Set the common mode filter frequency such that it does not

APPLICATIONS INFORMATION

degrade the LTC6373's inherent AC CMRR. To avoid any possibility of common mode to differential mode signal conversion, match the common mode filter frequencies (on positive and negative inputs of LTC6373) to 1% or better. Then the differential mode filter frequency can be set for the bandwidth of the signal to be processed in the application. Setting the differential mode filter frequency close to the sensor's bandwidth also minimizes any noise pickup along the leads. If the sensor is an RTD or a resistive strain gauge in close proximity to the LTC6373, then the series resistors R_S can be omitted. As an example, if the bandwidth of the signal of interest is 100kHz whereas the interference frequency is 10MHz and above, an appropriate choice for differential mode filter ($FilterFreq_{DIFF}$) and common mode filter ($FilterFreq_{CM}$) frequencies could be 200kHz/4MHz. Assuming R_S is chosen to be 1kΩ, using the formula provided earlier in this section results in C_C = 39pF and C_D = 390pF.

Error Budget Analysis

Figure 7 shows the LTC6373 in a typical application to buffer and amplify the differential output of a bridge transducer. The LTC6373 is programmed to a gain of 8V/V in this example and amplifies a differential, full-scale (FS) voltage of 100mV = 0.1V at transducer's output (or LTC6373's input). Table 2 shows the error budget in this application, listing various error sources in parts per million (ppm) normalized to full-scale voltage (0.1V) and across the temperature range of 25°C to 85°C. The LTC6373 achieves superior performance compared to all other monolithic programmable-gain instrumentation amplifiers (PGIA) in the market, enabling more accurate measurements.

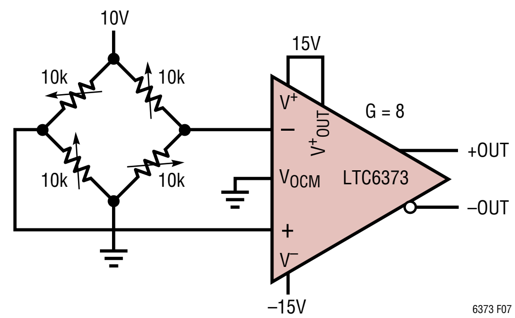


Figure 7. Precision Bridge Amplifier

Table 2. Error Budget Analysis

ERROR SOURCE	CALCULATION: LTC6373 (G = 8)	CALCULATION: CLOSEST COMPETITOR PGIA (G = 8)	ERROR, ppm OF INPUT FULL SCALE (FS): LTC6373 (G = 8)	ERROR, ppm OF INPUT FULL SCALE (FS): CLOSEST COMPETITOR PGIA (G = 8)
Absolute Accuracy at T_A = 25°C				
Gain Error	0.015% FS	0.05% FS	150	500
Offset Voltage (RTI)	(104µV)/0.1V	(1500µV)/0.1V	1040	15000
Input Offset Current	[(25pA)(10kΩ)/2]/0.1V	[(100pA)(10kΩ)/2]/0.1V	1	5
CMRR	[(5V)/(100dB)]/0.1V	[(5V)/(95dB)]/0.1V	500	889
		Total Accuracy Error	**1691**	**16394**
Temperature Drift to 85°C				
Gain Drift	(1ppm/°C)(60°C)	(10ppm/°C)(60°C)	60	600
Offset Voltage Drift (RTI)	[(1.8µV/°C)(60°C)]/0.1V	[(6µV/°C)(60°C)]/0.1V	1080	3600
		Total Drift Error	**1140**	**4200**
Resolution				
Gain Nonlinearity	3ppm	20ppm	3	20
Typ 0.1Hz to 10Hz Input Voltage Noise	$(1.2µV_{P-P})/0.1V$	$(1µV_{P-P})/0.1V$	12	10
		Total Resolution Error	**15**	**30**
		Grand Total Error	**2846**	**20624**

Rev. 0

APPLICATIONS INFORMATION

Dynamic Power Consumption Calculation

As shown in the Simplified Block Diagram of Figure 1, the LTC6373 has three internal chains of gain setting resistors. To achieve a low wideband noise for the LTC6373, a relatively small value, 4kΩ, has been chosen for the total resistance of each chain. The voltages across the three chains are:

1) $V_{OUT}A1$ to –OUT

2) $V_{OUT}A2$ to +OUT

3) $V_{OUT}A1$ to $V_{OUT}A2$

Each of these voltages is imposed across what is effectively one 4kΩ resistor, establishing currents in them. These three currents are independent of each other and the part's quiescent supply current (I_S), and all of them are drawn from the supplies.

For example, assume LTC6373 is being used with ±15V supplies (i.e., $V^+ = V^+_{OUT} = 15V$, $V^- = –15V$), $V_{OCM} = 0V$, G = 2, and has input voltages of +IN = 3V and –IN = –3V (i.e., $V_{ICM} = 0V$, $V_{INDIFF} = 6V$). The resulting output voltage is $V_{OUTDIFF} = 2 \bullet V_{INDIFF} = 12V$. Since $V_{OUTCM} = V_{OCM} = 0V$, this implies that the value of LTC6373's output voltages are +OUT = 6V, –OUT = –6V.

Since the gain is applied in the A1 and A2 amplifiers, the output voltages of these internal amplifiers are $V_{OUT}A1$ = +6V and $V_{OUT}A2$ = –6V, respectively.

Thus, the voltages and currents in each 4kΩ resistor chain are:

$$I_1 = [(V_{OUT}A1) - (-OUT)]/4k\Omega = [6V - (-6V)]/4k\Omega = 3mA$$

$$I_2 = [(+OUT) - (V_{OUT}A2)]/4k\Omega = [6V - (-6V)]/4k\Omega = 3mA$$

$$I_3 = [(V_{OUT}A1) - (V_{OUT}A2)]/4k\Omega = [6V - (-6V)]/4k\Omega = 3mA$$

Therefore, the total supply current is:

$$I_{TOTAL} = I_S + I_1 + I_2 + I_3 = 4.4mA + 3 \bullet 3mA = 13.4mA$$

In case the output pins (+OUT, –OUT) of the LTC6373 connect to resistive loads, the currents provided by the LTC6373 to these loads should also be added to the calculations above.

Board Layout and Bypass Capacitors

It is recommended that high quality 0.1µF ceramic bypass capacitors be placed directly between the V^+ pin and the V^- pin (exposed pad), between V^+ and ground plane, and between V^- and ground plane with minimal routing. In applications where V^+_{OUT} pin is not directly connected to V^+, it is recommended that additional high quality 0.1µF ceramic capacitors be used to bypass V^+_{OUT} to ground and V^+_{OUT} to V^-, again with minimal routing. Small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than leaded capacitors, and perform best with the LTC6373.

Always keep in mind the differential nature of the LTC6373. At the inputs, keep any (intended or parasitic) resistance and capacitance as balanced and symmetric as possible to preserve AC CMRR performance of the amplifier. Apply the same practice at the output, because it is equally critical that the load impedances seen by both outputs (intended or parasitic) be as balanced and symmetric as possible. This will help preserve the balanced operation of the LTC6373 that minimizes the generation of even-order harmonics and maximizes the rejection of common mode noise and signals.

To minimize thermocouple induced errors, further attention must be given to board layout and component selection. It is good practice to minimize the number of junctions in the LTC6373's input signal paths and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

The V_{OCM} pin should be bypassed to the ground plane with a high quality 0.1µF ceramic capacitor. This will prevent common mode signals and noise on this pin from being inadvertently converted to differential signals and noise by

APPLICATIONS INFORMATION

impedance mismatches internally to the IC. Additionally, the CAP pin should be bypassed to the ground plane with a high quality 180pF ceramic capacitor to ensure proper operation of LTC6373 across its different gain settings.

To prevent coupling noise onto LTC6373, shield fast switching digital signals where they are in proximity of analog signals on the board.

Driving High Precision ADCs

The LTC6373 makes an excellent PGIA for use in data acquisition systems. Attributes such as fully differential outputs, good DC precision, low noise, low distortion, and high bandwidth enable LTC6373 to drive ADCs directly in many signal conditioning applications. The recommended list of precision SAR ADCs for use with the LTC6373 is shown in Table 3. The circuit in Figure 8 shows an example of the LTC6373 driving a precision ADC such as the AD4020 (a 20-bit, 1.8Msps, SAR ADC) or AD7134 (a 24-bit, 1.5Msps, Continuous-Time, Σ-Δ ADC). The LTC6373 is DC-coupled on the input and the output, which eliminates the need for a transformer to drive the ADC. The LTC6373 gain is programmed to its desired setting using A2/A1/A0 pins, as previously described in the Gain Selection section of this data sheet. In the example of Figure 8, the LTC6373 is being used in a differential input to differential output configuration with dual supplies of ±15V. It can also be used in a single-ended input to differential output configuration.

The V_{OCM} pin is biased to $V_{REF}/2$ (which is provided directly by the ADC in some products). This achieves level shifting of the outputs of the LTC6373 to match the desired input common mode of the ADC. In Figure 8, each of the LTC6373 outputs swings between 0V and V_{REF} (opposite in phase), thus providing $2V_{REF}$ peak-to-peak differential signal to the ADC inputs. In some cases, an RC network between the LTC6373 outputs and the ADC inputs is required providing a single-pole, low-pass filter to help reduce nonlinear charge kickback due to ADC input switching as well as limiting the broadband noise.

Table 3. Recommended SAR ADCs

Resolution (Bits)	Product	Max Throughput (Msps)	Power @ Max Throughput (mW)	Typical SNR (dB)
20	AD4020	1.8	15	100.5
	LTC2378-20	1	21	104
18	AD4003	2	16	100.5
	LTC2379-18	1.6	18	101.2
16	AD4001	2	16	96.2
	LTC2380-16	2	19	96.2

Applications Information

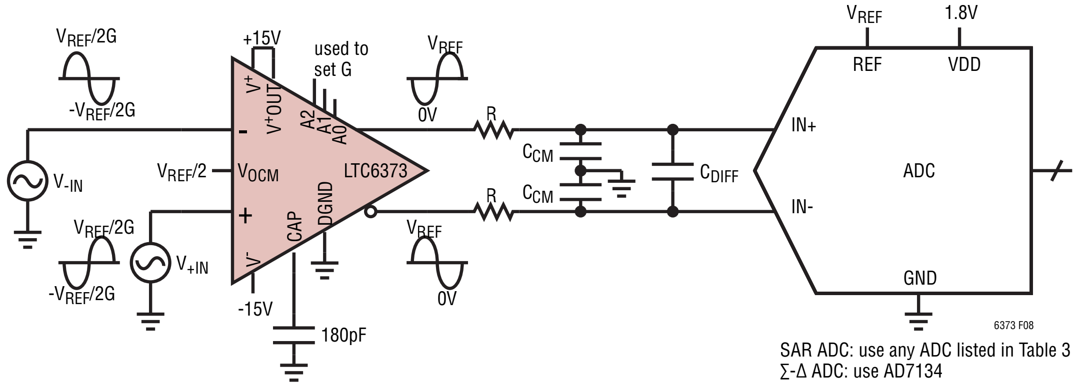


Figure 8. LTC6373 Driving Precision ADC

As a more specific example, Figure 9 and Figure 10 show typical Signal-to-Noise Ratio (SNR) and Total Harmonic Distortion (THD) of the LTC6373 driving the AD4020 SAR ADC (with high-Z mode enabled) at a near full-scale signal for various ADC throughputs. The recommended RC filter values used in Figure 8 for optimum performance at each throughput are listed in Table 4, as well as the selected reference voltage (V_{REF}).

Table 4. RC Filter Selection for LTC6373 Driving AD4020 (at Various Throughputs)

ADC	Throughput (Msps)	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADC Inputs (V_{P-P})	R (Ω)	C_{CM} (pF)	C_{DIFF} (pF)	Typical SNR (dB)	Typical THD (dB)
AD4020	1.8	5	10	442	180	Open	See Figure 9	See Figure 10
	1	5	10	887	180	Open	See Figure 9	See Figure 10
	0.6	5	10	887	180	Open	See Figure 9	See Figure 10

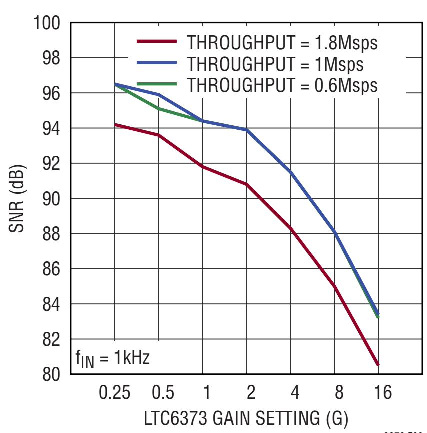


Figure 9. SNR for LTC6373 Driving AD4020

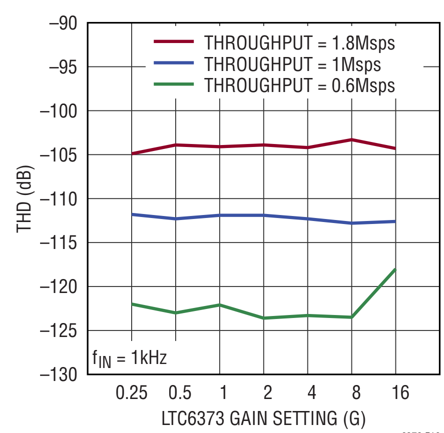


Figure 10. THD for LTC6373 Driving AD4020

APPLICATIONS INFORMATION

Table 5 lists the typical SNR and THD achieved when the ADC used in Figure 8 is AD7134 Σ-Δ ADC being driven directly (with no RC filter in between) by the LTC6373 at a near full-scale signal.

In some applications, it might be beneficial to use a separate amplifier/ADC driver between the LTC6373 and the precision ADC to ease the settling requirements on the LTC6373 and improve the linearity and THD performance of the signal chain. An implementation of such signal chain can be achieved by using the ADAQ4003, a precision data acquisition μModule which integrates multiple signal conditioning and processing blocks inside a single package. These blocks include a fully differential ADC driver, a stable reference buffer, an 18-bit, 2Msps, SAR ADC, as well as critical passive components necessary for optimum performance. This μModule achieves 4X footprint reduction by itself (compared to discrete solution) without sacrificing any performance.

The ADAQ4003 offers pin-selectable gain or attenuation options, giving the user the flexibility to match to their input signal range. This is showcased in Figures 11-19 as LTC6373 is directly driving the ADAQ4003 at its 3 different gain options, in each case providing the signal amplitude necessary to utilize the maximum $2V_{REF}$ peak-to-peak differential signal range of the ADC inside the ADAQ4003 μModule.

Table 5. SNR and THD Results for LTC6373 Directly Driving AD7134 (at 250ksps)

ADC	LTC6373 Gain Setting (G)	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADC Inputs (V_{P-P})	R (Ω)	C_{CM} (pF)	C_{DIFF} (pF)	f_{IN} (kHz)	Typical SNR (dB)	Typical THD (dB)
AD7134	0.25	4.096	8.192	0	Open	Open	1	108.4	–124
							20	107.7	–97
	1	4.096	8.192	0	Open	Open	1	107.2	–121
							20	106.9	–100
	16	4.096	8.192	0	Open	Open	1	94.3	–112
							20	94.3	–93

Table 6. Details for LTC6373 Driving ADAQ4003 at 3 Different Gain Options and Signal Amplitudes

ADAQ4003 Gain	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADAQ4003 Inputs (V_{P-P})	Circuit Configuration	Typical SNR (dB)	Typical THD (dB)
0.454	5	22	See Figure 11	See Figure 12	See Figure 13
0.9	5	11	See Figure 14	See Figure 15	See Figure 16
1.9	5	5.2	See Figure 17	See Figure 18	See Figure 19

APPLICATIONS INFORMATION

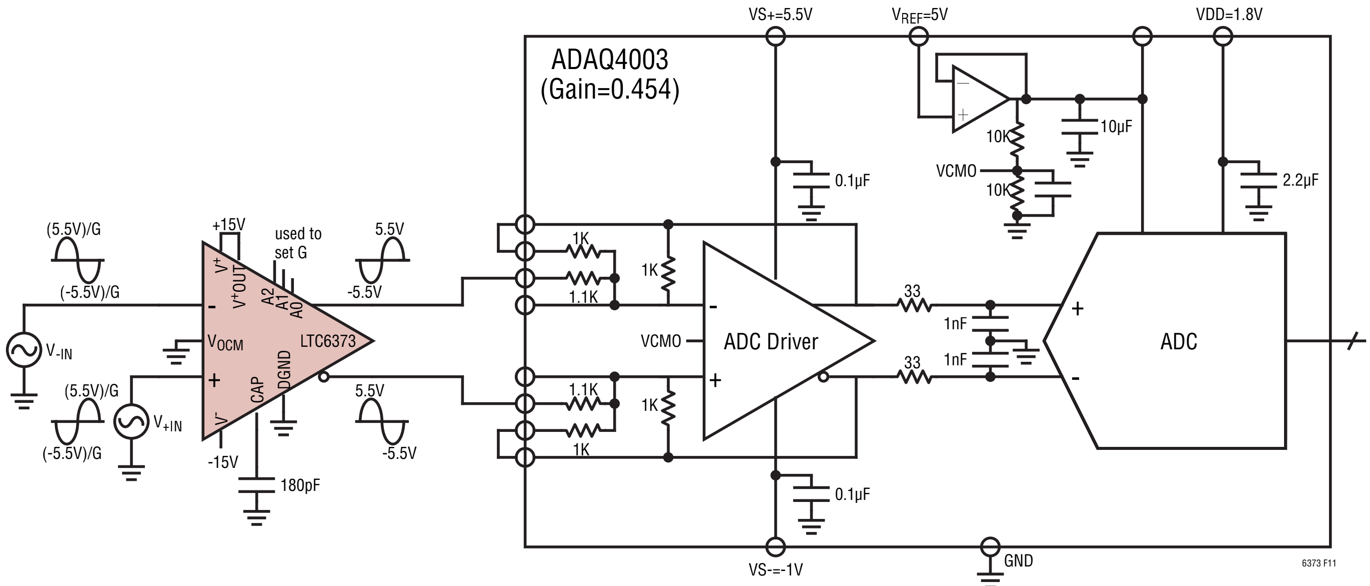


Figure 11. LTC6373 Driving ADAQ4003 (Gain = 0.454)

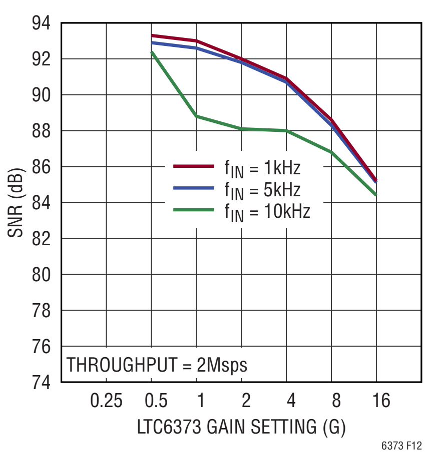


Figure 12. SNR for LTC6373 Driving ADAQ4003 (Gain = 0.454)

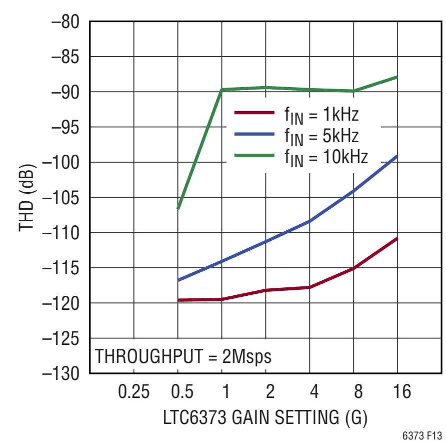


Figure 13. THD for LTC6373 Driving ADAQ4003 (Gain = 0.454)

Rev. 0

APPLICATIONS INFORMATION

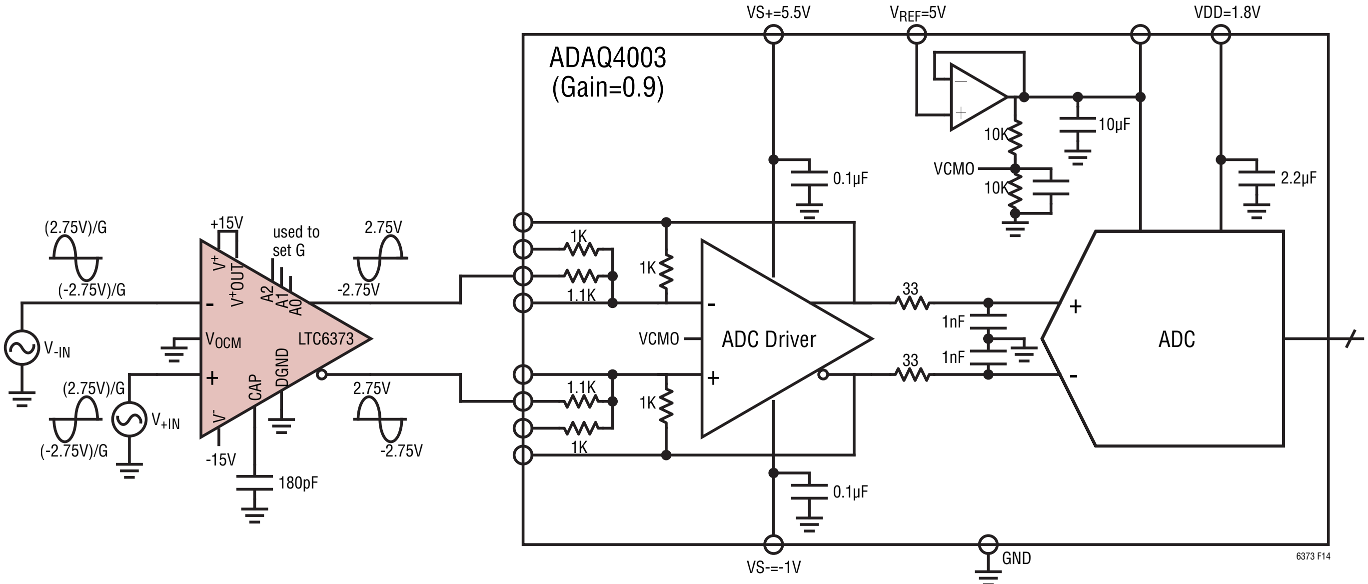


Figure 14. LTC6373 Driving ADAQ4003 (Gain = 0.9)

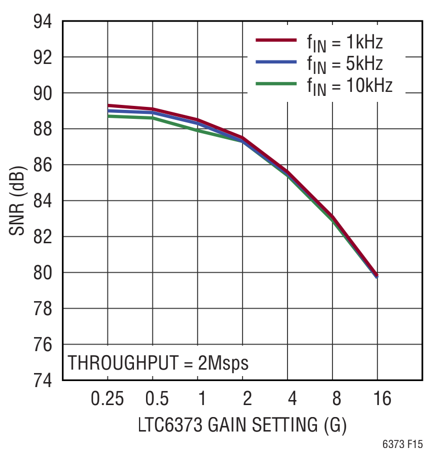


Figure 15. SNR for LTC6373 Driving ADAQ4003 (Gain = 0.9)

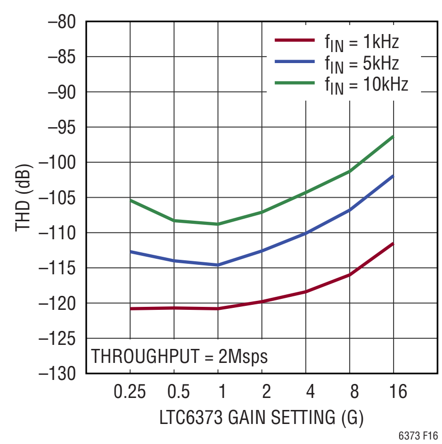


Figure 16. THD for LTC6373 Driving ADAQ4003 (Gain = 0.9)

APPLICATIONS INFORMATION

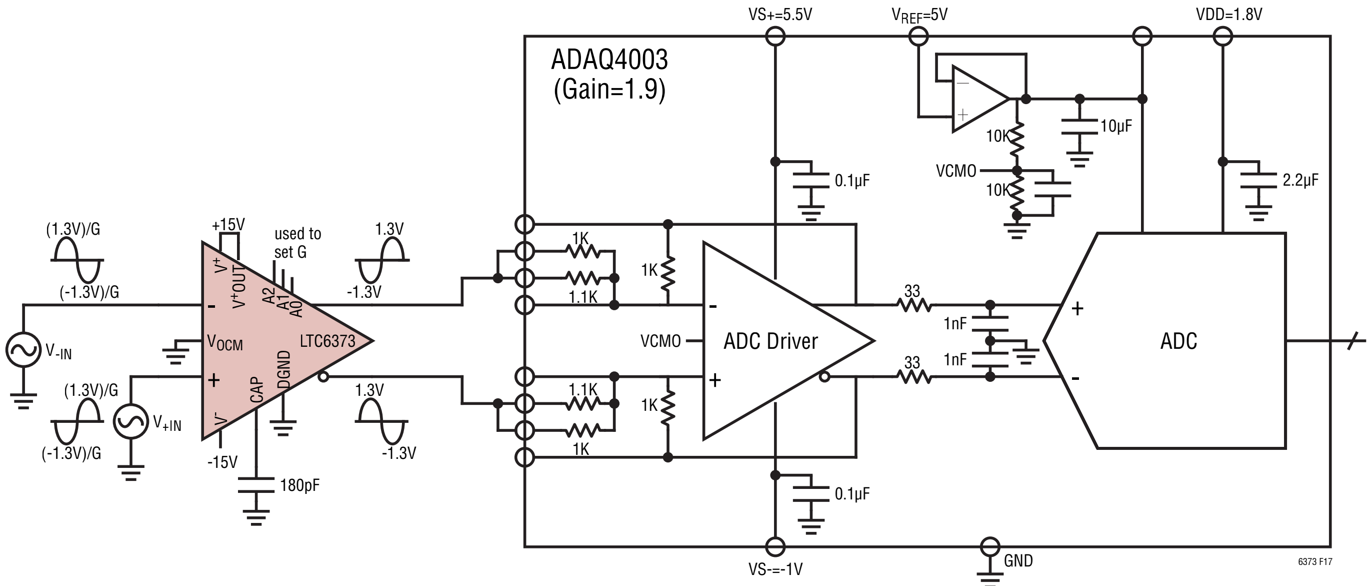


Figure 17. LTC6373 Driving ADAQ4003 (Gain = 1.9)

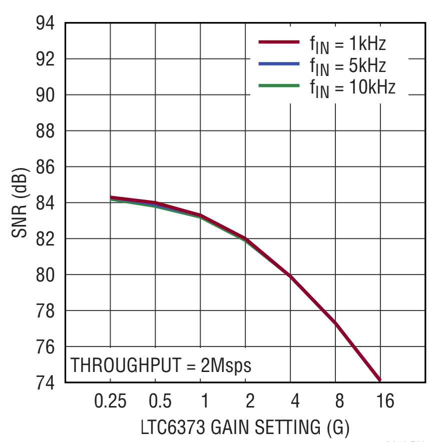


Figure 18. SNR for LTC6373 Driving ADAQ4003 (Gain = 1.9)

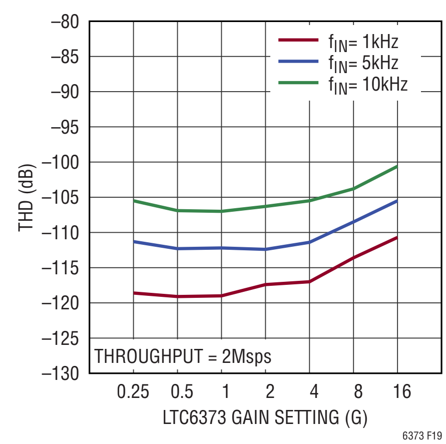


Figure 19. THD for LTC6373 Driving ADAQ4003 (Gain = 1.9)

APPLICATIONS INFORMATION

As another data acquisition system example, the circuit of Figure 20 shows the LTC6373 driving the AD7768-1 (a 24-bit, 256ksps, Σ-Δ ADC) through the ADA4945-1 (a high speed, fully differential ADC driver). The ADC driver in this circuit has been configured with a closed-loop gain of 1.3V/V (by using matched discrete resistors) and once again the LTC6373 in conjunction with the ADA4945-1 provide the maximum $2V_{REF}$ peak-to-peak differential signal range needed at the AD7768-1 inputs. More details about this circuit can be found in Table 7 and the typical SNR and THD achieved by this signal chain are illustrated in Figure 21 and Figure 22.

Table 7. Details for LTC6373 Driving AD7768-1 Through ADA4945-1

ADC	V_{REF} (V)	Signal Level at LTC6373 Outputs = ADC Driver Inputs (V_{P-P})	Signal Level at ADC Driver Outputs = ADC Inputs (V_{P-P})	Typical SNR (dB)	Typical THD (dB)
AD7768-1	4.096	6.3	8.192	See Figure 21	See Figure 22

APPLICATIONS INFORMATION

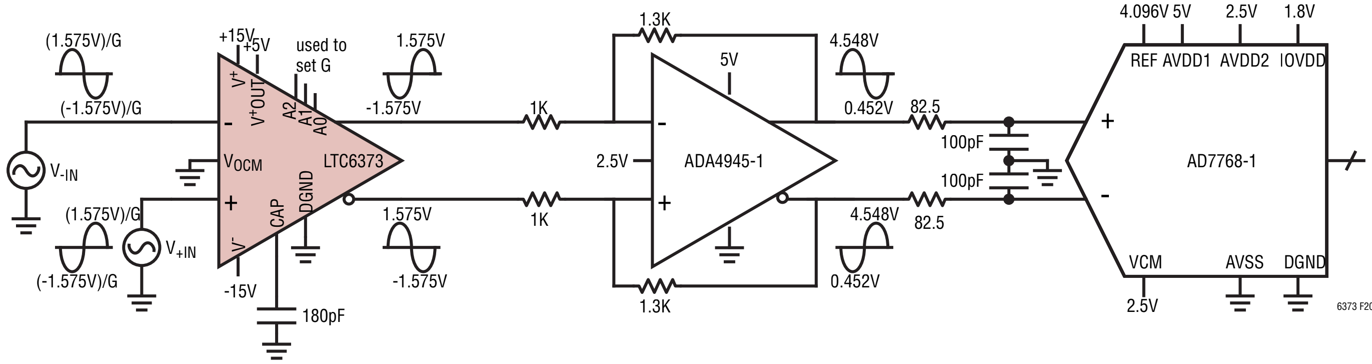


Figure 20. LTC6373 (PGIA) + ADA4945-1 (ADC Driver) + AD7768-1 (ADC) Signal Chain

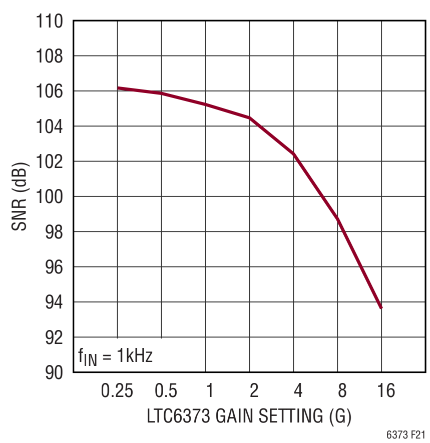


Figure 21. SNR for LTC6373 + ADA4945-1 + AD7768-1 Signal Chain

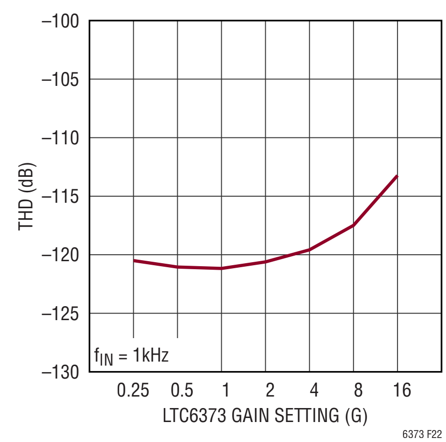
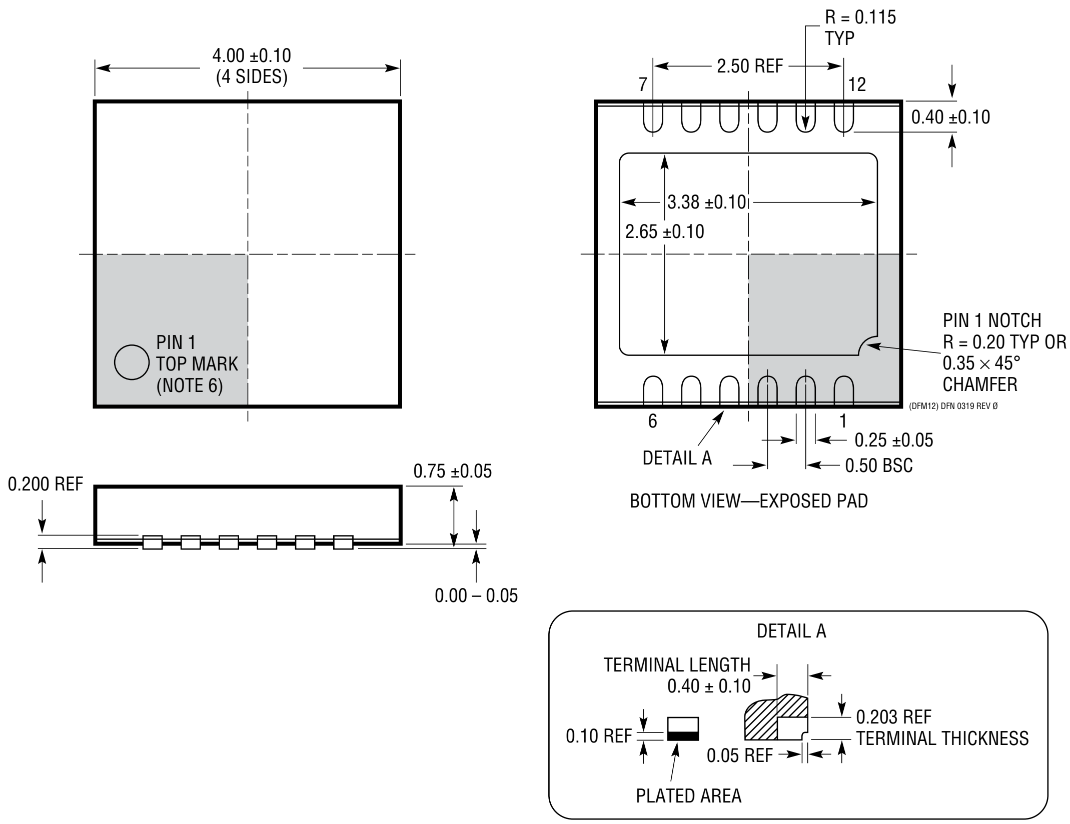


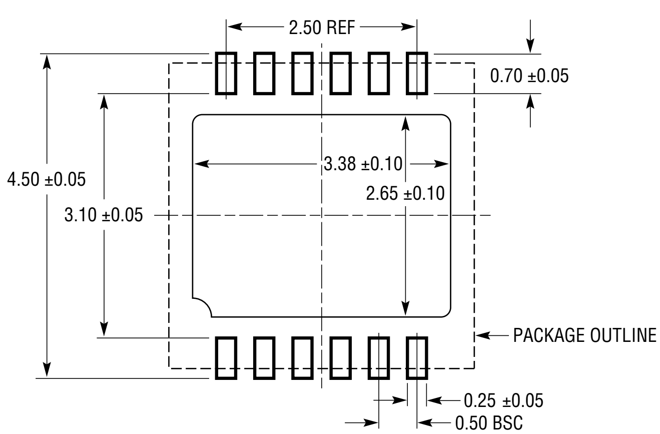
Figure 22. THD for LTC6373 + ADA4945-1 + AD7768-1 Signal Chain

PACKAGE DESCRIPTION

DFM Package
12-Lead Plastic Side Solderable DFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1791 Rev Ø)



NOTE:
1. PACKAGE OUTLINE DOES NOT CONFORM TO JEDEC MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.