200MHz, Low Noise, Low Power Fully Differential Input/Output Amplifier/Driver

FEATURES

- **Very Low Distortion: ($2V_{P-P}$, 3MHz): –95dBc**
- **Fully Differential Input and Output**
- **Low Noise: 2.8nV/√Hz Input-Referred**
- **200MHz Gain-Bandwidth Product**
- **Built-In Clamp: Fast Overdrive Recovery**
- **Slew Rate: 200V/µs**
- Adjustable Output Common Mode Voltage
- Rail-to-Rail Output Swing
- Input Range Extends to Ground
- Large Output Current: 60mA (Typ)
- DC Voltage Offset <1.5mV (Max)
- 10.8mA Supply Current
- 2.7V to 5.25V Supply Voltage Range
- Low Power Shutdown
- Tiny 3mm × 3mm × 0.75mm 16-Pin QFN Package

APPLICATIONS

- Differential Input A/D Converter Driver
- Single-Ended to Differential Conversion/Amplification
- Common Mode Level Translation
- Low Voltage, Low Noise, Signal Processing

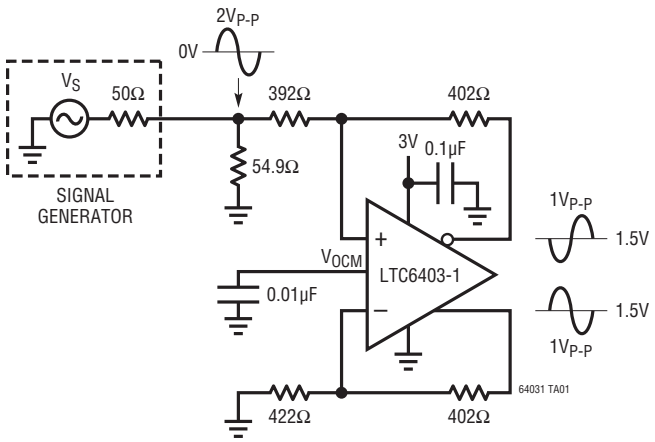
DESCRIPTION

The LTC®6403-1 is a precision, very low noise, low distortion, fully differential input/output amplifier optimized for 3V to 5V, single supply operation. The LTC6403-1 is unity gain stable. The LTC6403-1 closed-loop bandwidth extends from DC to 200MHz. In addition to the normal unfiltered outputs (+OUT and –OUT), the LTC6403-1 has a built-in 44.2MHz differential single-pole lowpass filter and an additional pair of filtered outputs (+OUTF, and –OUTF). An input referred voltage noise of 2.8nV/√Hz enables the LTC6403-1 to drive state-of-the-art 14- to 18-bit ADCs while operating on the same supply voltage, saving system cost and power. The LTC6403-1 maintains its performance for supplies as low as 2.7V. It draws only 10.8mA, and has a hardware shutdown feature which reduces current consumption to 170µA.

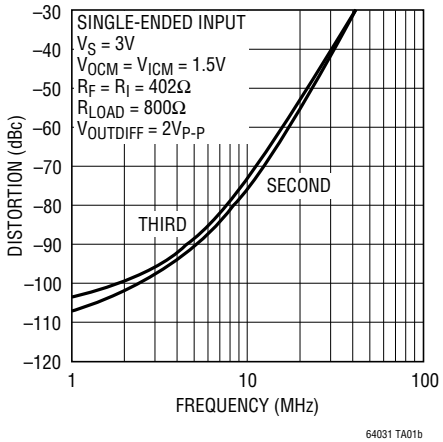
The LTC6403-1 is available in a compact 3mm × 3mm 16-pin leadless QFN package and operates over a –40°C to 125°C temperature range.

TYPICAL APPLICATION

Single-Ended Input to Differential Output With Common Mode Level Shifting



Harmonic Distortion vs Frequency

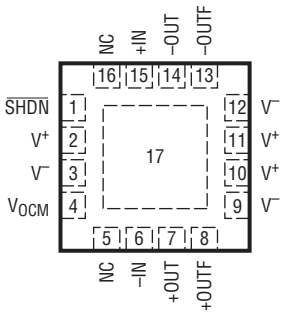


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 5.5V
Input Voltage
(+IN, –IN, V_{OCM}, $\overline{SHDN}$) (Note 2) ..... V^+ to V^-
Input Current
(+IN, –IN, V_{OCM}, $\overline{SHDN}$) (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4)
LTC6403C-1/LTC6403I-1 ..... –40°C to 85°C
LTC6403H-1 ..... –40°C to 125°C
Specified Temperature Range (Note 5)
LTC6403C-1/LTC6403I-1 ..... –40°C to 85°C
LTC6403H-1 ..... –40°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 160°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC6403-1#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6403CUD-1#PBF	LTC6403CUD-1#TRPBF	LDBM	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC6403IUD-1#PBF	LTC6403IUD-1#TRPBF	LDBM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC6403HUD-1#PBF	LTC6403HUD-1#TRPBF	LDBM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

LTC6403-1 DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$ = OPEN, R_I = 402Ω, R_F = 402Ω, R_L = OPEN, R_{BAL} = 100k (See Figure 1) unless otherwise noted. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$). V_{INDIFF} is defined as ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_S = 2.7V V_S = 3V V_S = 5V	● ● ●		±0.4 ±0.4 ±0.4	±1.5 ±1.5 ±2	mV mV mV
$\Delta V_{OSDIFF}/\Delta T$	Differential Offset Voltage Drift (Input Referred)	V_S = 2.7V V_S = 3V V_S = 5V			1 1 1		µV/°C µV/°C µV/°C
I_B	Input Bias Current (Note 6)	V_S = 2.7V V_S = 3V V_S = 5V	● ● ●	–25 –25 –25	–7.5 –7.5 –7.5	0 0 0	µA µA µA
I_{OS}	Input Offset Current (Note 6)	V_S = 2.7V V_S = 3V V_S = 5V	● ● ●		±0.2 ±0.2 ±0.2	±5 ±5 ±5	µA µA µA

LTC6403-1 DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$ = OPEN, R_I = 402Ω, R_F = 402Ω, R_L = OPEN, R_{BAL} = 100k (See Figure 1) unless otherwise noted. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$). V_{INDIFF} is defined as ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	Common Mode Differential Mode			1.7 14		MΩ kΩ
C_{IN}	Input Capacitance	Differential Mode			1		pF
e_n	Differential Input Referred Noise Voltage Density	f = 1MHz			2.8		nV/√Hz
i_n	Input Noise Current Density	f = 1MHz			1.8		pA/√Hz
e_{nVOCM}	Input Referred Common Mode Output Noise Voltage Density	f = 1MHz, V_{OCM} Shorted to Ground, V^+ = 1.5V, V^- = –1.5V			17		nV/√Hz
V_{ICMR}	Input Signal Common Mode Range (Note 7)	V_S = 3V V_S = 5V	● ●	0 0		1.6 3.6	V V
CMRRI	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$ (Note 8)	V_S = 3V, ΔV_{ICM} = 0.75V V_S = 5V, ΔV_{ICM} = 1.25V	● ●	50 50	72 72		dB dB
CMRRIO	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$ (Note 8)	V_S = 5V, ΔV_{OCM} = 2V	●	50	90		dB
PSRR	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$) (Note 9)	V_S = 2.7V to 5.25V	●	60	97		dB
PSRRCM	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$) (Note 9)	V_S = 2.7V to 5.25V	●	45	63		dB
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = 5V, ΔV_{OCM} = 2V	●		1		V/V
ΔG_{CM}	Common Mode Gain Error (100 • (G_{CM} – 1))	V_S = 5V, ΔV_{OCM} = 2V	●	–0.4	–0.1	0.3	%
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V Single-Ended Input Differential Input	 ● ●		 –63 –66	 –45 –45	 dB dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} – V_{OCM}$)	V_S = 2.7V V_S = 3V V_S = 5V	● ● ●		±10 ±10 ±10	±25 ±25 ±25	mV mV mV
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift	V_S = 2.7V V_S = 3V V_S = 5V			20 20 20		µV/°C µV/°C µV/°C
V_{OUTCMR}	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin) (Note 7)	V_S = 3V V_S = 5V	● ●	1.1 1.1		2 4	V V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	15	23	32	kΩ
V_{OCM}	Voltage at the V_{OCM} Pin (Self-Biased)	V_S = 3V, V_{OCM} = Open	●	1.45	1.5	1.55	V
V_{OUT}	Output Voltage, High, Either Output Pin (Note 10)	V_S = 3V, I_L = 0 –40°C to 85°C –40°C to 125°C V_S = 3V, I_L = 5mA –40°C to 85°C –40°C to 125°C V_S = 3V, I_L = 20mA –40°C to 85°C –40°C to 125°C	 ● ● ● ● ● ●		 190 194 190 193 340 342	 300 330 300 330 490 520	 mV mV mV mV mV mV
		V_S = 5V, I_L = 0 –40°C to 85°C –40°C to 125°C V_S = 5V, I_L = 5mA –40°C to 85°C –40°C to 125°C V_S = 5V, I_L = 20mA –40°C to 85°C –40°C to 125°C	 ● ● ● ● ● ●		 170 173 195 197 380 383	 300 330 340 370 550 580	 mV mV mV mV mV mV

LTC6403-1 DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$ = OPEN, R_I = 402Ω, R_F = 402Ω, R_L = OPEN, R_{BAL} = 100k (See Figure 1) unless otherwise noted. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$). V_{INDIFF} is defined as ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage, Low, Either Output Pin (Note 10)	V_S = 3V, I_L = 0					
		–40°C to 85°C	●		150	220	mV
		–40°C to 125°C	●		154	250	mV
		V_S = 3V, I_L = –5mA					
		–40°C to 85°C	●		165	245	mV
		–40°C to 125°C	●		171	275	mV
		V_S = 3V, I_L = –20mA					
		–40°C to 85°C	●		210	300	mV
		–40°C to 125°C	●		224	330	mV
		V_S = 5V, I_L = 0					
		–40°C to 85°C	●		165	265	mV
		–40°C to 125°C	●		170	295	mV
		V_S = 5V, I_L = –5mA					
		–40°C to 85°C	●		175	275	mV
		–40°C to 125°C	●		182	305	mV
		V_S = 5V, I_L = –20mA					
		–40°C to 85°C	●		225	350	mV
		–40°C to 125°C	●		242	380	mV
I_{SC}	Output Short-Circuit Current, Either Output Pin (Note 11)	V_S = 2.7V	●	±30	±58		mA
		V_S = 3V	●	±30	±60		mA
		V_S = 5V	●	±35	±74		mA
A_{VOL}	Large-Signal Voltage Gain	V_S = 3V			90		dB
V_S	Supply Voltage Range		●	2.7		5.25	V
I_S	Supply Current	V_S = 2.7V	●		10.7	11.8	mA
		V_S = 3V	●		10.8	11.8	mA
		V_S = 5V	●		11	12.1	mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	V_S = 2.7V	●		0.16	0.5	mA
		V_S = 3V	●		0.17	0.5	mA
		V_S = 5V	●		0.26	1	mA
V_{IL}	$\overline{SHDN}$ Input Logic Low	V_S = 2.7V to 5V	●			V^+ – 2.1	V
V_{IH}	$\overline{SHDN}$ Input Logic High	V_S = 2.7V to 5V	●	V^+ – 0.6			V
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pull-Up Resistor	V_S = 5V, $V_{\overline{SHDN}}$ = 2.9V to 0V		40	66	90	kΩ
t_{ON}	Turn-On Time	V_S = 3V, $V_{\overline{SHDN}}$ = 0.5V to 3V			4		µs
t_{OFF}	Turn-Off Time	V_S = 3V, $V_{\overline{SHDN}}$ = 3V to 0.5V			350		ns

LTC6403-1 AC ELECTRICAL CHARACTERISTICS

The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$ = OPEN, R_I = 402Ω, R_F = 402Ω, R_T = 25.5Ω, unless otherwise noted (See Figure 2). V_S is defined ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$). V_{INDIFF} is defined as ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{OVDR}	Output Overdrive Recovery	No Glitches			70		ns
SR	Slew Rate	V_S = 3V			200		V/µS
		V_S = 5V			200		V/µS
GBW	Gain-Bandwidth Product	V_S = 3V			200		MHz
		V_S = 5V			200		MHz
f_{3dB}	–3dB Frequency (See Figure 2)	V_S = 3V	•	100	200		MHz
		V_S = 5V	•	100	200		MHz

LTC6403-1 AC ELECTRICAL CHARACTERISTICS

The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = Mid-Supply, $V_{\overline{SHDN}}$ = OPEN, R_I = 402Ω, R_F = 402Ω, R_T = 25.5Ω, unless otherwise noted (See Figure 2). V_S is defined ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$). V_{INDIFF} is defined as ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	3MHz Distortion	V_S = 3V, $V_{OUTDIFF}$ = $2V_{P-P}$ Single-Ended Input					
HD2		2nd Harmonic			–97		dBc
HD3		3rd Harmonic			–95		dBc
	3MHz Distortion	V_S = 3V, $V_{OUTDIFF}$ = $2V_{P-P}$ Differential Input					
HD2		2nd Harmonic			–106		dBc
HD3		3rd Harmonic			–94		dBc
IMD	Third-Order IMD at 10MHz f1 = 9.5MHz, f2 = 10.5MHz	V_S = 3V, $V_{OUTDIFF}$ = $2V_{P-P}$ Envelope			–72		dBc
OIP3	Equivalent OIP3 at 3MHz (Note 12)	V_S = 3V			48		dBm
t_S	Settling Time 2V Step at Output	V_S = 3V, Single-Ended Input					
		1% Settling			20		ns
		0.1% Settling			30		ns
NF	Noise Figure, f = 3MHz	R_{SOURCE} = 804Ω, R_I = 402Ω, R_F = 402Ω, V_S = 3V			10.8		dB
		R_{SOURCE} = 200Ω, R_I = 100Ω, R_F = 402Ω, V_S = 3V			8.9		dB
$f_{3dBFILTER}$	Differential Filter 3dB Bandwidth				44.2		MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs +IN, –IN are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA. Input pins (+IN, –IN, V_{OCM}, and $\overline{SHDN}$) are also protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely. Long term application of output currents in excess of the absolute maximum ratings may impair the life of the device.

Note 4: The LTC6403C-1/LTC6403I-1 are guaranteed functional over the operating temperature range –40°C to 85°C. The LTC6403H-1 is guaranteed functional over the operating temperature range –40°C to 125°C.

Note 5: The LTC6403C-1 is guaranteed to meet specified performance from 0°C to 70°C. The LTC6403C-1 is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6403I-1 is guaranteed to meet specified performance from –40°C to 85°C. The LTC6403H-1 is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Input bias current is defined as the average of the input currents flowing into Pin 6 and Pin 15 (–IN, and +IN). Input offset current is defined as the difference of the input currents flowing into Pin 15 and Pin 6 ($I_{OS} = I_B^+ – I_B^-$)

Note 7: Input common mode range is tested using the test circuit of Figure 1 by measuring the differential gain with a ±1V differential output with V_{ICM} = mid-supply, and also with V_{ICM} at the input common mode range limits listed in the Electrical Characteristics table, verifying that the differential gain has not deviated from the mid supply common mode input case by more than 1%, and the common mode offset (V_{OSCM}) has not deviated from the mid-supply case by more than ±10mV.

The voltage range for the output common mode range is tested using the test circuit of Figure 1 by applying a voltage on the V_{OCM} pin and testing at both mid supply and at the Electrical Characteristics table limits to verify that the differential gain has not deviated from the mid supply V_{OCM} case by more than 1%, and the common mode offset (V_{OSCM}) has not deviated by more than ±10mV from the mid supply case.

Note 8: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred voltage offset. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred voltage offset. These specifications are strongly dependent on feedback ratio matching between the two outputs and their respective inputs, and it is difficult to measure actual amplifier performance. See The Effects of Resistor Pair Mismatch in the Applications Information section of this data sheet. For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

Note 9: Differential power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred voltage offset. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset, $V_{OUTCM} – V_{OCM}$.

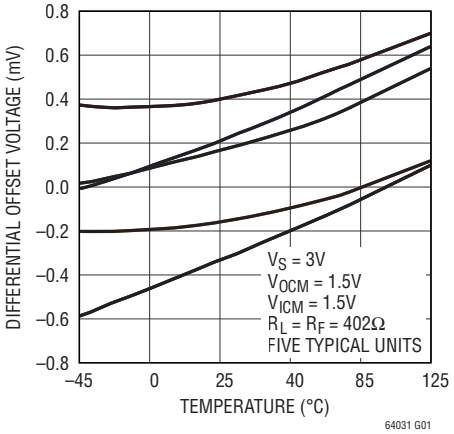
Note 10: Output swings are measured as differences between the output and the respective power supply rail.

Note 11: Extended operation with the output shorted may cause junction temperatures to exceed the 150°C limit and is not recommended. See Note 3 for more details.

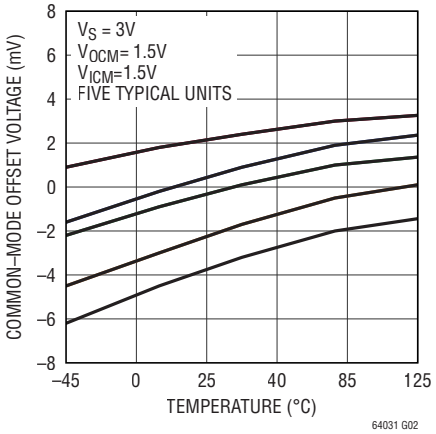
Note 12: A resistive load is not required when driving an AD converter with the LTC6403-1. Therefore, typical output power is very small. In order to compare the LTC6403-1 with amplifiers that require 50Ω output load, the LTC6403-1 output voltage swing driving a given R_L is converted to OIP3 as if it were driving a 50Ω load. Using this modified convention, $2V_{P-P}$ is by definition equal to 10dBm, regardless of actual R_L.

TYPICAL PERFORMANCE CHARACTERISTICS

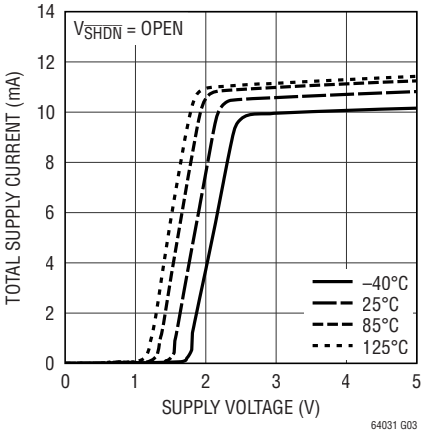
Differential Offset Voltage vs Temperature



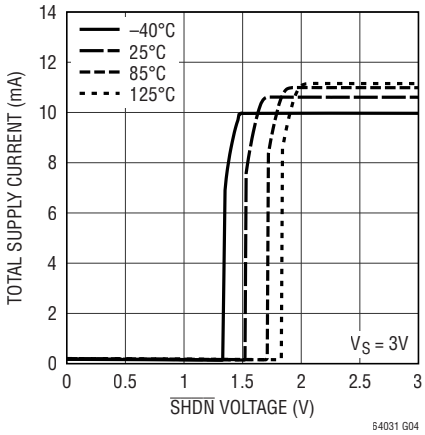
Common Mode Offset Voltage vs Temperature



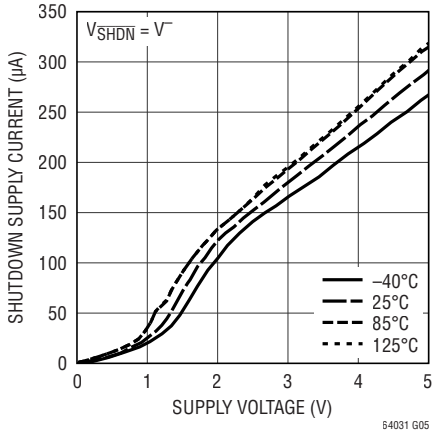
Supply Current vs Supply Voltage



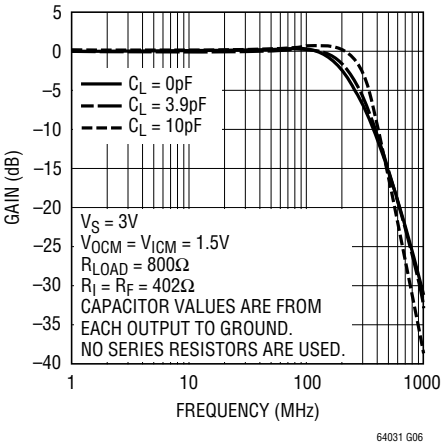
Supply Current vs $\overline{SHDN}$ Voltage



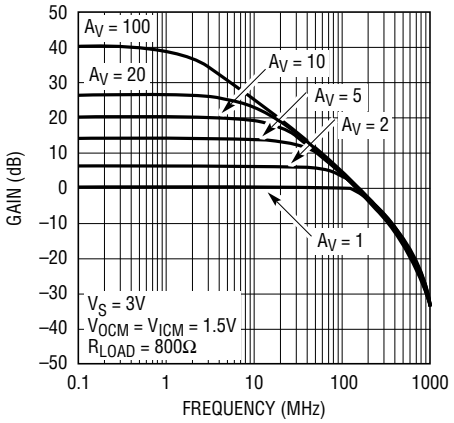
Shutdown Supply Current vs Supply Voltage



Frequency Response vs Load Capacitance



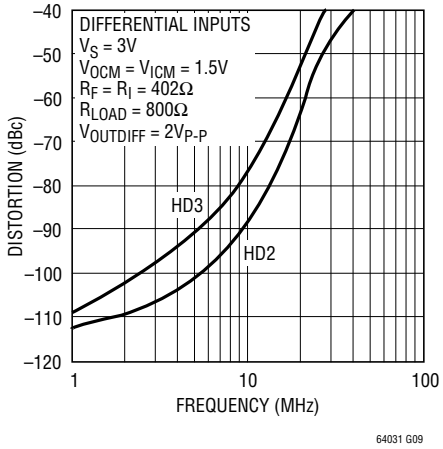
Frequency Response vs Gain



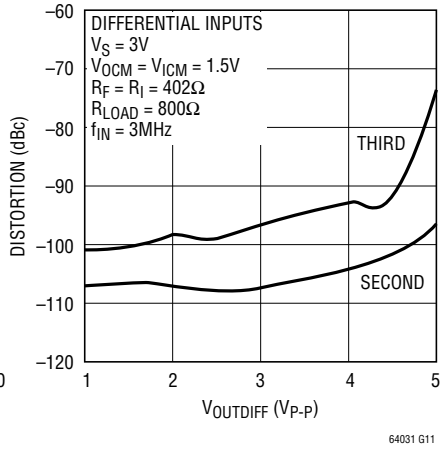
A_V (V/V)	R_I(Ω)	R_F(Ω)
1	402	402
2	402	806
5	402	2k
10	402	4.02k
20	402	8.06k
100	402	40.2k

TYPICAL PERFORMANCE CHARACTERISTICS

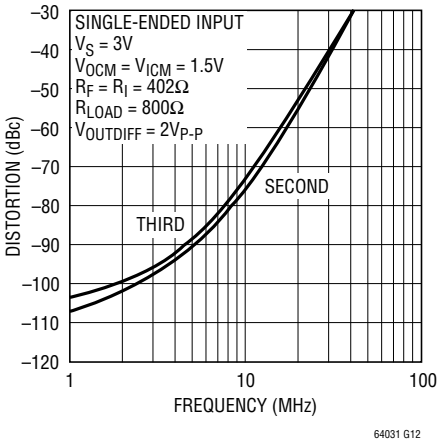
Harmonic Distortion vs Frequency



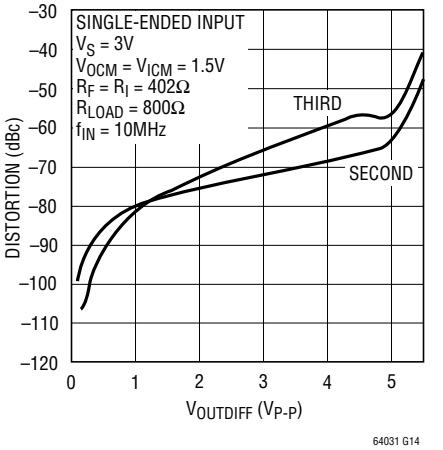
Harmonic Distortion vs Output Amplitude



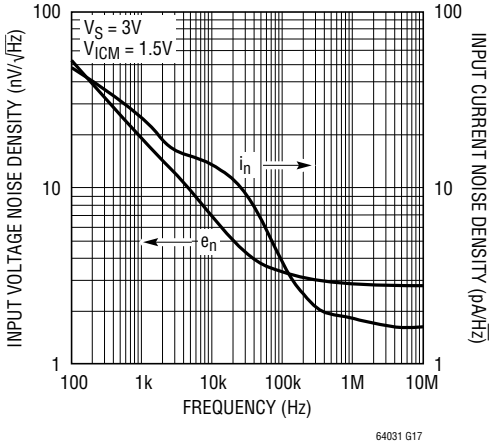
Harmonic Distortion vs Frequency



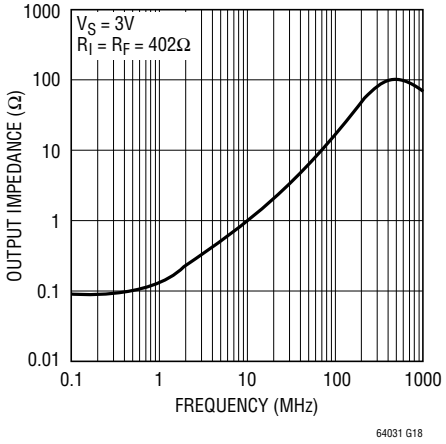
Harmonic Distortion vs Output Amplitude



Input Noise Density vs Frequency

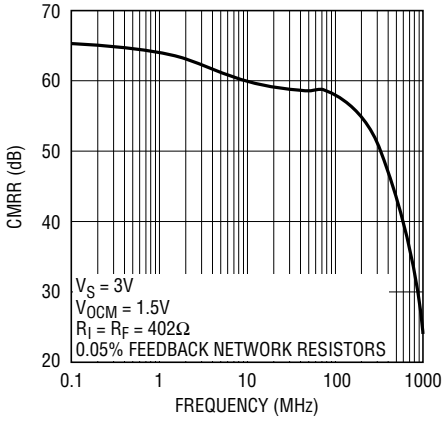


Differential Output Impedance vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

CMRR vs Frequency



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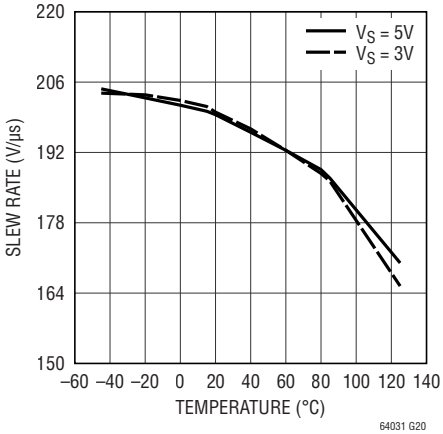
Differential Slew Rate vs Temperature



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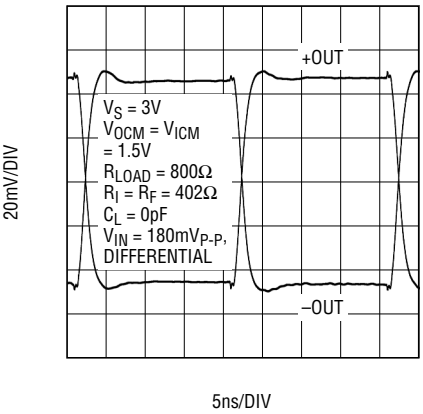
Small Signal Step Response



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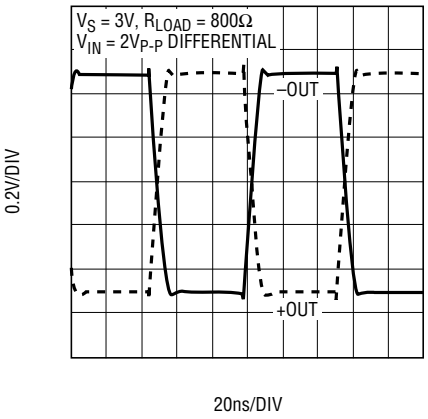
Large Signal Step Response



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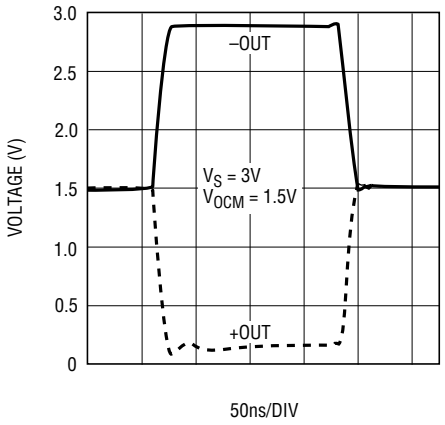
Overdrive Transient Response



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PIN FUNCTIONS

$\overline{\text{SHDN}}$ (Pin 1): When $\overline{\text{SHDN}}$ is floating or directly tied to V^+, the LTC6403-1 is in the normal (active) operating mode. When Pin 1 is pulled a minimum of 2.1V below V^+, the LTC6403-1 enters into a low power shutdown state. See Applications Information for more details.

V^+, V^- (Pins 2, 10, 11 and Pins 3, 9, 12): Power Supply Pins. Three pairs of power supply pins are provided to keep the power supply inductance as low as possible to prevent any degradation of amplifier 2nd harmonic performance. It is critical that close attention be paid to supply bypassing. For single supply applications (Pins 3, 9 and 12 grounded) it is recommended that high quality 0.1µF surface mount ceramic bypass capacitors be placed between Pins 2 and 3, between Pins 11 and 12, and between Pins 10 and 9 with direct short connections. Pins 3, 9 and 10 should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that at least two additional high quality, 0.1µF ceramic capacitors are used to bypass pin V^+ to ground and V^- to ground, again with minimal routing. For driving large loads (<200Ω), additional bypass capacitance may be needed for optimal performance. Keep in mind that small geometry (e.g. 0603) surface mount ceramic capacitors have a much higher self resonant frequency than do leaded capacitors, and perform best in high speed applications.

V_{OCM} (Pin 4): Output Common Mode Reference Voltage. The voltage on V_{OCM} sets the output common mode voltage level (which is defined as the average of the voltages on the +OUT and –OUT pins). The V_{OCM} pin is the midpoint of an internal resistive voltage divider between V^+ and V^- that develops a (default) mid-supply voltage potential to maximize output signal swing. The V_{OCM} pin can be overdriven by an external voltage reference capable of driving the input impedance presented by the V_{OCM} pin. On the LTC6403-1, the V_{OCM} pin has an input resistance of approximately 23k to a mid-supply potential. The V_{OCM} pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.01µF, (unless you are using split supplies, then connect directly to a low impedance, low noise ground plane) to minimize common mode noise from being converted to differential noise by impedance mismatches both external and internal to the IC.

NC (Pins 5, 16): No Connection. These pins are not connected internally.

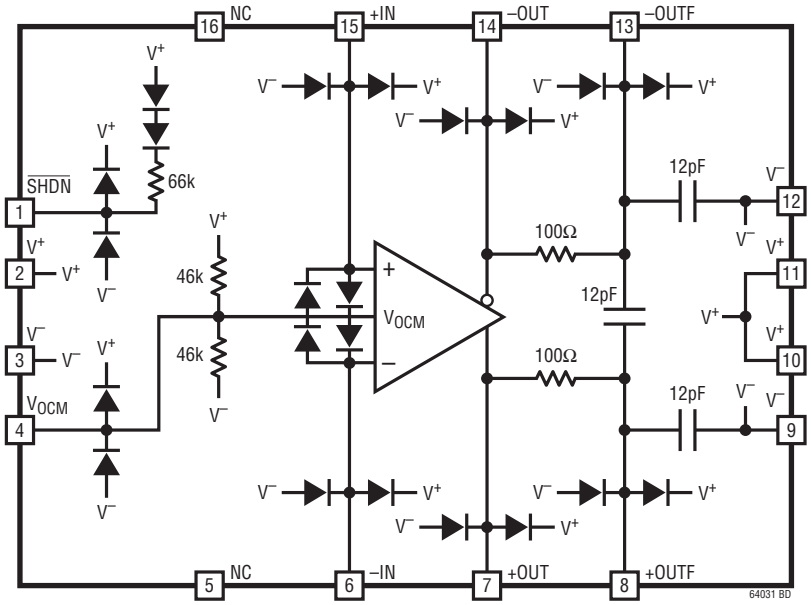
+OUT, –OUT (Pins 7, 14): Unfiltered Output Pins. Each amplifier output is designed to drive a load capacitance of 10pF. This means the amplifier can drive 10pF from each output to ground or 5pF differentially. Larger capacitive loads should be decoupled with at least 25Ω resistors from each output.

+OUTF, –OUTF (Pins 8, 13): Filtered Output Pins. These pins have a series 100Ω resistor connected between the filtered and unfiltered outputs and three 12pF capacitors. Both +OUTF and –OUTF have 12pF to V^-, plus an additional 12pF differentially between +OUTF and –OUTF. This filter creates a differential lowpass pole with a –3dB bandwidth of 44.2MHz.

+IN, –IN (Pins 15, 6): Noninverting and Inverting Input pins of the amplifier, respectively. For best performance, it is highly recommended that stray capacitance be kept to an absolute minimum by keeping printed circuit connections as short as possible and stripping back nearby surrounding ground plane away from these pins.

Exposed Pad (Pin 17): Tie the pad to V^- (Pins 3, 9, and 12). If split supplies are used, do not tie the pad to ground.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

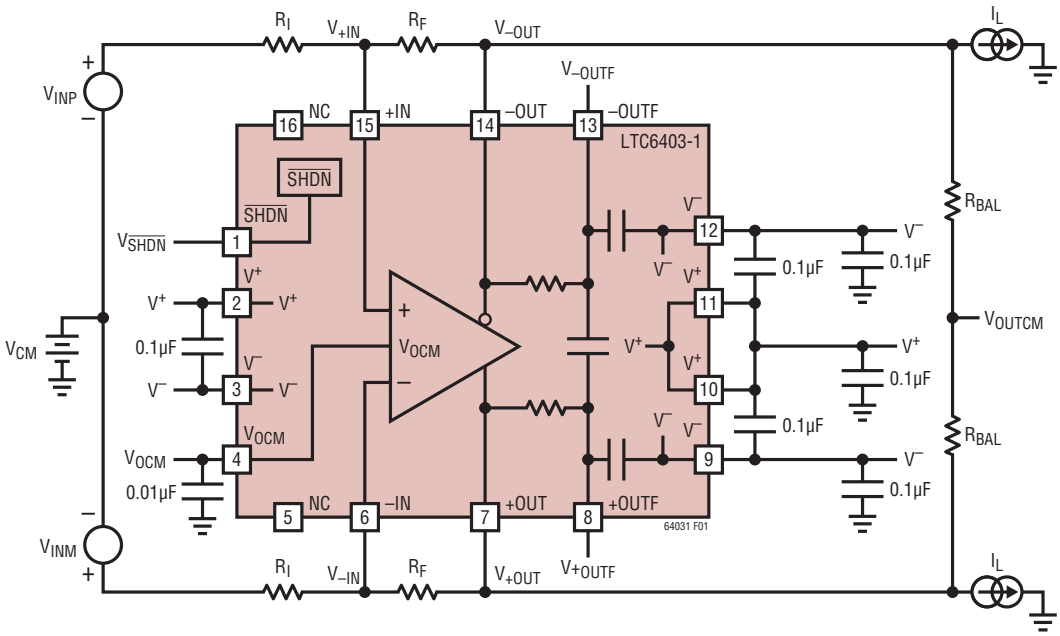


Figure 1. DC Test Circuit

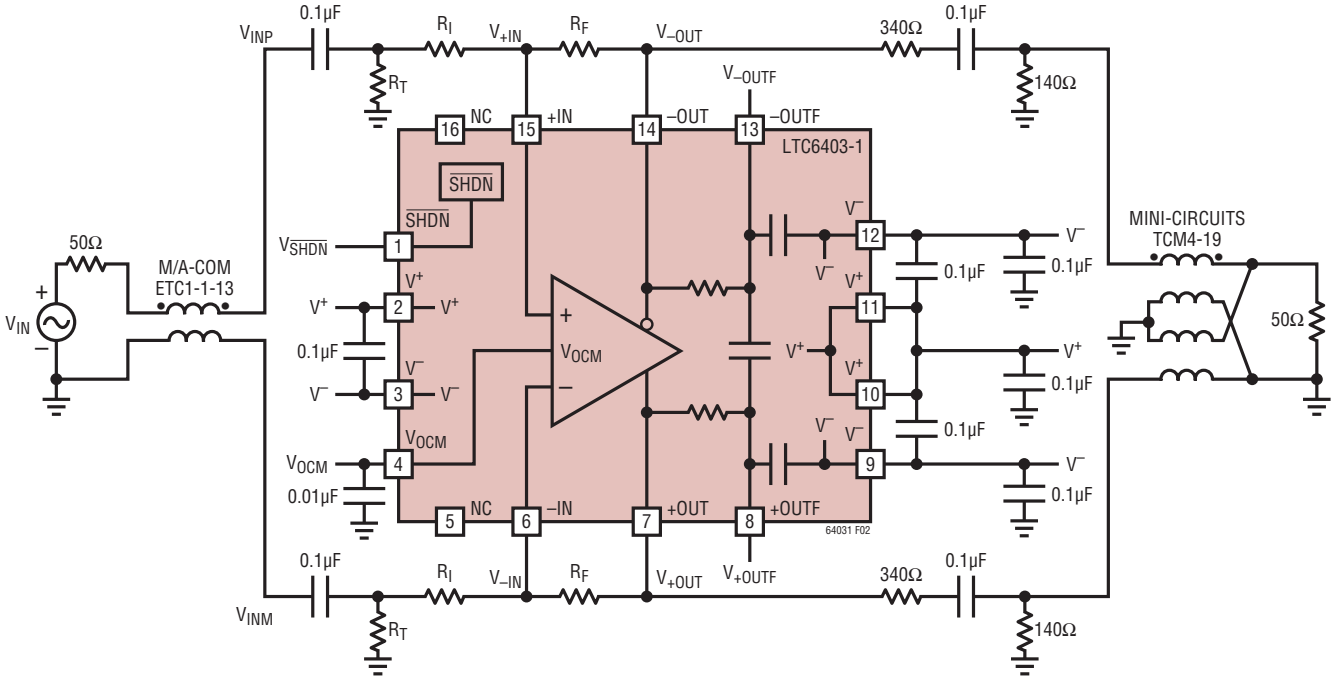


Figure 2. AC Test Circuit (–3dB BW Testing)

APPLICATIONS INFORMATION

Functional Description

The LTC6403-1 is a small outline, wide band, low noise, and low distortion fully-differential amplifier with accurate output phase balancing. The LTC6403-1 is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LTC6403-1's output is capable of swinging rail-to-rail on supplies as low as 2.7V, which makes the amplifier ideal for converting ground referenced, single-ended signals into V_{OCM} referenced differential signals in preparation for driving low voltage, single-supply, differential input ADCs. Unlike traditional op amps which have a single output, the LTC6403-1 has two outputs to process signals differentially. This allows for two times the signal swing in low voltage systems when compared to single-ended output amplifiers. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and less susceptibility to common mode noise (like power supply noise). The LTC6403-1 can be used as a single ended input to differential output amplifier, or as a differential input to differential output amplifier.

The LTC6403-1's output common mode voltage, defined as the average of the two output voltages, is independent of the input common mode voltage, and is adjusted by applying a voltage on the V_{OCM} pin. If the pin is left open, an internal resistive voltage divider develops a potential halfway between the V^+ and V^- pin voltages. Whenever V_{OCM} is not hard tied to a low impedance ground plane, it is recommended that a high quality ceramic capacitor is used to bypass the V_{OCM} pin to a low impedance ground plane (See Layout Considerations in this document). The LTC6403-1's internal common mode feedback path forces accurate output phase balancing to reduce even order harmonics, and centers each individual output about the potential set by the V_{OCM} pin.

$$V_{OUTCM} = V_{OCM} = \frac{V_{+OUT} + V_{-OUT}}{2}$$

The outputs (+OUT and –OUT) of the LTC6403-1 are capable of swinging rail-to-rail. They can source or sink up to approximately 60mA of current.

Additional outputs (+OUTF and –OUTF) are available that provide filtered versions of the +OUT and –OUT outputs. An on-chip single pole RC passive filter bandlimits the filtered outputs to a –3dB frequency of 44.2MHz. The user has a choice of using the unfiltered outputs, the filtered outputs, or modifying the filtered outputs to adjust the frequency response by adding additional components (see Output Filter Considerations and Use section).

In applications where the full bandwidth of the LTC6403-1 is desired, the unfiltered outputs (+OUT and –OUT) should be used. The unfiltered outputs +OUT and –OUT are designed to drive 10pF to ground (or 5pF differentially). Capacitances greater than 10pF will produce excess peaking, which can be mitigated by placing at least 25Ω in series with the output.

Input Pin Protection

The LTC6403-1's input stage is protected against differential input voltages that exceed 1.4V by two pairs of back to back diodes connected in anti-parallel series between +IN and –IN (Pins 6 and 15). In addition, the input pins have steering diodes to either power supply. If the input pair is over-driven, the current should be limited to under 10mA to prevent damage to the IC. The LTC6403-1 also has steering diodes to either power supply on the V_{OCM}, and $\overline{SHDN}$ pins (Pins 4 and 1), and if exposed to voltages which exceed either supply, they too, should be current limited to under 10mA.

$\overline{SHDN}$ Pin

If the $\overline{SHDN}$ pin (Pin 1), is pulled 2.1V below the positive supply, the LTC6403-1 will power down. The pin has the Thevenin equivalent impedance of approximately 66k to V^+. If the pin is left unconnected, an internal pull-up resistor of 150k will keep the part in normal active operation. Care should be taken to control leakage currents at this pin to under 1µA to prevent inadvertently putting the LTC6403-1 into shutdown. In shutdown, all biasing current sources are shut off, and the output pins, +OUT and –OUT, will each appear as an open collector with a non-linear capacitor in parallel and steering diodes to either supply. Because of the non-linear capacitance, the outputs still have the ability

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to sink and source small amounts of transient current if exposed to significant voltage transients. The inputs (+IN and –IN) appear as anti-parallel diodes which can conduct if voltage transients at the input exceed 1.4V. The inputs also have steering diodes to either supply. The turn-on time between the shutdown and active states is typically 4µs, and turn-off time is typically 350ns.

General Amplifier Applications

As levels of integration have increased and correspondingly, system supply voltages decreased, there has been a need for ADCs to process signals differentially in order to maintain good signal to noise ratios. These ADCs are typically operated from a single supply voltage which can be as low as 3V (2.7V min), and will have an optimal common mode input range near mid-supply. The LTC6403-1 makes interfacing to these ADCs trivial, by providing both single ended to differential conversion as well as common mode level shifting. The front page of this datasheet shows a typical application. Referring to Figure 1, the gain to $V_{OUTDIFF}$ from V_{INM} and V_{INP} is:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \frac{R_F}{R_I} \bullet (V_{INP} - V_{INM})$$

Note from the above equation, the differential output voltage (V_{+OUT} – $V_{–OUT}$) is completely independent of input and output common mode voltages. This makes the LTC6403-1 ideally suited for pre-amplification, level shifting and conversion of single-ended input signals to differential output signals in preparation for driving differential input ADCs.

Effects of Resistor Pair Mismatch

Figure 3 shows a circuit diagram with takes into consideration that real world resistors will not perfectly match. Assuming infinite open loop gain, the differential output relationship is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \frac{R_F}{R_I} \bullet V_{INDIFF} + \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{INCM} - \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{OCM}$$

where:

R_F is the average of R_{F1}, and R_{F2}, and R_I is the average of R_{I1}, and R_{I2}.

β_{AVG} is defined as the average feedback factor (or gain) from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I1}}{R_{I1}+R_{F1}} + \frac{R_{I2}}{R_{I2}+R_{F2}} \right)$$

$\Delta\beta$ is defined as the difference in feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2}+R_{F2}} - \frac{R_{I1}}{R_{I1}+R_{F1}}$$

V_{INCM} is defined as the average of the two input voltages V_{INP}, and V_{INM} (also called the source-referred input common mode voltage):

$$V_{INCM} = \frac{1}{2} \bullet (V_{INP} + V_{INM})$$

and V_{INDIFF} is defined as the difference of the input voltages:

$$V_{INDIFF} = V_{INP} - V_{INM}$$

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs.

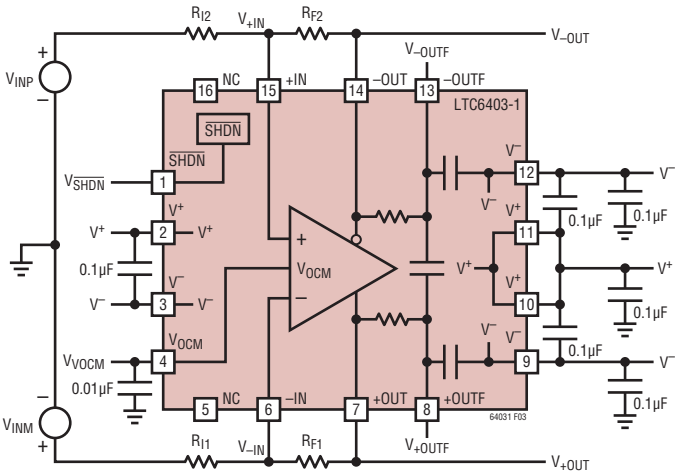

Figure 3. Real World Application With Feedback Resistor Pair Mismatch

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Setting the differential input to zero (V_{INDIFF} = 0), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx (V_{INCM} - V_{OCM}) \bullet \frac{\Delta\beta}{\beta_{AVG}}$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 1% resistors or better will mitigate most problems, and will provide about 34dB worst case of common mode rejection. Using 0.1% resistors will provide about 54dB of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin. Directly shorting V_{OCM} to this ground or bypassing the V_{OCM} with a high quality 0.1µF ceramic capacitor to this ground plane will further mitigate against common mode signals being converted to differential.

There may be concern on how feedback ratio mismatch affects distortion. Distortion caused by feedback ratio mismatch using 1% resistors or better is negligible. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage, resistor mismatch can make the apparent voltage offset of the amplifier appear worse than specified.

The apparent input referred offset induced by feedback ratio mismatch is derived from the above equation:

$$V_{OSDIFF(APPARENT)} \approx (V_{INCM} - V_{OCM}) \bullet \Delta\beta$$

Using the LTC6403-1 in a single supply application on a single 5V supply with 1% resistors, and the input common mode grounded, with the V_{OCM} pin biased at mid-supply, the worst case mismatch can induce 25mV of apparent offset voltage. With 0.1% resistors, the worst case apparent offset reduces to 2.5mV.

Input Impedance and Loading Effects

The input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on whether the sources V_{INP} and V_{INM} are fully differential. For balanced input sources (V_{INP} = $-V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single ended inputs, because of the signal imbalance at the input, the input impedance increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left(\frac{R_F}{R_I + R_F}\right)\right)}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the source's output impedance be compensated. If input impedance matching is required by the source, R1 should be chosen (see Figure 4):

$$R_1 = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

According to Figure 4, the input impedance looking into the differential amp (R_{INM}) reflects the single ended source case, thus:

$$R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left(\frac{R_F}{R_I + R_F}\right)\right)}$$

R2 is chosen to balance R1 || RS:

$$R_2 = \frac{R_I \bullet R_S}{R_I + R_S}$$

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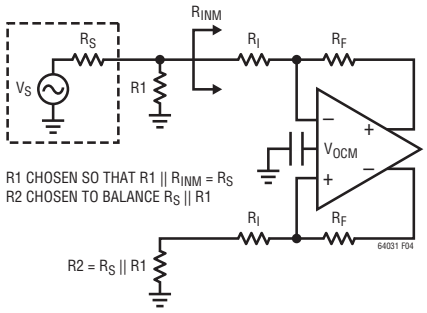

Figure 4. Optimal Compensation for Signal Source Impedance

Input Common Mode Voltage Range

The LTC6403-1's input common mode voltage (V_{ICM}) is defined as the average of the two input voltages, V_{+IN}, and $V_{–IN}$. It extends from $V^–$ to 1.4V below V^+.

For fully differential input applications, where $V_{INP} = –V_{INM}$, the input common mode voltage is approximately (Refer to Figure 5):

$$V_{ICM} = \frac{V_{+IN} + V_{–IN}}{2} \approx V_{VOCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

With singled ended inputs, there is an input signal component to the input common mode voltage. Applying only

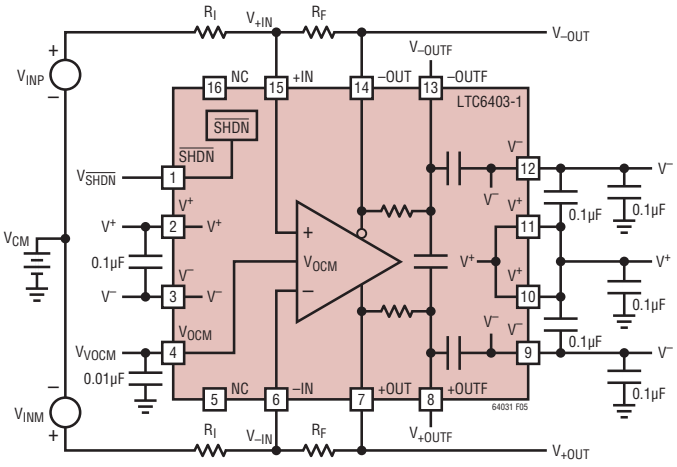

Figure 5. Circuit for Common Mode Range

V_{INP} (setting V_{INM} to zero), the input common voltage is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{–IN}}{2} \approx V_{VOCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right) + \frac{V_{INP}}{2} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

Output Common Mode Voltage Range

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{VOCM} = \frac{V_{+OUT} + V_{–OUT}}{2}$$

The V_{OCM} pin sets this average by an internal common mode feedback loop. The output common mode range extends from 1.1V above $V^–$ to 1V below V^+. The V_{OCM} pin sits in the middle of an internal voltage divider which sets the default mid-supply open circuit potential.

In single supply applications, where the LTC6403-1 is used to interface to an ADC, the optimal common mode input range to the ADC is often determined by the ADC's reference. If the ADC makes a reference available for setting the input common mode voltage, it can be directly tied to the V_{OCM} pin, but must be capable of driving the input impedance presented by the V_{OCM} as listed in the Electrical Characteristics Table. This impedance can be assumed to be connected to a mid-supply potential. If an external reference drives the V_{OCM} pin, it should still be bypassed with a high quality 0.01µF or higher capacitor to a low impedance ground plane to filter any thermal noise and to prevent common mode signals on this pin from being inadvertently converted to differential signals.

Output Filter Considerations and Use

Filtering at the output of the LTC6403-1 is often desired to provide either anti-aliasing or improved signal to noise ratio. To simplify this filtering, the LTC6403-1 includes an additional pair of differential outputs (+OUTF and –OUTF) which incorporate an internal lowpass filter network with a –3dB bandwidth of 44.2MHz (Figure 6).

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These pins each have an output impedance of 100Ω. Internal capacitances are 12pF to V⁻ on each filtered output, plus an additional 12pF capacitor connected differentially between the two filtered outputs. This resistor/capacitor combination creates filtered outputs that look like a series 100Ω resistor with a 36pF capacitor shunting each filtered output to AC ground, providing a –3dB bandwidth of 44.2MHz, and a noise bandwidth of 69.4MHz. The filter cutoff frequency is easily modified with just a few external components. To increase the cutoff frequency, simply add 2 equal value resistors, one between +OUT and +OUTF and the other between –OUT and –OUTF (Figure 7). These resistors, in parallel with the internal 100Ω resistors, lower the overall resistance and therefore increase filter bandwidth. For example, to double the filter bandwidth, add two external 100Ω resistors to lower the series filter resistance to 50Ω. The 36pF of capacitance remains unchanged, so filter bandwidth doubles. Keep in mind, the series resistance also serves to decouple the outputs from load capacitance. The unfiltered outputs of the LTC6403-1 are designed to drive 10pF to ground or 5pF differentially, so care should be taken to not lower the effective impedance between +OUT and +OUTF or –OUT and –OUTF below 25Ω.

To decrease filter bandwidth, add two external capacitors, one from +OUTF to ground, and the other from –OUTF to ground. A single differential capacitor connected between +OUTF and –OUTF can also be used, and since it is being driven differentially it will appear at each filtered output as a single-ended capacitance of twice the value. To halve the filter bandwidth, for example, two 36pF capacitors could be added (one from each filtered output to ground). Alternatively, one 18pF capacitor could be added between the filtered outputs, again halving the filter bandwidth. Combinations of capacitors could be used as well; a three capacitor solution of 12pF from each filtered output to ground plus a 12pF capacitor between the filtered outputs would also halve the filter bandwidth (Figure 8).

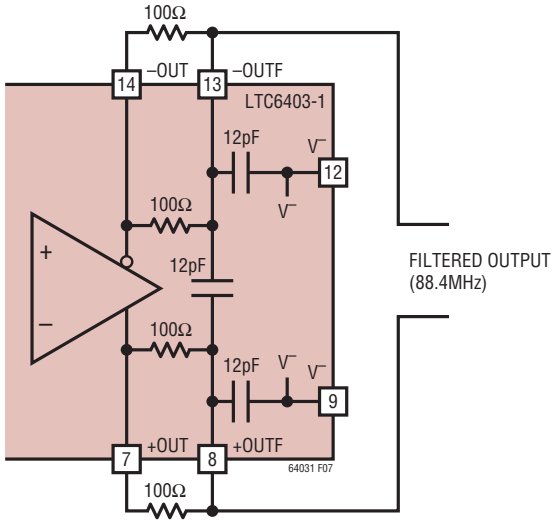

Figure 7. LTC6403-1 Filter Topology Modified for 2x Filter Bandwidth (2 External Resistors)

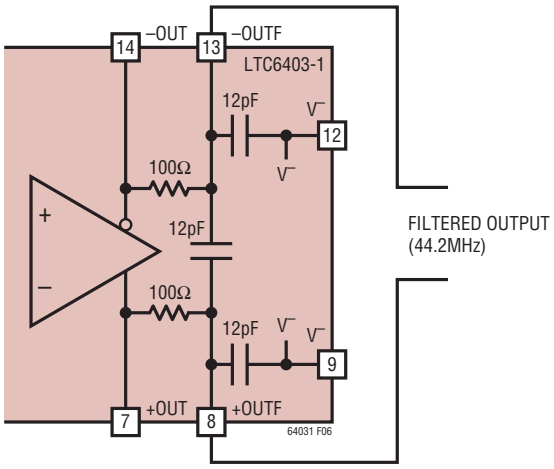

Figure 6. LTC6403-1 Internal Filter Topology

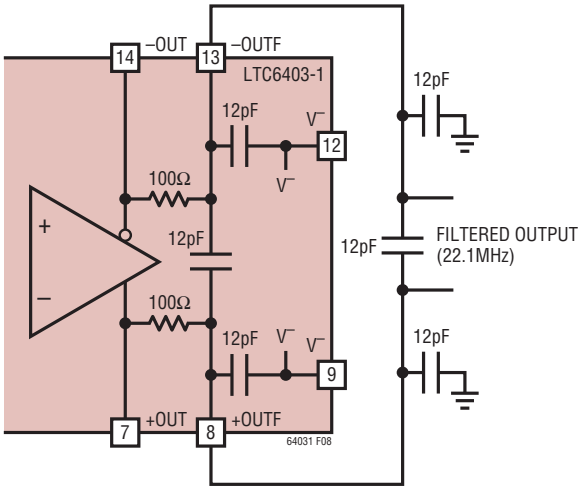

Figure 8. LTC6403-1 Filter Topology Modified for 1/2x Filter Bandwidth (3 External Capacitors)

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Noise Considerations

The LTC6403-1's input referred voltage noise is on the order of 2.8nV/$\sqrt{Hz}$. Its input referred current noise is on the order of 1.8pA/$\sqrt{Hz}$. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A noise model is shown in Figure 9. The output noise generated by both the amplifier and the feedback components is governed by the equation:

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet (I_n \bullet R_F)^2 + 2 \bullet \left(e_{nRI} \bullet \left(\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet e_{nRF}{}^2}$$

A plot of this equation, and a plot of the noise generated by the feedback components for the LTC6403-1 is shown in Figure 10.

The LTC6403-1's input referred voltage noise contributes the equivalent noise of a 480Ω resistor. When the feedback network is comprised of resistors whose values are less than this, the LTC6403-1's output noise is voltage noise dominant (See Figure 10.):

$$e_{no} \approx e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)$$

Feedback networks consisting of resistors with values greater than about 1k will result in output noise which is resistor noise and amplifier current noise dominant.

$$e_{no} \approx \sqrt{2} \bullet \sqrt{(I_n \bullet R_F)^2 + \left(1+\frac{R_F}{R_I}\right) \bullet 4 \bullet k \bullet T \bullet R_F}$$

Lower resistor values (<400Ω) always result in lower noise at the penalty of increased distortion due to increased loading of the feedback network on the output. Higher

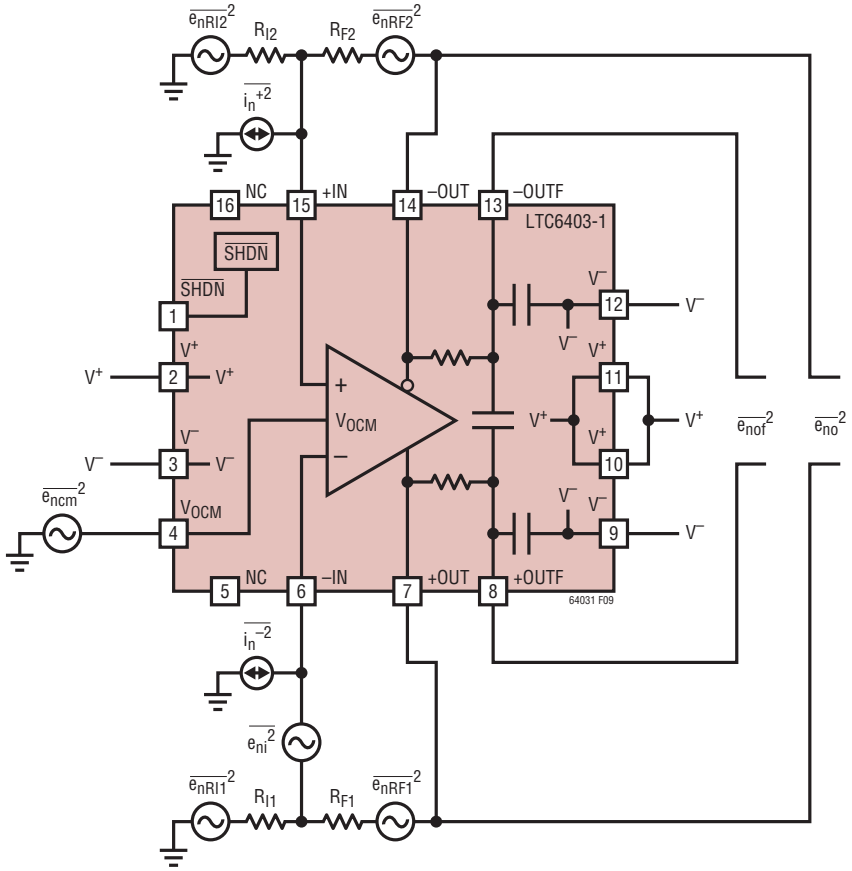


Figure 9. Noise Model of the LTC6403-1

APPLICATIONS INFORMATION

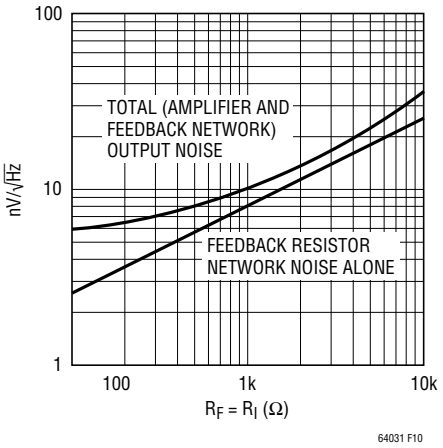


Figure 10. LTC6403-1 Output Spot Noise vs Spot Noise Contributed by Feedback Network Alone

resistor values (but still less than 2k) will result in higher output noise, but improved distortion due to less loading on the output. The optimal feedback resistance for the LTC6403-1 runs between 400Ω to 2k.

The differential filtered outputs +OUTF and –OUTF will have a little higher spot noise than the unfiltered outputs (due to the two 100Ω resistors which contribute 1.3nV/√Hz each), but actually will provide superior signal-to-noise ratios in noise bandwidths exceeding 69.4Mhz due to the noise-filtering function the filter provides.

Layout Considerations

Because the LTC6403-1 is a very high speed amplifier, it is sensitive to both stray capacitance and stray inductance. Three pairs of power supply pins are provided to keep the power supply inductance as low as possible to prevent any degradation of amplifier 2nd Harmonic distortion performance. It is critical that close attention be paid to supply bypassing. For single supply applications (Pins 3, 9 and 12 grounded) it is recommended that 3 high quality 0.1µF surface mount ceramic bypass capacitor be placed between pins 2 and 3, between pins 11and 12, and between pins10 and 9 with direct short connections. Pins 3, 9 and 10 should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that at least two additional high quality, 0.1µF ceramic capacitors are used to bypass pin V^+ to ground and $V^–$ to ground, again with minimal routing. For driving large loads (<200Ω), additional bypass capacitance may be needed for optimal performance. Keep in mind that small geometry (e.g. 0603) surface mount ceramic capacitors have a much higher self resonant frequency than do leaded capacitors, and perform best in high speed applications.

Any stray parasitic capacitances to ground at the summing junctions +IN, and –IN should be kept to an absolute minimum even if it means stripping back the ground plane away from any trace attached to this node. This becomes especially true when the feedback resistor network uses resistor values >2k in circuits with $R_F = R_I$. Excessive peaking in the frequency response can be mitigated by adding small amounts of feedback capacitance around R_F. Always keep in mind the differential nature of the LTC6403-1, and that it is critical that the load impedances seen by both outputs (stray or intended) should be as balanced and symmetric as possible. This will help preserve the natural balance of the LTC6403-1, which minimizes the generation of even order harmonics, and preserves the rejection of common mode signals and noise.

It is highly recommended that the V_{OCM} pin be either hard tied to a low impedance ground plane (in split supply applications), or bypassed to ground with a high quality ceramic capacitor whose value exceeds 0.01µF. This will help stabilize the common mode feedback loop as well as prevent thermal noise from the internal voltage divider and other external sources of noise from being converted to differential noise due to divider mismatches in the feedback networks. It is also recommended that the resistive feedback networks comprise 1% resistors (or better) to enhance the output common mode rejection. This will also prevent the V_{OCM}-referred common mode noise of the common mode amplifier path (which cannot be filtered) from being converted to differential noise, degrading the differential noise performance.

APPLICATIONS INFORMATION

Interfacing the LTC6403-1 to A/D Converters

The LTC6403-1's rail-to-rail output and fast settling time make the LTC6403-1 ideal for interfacing to low voltage, single supply, differential input ADCs. The sampling process of ADCs creates a sampling glitch caused by switching in the sampling capacitor on the ADC front end which momentarily shorts the output of the amplifier as charge is transferred between the amplifier and the sampling capacitor. The amplifier must recover and settle from this load transient before this acquisition period ends for a valid representation of the input signal. In general, the LTC6403-1 will settle much more quickly from these periodic load impulses than from a 2V input step, but it is a good idea to either use the filtered outputs to drive the ADC (Figure 11 shows an example of this), or to place a discrete R-C filter network between the differential unfiltered outputs of the LTC6403-1 and the input of the ADC to help absorb the charge injection that comes out of the ADC from the sampling process. The capacitance of the filter network serves as a charge reservoir to provide high frequency charging during the sampling process, while the two resistors of the filter network are used to dampen and attenuate any charge kickback from the ADC. The selection of the R-C time constant is trial and error for a given ADC, but the following guidelines are recommended: Choosing too large of a resistor in the decoupling network will create a voltage divider between the dynamic input impedance of the ADC and the decoupling resistors leaving insufficient settling time. Choosing too small of a resistor will possibly prevent the resistor from properly dampening the load transient caused by the sampling process, prolonging the time required for settling. 16-bit applications require a minimum of 11 R-C time constants to settle. It is recommended that the capacitor chosen have a high quality dielectric (for example, C0G multilayer ceramic).

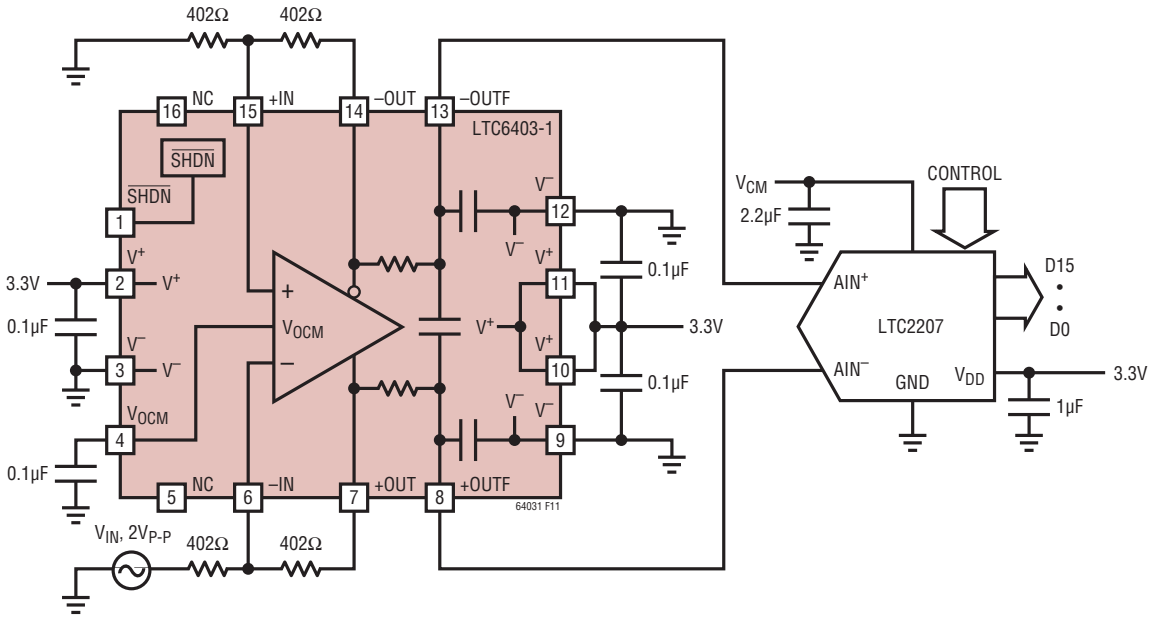
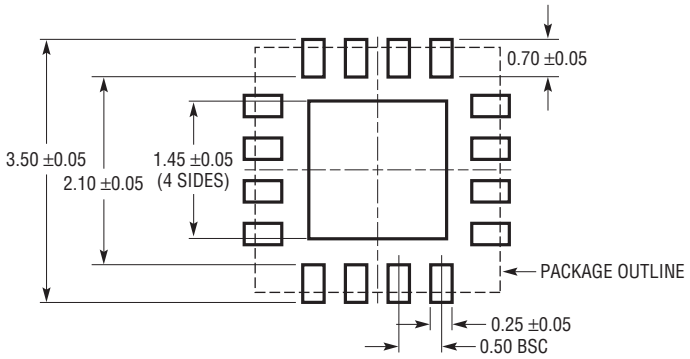


Figure 11. Interfacing the LTC6403-1 to ADC (Shared 3.3V Supply Voltage)

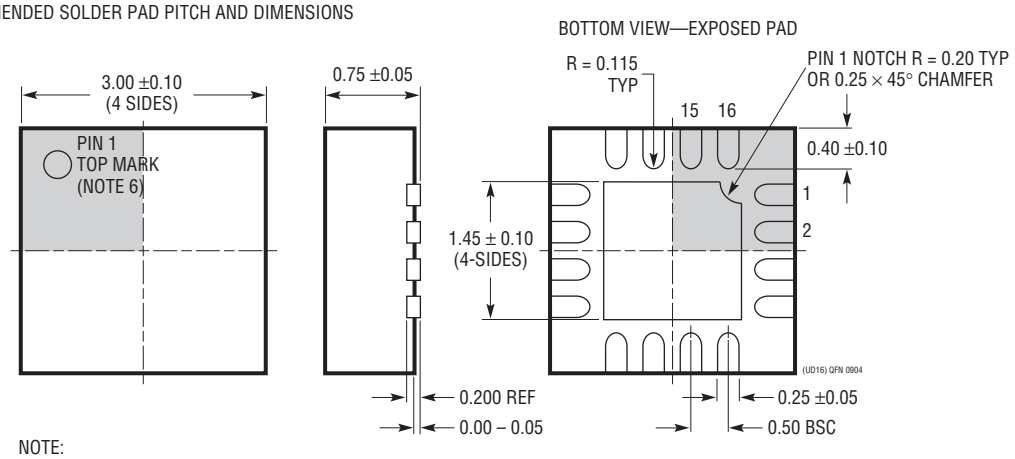
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6403-1#packaging for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	06/17	Added a –40°C to 125°C H-grade version and its performance characteristics.	2 - 8