# 800MHz, 31dB Range Analog-Controlled VGA

## FEATURES

- **800MHz –3dB Small-Signal Bandwidth**
- **Continuously-Adjustable Gain Control**
- **–14dB to +17dB Linear-in-dB Gain Range**
- **35dBm OIP3 at 240MHz Across All Gain Settings**
- **10dB Noise Figure at Maximum Gain**
- **(IIP3 – NF) = +8dBm at 240MHz Across All Gains**
- 2.7nV/√Hz Input Referred Noise
- Differential Inputs and Outputs
- 50Ω Input Impedance Across all Gains
- Single Supply Operation from 3V to 3.6V
- 110mA Supply Current
- 4mm × 4mm × 0.75mm 24-Pin QFN Package

## APPLICATIONS

- IF Signal Chain Automatic Gain Control (AGC)
- 2.5G and 3G Cellular Basestation Transceivers
- WiMAX, WiBro, WLAN Receivers
- Satellite and GPS Receiver IF

## DESCRIPTION

The LTC®6412 is a fully differential variable gain amplifier with linear-in-dB analog gain control. It is designed for AC-coupled operation in IF receiver chains from 1MHz to 500MHz. The part has a constant OIP3 across a wide output amplitude range and across the 31dB gain control range. The output noise (NF + Gain) is also flat versus gain to provide a uniform spurious-free dynamic range (SFDR) >120dB over the full gain control range at 240MHz.

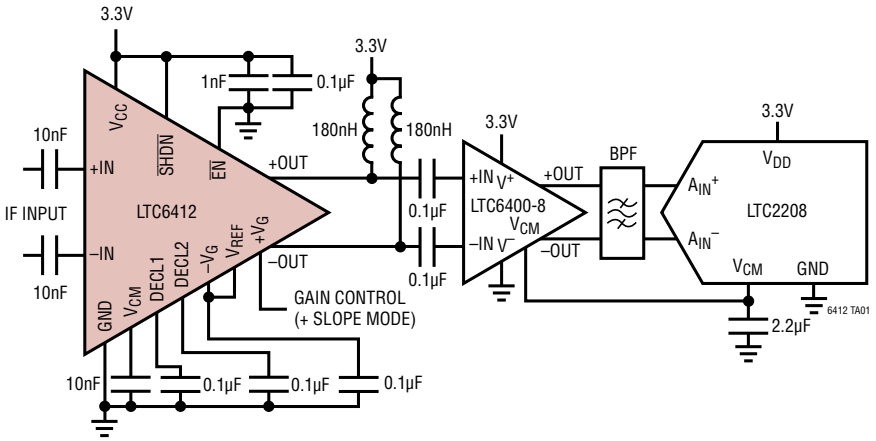
The LTC6412 is ideal for interfacing with the LT®5527 and LT5557 downconverting mixers, LTC6410-6 IF amplifier and the LTC6400/LTC6401/LTC6416 ADC drivers for use in 12-, 14-, and 16-bit ADC applications.

The LTC6412 recovers quickly from an overdrive condition, and the $\overline{EN}$ pin allows for a fast output signal disable to protect sensitive downstream components. Asserting the $\overline{SHDN}$ pin reduces the current consumption below 1mA for power-down or sleep modes.

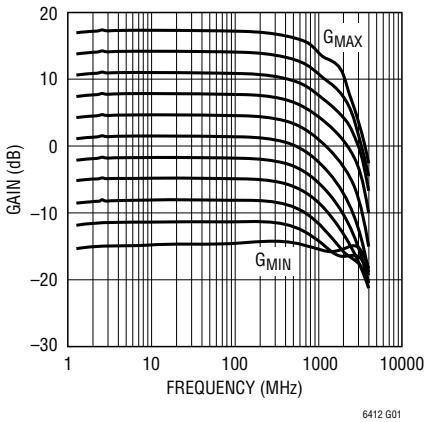


## TYPICAL APPLICATION

**3.3V Fully Differential 240MHz IF Receiver Chain with 31dB Gain Control**




**VGA Gain vs Frequency Over Gain Control Range**

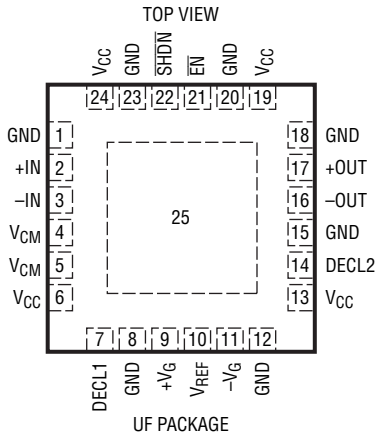


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Total Supply Voltage ($V_{CC}$ to GND).....3.8V
Amplifier Input Current (+IN, –IN).....±20mA
Amplifier Output Current (+OUT, –OUT).....±70mA
Input Current (+$V_G$, –$V_G$, $V_{REF}$, $\overline{EN}$, $\overline{SHDN}$ ).....±10mA
Input Current ($V_{CM}$, DECL1, DECL2).....±10mA
RF Input Power, Continuous, 50Ω.....+15dBm
RF Input Power, 100µs pulse, 50Ω .....+20dBm
Operating Temperature Range (Note 2).... –40°C to 85°C
Specified Temperature Range (Note 3) .... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C
Junction Temperature ..... 150°C

## PIN CONFIGURATION




UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6412CUF#PBF | LTC6412CUF#TRPBF | 6412 | 24-Lead (4mm × 4mm) Plastic QFN | 0°C to 70°C |
| LTC6412IUF#PBF | LTC6412IUF#TRPBF | 6412 | 24-Lead (4mm × 4mm) Plastic QFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## DC ELECTRICAL CHARACTERISTICS

**The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. DC electrical performance measured using DC test circuit schematic. $V_{IN(DIFF)}$ is defined as (+IN) – (–IN). $V_{OUT(DIFF)}$ is defined as (+OUT) – (–OUT). $V_{IN(CM)}$ is defined as [(+IN) + (–IN)]/2. $V_{OUT(CM)}$ is defined as [(+OUT) + (–OUT)]/2. Unless noted otherwise, default operating conditions are $V_{CC}$ = 3.3V, $\overline{EN}$ = 0.8V, $\overline{SHDN}$ = 2.2V, $+V_G$ tied to $V_{REF}$ (negative gain slope mode), $V_{OUT(CM)}$ = 3.3V. Differential power gain defined at $Z_{SOURCE}$ = 50Ω differential and $Z_{LOAD}$ = 200Ω differential.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Gain Characteristics** | | | | | | | |
| $G_{MAX}$ | Maximum Differential Power Gain (Note 4) | $-V_G$ = 0V, $V_{IN(DIFF)}$ = 100mV | <br>● | 16.1<br>15.5 | 17.1 | 18.1<br>18.7 | dB<br>dB |
| $G_{MIN}$ | Minimum Differential Power Gain (Note 4) | $-V_G$ = 1.2V, $V_{IN(DIFF)}$ = 200mV | <br>● | –16.2<br>–16.8 | –14.9 | –13.6<br>–13.0 | dB<br>dB |
| $G_{RANGE}$ | Differential Power Gain Range | $G_{MAX}$-$G_{MIN}$ | <br>● | 30.7<br>30.1 | 31.9 | 33.1<br>33.7 | dB<br>dB |
| $TC_{GAIN}$ | Temperature Coefficient of Gain at Fixed $V_G$ | $-V_G$ = 0V to 1.2V | | | –0.007 | | dB/°C |
| $G_{SLOPE}$ | Gain Control Slope | $-V_G$ = 0.2V to 1.0V, 85 Points, Slope of the Least-Square Fit Line | <br>● | –34.1<br>–34.7 | –32.9 | –31.7<br>–31.1 | dB/V<br>dB/V |
| $G_{CONF(AVE)}$ | Average Conformance Error to Gain Slope Line | $-V_G$ = 0.2V to 1.0V, 85 Points, Standard Error to the Least-Square Fit Line | | | 0.12 | 0.20 | dB |
| $G_{CONF(MAX)}$ | Maximum Conformance Error to Gain Slope Line | $-V_G$ = 0.2V to 1.0V, 85 points, Maximum Error to the Least-Square Fit Line | | | 0.20 | 0.45 | dB |
| **+IN and –IN Pins** | | | | | | | |
| $R_{IN(GMAX)}$ | Differential Input Resistance at Maximum Gain | $-V_G$ = 0V, $V_{IN(DIFF)}$ = 100mV | <br>● | 49<br>47 | 57 | 65<br>67 | Ω<br>Ω |
| $R_{IN(GMIN)}$ | Differential Input Resistance at Minimum Gain | $-V_G$ = 1.2V, $V_{IN(DIFF)}$ = 200mV | <br>● | 49<br>47 | 57 | 65<br>67 | Ω<br>Ω |
| $V_{INCM(GMAX)}$ | Input Common Mode Voltage at Maximum Gain | $-V_G$ = 0V, DC Blocking Capacitor to Input | | | 640 | | mV |
| $V_{INCM(GMIN)}$ | Input Common Mode Voltage at Minimum Gain | $-V_G$ = 1.2V, DC Blocking Capacitor to Input | | | 640 | | mV |
| **$+V_G$, $-V_G$, and $V_{REF}$ Pins** | | | | | | | |
| $R_{IH(+VG)}$ | $+V_G$ Input High Resistance | $+V_G$ = 1.0V, $-V_G$ Tied to $V_{REF}$, $R_{IN(+VG)}$ = 1V/Δ $I_{IL(+VG)}$ | <br>● | 7.8<br>7.2 | 9.2 | 10.6<br>11.6 | kΩ<br>kΩ |
| $R_{IH(-VG)}$ | $-V_G$ Input High Resistance | $-V_G$ = 1.0V, $+V_G$ Tied to $V_{REF}$, $R_{IN(-VG)}$ = 1V/Δ $I_{IL(-VG)}$ | <br>● | 7.8<br>7.2 | 9.2 | 10.6<br>11.6 | kΩ<br>kΩ |
| $I_{IL(+VG)}$ | $+V_G$ Input Low Current | $+V_G$ = 0V, $-V_G$ Tied to $V_{REF}$ | <br>● | –9<br>–10 | –5 | –1<br>–1 | µA<br>µA |
| $I_{IL(-VG)}$ | $-V_G$ Input Low Current | $-V_G$ = 0V, $+V_G$ Tied to $V_{REF}$ | <br>● | –9<br>–10 | –5 | –1<br>–1 | µA<br>µA |
| $V_{REF}$ | Internal Bias Voltage | $-V_G$ = 0V, $+V_G$ Tied to $V_{REF}$ | <br>● | 590<br>580 | 615 | 640<br>650 | mV<br>mV |

## DC ELECTRICAL CHARACTERISTICS

**The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. DC electrical performance measured using DC test circuit schematic. $V_{IN(DIFF)}$ is defined as (+IN) – (–IN). $V_{OUT(DIFF)}$ is defined as (+OUT) – (–OUT). $V_{IN(CM)}$ is defined as [(+IN) + (–IN)]/2. $V_{OUT(CM)}$ is defined as [(+OUT) + (–OUT)]/2. Unless noted otherwise, default operating conditions are $V_{CC}$ = 3.3V, $\overline{EN}$ = 0.8V, $\overline{SHDN}$ = 2.2V, $+V_G$ tied to $V_{REF}$ (negative gain slope mode), $V_{OUT(CM)}$ = 3.3V. Differential power gain defined at $Z_{SOURCE}$ = 50Ω differential and $Z_{LOAD}$ = 200Ω differential.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$\overline{SHDN}$ Pin** | | | | | | | |
| $V_{IL(\overline{SHDN})}$ | $\overline{SHDN}$ Input Low Voltage | | ● | | | 0.8 | V |
| $V_{IH(\overline{SHDN})}$ | $\overline{SHDN}$ Input High Voltage | | ● | 2.2 | | | V |
| $I_{IL(\overline{SHDN})}$ | $\overline{SHDN}$ Input Low Current | $\overline{SHDN}$ = 0.8V | ● | –60 | –30 | –1 | µA |
| $I_{IH(\overline{SHDN})}$ | $\overline{SHDN}$ Input High Current | $\overline{SHDN}$ = 2.2V | ● | –30 | –15 | –1 | µA |
| **$\overline{EN}$ Pin** | | | | | | | |
| $V_{IL(\overline{EN})}$ | $\overline{EN}$ Input Low Voltage | | ● | | | 0.8 | V |
| $V_{IH(\overline{EN})}$ | $\overline{EN}$ Input High Voltage | | ● | 2.2 | | | V |
| $I_{IL(\overline{EN})}$ | $\overline{EN}$ Input Low Current | $\overline{EN}$ = 0.8V | ● | –60 | –30 | –1 | µA |
| $I_{IH(\overline{EN})}$ | $\overline{EN}$ Input High Current | $\overline{EN}$ = 2.2V | ● | –30 | –15 | –1 | µA |
| **Power Supply** | | | | | | | |
| $V_S$ | Operating Supply Range | | ● | 3.0 | 3.3 | 3.6 | V |
| $I_{S(TOT)}$ | Total Supply Current | All $V_{CC}$ Pins Plus +OUT and –OUT Pins | <br>● | | 110 | 135<br>140 | mA<br>mA |
| $I_{S(OUT)}$ | Sum of Supply Current to OUT Pins | $I_{S(OUT)} = I_{+OUT} + I_{–OUT}$ | <br>● | | 44 | 55<br>60 | mA<br>mA |
| $I_{\Delta(OUT)}$ | Delta of Supply Current to OUT Pins | Current Imbalance to +OUT and –OUT | <br>● | | 0.5 | 1.5<br>2.0 | mA<br>mA |
| $I_{S(\overline{SHDN})}$ | Supply Current in Shutdown | $I_{S(OUT)}$ at $\overline{SHDN}$ = 0.8V | <br>● | | 0.5 | 1.3<br>2.0 | mA<br>mA |
| $PSRR_{MAX}$ | Power Supply Rejection Ratio at Max Gain | $–V_G$ = 0V, Output Referred | | 40 | 53 | | dB |
| $PSRR_{MIN}$ | Power Supply Rejection Ratio at Min Gain | $–V_G$ = 1.2V, Output Referred | | 40 | 53 | | dB |

## AC ELECTRICAL CHARACTERISTICS

**The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. Typical AC electrical performance measured in demo board DC1464A (Figure 3, Test Circuit A) unless otherwise noted. Default operating conditions are $V_{CC}$ = 3.3V, $\overline{EN}$ = 0.8V, $\overline{SHDN}$ = 2.2V, $+V_G$ tied to $V_{REF}$ (negative gain slope mode), and $Z_{SOURCE} = Z_{LOAD}$ = 50Ω unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Small Signal** | | | | | | | |
| $BW_{GMAX}$ | –3dB Bandwidth for Sdd21 at Maximum Gain | $–V_G$ = 0V, Test Circuit B | | | 800 | | MHz |
| $BW_{GMIN}$ | –3dB Bandwidth for Sdd21 at Minimum Gain | $–V_G$ = 1.2V, Test Circuit B | | | 800 | | MHz |
| Sdd11 | Input Match at $Z_{SOURCE}$ = 50Ω Differential | $–V_G$ = 0V to 1.2V, 10MHz-500MHz, Test Circuit B | | | –20 | | dB |
| Sdd22 | Output Match at $Z_{LOAD}$ = 200Ω Differential | $–V_G$ = 0V to 1.2V, 10MHz-250MHz, Test Circuit B | | | –10 | | dB |
| Sdd12 | Reverse Isolation | $–V_G$ = 0V to 1.2V, 10MHz-500MHz, Test Circuit B | | | -80 | | dB |
| **Transient Response** | | | | | | | |
| $t_{STEP(6dB)}$ | 6dB Gain Step Response Time | Peak $P_{OUT}$ = +4dBm, $–V_G$ = 0.2V to 0.4V, Time to Settle Within 1dB of Final $P_{OUT}$ | | | 0.4 | | µs |
| $t_{STEP(12dB)}$ | 12dB Gain Step Response Time | Peak $P_{OUT}$ = +4dBm, $–V_G$ = 0.2V to 0.6V, Time to Settle Within 1dB of Final $P_{OUT}$ | | | 0.4 | | µs |
| $t_{STEP(20dB)}$ | 20dB Gain Step Response Time | Peak $P_{OUT}$ = +4dBm, $–V_G$ = 0.2V to 0.8V, Time to Settle Within 1dB of Final $P_{OUT}$ | | | 0.4 | | µs |
| $t_{OVDR}$ | Overdrive Recovery Time at 70MHz | $–V_G$ = 0V, $P_{IN}$ = +3dBm to –17dBm, Time to Settle Within 1dB of Final $P_{OUT}$ | | | 25 | | ns |
| $t_{OFF}$ | Output Amplifier Disable Time | $P_{OUT}$ = 0dBm at $\overline{EN}$ = 0V, $–V_G$ = 0V, $\overline{EN}$ = 0V to 3V, Time for $P_{OUT} \leq$ –20dBm | | | 25 | | ns |
| $t_{ON}$ | Output Amplifier Enable Time | $P_{OUT}$ = 0dBm at $\overline{EN}$ = 0V, $–V_G$ = 0V, $\overline{EN}$ = 3V to 0V, Time for $P_{OUT} \geq$ –1dBm | | | 20 | | ns |
| **70MHz Signal** | | | | | | | |
| $G_{MAX}$ | Maximum Gain | $–V_G$ = 0V, Test Circuit B | | | 17 | | dB |
| $G_{MIN}$ | Minimum Gain | $–V_G$ = 1.2V, Test Circuit B | | | –15 | | dB |
| $G_{RANGE}$ | Gain Range | $G_{MAX}$-$G_{MIN}$ | | | 32 | | dB |
| HD2 | Second Harmonic Distortion | $P_{OUT}$ = 0dBm, $–V_G$ = 0V to 1.0V | | | –80 | | dBc |
| HD3 | Third Harmonic Distortion | $P_{OUT}$ = 0dBm, $–V_G$ = 0V to 1.0V | | | –80 | | dBc |
| IM3 | Third-Order Intermodulation | $f_1$ = 69.5MHz, $f_2$ = 70.5MHz, $P_{OUT}$ = –6dBm/Tone, $–V_G$ = 0V to 1.0V | | | –90 | | dBc |
| OIP3 | Output Third-Order Intercept | $f_1$ = 69.5MHz, $f_2$ = 70.5MHz, $P_{OUT}$ = –6dBm/Tone, $–V_G$ = 0V to 1.0V | | | 39 | | dBm |
| $P1dB_{GMAX}$ | Output 1dB Compression Point at Max Gain | $–V_G$ = 0V (Note 6) | | | 13 | | dBm |
| $NF_{GMAX}$ | Noise Figure at Maximum Gain | $–V_G$ = 0V (Note 5) | | | 10 | | dB |
| $NF_{GMIN}$ | Noise Figure at Minimum Gain | $–V_G$ = 1.2V (Note 5) | | | 42 | | dB |
| **140MHz Signal** | | | | | | | |
| $G_{MAX}$ | Maximum Gain | $–V_G$ = 0V, Test Circuit B | | | 17 | | dB |
| $G_{MIN}$ | Minimum Gain | $–V_G$ = 1.2V, Test Circuit B | | | –15 | | dB |
| $G_{RANGE}$ | Gain Range | $G_{MAX}$-$G_{MIN}$ | | | 32 | | dB |
| HD2 | Second Harmonic Distortion | $P_{OUT}$ = 0dBm, $–V_G$ = 0V to 1.0V | | | –80 | | dBc |
| HD3 | Third Harmonic Distortion | $P_{OUT}$ = 0dBm, $–V_G$ = 0V to 1.0V | | | –75 | | dBc |

## AC ELECTRICAL CHARACTERISTICS

**The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. Typical AC electrical performance measured in demo board DC1464A (Figure 3, Test Circuit A) unless otherwise noted. Default operating conditions are $V_{CC}$ = 3.3V, $\overline{EN}$ = 0.8V, $\overline{SHDN}$ = 2.2V, $+V_G$ tied to $V_{REF}$ (negative gain slope mode), and $Z_{SOURCE} = Z_{LOAD}$ = 50Ω unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| IM3 | Third-Order Intermodulation | $f_1$ = 139.5MHz, $f_2$ = 140.5MHz, $P_{OUT}$ = –6dBm/Tone, $–V_G$ = 0V to 1.0V | | | –88 | | dBc |
| OIP3 | Output Third-Order Intercept | $f_1$ = 139.5MHz, $f_2$ = 140.5MHz, $P_{OUT}$ = –6dBm/Tone, $–V_G$ = 0V to 1.0V | | | 38 | | dBm |
| $P1dB_{GMAX}$ | Output 1dB Compression Point at Max Gain | $–V_G$ = 0V (Note 6) | | | 13 | | dBm |
| $NF_{GMAX}$ | Noise Figure at Maximum Gain | $–V_G$ = 0V (Note 5) | | | 10 | | dB |
| $NF_{GMIN}$ | Noise Figure at Minimum Gain | $–V_G$ = 1.2V (Note 5) | | | 42 | | dB |
| **240MHz Signal** | | | | | | | |
| $G_{MAX}$ | Maximum Gain | $–V_G$ = 0V, Test Circuit B | | | 17 | | dB |
| $G_{MIN}$ | Minimum Gain | $–V_G$ = 1.2V, Test Circuit B | | | –14 | | dB |
| $G_{RANGE}$ | Gain Range | $G_{MAX}$-$G_{MIN}$ | | | 31 | | dB |
| HD2 | Second Harmonic Distortion | $P_{OUT}$ = 0dBm, $–V_G$ = 0V to 1.0V | | | –70 | | dBc |
| HD3 | Third Harmonic Distortion | $P_{OUT}$ = 0dBm, $–V_G$ = 0V to 1.0V | | | –70 | | dBc |
| IM3 | Third-Order Intermodulation | $f_1$ = 239.5MHz, $f_2$ = 240.5MHz, $P_{OUT}$ = –6dBm/Tone, $–V_G$ = 0V to 1.0V | | | –82 | | dBc |
| OIP3 | Output Third-Order Intercept | $f_1$ = 239.5MHz, $f_2$ = 240.5MHz, $P_{OUT}$ = –6dBm/Tone, $–V_G$ = 0V to 1.0V | | | 35 | | dBm |
| $P1dB_{GMAX}$ | Output 1dB Compression Point at Max Gain | $–V_G$ = 0V (Note 6) | | | 12 | | dBm |
| $NF_{GMAX}$ | Noise Figure at Maximum Gain | $–V_G$ = 0V (Note 5) | | | 10 | | dB |
| $NF_{GMIN}$ | Noise Figure at Minimum Gain | $–V_G$ = 1.2V (Note 5) | | | 42 | | dB |
| **280MHz/320MHz Signal** | | | | | | | |
| $G_{MAX}$ | Maximum Gain | f = 320MHz, $P_{OUT}$ = –3dBm, $–V_G$ = 0V | | | 16.9 | | dB |
| $G_{MID}$ | Medium Gain | f = 320MHz, $P_{OUT}$ = –5dBm, $–V_G$ = 0.6V | | | 1.5 | | dB |
| $G_{MIN}$ | Minimum Gain | f = 320MHz, $P_{OUT}$ = –5dBm, $–V_G$ = 1.2V | | | –14.2 | | dB |
| $G_{RANGE}$ | Gain Range | 320MHz, $G_{MAX}$-$G_{MIN}$ | | 29.7 | 31.1 | 32.5 | dB |
| $IM3_{GMAX}$ | Third-Order Intermodulation at Max Gain | $f_1$ = 280MHz, $f_2$ = 320MHz, $P_{OUT}$ = –3dBm/Tone, $–V_G$ = 0V | | | –72 | | dBc |
| $IM3_{GMID}$ | Third-Order Intermodulation at Mid Gain | $f_1$ = 280MHz, $f_2$ = 320MHz, $P_{OUT}$ = –5dBm/Tone, $–V_G$ = 0.6V | | | –71 | –65 | dBc |
| $IM3_{GMIN}$ | Third-Order Intermodulation at Min Gain | $f_1$ = 280MHz, $f_2$ = 320MHz, $P_{OUT}$ = –5dBm/Tone, $–V_G$ = 1.2V | | | –56 | | dBc |
| $OIP3_{GMAX}$ | Output Third-Order Intercept at Max Gain | $f_1$ = 280MHz, $f_2$ = 320MHz, $P_{OUT}$ = –3dBm/Tone, $–V_G$ = 0V | | | 31.0 | | dBm |
| $OIP3_{GMID}$ | Output Third-Order Intercept at Mid Gain | $f_1$ = 280MHz, $f_2$ = 320MHz, $P_{OUT}$ = –5dBm/Tone, $–V_G$ = 0.6V | | 26.0 | 30.5 | | dBm |
| $OIP3_{GMIN}$ | Output Third-Order Intercept at Min Gain | $f_1$ = 280MHz, $f_2$ = 320MHz, $P_{OUT}$ = –5dBm/Tone, $–V_G$ = 1.2V | | | 23.0 | | dBm |

## AC ELECTRICAL CHARACTERISTICS

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **380MHz Signal** | | | | | | | |
| $G_{MAX}$ | Maximum Gain | $-V_G$ = 0V, Test Circuit B | | | 17 | | dB |
| $G_{MIN}$ | Minimum Gain | $-V_G$ = 1.2V, Test Circuit B | | | –14 | | dB |
| $G_{RANGE}$ | Gain Range | $G_{MAX}$-$G_{MIN}$ | | | 31 | | dB |
| IM3 | Third-Order Intermodulation | $f_1$ = 379.5MHz, $f_2$ = 380.5MHz, $P_{OUT}$ = –6dBm/Tone, $-V_G$ = 0V to 1.0V | | | –72 | | dBc |
| OIP3 | Output Third-Order Intercept | $f_1$ = 379.5MHz, $f_2$ = 380.5MHz, $P_{OUT}$ = –6dBm/Tone, $-V_G$ = 0V to 1.0V | | | 30 | | dBm |
| $P1dB_{GMAX}$ | Output 1dB Compression Point at Max Gain | $-V_G$ = 0V (Note 6) | | | 11 | | dBm |
| $NF_{GMAX}$ | Noise Figure at Maximum Gain | $-V_G$ = 0V (Note 5) | | | 10.5 | | dB |
| $NF_{GMIN}$ | Noise Figure at Minimum Gain | $-V_G$ = 1.2V (Note 5) | | | 42 | | dB |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. RF input power rating is guaranteed by design and engineering characterization, but not production tested. The absolute maximum continuous RF input power shall not exceed +15dBm

**Note 2:** The LTC6412C/LTC6412I are guaranteed functional over the operating temperature range of –40°C to 85°C.

**Note 3:** The LTC6412C is guaranteed to meet specified performance from 0°C to 70°C. It is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6412I is guaranteed to meet specified performance from –40°C to 85°C.

**Note 4:** Power gain is defined at $Z_{SOURCE}$ = 50Ω and $Z_{LOAD}$ = 200Ω. Voltage gain for this test condition is 6dB higher than the stated power gain.

**Note 5:** $e_n$ can be calculated from 50Ω NF with the formula:

$$e_n = \sqrt{\{4kT(50)(10^{NF/10} - 1)\}}$$

where

$e_n$ = Input referred voltage noise in $V/\sqrt{Hz}$

NF = 50Ω noise figure in dB

k = Boltzmann's constant = $1.38 \bullet 10^{-23}$J/°K

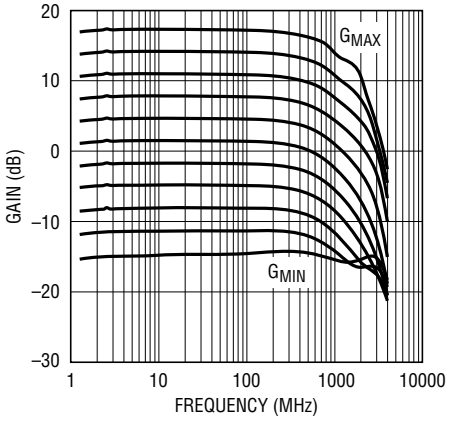
T = Absolute temperature in °K = °C + 273

**Note 6:** P1dB compression of the output amplifier cannot be achieved in the minimum gain state while complying with the absolute maximum rating for input RF power.

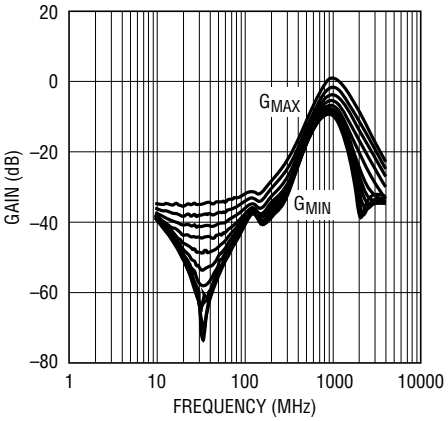
## TYPICAL PERFORMANCE CHARACTERISTICS

**Electrical Performance in Test Circuits A and B at $T_A$ = 25°C and $V_{CC}$ = 3.3V unless otherwise noted.**

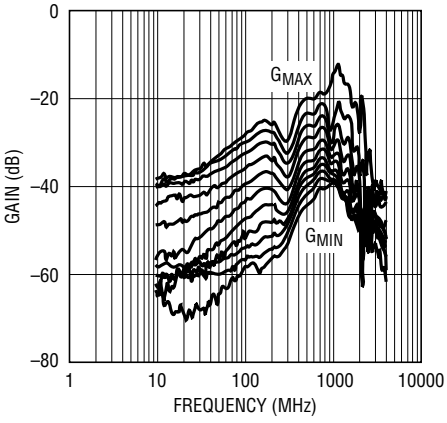
### Differential Gain (Sdd21) vs Frequency Over 11 Gain Settings



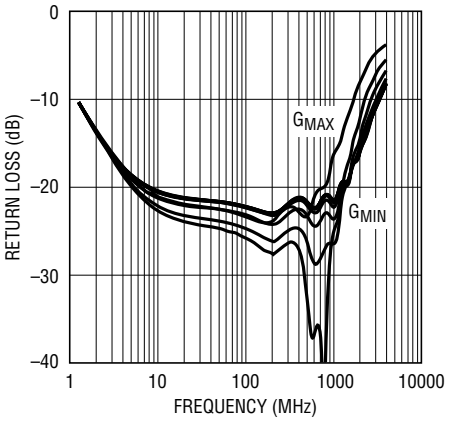

### Common Mode Gain (Scc21) vs Frequency Over 11 Gain Settings



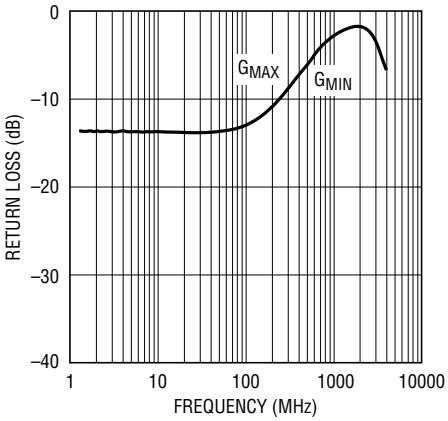

### CM-to-DM Gain (Sdc21) vs Frequency Over 11 Gain Settings



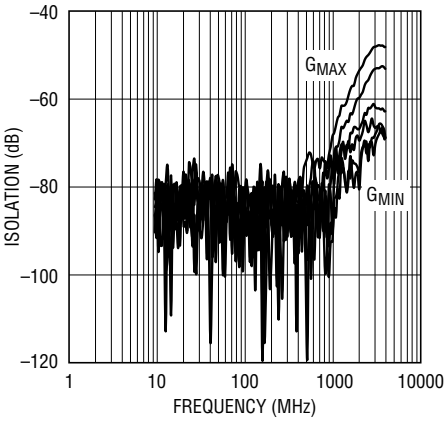

### Differential Input Match (Sdd11) vs Frequency Over 11 Gain Settings



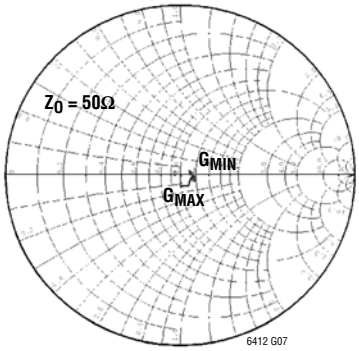

### Differential Output Match (Sdd22) vs Frequency Over 11 Gain Settings



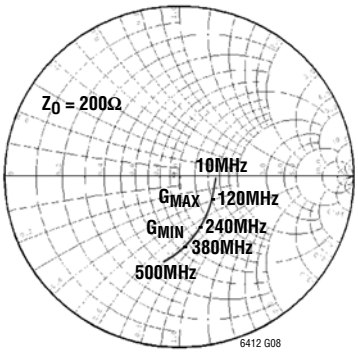

### Differential Reverse Isolation (Sdd12) vs Frequency Over 6 Gain Settings



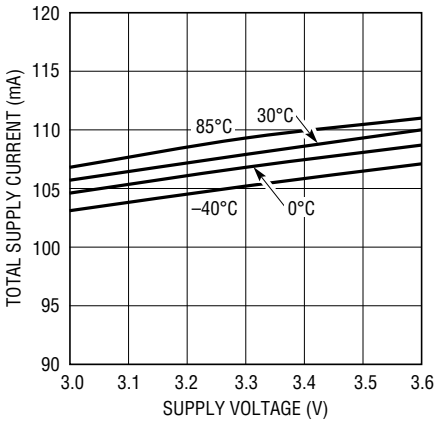

### Differential Input Smith Chart (Sdd11) 10MHz to 500MHz Over 6 Gain Settings




### Differential Output Smith Chart (Sdd22) 10MHz to 500MHz Over 6 Gain Settings



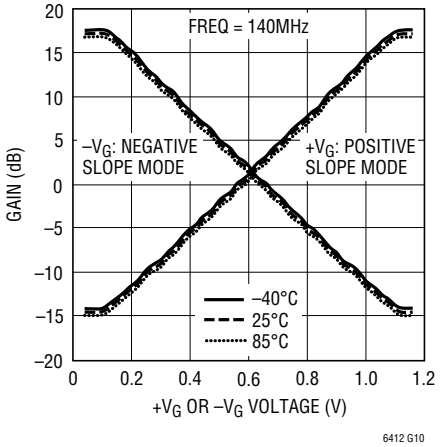

### Supply Current vs Supply Voltage Over Temperature



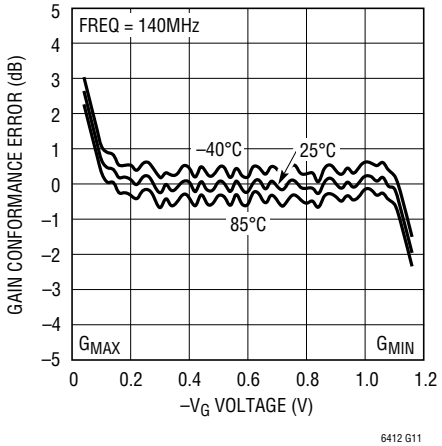
# TYPICAL PERFORMANCE CHARACTERISTICS

**Electrical Performance in Test Circuits A and B at $T_A$ = 25°C and $V_{CC}$ = 3.3V unless otherwise noted.**

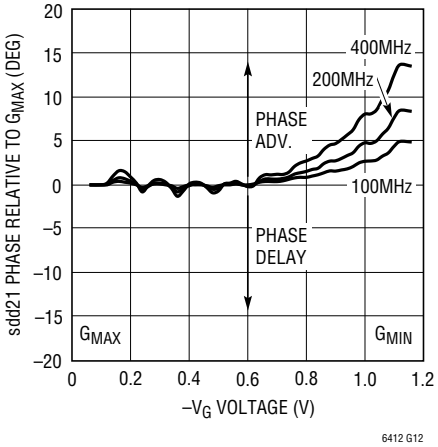
### Differential Gain (Sdd21) vs Control Voltage Over Temperature



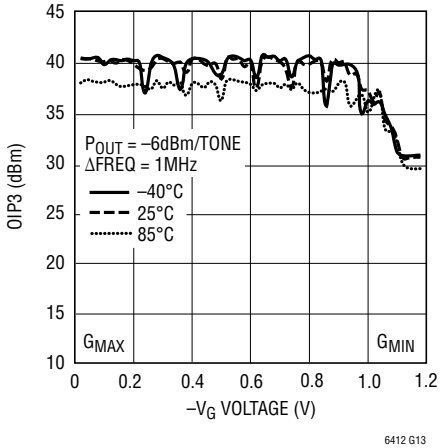

### Gain (Sdd21) Conformance Error vs Control Voltage Over Temperature



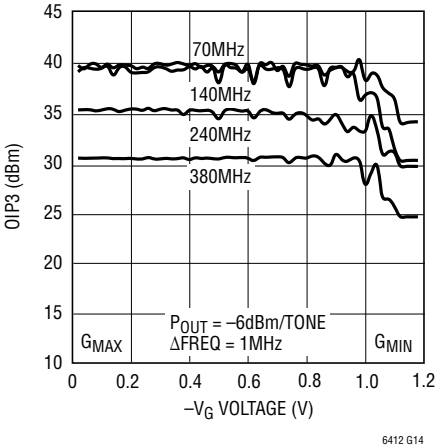

### Relative Phase (Sdd21) vs Control Voltage Over Frequency



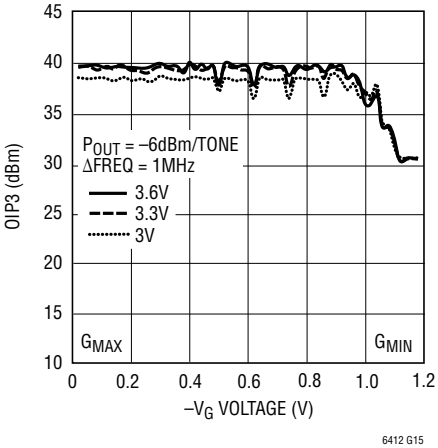

### Output IP3 at 140MHz vs Control Voltage Over Temperature



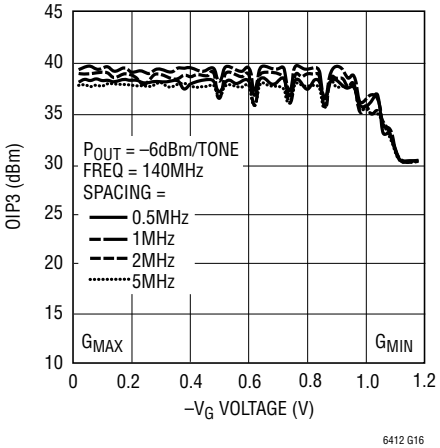

### Output IP3 vs Control Voltage Over Frequency



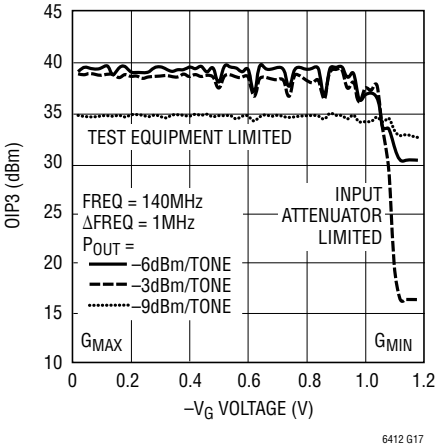

### Output IP3 at 140MHz vs Control Voltage Over $V_{CC}$



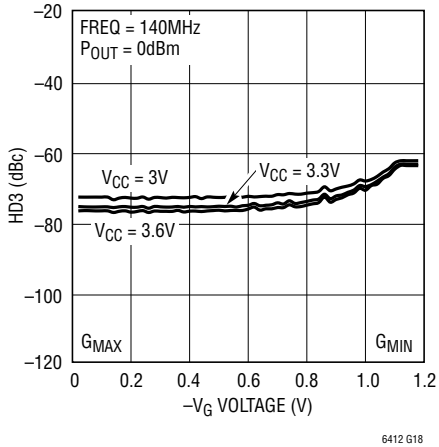

### Output IP3 vs Control Voltage Over Tone Spacing




### Output IP3 vs Control Voltage Over Output Power per Tone



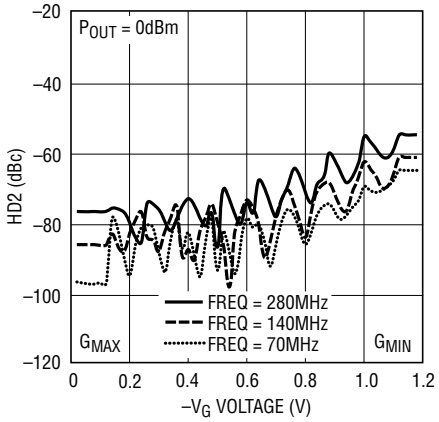

### 3rd Harmonic Distortion vs Control Voltage Over $V_{CC}$



# TYPICAL PERFORMANCE CHARACTERISTICS

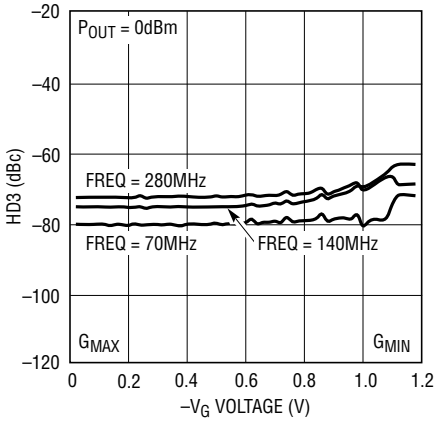
**Electrical Performance in Test Circuits A and B at $T_A$ = 25°C and $V_{CC}$ = 3.3V unless otherwise noted.**

### 2nd Harmonic vs Distortion vs Control Voltage Over Frequency



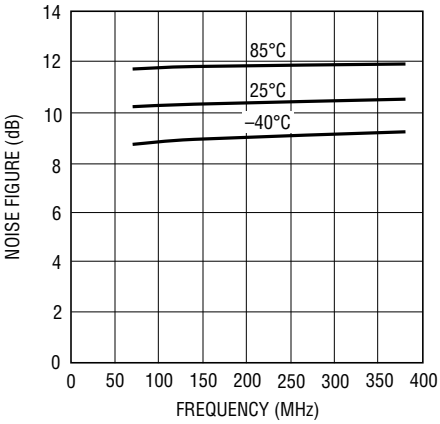

6412 G19

### 3rd Harmonic Distortion vs Control Voltage Over Frequency



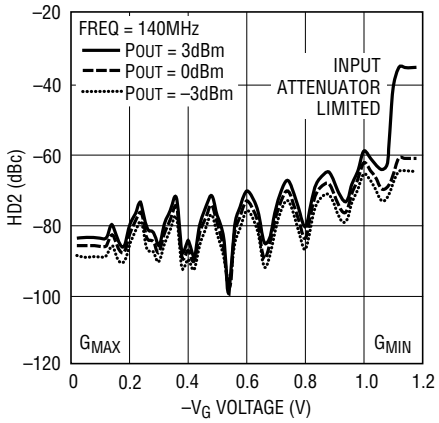

6412 G20

### Noise Figure at $G_{MAX}$ vs Frequency Over Temperature



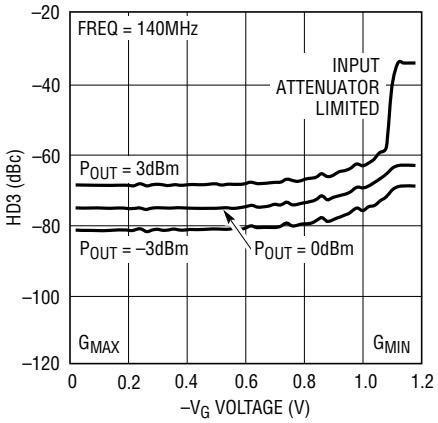

6412 G21

### 2nd Harmonic Distortion vs Control Voltage Over $P_{OUT}$



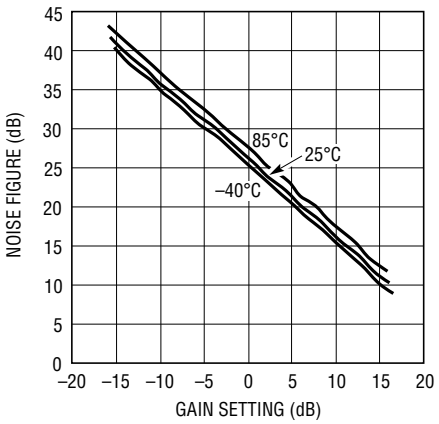

6412 G22

### 3rd Harmonic Distortion vs Control Voltage Over $P_{OUT}$



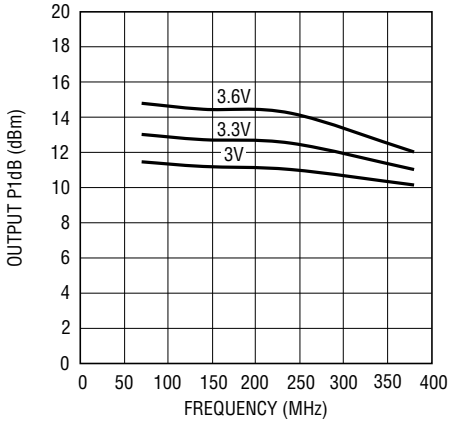

6412 G23

### 140MHz Noise Figure vs Gain Setting Over Temperature



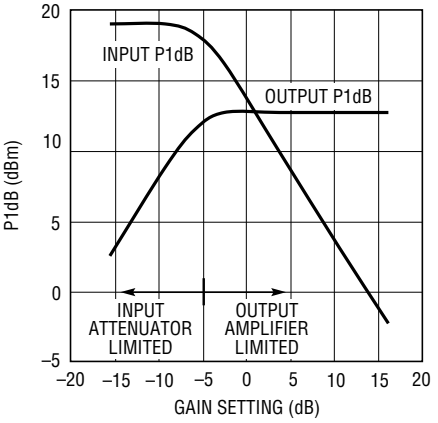

6412 G24

### Output $P_{1dB}$ at $G_{MAX}$ vs Frequency Over Supply Voltage



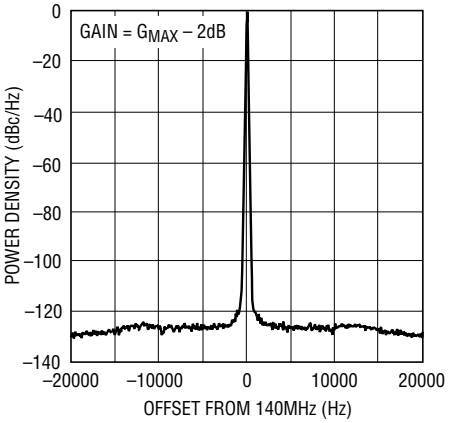

6412 G25

### Input and Output $P_{1dB}$ vs Gain Setting at 140MHz




6412 G26

### 140MHz Sideband Noise Near $G_{MAX}$ at $P_{OUT}$ = +8dBm

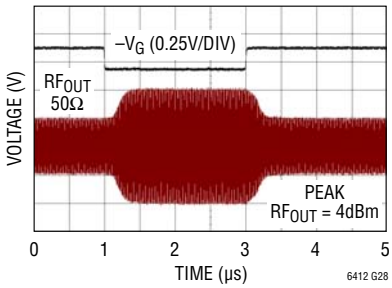



6412 G27

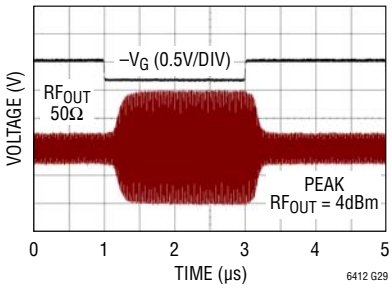
# TYPICAL PERFORMANCE CHARACTERISTICS

**Electrical Performance in Test Circuits A and B at $T_A$ = 25°C and $V_{CC}$ = 3.3V unless otherwise noted.**

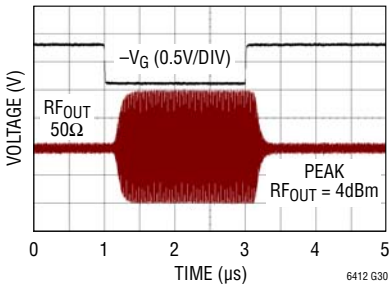
### 6dB Gain Control Step 70MHz Time Domain Response



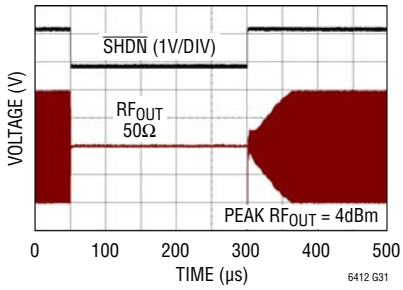

### 10dB Gain Control Step 70MHz Time Domain Response



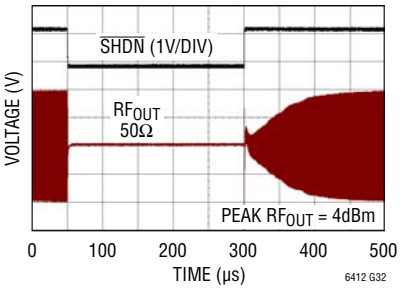

### 20dB Gain Control Step 70MHz Time Domain Response



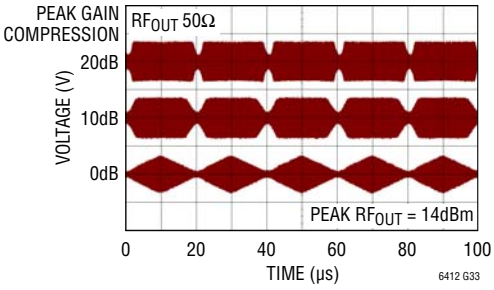

### $\overline{SHDN}$ Step at $G_{MAX}$ with $\overline{EN}$ = 0V 70MHz Time Domain Response



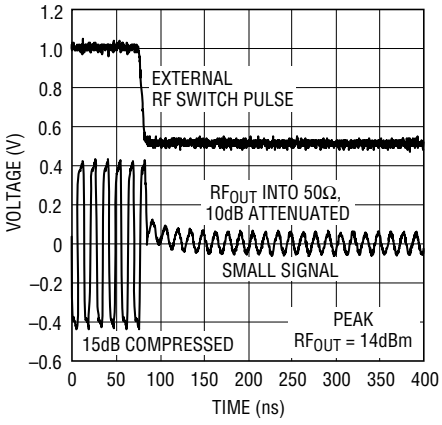

### $\overline{SHDN}$ Step at G = 3dB with $\overline{EN}$ = 0V 70MHz Time Domain Response



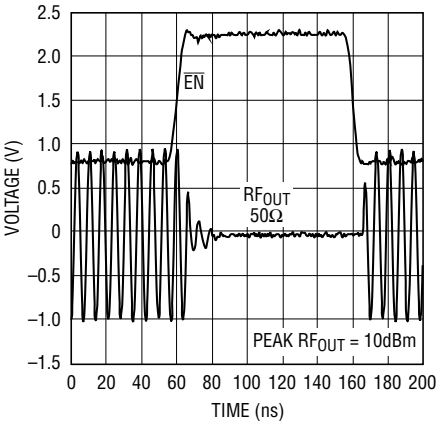

### Overdrive Compression at $G_{MAX}$ 70MHz Time Domain Response



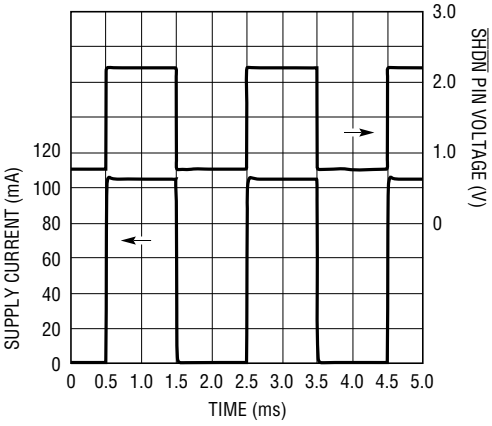

### Overdrive Recovery at $G_{MAX}$ 70MHz Time Domain Response




### Output $\overline{EN}$ Step at $G_{MAX}$ 140MHz Time Domain Response




### $\overline{SHDN}$ Supply Current Time Domain Response



## PIN FUNCTIONS

**GND (Pins 1, 8, 12, 15, 18, 20, 23):** Ground. Pins are connected to each other internally. For best RF performance, all ground pins should be connected to the printed circuit board ground plane.

**+IN (Pin 2):** Positive Signal Input Pin. Has an internally generated DC Bias. A 10nF DC blocking capacitor is recommended.

**–IN (Pin 3):** Negative Signal Input Pin. Has an internally generated DC Bias. A 10nF DC blocking capacitor is recommended.

**$V_{CM}$ (Pins 4, 5):** Input Common Mode Voltage Pins. Two pins are tied together internally and serve as a virtual ground for the differential inputs, +IN and –IN. Capacitive decoupling to ground with 10nF close to the pins is recommended to help terminate any residual common mode input signal.

**$V_{CC}$ (Pins 6, 13, 19, 24):** Positive Power Supply. All four pins must be tied to the same voltage, usually 3.3V. Bypass each pin with 1000pF and 0.1µF capacitors close to the pins.

**DECL1 (Pin 7):** Decoupling Pin. Serves to reduce internal noise. Bypass to ground with a 0.1µF capacitor close to the pin.

**+$V_G$ (Pin 9):** Positive Gain Control Pin. Input signal pin used for positive mode gain control. Otherwise, pin is typically connected to $V_{REF}$ for negative mode gain control. Pin is internally pulled to ground with a 10k resistor. In positive gain slope mode, the gain control slope is approximately +32dB/V at 140MHz with a gain control range of 0.1V to 1.1V.

**$V_{REF}$ (Pin 10):** Internal Bias Voltage Pin. Typically tied to –$V_G$ pin for positive gain control or tied to +$V_G$ for negative gain control. Determines the midpoint voltage of the gain-vs-$V_G$ characteristic. Bypass to ground with 0.1µF capacitor close to the pin. Not intended for use as an external reference voltage.

**–$V_G$ (Pin 11):** Negative Gain Control Pin. Input signal pin used for negative mode gain control. Otherwise, pin is typically connected to $V_{REF}$ for positive mode gain control. Pin is internally pulled to ground with a 10k resistor. In negative gain slope mode, the gain control slope is approximately –32dB/V at 140MHz with a gain control range of 0.1V to 1.1V.

**DECL2 (Pin 14):** Decoupling Pin. Serves to reduce internal noise. Bypass to ground with a 1000pF capacitor close to the pin.

**–OUT (Pin 16):** Negative Amplifier Output Pin. A transformer with a center tap tied to $V_{CC}$ or a choke inductor is recommended to conduct DC quiescent current to the open-collector output device. For best performance, DC bias voltage to –OUT must be within 100mV of $V_{CC}$.

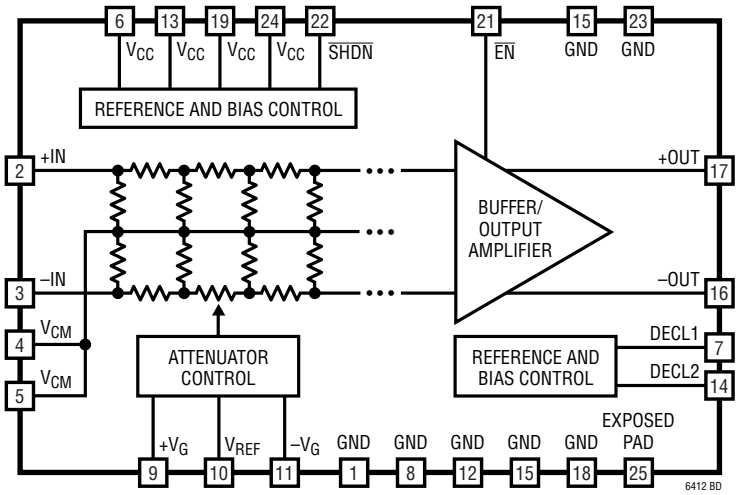
**+OUT (Pin 17):** Positive Amplifier Output Pin. A transformer with a center tap tied to $V_{CC}$ or a choke inductor is recommended to conduct DC quiescent current to the open-collector output device. For best performance, DC bias voltage to +OUT must be within 100mV of $V_{CC}$.

**$\overline{EN}$ (Pin 21):** Output Signal Enable Pin. Pin is internally pulled high with 100kΩ to $V_{CC}$. Assert pin to a low voltage to enable the output amplifier signal. Output amplifier impedance and DC current are not affected by the $\overline{EN}$ state. Connect pin to ground if enable function is not used.

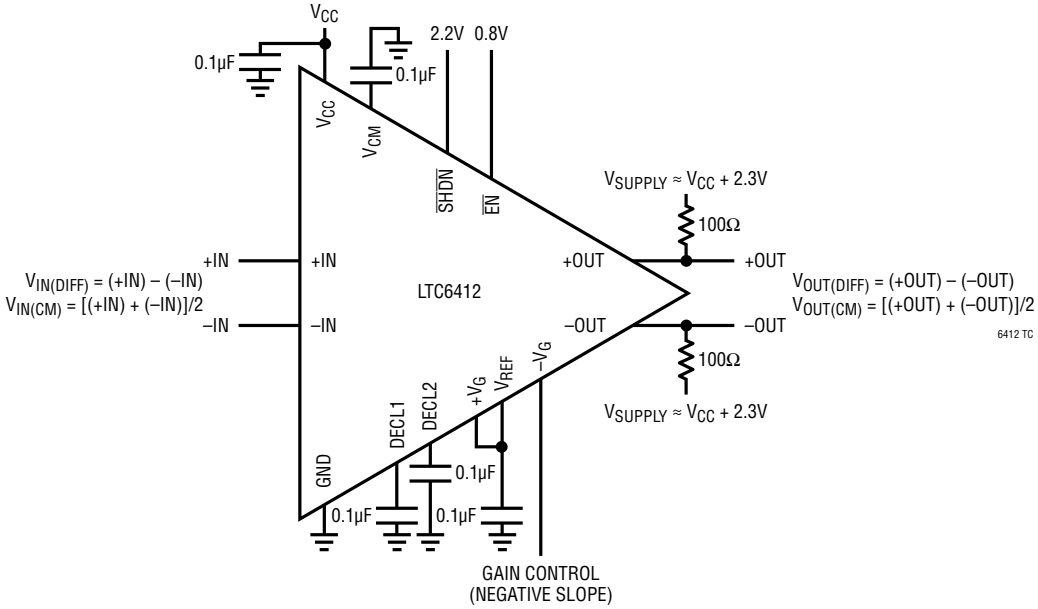
**$\overline{SHDN}$ (Pin 22):** Shutdown Pin. Pin is internally pulled high with 100kΩ to $V_{CC}$. Assert pin to a low voltage to shut down the circuit and greatly reduce the supply current. Proper sequencing of the $\overline{EN}$ and $\overline{SHDN}$ pins is required to avoid non-monotonic output signal behavior. See Applications Information section for details. Connect pin to $V_{CC}$ if shutdown function is not used.

**Exposed Pad (Pin 25):** Ground. The Exposed Pad should have multiple via holes to an underlying ground plane for low inductance and good thermal dissipation.

## BLOCK DIAGRAM




## DC TEST CIRCUIT



## OPERATION

The LTC6412 employs an interpolated, tapped attenuator circuit architecture to generate the variable-gain characteristic of the amplifier. The tapped attenuator is fed to a buffer and output amplifier to complete the differential signal path shown in the Block Diagram. This circuit architecture provides good RF input power handling capability along with a constant output noise and output IP3 characteristic that are desirable for most IF signal chain applications. The internal control circuitry takes the gain control signal from the $\pm V_G$ terminals and converts this to an appropriate set of control signals to the attenuator ladder. The attenuator control circuit ensures that the linear-in-dB gain response is continuous and monotonic over the gain range for both slow and fast moving input control signals while exhibiting very little input impedance variation over gain. These design considerations result in a gain-vs-$V_G$ characteristic with a ±0.1dB ripple and a 0.5µs gain response time that is slower than a similar digital step attenuator design.

An often overlooked characteristic of an analog-controlled VGA is upconverted amplitude modulation (AM) noise from the gain control terminals. The VGA behaves as a 2-quadrant multiplier, so some minimal care is required to avoid excessive AM sideband noise generation. The following table demonstrates the effect of the baseline 20nV/$\sqrt{Hz}$ equivalent input control noise from the LTC6412 circuit along with the effect of a higher combined input noise due to a noisy external control circuit.

| CONTROL INPUT TOTAL NOISE VOLTAGE (nV/$\sqrt{Hz}$) | PEAK AM NOISE AT 10kHz OFFSET NEAR MAXIMUM GAIN (dBc/Hz) |
|---|---|
| 20 | –142 |
| 40 | –136 |
| 70 | –131 |
| 100 | –128 |
| 200 | –122 |

The baseline equivalent 20nV/$\sqrt{Hz}$ input noise is seen to produce worst-case AM sidebands of –142dBc/Hz which is near the –147dBm/Hz output noise floor at maximum gain for a nominal 0dBm output signal. An input control noise voltage less than 80nV/$\sqrt{Hz}$ is generally recommended to avoid measurable AM sideband noise. While op amp control circuit output noise voltage is usually below 80nV/$\sqrt{Hz}$, some low power DAC outputs exceed 150nV/$\sqrt{Hz}$. DACs with output noise in the range of 100nV/$\sqrt{Hz}$ to 150nV/$\sqrt{Hz}$ can usually be accommodated with a suitable 2:1 or 3:1 resistor divider network on the DAC output to suppress the noise amplitude by the same ratio. Noisy DACs in excess of 150nV/$\sqrt{Hz}$ should be avoided if minimal AM noise is important in the application.

## APPLICATIONS INFORMATION

### Introduction

The LTC6412 is a high linearity, fully-differential analog-controlled variable-gain amplifier (VGA) optimized for application frequencies in the range of 1MHz to 500MHz. The VGA architecture provides a constant OIP3 and constant output noise level (NF + Gain) over the 31dB gain-control range and thus exhibits a uniform spurious-free dynamic range (SFDR) over gain. This constant SFDR characteristic is ideal for use in receiver IF chains that are upstream from a signal sink such as a demodulator or ADC.

The low supply voltage requirements and fully differential design are compatible with many other LTC mixer, amplifier and ADC products for use in compact, low voltage, fully differential receiver chains. For non-differential systems, the 50Ω input impedance and 200Ω output impedance are easily converted to single-ended 50Ω ports with inexpensive 1:1 and 4:1 baluns.

### Gain Characteristics

The LTC6412 provides a continuously adjustable gain range of –14dB to 17dB that is linear-in-dB with respect to the control voltages applied to $+V_G$ and $–V_G$. These control pins can be operated with a differential signal, but it is more common to operate one of the $V_G$ pins with a single-ended control signal while connecting the other $V_G$ pin to the provided $V_{REF}$ pin. In this way, either a positive gain-control slope or negative gain-control slope is easily achieved:

*Negative Gain-Control Slope.* Tie $+V_G$ to $V_{REF}$ and apply gain control voltage to the $–V_G$ pin. Gain decreases with increasing $–V_G$ voltage.

*Positive Gain-Control Slope.* Tie $–V_G$ to $V_{REF}$ and apply gain control voltage to the $+V_G$ pin. Gain increases with increasing $+V_G$ voltage.

When connected in this typical single-ended configuration, the active control input range extends from 0.1V to 1.1V. This control input range can be extended using a resistor divider with a suitably low output resistance. For example, two series resistors of 1k each would extend the control input range from 0.2V to 2.2V while providing an effective 500Ω Thevinin equivalent source resistance, a relatively small loading effect compared to the 10k input resistance of the $+V_G$/$–V_G$ terminals.

### Port Characteristics

The LTC6412 provides a nominal 50Ω differential input impedance and 200Ω differential output impedance over the operating frequency range.

The input impedance characteristic derives from the differential attenuator ladder shown in the Block Diagram. The internal circuit controls the RF connections to this attenuator ladder and generates the appropriate common mode DC voltage to this port. The differential attenuator ladder creates a virtual ground node that needs a capacitor bypass to ground at the $V_{CM}$ pin to effectively attenuate any common mode signal presented to the input port. The $+V_{IN}$ and $–V_{IN}$ pins are connected to the input signal through DC blocking capacitors as shown in Test Circuit A and Test Circuit B, Figures 1-4.

The output impedance characteristic derives from the open-collector equivalent circuit shown in Figure 7. The action of the differential shunt, lowpass filter, and internal feedback presents an effective differential output impedance of 200Ω to 300Ω between the +OUT and –OUT pins over the operating band. The $+V_{OUT}$ and $–V_{OUT}$ pins are connected to the output port using shunt inductors or a transformer to provide a DC path to the supply voltage. The DC block to the circuit output is usually accomplished using series capacitors. These blocking capacitors can be avoided if a flux transformer is used at the output. Figure 9 illustrates a few common inductor and balun transformer methods for coupling the AC signal and DC supply to the output pins. This is discussed further in the Typical Application Circuits section.

### Power Supplies

Inductance to the supply path can degrade the performance of the LTC6412. It is recommended that low inductance bypass capacitors are installed very close to each of the $V_{CC}$ pins. 1000pF and 0.1µF parallel capacitors are recommended with the smaller capacitor placed closer to the $V_{CC}$ pin. Do not leave any supply pins disconnected. For best performance, DC bias voltage to the +OUT and –OUT pins must be within 100mV of $V_{CC}$. The Exposed Pad on the underside of the package must be connected to ground with low inductance and low thermal resistance. Refer to details of DC1464A (Test Circuit A) for an example of proper

## APPLICATIONS INFORMATION

grounding and supply decoupling. Failure to provide low impedance supply and ground at high frequencies can cause oscillations and increased distortion.

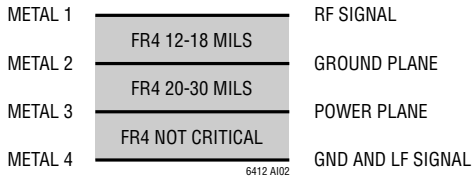
### Enable/Shutdown

Both the $\overline{EN}$ pin and $\overline{SHDN}$ pin are self-biased to $V_{CC}$ through their respective 100k pull-up resistors, so the default open-pin state is powered on with the output amplifier signal path disabled. Pulling the $\overline{EN}$ pin low completes the signal path from the attenuator ladder through the output amplifier. The $\overline{EN}$ pin essentially provides a fast muting function while the $\overline{SHDN}$ pin provides slower power on/off function.

For applications requiring the $\overline{SHDN}$ function, it is recommended that the output amplifier signal path be disabled with a high $\overline{EN}$ voltage before transitioning the $\overline{SHDN}$ signal. When enabling the amplifier, allow at least 5ms dwell time between the rising $\overline{SHDN}$ transition and the falling $\overline{EN}$ transition to avoid non-monotonic output signal behavior though the VGA. The opposite delay sequence is recommended for the falling $\overline{SHDN}$ transition, but this is less critical as the output signal amplitude will drop abruptly regardless of the $\overline{EN}$ pin.


### Layout/Grounding

The high frequency performance of the LTC6412 requires special attention to proper RF grounding, bias decoupling and termination. The recommended PCB stack-up for a 4-layer board is shown below for 1oz copper clad FR-4 laminate with a relative dielectric constant, $\varepsilon_r$ = 4.2-4.5 at 1GHz.




The topside metal and silkscreen drawings for Test Circuit A illustrate the recommended decoupling capacitor placement, signal routing and grounding. Ground vias directly beneath the Exposed Pad are critical; use as many as possible. Ground vias to the other ground pins are less critical.

### ESD

The LTC6412 is protected with reverse-biased ESD diodes on all I/O pins. If any I/O pin is forced one diode drop above the positive supply or one diode drop below the negative supply, then large currents may flow through the diodes. No damage to the devices will occur if the current is kept below 10 mA. The +OUT/–OUT pins have additional series diodes to the positive supply and can sustain approximately 2V overshoot above the positive supply before conducting appreciable currents.

### Signal Compression Characteristics

The graph entitled, Input and Output P1dB, illustrates an important characteristic of the LTC6412 VGA. At gain settings above –5dB, the output amplifier limits the linear power handling capability, but at gain settings below –5dB, the input attenuator ladder limits the linear power handling capability. The linear input power limitations at minimum gain do not affect the overall performance of a signal chain if the preceding mixer or amplifier stage exhibits an OP1dB < 19dBm and an OIP3 < 50dBm.

### Test Circuits

The fully-differential nature of the LTC6412 design requires two test circuits to generate the performance information presented in this data sheet.

Test Circuit A is DC1464A, a 2-port demonstration circuit with input/output balun transformers to allow for direct connection to a 2-port network analyzer or other single-ended 50Ω test system. The balun transformers limit the high and low frequency performance of the LTC6412 but allow for simple and reasonably accurate measurements from 70MHz to 380MHz. The gain control signal is supplied to either of the $V_G$ turrets for DC control measurements or through the $V_{GAIN}$ SMA connector for transient control signal measurements. Clip leads to the gain control turrets are susceptible to noise pickup and should be lowpass

## APPLICATIONS INFORMATION

filtered to avoid AM upconversion artifacts. While using the $\pm V_G$ turrets, a 4.7µF capacitor from the $V_{GAIN}$ SMA input to ground provides an effective lowpass filter.

Typical data curves quoted for Test Circuit A are measured at the plane of the SMA connectors and are NOT corrected for any losses introduced by the input and output baluns, estimated at approximately 0.5dB and 1.2dB, respectively. All typical AC data reported in this data sheet correspond to Test Circuit A, except for mixed-mode S-parameters of the form Sdd21, Scc21, etc.

Test Circuit B uses a 4-port network analyzer to measure differential mode and common mode S-parameters beyond the frequency limitations imposed by the balun transformers and associated circuitry. A matching calibration set establishes the measurement reference planes shown in Test Circuit B. The output plane is defined at the edge of the package while the input plane is defined at the edge of the input pair of 0402 capacitors. The IC land and ground via pattern are identical to that shown for Test Circuit A. The ground via pattern directly beneath the package is critical to provide the proper RF ground to produce the RF characteristics quoted in this data sheet. All mixed-mode S-parameter typical data curves of the form SxyAB correspond to Test Circuit B following the definitions described in Figures 5 and 6.

### Typical Application Circuits

Grounding and supply decoupling should closely follow the suggested layout shown for Test Circuit A, but the input and output networks can be customized to suit various application requirements.

On the input side, the differential port impedance is very close to 50Ω over all gain settings and application frequencies. In a differential signal chain, the differential input signal is easily supplied from a preceding differential output stage with a suitable DC blocking capacitor of approximately 10nF. If the system employs a single-ended input signal to the VGA, then a suitable balun is required to convert to a differential input signal. The passive conversion from 50Ω single-ended to 50Ω differential is most effectively accomplished with a 1:1 transmission-line balun such as the ETC1-1-13 or MABA-007159. These 1:1 balun devices are relatively inexpensive and offer excellent electrical characteristics such as low loss, broad band response and good phase matching.

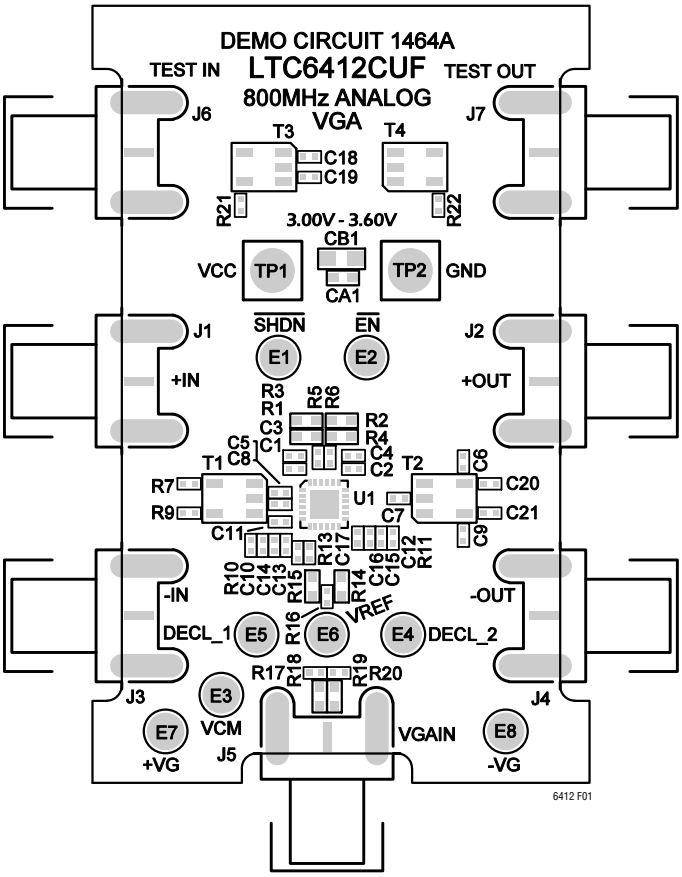



**Figure 1. Top Silkscreen for DC1464A. Test Circuit A**

On the output side, the differential port admittance is very close to 300Ω||1.5pF across all gain settings and application frequencies. This output port circuit must provide a path for DC output supply current as well as any balun, matching, or filtering functions required by the application. Thus, the design options for the output circuitry are more varied. A brief list of the more common output circuits is shown in Figure 9 along with a few design guidelines to estimate component values. Final design simulations should use the small-signal equivalent circuit model in Figure 8 to properly account for loading effects of the output terminals.

Figure 9a shows the simplest differential output configuration employing two suitable inductors, L1 = L2, to pass the DC supply current without loading the output nodes at the application frequency. The PCB trace widths

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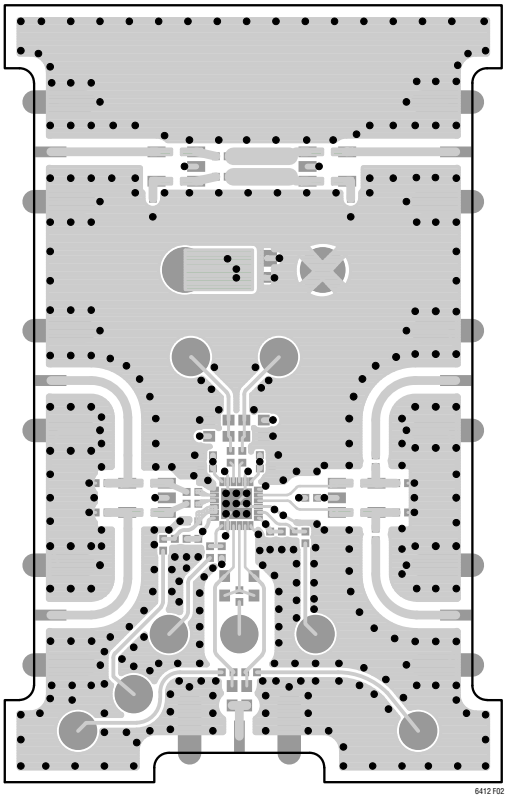


**Figure 2. Top Metal for DC1464A. Test Circuit A**

from the output pins should be narrow in keeping with the high impedance of these terminals; 8 to 10mil trace width on 1oz copper is a good choice. The 0.1µF capacitors serve to DC block and decouple as needed. These capacitor values are adequate down to a few MHz and can be scaled down for higher application frequencies.

If bandpass filtering is needed at the VGA output of Figure 9a, then L1 and L2 can be designed to resonate with a shunt capacitor, $C_O$, at the frequency of interest, $\omega = 1/\sqrt{C_O(L1 + L2)}$. Alternately, L1 = L2 can be designed to resonate with two separate capacitors, C1 = C2, so any common mode noise is filtered as well.

Figure 9b shows a further variation of the tuned differential output where the DC blocking capacitors are brought inside the tank resonator to participate in the bandpass filter and transform the VGA output impedance to a lower value. Here too, the $C_O$ capacitor can be split into two separate shunt capacitors to ground, so any common mode noise is filtered as well.

Figure 9c shows a flux transformer used to achieve a 50Ω single-ended output. The flux transformer does not provide the large bandwidth typical of the output transmission-line transformer shown in Figure 3, but it usually performs well over smaller bandwidths, especially when tuned with shunt capacitors (not shown). The flux transformer design eliminates DC blocking capacitors and is attractive in rugged applications where the amplifier output is subjected to ESD events and other forms of transient electrical overstress that do not pass through a typical RF flux transformer such as the MABAES0061.

Figure 9d shows a discrete LC balun suitable for bandwidths of approximately 15% to 30%. Larger bandwidths are difficult to achieve with the number of components shown, and smaller bandwidths are often limited by component tolerance effects. Despite these limitations, the discrete LC balun can be a cost effective output circuit solution. At resonance, the tuned circuit produces an impedance transformation along with the differential-to-single-ended conversion.

### DC-Coupled Operation

The LTC6412 is intended for AC-coupled operation. The translation between the fixed input DC common mode voltage and higher open-collector output DC bias point makes it impractical to use in DC-coupled applications.

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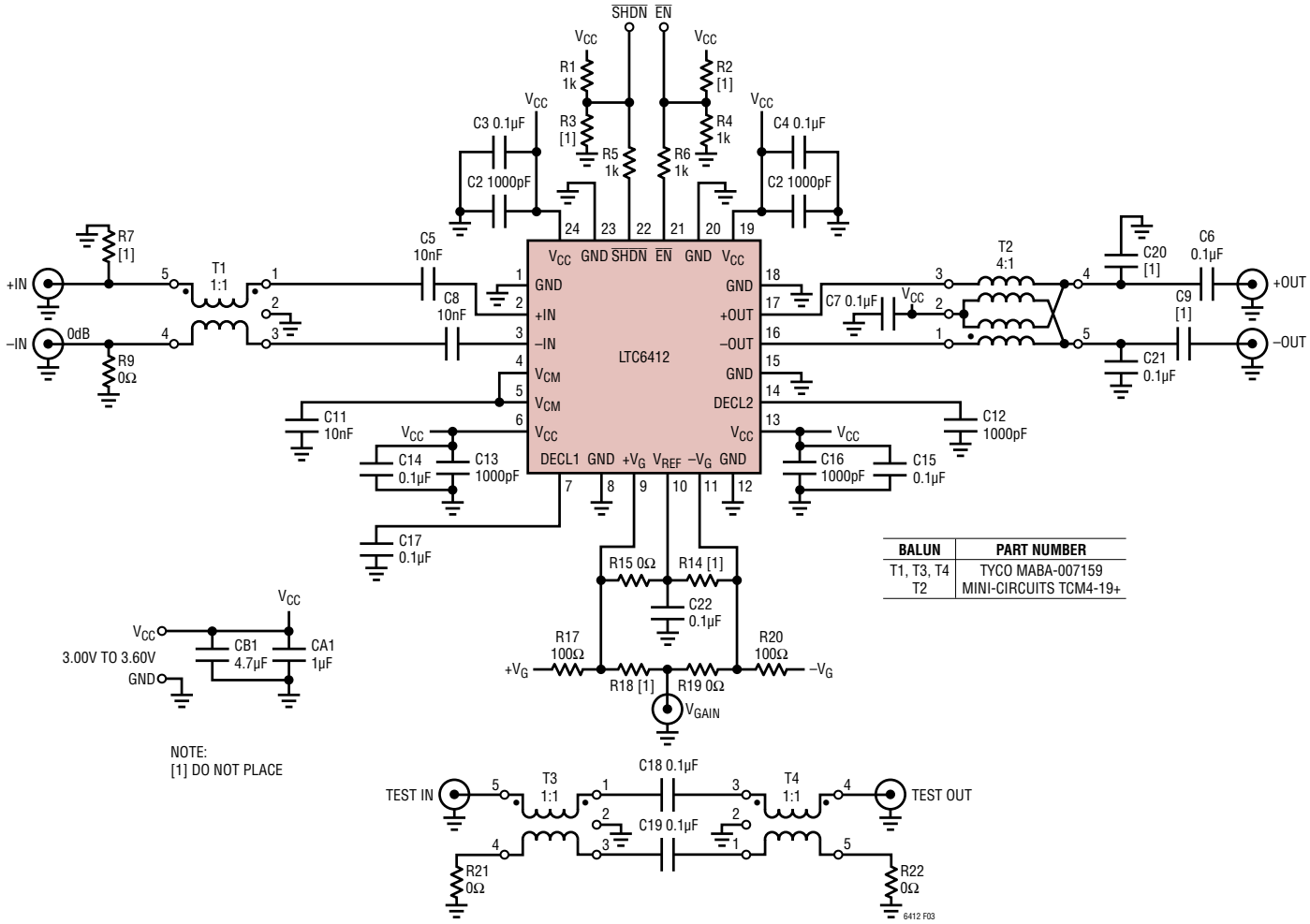



| BALUN | PART NUMBER |
|---|---|
| T1, T3, T4 | TYCO MABA-007159 |
| T2 | MINI-CIRCUITS TCM4-19+ |

**Figure 3. Demo Board DC1464A Circuit Schematic. Test Circuit A**

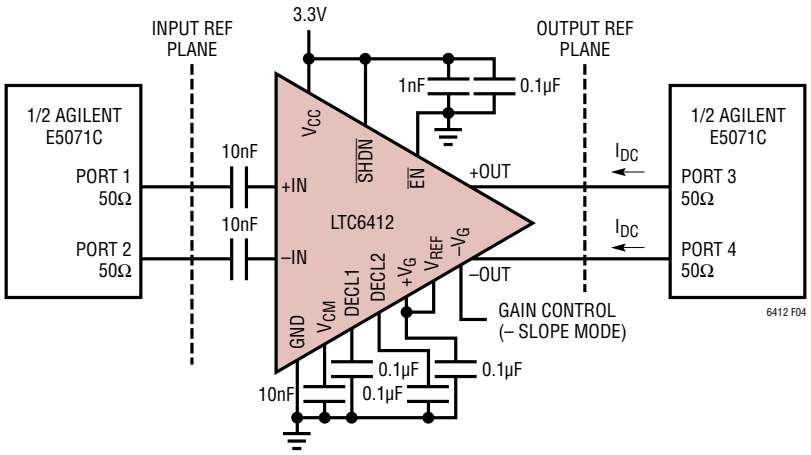



**Figure 4. 4-Port Analysis Schematic. Test Circuit B**

## APPLICATIONS INFORMATION

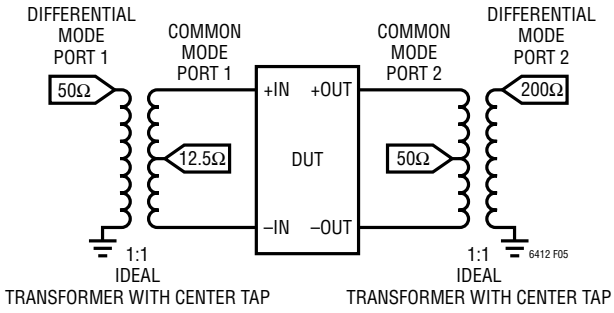



**Figure 5. Schematic of Mixed-Mode S-Parameters Reported for Test Circuit B**

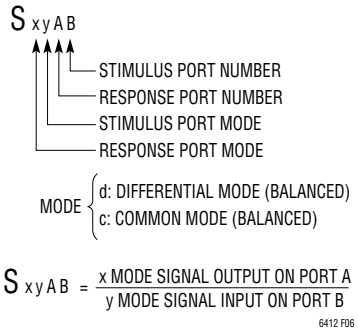



**Figure 6. Definition of Mixed-Mode S-Parameters Reported for Test Circuit B**

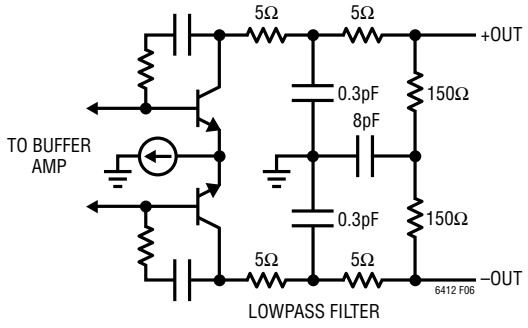



**Figure 7. Large-Signal Output Equivalent Circuit Schematic**

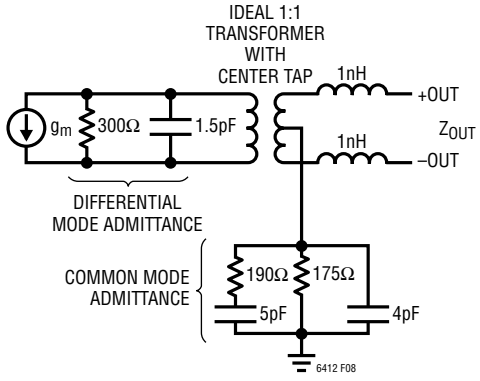



**Figure 8. Small-Signal Output Equivalent Circuit Model**

## APPLICATIONS INFORMATION

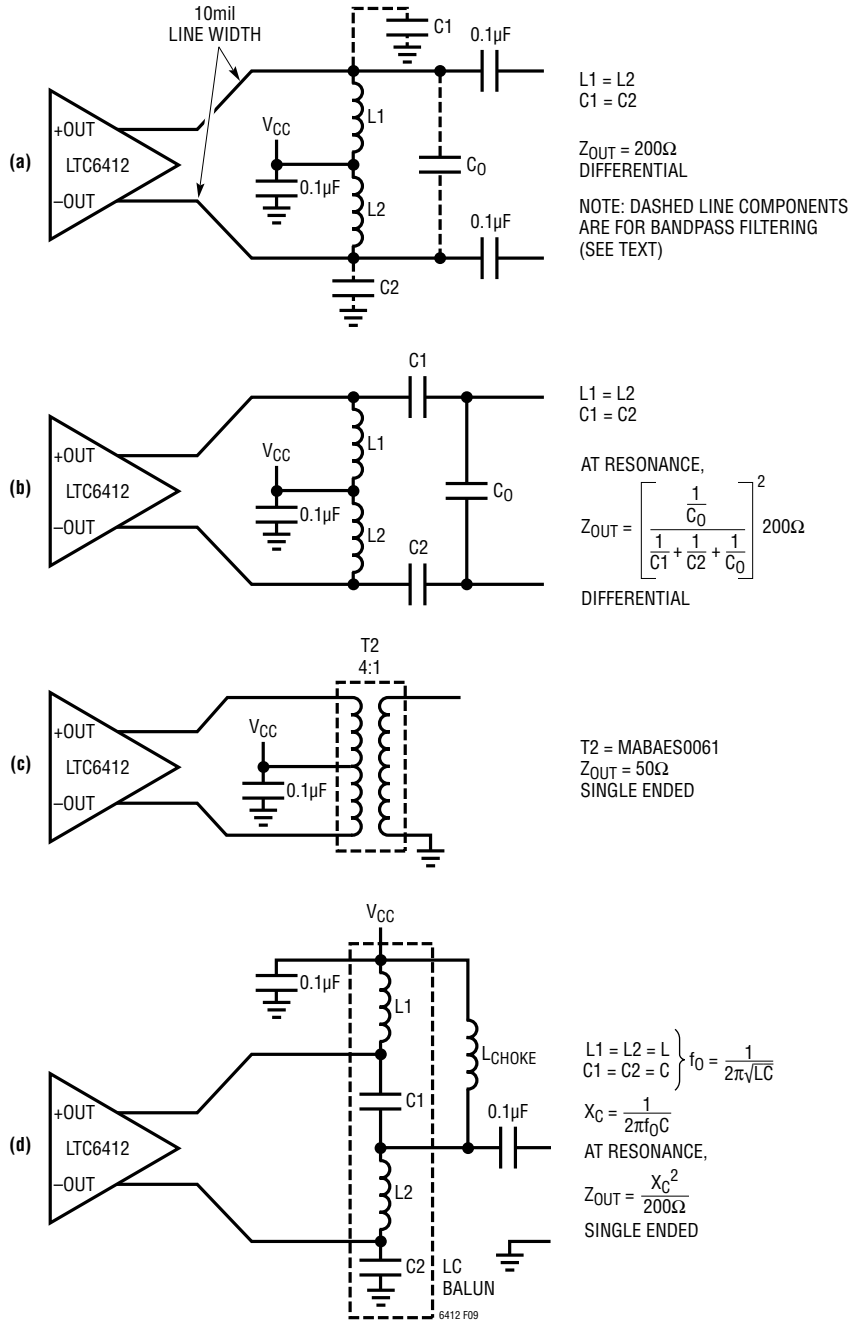
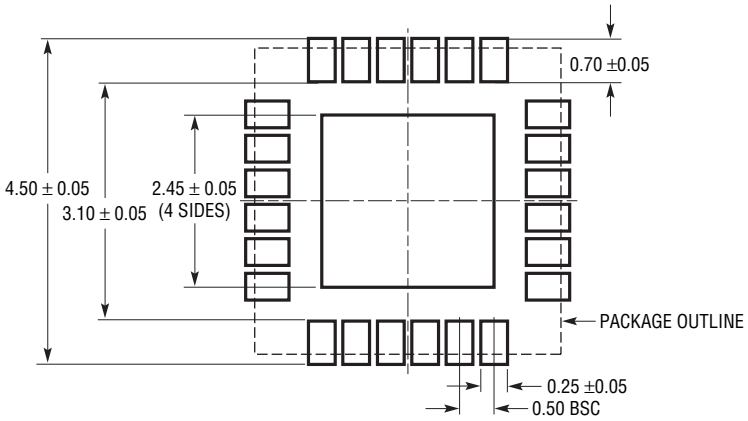


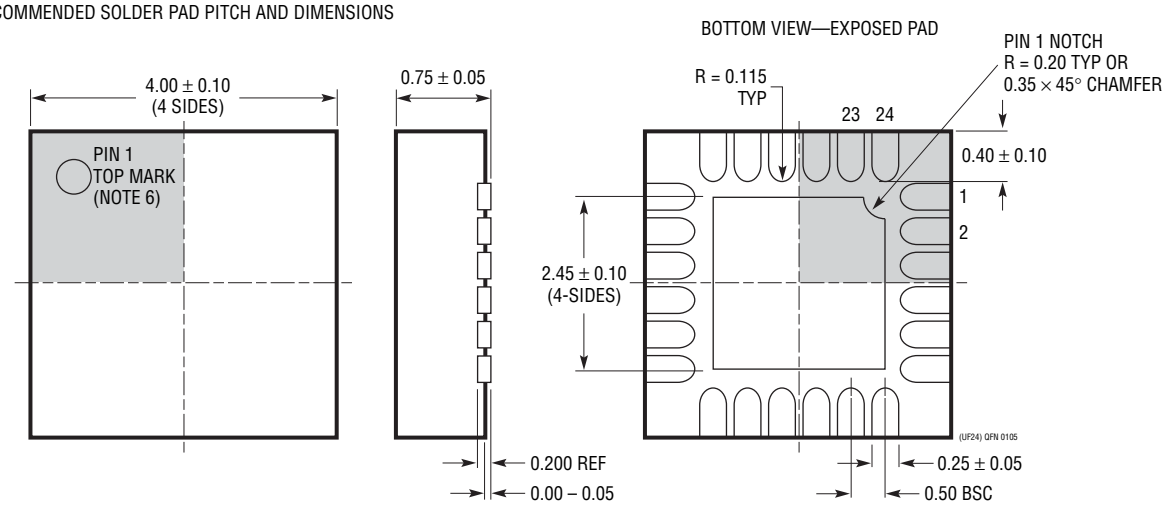

**Figure 9. Output AC/DC Coupling, Filter and Balun Circuit Design Options**

# PACKAGE DESCRIPTION

**UF Package**
**24-Lead Plastic QFN (4mm × 4mm)**
(Reference LTC DWG # 05-08-1697)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS




NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 4/10 | Change $TC_{GAIN}$ Typical to –0.007dB/°C in DC Electrical Characteristics | 3 |