100kHz to 1.4GHz Differential ADC Driver/IF Amplifier

FEATURES

- **100kHz to 1400MHz Bandwidth**
- **54.4dBm OIP3 at 1MHz into a 100Ω Diff Load**
- **48.0dBm OIP3 at 150MHz into a 100Ω Diff Load**
- **Up to 15dBm Output Power**
- **NF = 3.0dB at 240MHz**
- **Low 1/f Noise Corner**
- **User Defined Low Frequency**
- **15.2dB Fixed Power Gain**
- **A-Grade 100% OIP3 Tested at 150MHz**
- 0.8 nV/√Hz Total Input Noise
- >2.75V_{P-P} Linear Output Swing
- P1dB = 22.5dBm
- Insensitive to V_{CC} Variation
- Input/Output Internally Matched to 100Ω Differential
- Single 5V Supply
- DC Power = 850mW
- Unconditionally Stable

APPLICATIONS

- Differential 1GHz Bandwidth ADC Driver
- Wideband Test Instrument Amplifier
- Differential IF Amplifier
- 50Ω/75Ω Balanced IF Amplifier

DESCRIPTION

The LTC®6432-15 is an ultra-high dynamic range differential gain block amplifier designed to drive high resolution, high speed ADCs. It offers a full GHz of data bandwidth for complex spectrally efficient modulations schemes or where resistance to blockers is critical. This unique device can simultaneously achieve low noise, incomparable linearity and flat gain over the 100kHz to 1GHz band.

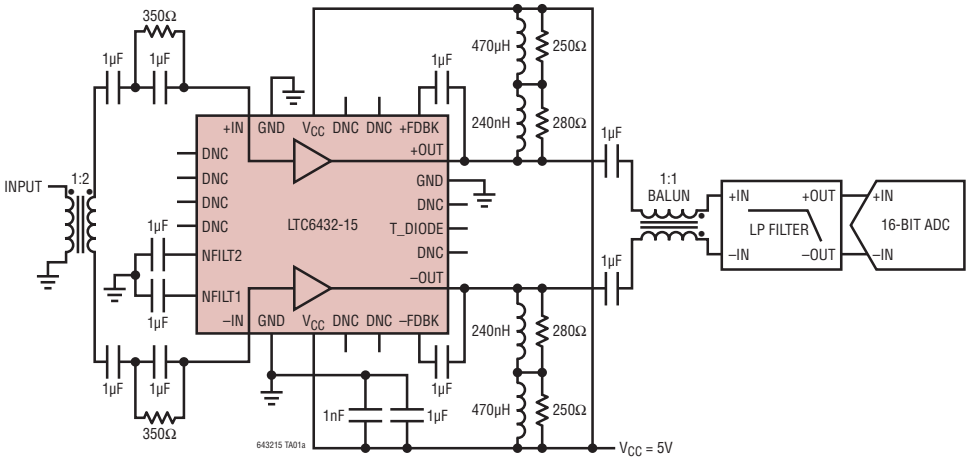
Unlike wideband GaAs PHEMTs, MESFETs and GaN FETs, this SiGe based amplifier exhibits low 1/f noise and can be used down to 100kHz.

The LTC6432-15 is designed for ease of use requiring a minimum of support components. Impedance matching, temperature compensation and bias control are handled internally to ensure consistent performance over environmental changes.

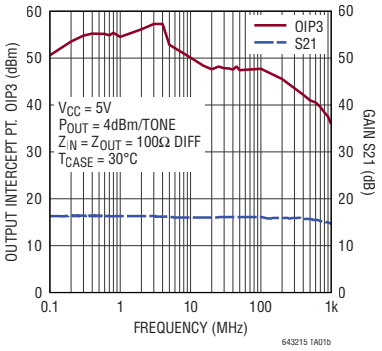
All A-Grade LTC6432-15 devices are tested and guaranteed for OIP3 at 150MHz. The LTC6432-15 is housed in a 4mm × 4mm, 24L, QFN package with an exposed pad for thermal management and low inductance.

For a single-ended 50Ω IF Gain Block with similar performance, see the related LTC6433-15.

TYPICAL APPLICATION



OIP3 and S21 vs Frequency

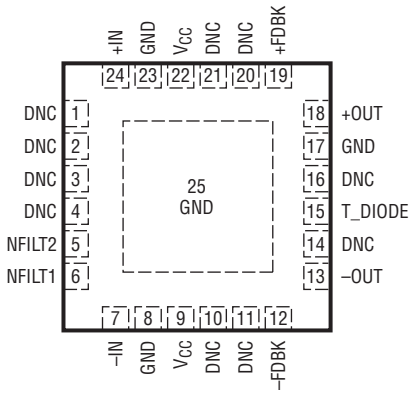


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC} to GND).....5.5V
Amplifier Output Current (+OUT) 105mA
Amplifier Output Current (–OUT) 105mA
RF Input Power, Continuous, 50Ω (Note 2)..... +15dBm
RF Input Power, 100µs pulse, 50Ω (Note 2) .....+20dBm
Operating Case Temperature
Range (T_{CASE}).....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Junction Temperature (T_J) ..... 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 40°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB.
CASE TEMPERATURE IS MEASURED ON THE BACKSIDE OF THE PCB.

ORDER INFORMATION

http://www.linear.com/product/LTC6432-15#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (T_{CASE})
LTC6432AIUF-15#PBF	LTC6432AIUF-15#TRPBF	43215	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC6432BIUF-15#PBF	LTC6432BIUF-15#TRPBF	43215	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

The LTC6432-15 is available in two grades. Grade A guarantees a minimum OIP3 at 150MHz while grade B does not. A- and B-grades are identified by a label on the shipping container.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω. Typical measured DC electrical performance using Test Circuit A (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Operating Supply Range			4.75	5	5.25	V
$I_{S,TOT}$	Total Supply Current	All V_{CC} Pins Plus +OUT and –OUT.	 ●	145 110	166	195 220	mA mA
$I_{S,OUT}$	Total Supply Current to OUT Pins	Current to +OUT and –OUT	 ●	130 100	152	185 200	mA mA
I_{VCC}	Current to V_{CC} Pin	Either V_{CC} Pin May Be Used	 ●	13 12.5	14	17 17.5	mA mA

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_{CASE} = 30°C (Note 3). V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted, measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Small Signal							
BW	–3dB Bandwidth	De-Embedded to Package w Ext. 1µF FDBK Capacitor		0.1	2000		MHz
S11	Differential Input Match, 100kHz to 1400MHz	De-Embedded to Package w Ext. 1µF FDBK Capacitor			–10		dB
S21	Forward Differential Power Gain, 100kHz to 400MHz	De-Embedded to Package w Ext. 1µF FDBK Capacitor			15.1		dB
S12	Reverse Differential Isolation, 100kHz to 4000MHz	De-Embedded to Package w Ext. 1µF FDBK Capacitor			–19		dB
S22	Differential Output Match, 100kHz to 1400MHz	De-Embedded to Package w Ext. 1µF FDBK Capacitor			–10		dB
Frequency = 100kHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			16.0		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			50.5 47		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			–97 –90		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–85		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–61		dBc
P1dB	Output 1dB Compression Point				22.5		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			6.6		dB
Frequency = 1MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			15.9		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			54.5 51		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			–105 –98		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–99.5		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–66.8		dBc
P1dB	Output 1dB Compression Point				22.5		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.9		dB
Frequency = 10MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			15.9		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			50.1 47		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			–96.2 –90		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–88.8		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–84		dBc
P1dB	Output 1dB Compression Point				22.7		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.6		dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_{CASE} = 30°C (Note 3). V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted, measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency = 50MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			15.9		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			48.0 45		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			–92 –86		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–85.5		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–90.5		dBc
P1dB	Output 1dB Compression Point				22.9		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			2.9		dB
Frequency = 150MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor	 ●	14.5 14.2	15.9	16.5 16.8	dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 8MHz, Z_O = 100Ω Grade A Grade B		47.0	50.3 47		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 8MHz, Z_O = 100Ω Grade A Grade B			–96.6 –90		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–92.2		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–86.5		dBc
P1dB	Output 1dB Compression Point				22.7		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.2		dB
Frequency = 240MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			15.8		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			45 42		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			–86 –80		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–93.7		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–81.5		dBc
P1dB	Output 1dB Compression Point				22.6		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.4		dB
Frequency = 300MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			15.8		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			43.5 40		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω Grade A Grade B			–83 –76		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–90.7		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–81.4		dBc
P1dB	Output 1dB Compression Point				22.5		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.6		dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_{CASE} = 30°C (Note 3). V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted, measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency = 500MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			15.4		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	Grade A Grade B		41 39		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	Grade A Grade B		–78 –74		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–82.9		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–67.4		dBc
P1dB	Output 1dB Compression Point				21.9		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.9		dB
Frequency = 1000MHz							
S21	Differential Power Gain	De-Embedded to Package w Ext. 1µF FDBK Capacitor			14.6		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	Grade A Grade B		36 33		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	Grade A Grade B		–68 –62		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–67.2		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–57.5		dBc
P1dB	Output 1dB Compression Point				19.2		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			4.8		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and characterization. This parameter is not tested.

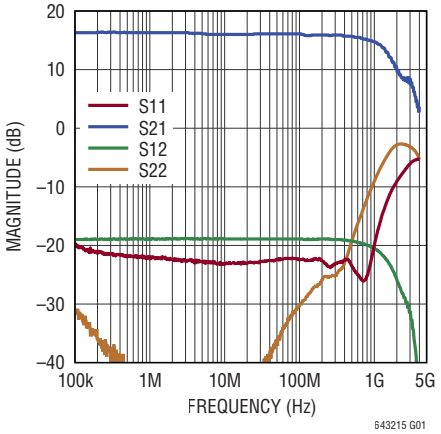
Note 3: The LTC6432-15 is guaranteed functional over the case operating temperature range of –40 C to 85°C.

Note 4: Small signal parameters S and Noise are de-embedded to the package pins, while large signal parameters are measured directly from the test circuit.

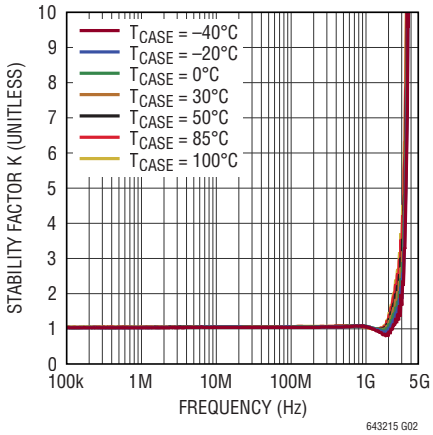
TYPICAL PERFORMANCE CHARACTERISTICS

T_{CASE} = 30°C, V_{CC} = 5V, Z_{IN} = Z_{OUT} = 100Ω Diff.
Unless otherwise noted, measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding.

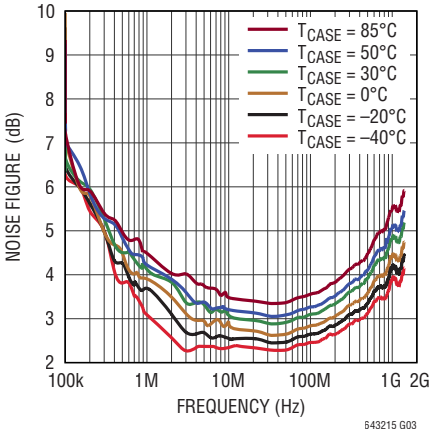
Differential S Parameters vs Frequency



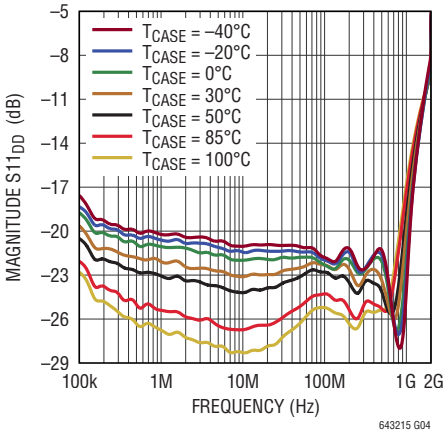
Differential Stability Factor K vs Frequency Over Temperature



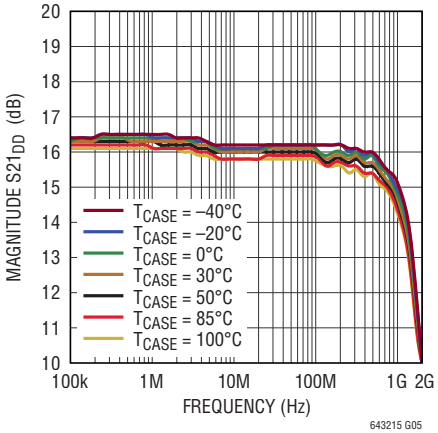
Differential Noise Figure vs Frequency Over Temperature



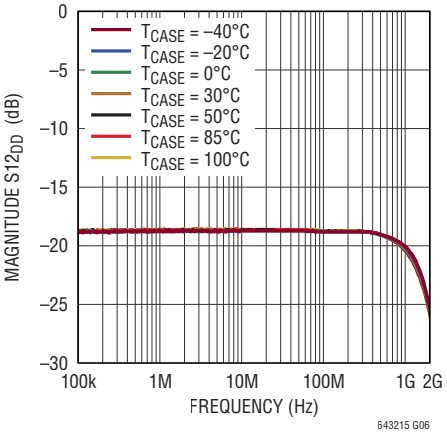
Differential Input match ($S11_{DD}$) vs Frequency Over Temperature



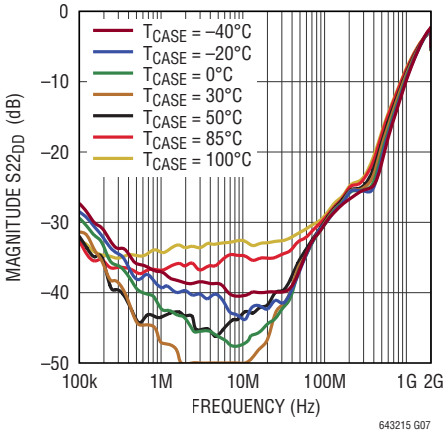
Differential Gain ($S21_{DD}$) vs Frequency Over Temperature



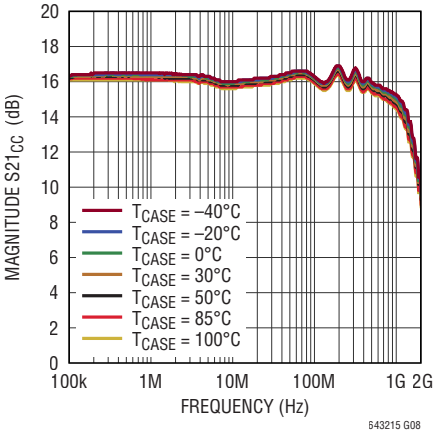
Differential Reverse Isolation ($S12_{DD}$) vs Frequency Over Temperature



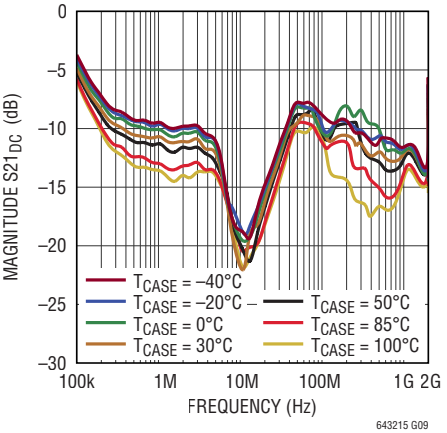
Differential Output Match ($S22_{DD}$) vs Frequency Over Temperature



Common Mode Gain ($S21_{CC}$) vs Frequency Over Temperature



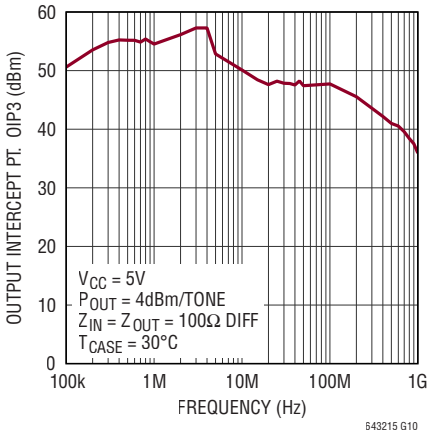
CM to DM Gain ($S21_{DC}$) vs Frequency Over Temperature



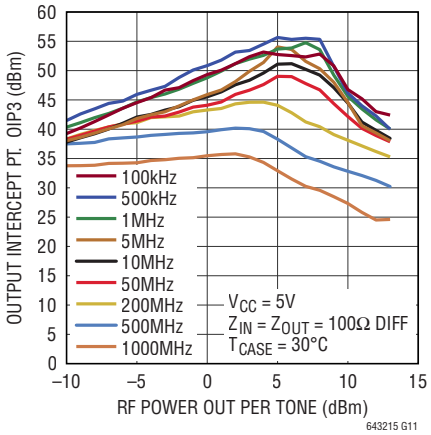
TYPICAL PERFORMANCE CHARACTERISTICS

T_{CASE} = 30°C, V_{CC} = 5V, Z_{IN} = Z_{OUT} = 100Ω Diff.
Unless otherwise noted, measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding.

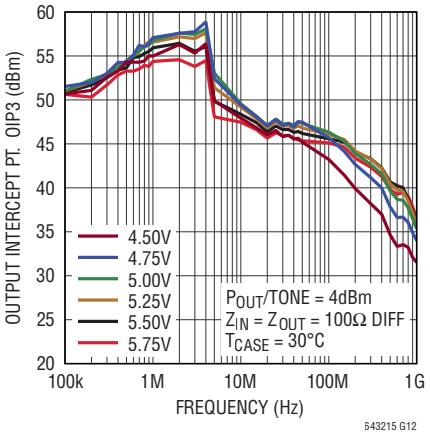
OIP3 vs Frequency



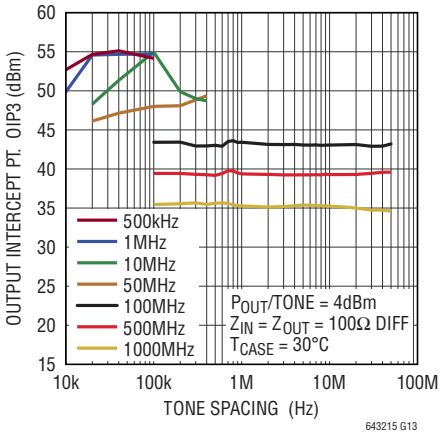
OIP3 vs RF Power Out/Tone Over Frequency



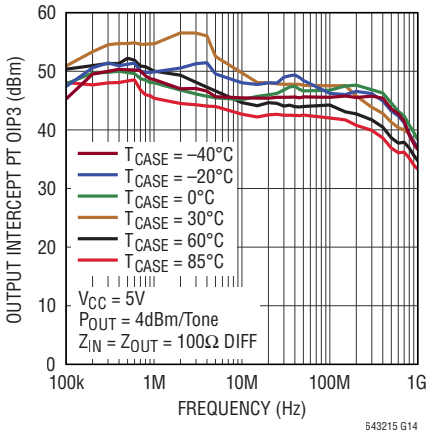
OIP3 vs Supply Voltage Over Frequency



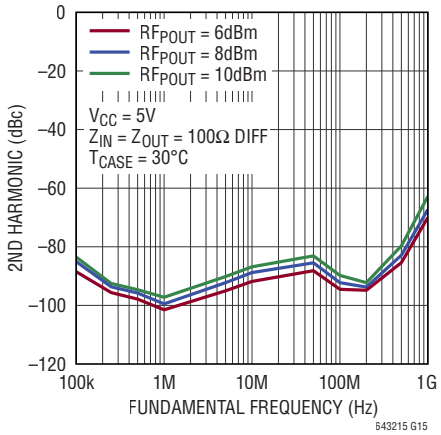
OIP3 vs Tone Spacing Over Frequency



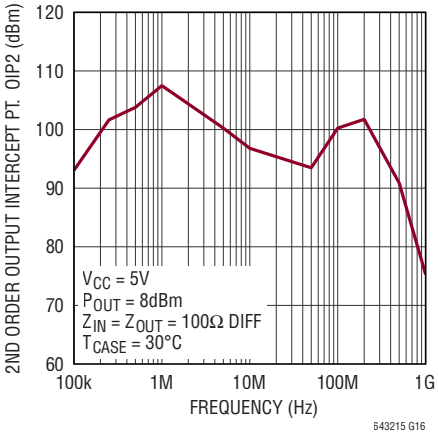
OIP3 vs Frequency Over Temperature



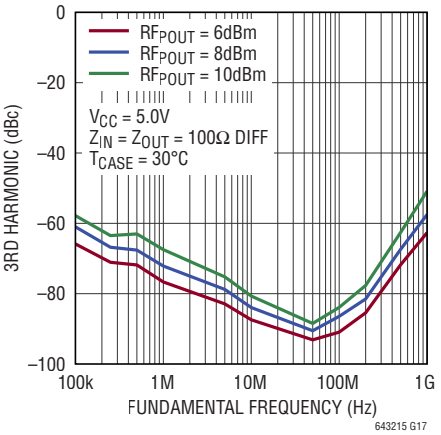
HD2 vs Frequency Over RF Power Out



OIP2 vs Frequency



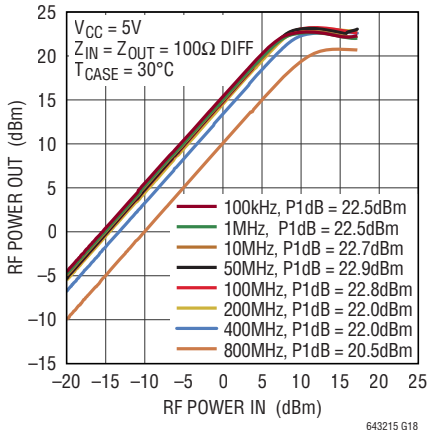
HD3 vs Frequency Over RF Power Out



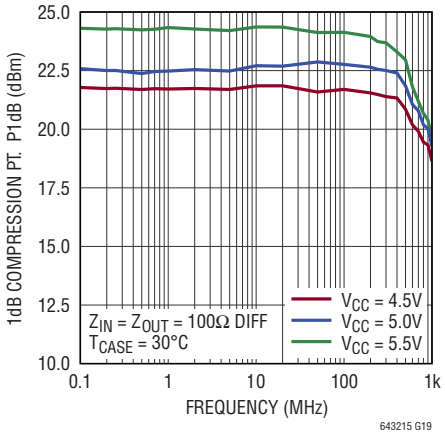
TYPICAL PERFORMANCE CHARACTERISTICS

T_{CASE} = 30°C, V_{CC} = 5V, Z_{IN} = Z_{OUT} = 100Ω Diff. Unless otherwise noted, measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding.

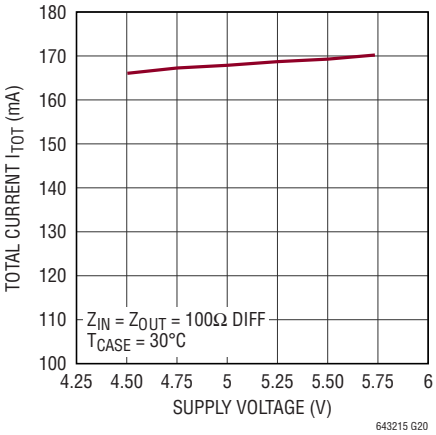
Output Power vs Input Power Over Frequency



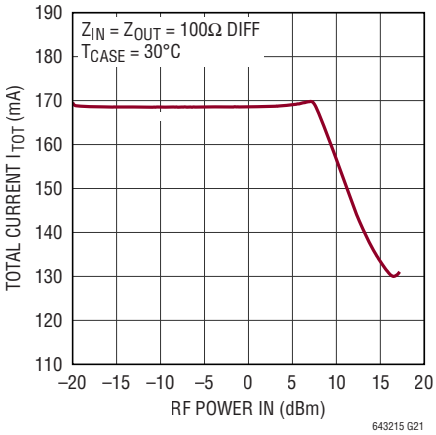
P1dB vs Frequency Over Supply Voltage



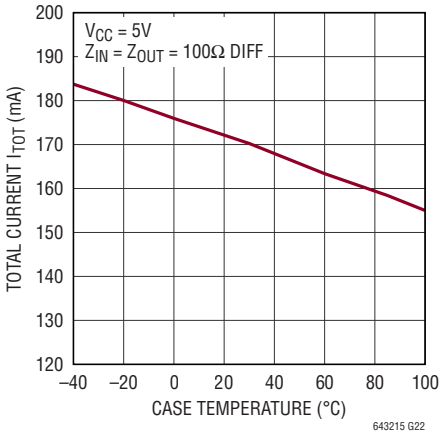
Total Current vs Supply Voltage



Total Current vs RF Power In



Total Current vs Temperature



PIN FUNCTIONS

DNC (Pins 1, 2, 3, 4, 10, 11, 14, 16, 20, 21): Do Not Connect. Do not connect to these pins, allow them to float. *Failure to float these pins may impair the performance of the LTC6432-15.*

NFILT2 (Pin 5): A 1µF capacitor to ground is required to reduce the low frequency noise of the internal bias supply.

NFILT1 (Pin 6): A 1µF capacitor to ground is required to reduce the low frequency noise of the internal bias supply.

–IN (Pin 7): Negative Signal Input Pin. This pin has an internally generated 2V DC bias. A DC blocking capacitor is required. See Application Information for specific recommendations.

GND (Pins 8, 17, 23 Exposed Pad Pin 25): Ground. For best RF performance, all ground pins should be connected to the printed circuit board ground plane. The Exposed Pad (Pin 25) should have multiple via holes to an underlying ground plane for low inductance and good thermal dissipation.

V_{CC} (Pins 9, 22): Positive Power Supply. Either or both V_{CC} pins should be connected to the 5V supply. Pins 9 and 22 are internally connected on chip. Bypass the V_{CC} Pin with 1000pF and 0.1µF capacitors. The 1000pF capacitor should be physically close to the V_{CC} Pin.

–FDBK (Pin 12): A 1µF capacitor is required between this pin and –OUT to extend the low frequency cutoff.

–OUT (Pin 13): Negative Amplifier Output Pin. A transformer with a center tap tied to V_{CC} or a choke inductor is required to provide DC current and RF isolation. For best performance select a choke with low loss and high Self Resonant Frequency (SRF). See Applications Information Section for more information.

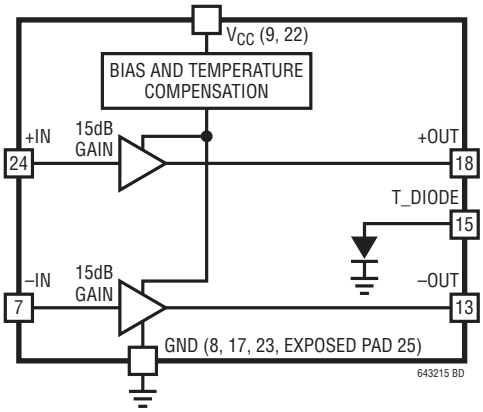
T_DIODE (Pin 15): Optional. A diode which can be forward biased to ground with up to 1mA of current. The measured voltage will be an indicator of the chip temperature.

+OUT (Pin 18): Positive Amplifier Output Pin. A transformer with a center tap tied to V_{CC} or a choke inductor tied to 5V supply is required to provide DC current and RF isolation. For best performance select a choke with low loss and high Self Resonant Frequency (SRF). See Applications Information Section for more information.

+FDBK (Pin 19): A 1µF capacitor is required between this pin and +OUT to extend the low frequency cutoff.

+IN (Pin 24): Positive Signal Input Pin. This pin has an internally generated 2V DC bias. A DC blocking capacitor is required. See Application Information Section for specific recommendations.

BLOCK DIAGRAM



TEST CIRCUIT A

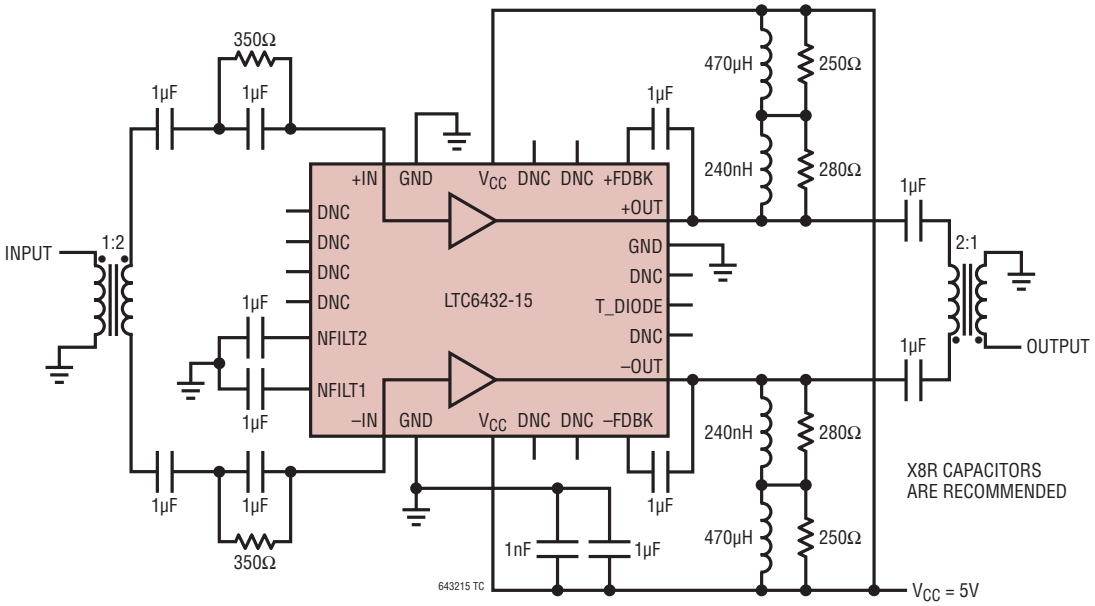


Figure 1. Differential Application Test Circuit A (Balanced Amp)

OPERATION

The LTC6432-15 is a highly linear, fixed gain differential amplifier. It can be considered a pair of 50Ω single-ended devices operating 180 degrees apart. Its core signal path consists of a single amplifier stage minimizing stability issues. The input is a Darlington pair for high input impedance and high current gain. Additional circuit enhancements increase the output impedance commensurate with the input impedance and minimize the effects of internal Miller capacitance.

The LTC6432-15 uses a classic RF gain block topology, with enhancements to achieve excellent linearity. Shunt and Series feedback elements are added to simultaneously lower the input/output impedance and match them to the 100Ω differential source and load. An internal bias controller optimizes the bias point for peak linearity over environmental changes. This circuit architecture provides low noise, good RF power handling capability and wide bandwidth; characteristics that are desirable for IF signal chain applications.

APPLICATIONS INFORMATION

The LTC6432-15 is a highly linear fixed gain amplifier designed for ease of use. Both the input and output are matched to 100Ω differential source and load impedance from 100kHz to 1000MHz using the specified evaluation circuit. Biasing and temperature compensation are also handled internally to deliver optimized performance. The designer need only supply input/output blocking caps, RF chokes, feedback caps, filter caps and decoupling caps for the 5V supply. However, because the device is capable of such wide band operation, a single application circuit will probably not result in optimized performance across the full frequency band.

Differential circuits minimize the common mode noise and 2nd harmonic distortion issues that plague many designs. The LTC6432's differential topology matches well with the differential inputs of an ADC. However, evaluation of these differential circuits is difficult, as high resolution, high frequency, differential test equipment is lacking.

Our test circuit is designed for evaluation with standard single-ended 50Ω test equipment. Therefore, 1:2 balun transformers have been added to the input and output to transform the LTC6432-15's 100Ω differential source/load impedance to 50Ω single-ended impedance, compatible with most test equipment.

Other than the balun, the evaluation circuit requires a minimum of external components. Input and output DC blocking caps are required as this device is internally biased for optimal operation. A frequency appropriate choke and decoupling caps provide DC bias to the RF ±OUT nodes. Only a single 5V supply is necessary to either of the V_{CC} pins on the device. Both V_{CC} pins are connected inside the package. Two V_{CC} pins are provided for the convenience of supply routing on the PCB. An optional parallel 1µF, 350Ω input network has been added to ensure low frequency stability.

The particular element values shown in Test Circuit A are chosen for wide bandwidth operation. Depending on the desired frequency, performance may be improved by proper selection of these supporting components.

Choosing the Right RF Choke

Not all choke inductors are created equal. It is always important to select an inductor with low R_{LOSS} as this will drop the available voltage to the device. Also look for an inductor with high self resonant frequency (SRF) as this will limit the upper frequency where the choke is useful. Above the SRF, the parasitic capacitance dominates and the choke's impedance will drop. For these reasons, wire wound inductors are preferred, while multilayer ceramic chip inductors should be avoided for an RF choke if possible. Since the LTC6432-15 is capable of such wideband operation, a single choke value will not result in optimized performance across its full frequency band. Table 1 list common frequency bands and suggested corresponding inductor values

APPLICATIONS INFORMATION

Table 1. Target Frequency and Suggested Inductor Values

FREQUENCY BAND (MHz)	INDUCTOR VALUE (H)	SRF (MHz)	MODEL NUMBER	MANUFACTURER
0.1 to 20	470µH	4	LPS5030	Coilcraft www.coilcraft.com
20 to 100	1500nH	100	0603LS	
100 to 500	560nH	525	0603LS	
500 to 1000	100nH	1150	0603LS	

Designing a Wideband Output Network

Often a single choke will not work over a wide bandwidth due to a low SRF or low inductance value. Using multiple choke stages, it is possible to extend the frequency range of the output network. This is best done using a circuit simulator and S parameters provided by the inductor manufacturer or measured by the user. Please refer to the output network in Figure 1 Test circuit A. Starting at OUT we connect two chokes in series, a 240nH RF choke and follow that with a 470µH choke to provide high AC impedance at 100kHz. It is important to place the lower valued (higher SRF) choke closer to the signal line for best performance. De-Qing resistors 250Ω and 280Ω respectively have been placed in parallel with the chokes. This flattens the loss of the output network and gives an overall flat gain response for the amplifier application circuit. With proper care selecting chokes, wideband performance is possible. In this case circuit A works over 13 octaves.

DC Blocking Capacitor

The role of a DC blocking capacitor is straightforward: block the path of DC current and allow a low series impedance path for the AC signal. Lower frequencies require a higher value of DC blocking capacitance. Generally, 1µF will suffice for operation down to 100kHz.

RF Bypass Capacitor

RF bypass capacitors act to shunt the AC signals to ground with a low impedance path. They prevent the AC signal from getting into the DC bias supply. It is best to place the bypass capacitor as close as possible to the DC supply pins of the amplifier. Any extra distance translates into additional series inductance which lowers the effectiveness of the bypass capacitor network. The suggested bypass capacitor network consists of two capacitors; a low value 1000pF capacitor to shunt high frequencies and a larger 1µF capacitor to handle lower frequencies. Use ceramic capacitors of appropriate physical size for each capacitance value (e.g. 0402 for the 1000pF, 0805 for the 0.1µF) to minimize the equivalent series resistance (ESR) of the capacitor.

High Valued Capacitors and Linearity degradation

One might not expect a passive element to create signal distortions. However, high value capacitors can create nonlinear responses at frequencies below 1MHz. Typically lower quality materials are used to create high density capacitors. High quality NPO and film capacitors have low capacitance density and become unmanageably large at 1µF values. Typical low quality capacitors have high voltage coefficients that deviate from their expected linear response, creating IM products and harmonics. We have found that automotive grade X8R capacitors have reasonable voltage coefficients at high capacitance densities and will not degrade the linearity of the LTC6432-15. We highly suggest their use in the 6 DC blocking capacitors and the 2 feedback capacitors shown in the application circuit.

Low Frequency Stability

Most RF gain blocks suffer from low frequency instability. To avoid stability issues, the LTC6432-15, contains an on-chip feedback network that lowers the gain and matches the input and output impedance of the intrinsic amplifier. This feedback network contains a series capacitor, whose value is limited by physical size. So at some low frequency, this feedback capacitor looks like an open circuit; the feedback fails, gain increases and gross impedance mismatches occur which can create instability. This situation is easily resolved with a parallel capacitor and a resistor network on the input. This is shown in Figure 1. This network provides resistive loss at low frequencies and is bypassed by the capacitor at the desired band of operation. However, if the LTC6432-15 is preceded by a low frequency termination such as a choke or balun transformer, the input stability network is not required.

APPLICATIONS INFORMATION

Exposed Pad and Ground Plane Considerations

As with any RF device, minimizing the ground inductance is critical. Care should be taken with PC board layouts using exposed pad packages, as the exposed pad provides the lowest inductive path to ground. The maximum allowable number of minimum diameter via holes should be placed underneath the exposed pad and connect to as many ground plane layers as possible. This will provide good RF ground and low thermal impedance. Maximizing the copper ground plane at the signal and microstrip ground will also improve the heat spreading and lower inductance. It is a good idea to cover the via holes with solder mask on the backside of the PCB to prevent the solder from wicking away from the critical PCB to exposed pad interface. One to two ounces of copper plating is suggested to improve heat spreading from the device.

Frequency limitations

The LTC6432-15 is a wide bandwidth amplifier but it is not intended for operation down to DC. The lower frequency cutoff is limited by on-chip matching elements. The cutoff may be arbitrarily pushed lower with off chip elements. However, the translation between the low fixed DC common mode input voltage and the higher open collector DC common mode output bias point make DC-coupled operation impractical.

Test Circuit A

Test Circuit A shown in Figure 1 is designed to allow for the evaluation of the LTC6432-15 with standard single-ended 50Ω test equipment. This allows the designer to verify the performance when the device is operated differentially. This evaluation circuit requires a minimum of external components. Since the LTC6432-15 operates over a very wide bandwidth, the evaluation test circuit is optimized for wideband operation. Obviously, for narrowband operation, the circuit can be further optimized.

Input and output DC blocking capacitors are required, as this device is internally DC biased for optimal performance. A frequency appropriate choke and decoupling capacitors are required to provide DC bias to the RF output nodes (+OUT and –OUT). A 5V supply should also be applied to one of the V_{CC} pins on the device. Two noise filtering capacitors should be tied to ground at NFILT1 and NFILT2 to suppress noise below 20MHz. In addition 1µF capacitors should be tied between +FDBK and +OUT and between –FDBK and –OUT to provide impedance matching below 20MHz.

Components for a suggested parallel 1µF, 350Ω stability network have been added to ensure low frequency stability. The 1µF capacitance can be increased to improve low frequency (<100kHz) performance, however the designer needs to be sure that the impedance presented at low frequency will not create an instability.

As mentioned earlier, the LTC6432-15 is extremely wideband. Its bandwidth is most often limited by the passive components surrounding it. The DC2496A evaluation board has provisions to allow characterization over the full bandwidth of the LTC6432-15 by substituting baluns and output networks. This balanced amplifier circuit is a replica of the Test Circuit A. It is useful for single-ended 50Ω amplifier requirements and is surprisingly wide band. Using this balanced arrangement and the frequency appropriate baluns, one can achieve the intermodulation and harmonic performance listed in the AC Electrical Characteristics of this data sheet. Besides its impressive intermodulation performance; the LTC6432-15 has impressive 2nd harmonic suppression as well. This makes it particularly well suited for multi-octave applications where the 2nd harmonic cannot be filtered.

This balanced circuit example uses two mini-circuits 1:2 baluns. The baluns were chosen for their bandwidth and frequency options. See Table 2. A pair of these baluns, back to back has less than 1.5dB of loss, so the penalty for this level of performance is minimal. Any 1:2 balun may be used to create a balanced amplifier with the LTC6432-15, but one must be careful that the balun does not degrade the linearity of the circuit.

The optional input stability network is only required when the balun's bandwidth reaches below 100kHz. It is included in the circuit as a comprehensive protection for any passive element placed at the LTC6432-15 input. Its performance degradation at low frequencies can be mitigated by increasing the 1µF capacitor's value.

APPLICATIONS INFORMATION

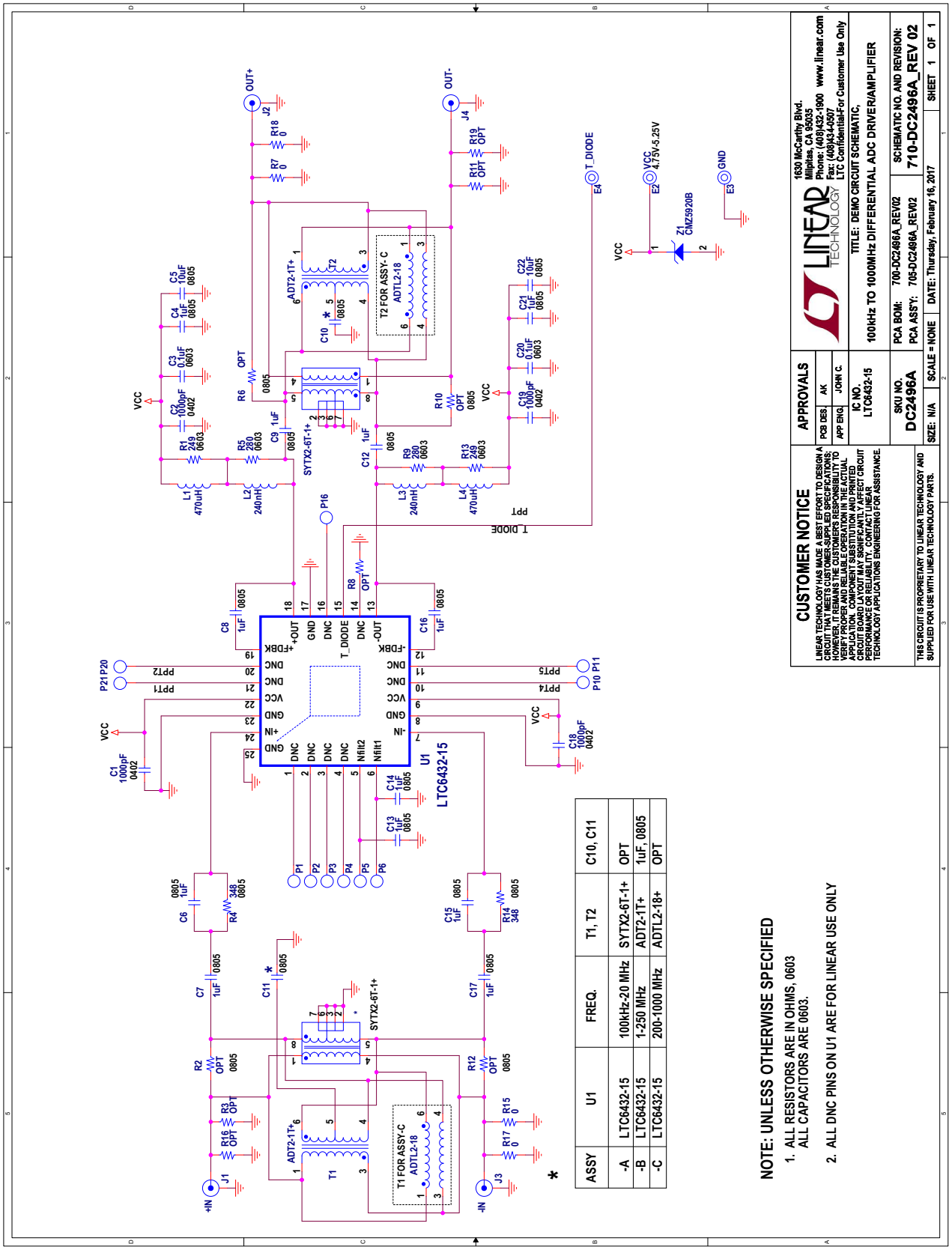


Figure 2. DC2496A Balanced Amplifier Circuit – 50Ω Input and 50Ω Output

APPLICATIONS INFORMATION

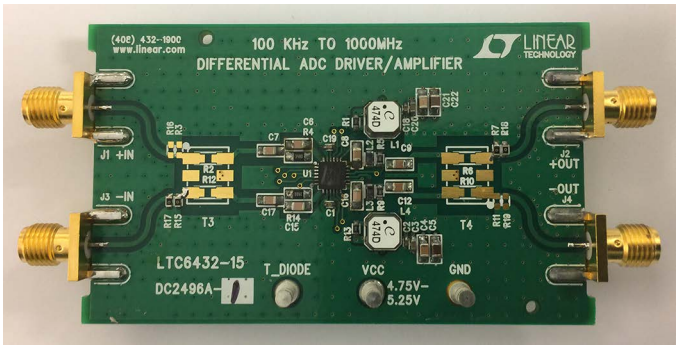


Figure 3. DC2496A Topside No Baluns Installed

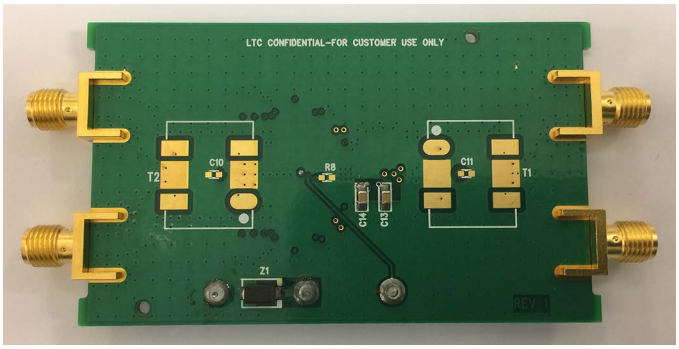


Figure 4. DC2496A Backside No Baluns Installed

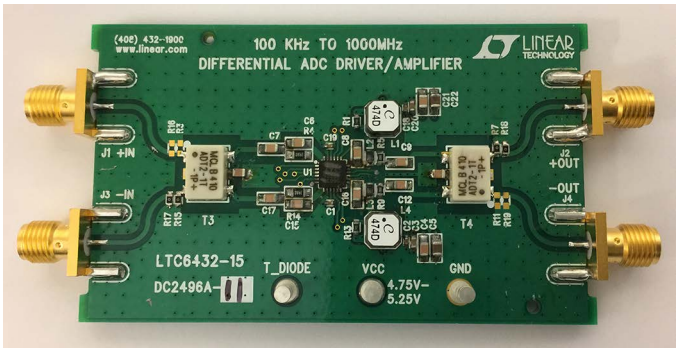


Figure 5. DC2496A Topside with Balun Installed

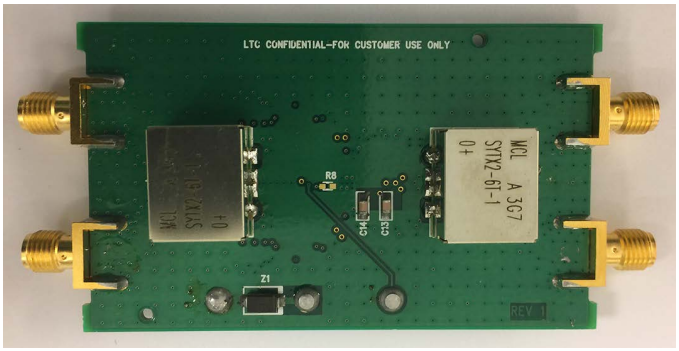


Figure 6. DC2496A Backside with Baluns Installed

Table 2. Target Frequency and Suggested 2:1 Balun

FREQUENCY BAND (MHz)	MODEL NUMBER	MANUFACTURER
0.1 to 20	SYTX2-6T-1+	Mini-Circuits www.minicircuits.com
1 to 250	ADT2-1T+	
20 to 400	ADT2-IT-1P+	
200 to 950	ADTL2-18+	

The DC2496A is designed for versatility to cover a wide range of applications. There are provisions for baluns on both the topside and backside of the DC2496A PCB. Please see Figures 3 through 6 for details. The smaller footprint ADTX2-X baluns can be mounted on the front while the larger SYTX2-6T balun can be mounted on the back. Table 2 lists the recommended Balun for each frequency range. Alternatively, the circuit can be operated differentially by using zero ohm jumpers across T3 and T4.

The plots below show the resulting small signal performance for each balun choice. More detailed results and operation details can be found in the DC2496A Quick Start Guide.

The LTC6432-15's differential output and high linearity make it the ideal solution to drive the demanding differential inputs of a high resolution ADC. In Figure 11 we show suggested circuit to drive an ADC. Both input and output are AC-coupled. A 1:2 Balun has been inserted at the input allowing a single-ended 50Ω input. The output impedance is 100Ω differential. However, a 1:1 Balun has been added to the output to suppress common mode signals. This is followed by a low pass filter to limit the noise presented to the ADC.

APPLICATIONS INFORMATION

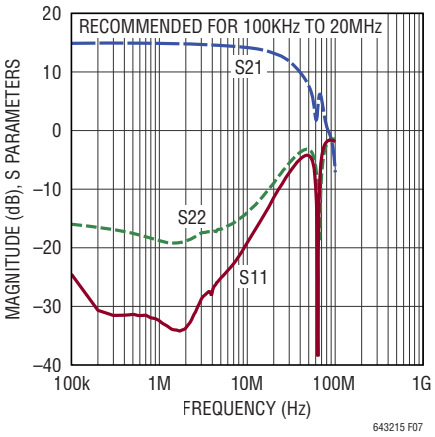


Figure 7. DC2496A with SYTX2 Baluns

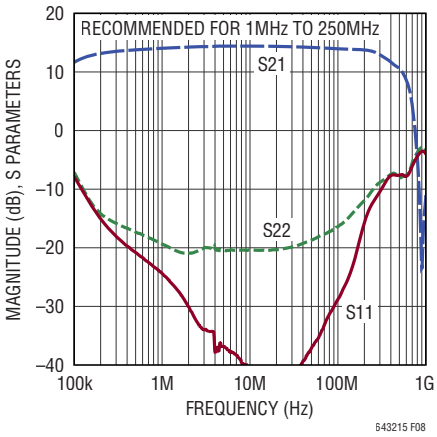


Figure 8. DC2496A with ADT2-1T Baluns

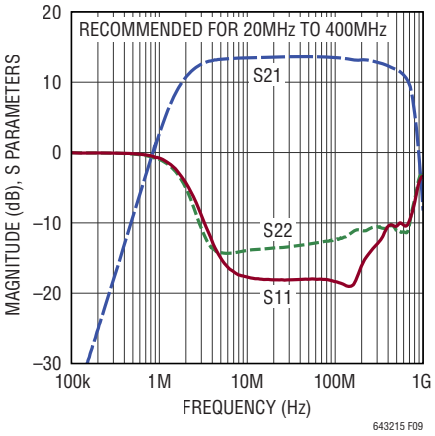


Figure 9. DC2496A with ADT2-1T-1P Baluns

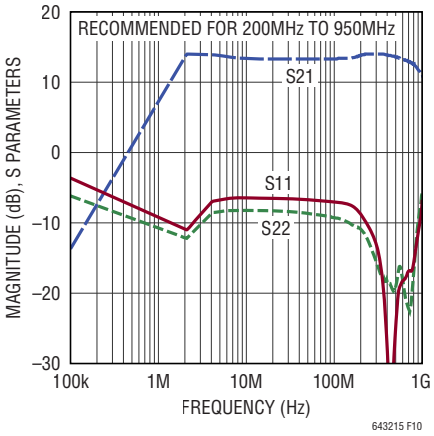


Figure 10. DC2496A with ADTL2-18 Baluns

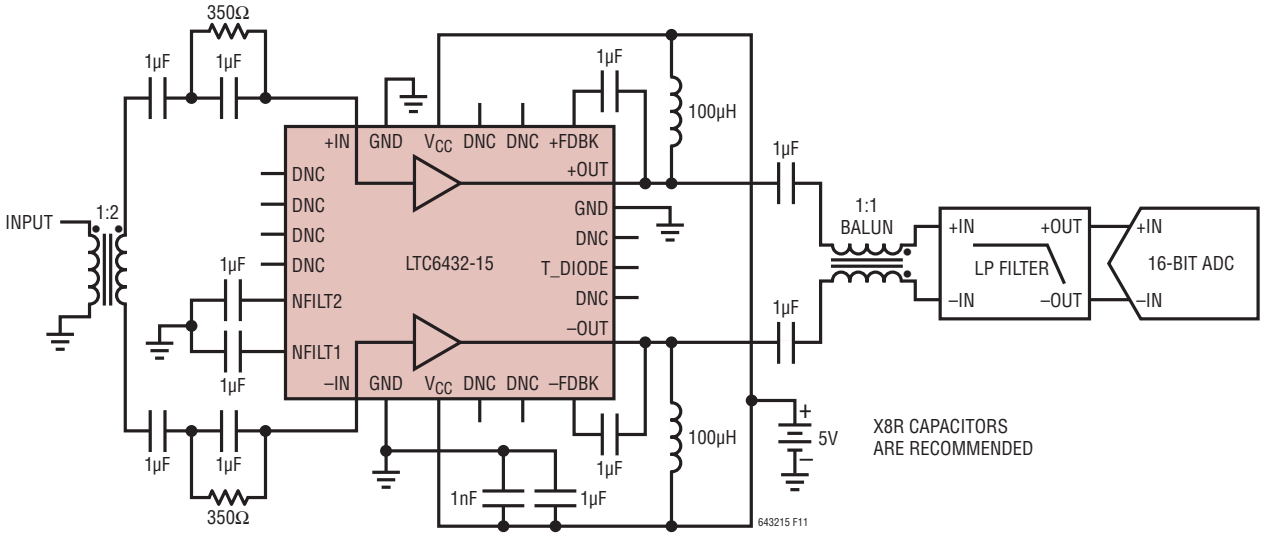


Figure 11

DIFFERENTIAL S PARAMETERS

5V, Z_{DIFF} = 100Ω, T_{CASE} = 30°C, de-embedded to package pins, 1µF capacitor +FDBK to OUT^+ and 1µF capacitor –FDBK to OUT^- DD: Differential in to differential out.

FREQUENCY (Hz)	$S11_{DD}$ (Mag)	$S11_{DD}$ (Ph)	$S21_{DD}$ (Mag)	$S21_{DD}$ (Ph)	$S12_{DD}$ (Mag)	$S12_{DD}$ (Ph)	$S22_{DD}$ (Mag)	$S22_{DD}$ (Ph)	GTU (Max)	STABILITY (k)
1.00E+05	–24.65	213.98	16.01	181.44	–18.97	1.08	–33.32	108.18	16.03	1.05
1.16E+05	–24.79	207.23	16.02	181.17	–18.89	1.05	–33.33	111.81	16.04	1.05
1.32E+05	–25.2	204.3	16.01	180.97	–18.89	1.53	–35.44	114.82	16.03	1.05
1.53E+05	–25.39	202.21	16.02	180.79	–18.74	1.31	–35.78	107.24	16.03	1.05
1.75E+05	–25.57	196.89	16	180.63	–18.97	2.09	–35.36	105.24	16.02	1.06
2.00E+05	–25.79	195.49	16.01	180.6	–18.86	1.12	–36.06	105.2	16.02	1.05
2.31E+05	–26.17	190.78	16	180.36	–18.92	1.28	–39.79	108.96	16.01	1.05
2.62E+05	–25.82	190.86	16	180.36	–18.94	0.73	–39.71	110.15	16.01	1.06
3.05E+05	–25.98	190.11	16.01	180.23	–18.85	0.79	–38.61	109.37	16.02	1.05
3.47E+05	–26.23	190.65	15.99	180.21	–18.98	0.85	–40.21	103.4	16	1.06
4.01E+05	–26.45	185.6	16	180.09	–18.84	0.86	–42.42	119.95	16.01	1.05
4.59E+05	–26.45	188.23	16	179.95	–18.91	0.84	–39.93	116.1	16.01	1.05
5.25E+05	–26.58	185.06	15.98	179.99	–18.79	–0.13	–41.67	99.54	15.99	1.05
6.06E+05	–26.29	183.94	15.98	179.93	–18.77	0.66	–46.44	115.06	15.99	1.05
6.88E+05	–26.23	181.89	15.98	179.89	–18.91	0.03	–42.61	121.63	15.99	1.06
7.99E+05	–26.37	181.41	15.98	179.92	–18.98	0.55	–43.66	121.57	15.99	1.06
9.10E+05	–26.08	180.72	15.97	179.86	–18.92	0.1	–43.9	107.29	15.98	1.06
1.05E+06	–26.42	180.43	15.96	179.75	–18.81	0.74	–44.98	111.22	15.97	1.05
1.20E+06	–26.64	182.6	15.96	179.82	–18.87	1.49	–48.41	89.98	15.97	1.06
1.38E+06	–26.64	179.74	15.96	179.8	–18.92	0.32	–45.69	70.77	15.97	1.06
1.59E+06	–26.27	180.38	15.96	179.62	–18.99	0.92	–46.98	70.78	15.97	1.06
1.80E+06	–26.84	178.66	15.94	179.67	–18.81	0.58	–46.36	39.09	15.95	1.05
2.10E+06	–27.03	179.86	15.94	179.66	–18.83	–0.31	–47.02	79.31	15.95	1.05
2.39E+06	–26.96	179.61	15.95	179.56	–18.68	0.06	–48.54	104.5	15.96	1.05
2.76E+06	–26.59	176.02	15.93	179.6	–18.82	–0.07	–45.61	39.58	15.94	1.05
3.16E+06	–27.18	175.48	15.95	179.52	–18.82	0.47	–50.75	6.16	15.95	1.05
3.62E+06	–27.27	176.96	15.93	179.52	–18.88	–1.04	–51.57	45.5	15.94	1.06
4.17E+06	–27.17	180.85	15.92	179.31	–18.78	–0.91	–47.24	56.08	15.93	1.05
4.73E+06	–27.01	177.52	15.93	179.38	–18.85	0.12	–51.03	–31.55	15.93	1.06
5.50E+06	–27.27	176.8	15.91	179.34	–18.87	0.02	–55.12	2.13	15.92	1.06
6.26E+06	–27.18	178.74	15.92	179.25	–18.75	–0.77	–63.87	–30.58	15.93	1.05
7.23E+06	–26.73	178.6	15.92	179.23	–18.89	–1.44	–50.17	–9.92	15.92	1.06
8.29E+06	–27.28	178.11	15.91	179.03	–18.78	–0.48	–51.41	12.11	15.92	1.05
9.48E+06	–27.26	179.63	15.92	179.01	–18.88	–0.56	–52.35	–41.82	15.93	1.06
1.09E+07	–27.26	179.73	15.91	178.89	–18.86	–0.95	–49.86	–24.68	15.92	1.06
1.24E+07	–27.21	180.03	15.92	178.77	–18.88	–1	–50.43	–51.11	15.92	1.06
1.44E+07	–27.13	181.01	15.91	178.58	–18.88	–1.13	–48.02	–52.74	15.92	1.06
1.64E+07	–27.37	179.77	15.91	178.43	–18.87	–1.23	–45.4	–49.5	15.92	1.06
1.90E+07	–27.4	180.64	15.91	178.21	–18.87	–1.36	–44.79	–59.22	15.91	1.06

DIFFERENTIAL S PARAMETERS

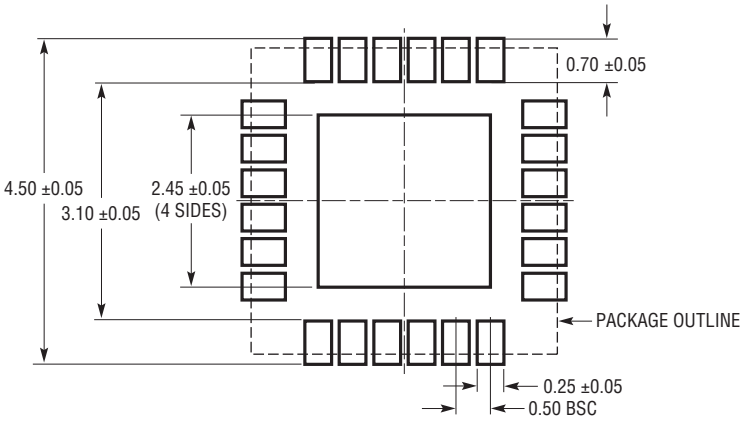
5V, Z_{DIFF} = 100Ω, T_{CASE} = 30°C, de-embedded to package pins, 1µF capacitor +FDBK to OUT^+ and 1µF capacitor –FDBK to OUT^- DD: Differential in to differential out.

FREQUENCY (MHz)	$S11_{DD}$ (Mag)	$S11_{DD}$ (Ph)	$S21_{DD}$ (Mag)	$S21_{DD}$ (Ph)	$S12_{DD}$ (Mag)	$S12_{DD}$ (Ph)	$S22_{DD}$ (Mag)	$S22_{DD}$ (Ph)	GTU (Max)	STABILITY (k)
2.17E+07	–27.32	181.3	15.9	177.93	–18.88	–1.67	–42.22	–52.54	15.91	1.06
2.49E+07	–27.12	181.43	15.9	177.69	–18.85	–1.99	–41.72	–64.62	15.91	1.06
2.87E+07	–26.96	181.05	15.9	177.36	–18.86	–2.43	–40.84	–61.81	15.91	1.06
3.26E+07	–27.24	182.44	15.89	177.04	–18.86	–2.53	–39.61	–70.18	15.9	1.06
3.78E+07	–26.86	183.1	15.89	176.6	–18.89	–3.1	–38.18	–68.88	15.9	1.06
4.31E+07	–26.76	182.65	15.9	176.13	–18.86	–3.54	–37.65	–74.32	15.91	1.06
4.98E+07	–26.62	181.26	15.89	175.61	–18.91	–3.78	–35.95	–76.76	15.9	1.06
5.70E+07	–26.75	181.06	15.89	175	–18.91	–4.63	–34.6	–83.01	15.9	1.06
6.52E+07	–26.95	182.92	15.9	174.31	–18.9	–5.13	–33.59	–87.34	15.91	1.06
7.53E+07	–26.88	179.75	15.9	173.46	–18.92	–6.03	–32.99	–86.88	15.91	1.06
8.54E+07	–26.47	180.29	15.9	172.59	–18.95	–6.61	–31.62	–89.71	15.91	1.06
9.92E+07	–26.82	179.69	15.91	171.39	–18.92	–7.57	–30.3	–97.21	15.92	1.06
1.13E+08	–26.63	178.99	15.92	170.17	–18.95	–8.7	–29.22	–95.47	15.93	1.06
1.31E+08	–26.88	176.87	15.92	168.6	–18.96	–9.88	–28.31	–100.54	15.94	1.06
1.50E+08	–26.83	177.15	15.94	166.88	–18.96	–11.16	–27.4	–104.6	15.95	1.06
1.71E+08	–27	176.62	15.95	164.91	–18.96	–13.01	–26.82	–107.66	15.97	1.06
1.97E+08	–27.59	176.01	15.96	162.38	–18.96	–14.59	–26.14	–110.04	15.97	1.06
2.24E+08	–27.5	179.18	15.96	159.78	–18.94	–16.96	–25.69	–111.52	15.98	1.05
2.60E+08	–27.45	180.64	15.93	156.29	–18.97	–19.81	–25.41	–112.18	15.95	1.06
2.96E+08	–27.43	181.86	15.88	152.81	–18.97	–22.79	–24.98	–108.99	15.9	1.06
3.42E+08	–27	182.3	15.8	148.49	–19	–26.46	–24.35	–103.45	15.82	1.06
3.92E+08	–26.74	180.54	15.7	144	–19.06	–30.32	–22.82	–96.37	15.73	1.07
4.49E+08	–26.64	178.86	15.59	139.1	–19.17	–34.98	–20.83	–92.76	15.64	1.07
5.18E+08	–27.17	178.07	15.46	133.25	–19.27	–39.99	–18.56	–92.28	15.53	1.08
5.88E+08	–27.89	179.84	15.37	127.38	–19.43	–45.32	–16.49	–94.9	15.48	1.09
6.82E+08	–28.41	192.17	15.23	119.35	–19.65	–52.66	–14.25	–100.15	15.4	1.09
7.77E+08	–27.7	208.65	15.07	111.07	–19.84	–59.66	–12.39	–106.24	15.34	1.09
8.98E+08	–24.34	220.03	14.89	100.45	–20.16	–68.72	–10.43	–114.78	15.32	1.09
1.03E+09	–20.91	217.95	14.59	89.13	–20.53	–78.35	–8.69	–124.05	15.25	1.07
1.18E+09	–17.61	208.58	14.14	75.71	–21.11	–89.5	–7.1	–134.83	15.16	1.05
1.36E+09	–14.62	192.85	13.4	59.47	–21.9	–103.24	–5.56	–148.41	14.96	1.02
1.54E+09	–12.38	175.97	12.41	45.07	–22.92	–115.67	–4.41	–161.86	14.63	1.01
1.79E+09	–10.26	150.16	11.29	29.07	–24.47	–130.06	–3.34	179.45	14.42	1.01
2.04E+09	–8.89	126.71	10.6	12.81	–25.73	–143.95	–2.83	161.69	14.4	1.02
2.36E+09	–7.68	98.74	9.25	354.9	–27.3	–157.95	–2.67	139.37	13.44	1.28
2.70E+09	–6.66	71.35	8.02	336.79	–29.27	–174.25	–2.8	116.2	12.31	1.86
3.09E+09	–5.78	43.7	7.98	310.66	–30.89	166.1	–3.19	92.85	12.16	2.35
3.56E+09	–5.28	15	5.73	281.01	–34.09	137.29	–3.99	66.89	9.47	5.21

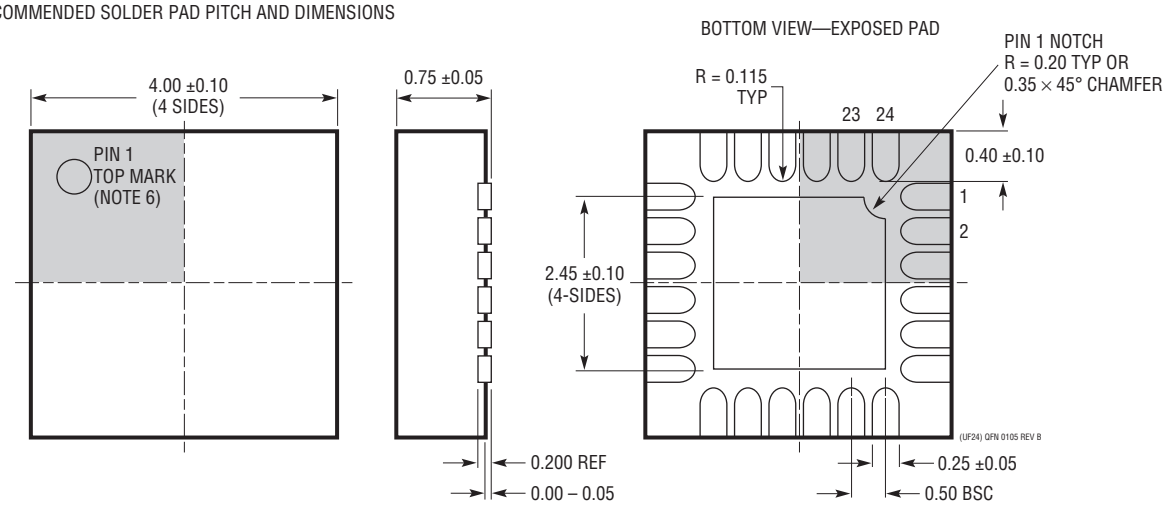
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6432-15#packaging for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE