Low Frequency to 1.4GHz 50Ω Gain Block IF Amplifier

FEATURES

- **Low Frequency to 1.4GHz Bandwidth**
- **100kHz to 1GHz Flat Gain from a Single Demo Circuit**
- **Low Frequency Cutoff Is User Defined**
- **15.9dB Power Gain**
- **52dBm OIP3 at 1MHz**
- **47dBm OIP3 at 150MHz**
- **NF = 3.22dB at 150MHz**
- **1nV/√Hz Total Input Noise Density at 150MHz**
- **S11 < –10dB Up to 1.2GHz**
- **S22 < –10dB Up to 1.0GHz**
- **>2V$_{P-P}$ Linear Output Swing**
- **P1dB =19.2dBm**
- **DC Power = 475mW**
- 50Ω Single-Ended Operation
- Insensitive to V_{CC} Variation
- A-Grade 100% OIP3 Tested at 150MHz
- Input/Output Internally Matched to 50Ω
- Single 5V Supply
- Unconditionally Stable

APPLICATIONS

- Single-Ended IF Amplifier
- ADC Driver
- CATV
- Test Equipment

DESCRIPTION

The LTC®6433-15 is a gain-block amplifier with excellent linearity at frequencies below 100kHz to beyond 1000MHz and with low associated output noise.

The unique combination of high linearity, low noise and low power dissipation makes this an ideal candidate for many signal-chain applications. The LTC6433-15 is easy to use, requiring a minimum of external components. It is internally input/output matched to 50Ω and it draws only 95mA from a single 5V supply.

The LTC6433-15 operates over a wide bandwidth. A single demonstration circuit offers flat gain from 100kHz to 1GHz.

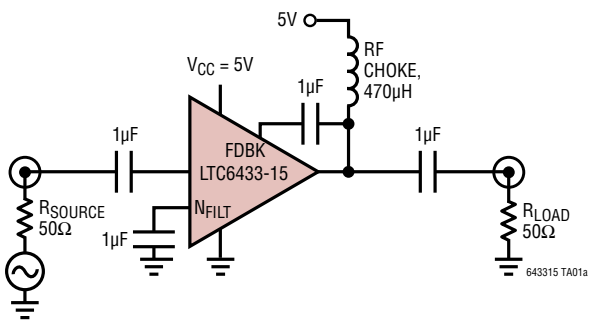
While this device is not capable of DC coupled operation, users can define the low frequency cut-off by appropriate choice of external components.

On-chip bias and temperature compensation maintain performance over environmental changes.

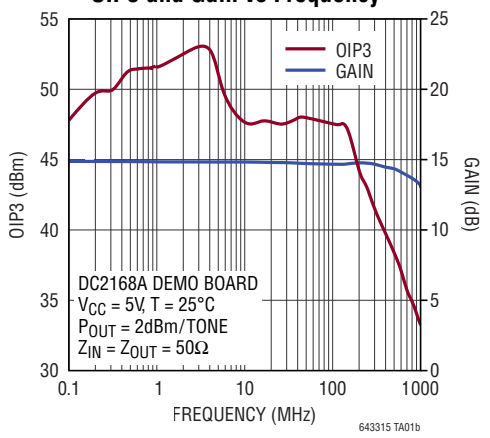
The LTC6433-15 uses a high performance SiGe BiCMOS process for excellent repeatability compared with similar GaAs amplifiers. All A-grade LTC6433-15 devices are tested and guaranteed for OIP3 at 150MHz. The LTC6433-15 is housed in a 4mm × 4mm 24-lead QFN package with an exposed pad for thermal management and low inductance.

TYPICAL APPLICATION

Single-Ended IF Amplifier



OIP3 and Gain vs Frequency

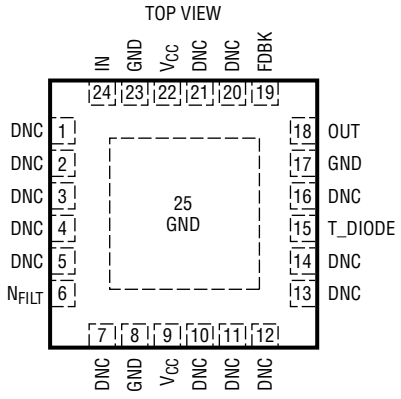


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC} to GND).....5.5V
Amplifier Output Current (OUT) 115mA
RF Input Power, Continuous, 50Ω (Note 2).....15dBm
RF Input Power, 100µs Pulse, 50Ω (Note 2) 20dBm
Operating Case Temperature
Range (T_{CASE}).....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Junction Temperature (T_J) ..... 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 44°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC6433-15#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6433AIUF-15#PBF	LTC6433AIUF-15#TRPBF	43315	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC6433BIUF-15#PBF	LTC6433BIUF-15#TRPBF	43315	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω. Typical measured DC electrical performance using Test Circuit A.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Operating Supply Range			4.75	5.0	5.25	V
$I_{S,TOT}$	Total Supply Current	All V_{CC} Pins Plus OUT	 ●	75 67	95	106 112	mA mA
$I_{S,OUT}$	Total Supply Current to OUT Pin	Current to OUT	 ●	62 55	82	92 95	mA mA
$I_{CC,OUT}$	Current to V_{CC} Pin	Either V_{CC} Pin May Be Used	 ●	12 12.5	13	16 17.5	mA mA
V_{DIODE}	Temperature Diode Voltage	T_Diode Current = 1mA			0.85		V
T_C	Diode Temperature Coefficient				1.4		mV/°C

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C (Note 3), V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Small Signal							
BW	–3dB Bandwidth	De-Embedded to Package (Low Frequency is User Defined)			2000		MHz
S11	Input Return Loss, 100kHz to 1700MHz	De-Embedded to Package			–10		dB
S21	Forward Power Gain, 100kHz to 300MHz	De-Embedded to Package			15.8		dB
S12	Reverse Isolation, 100kHz to 3000MHz	De-Embedded to Package			–19		dB
S22	Output Return Loss, 100kHz to 1000MHz	De-Embedded to Package			–10		dB
Frequency = 100kHz							
S21	Power Gain	De-Embedded to Package			16.0		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		47.8 46.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–91.6 –88.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–65.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–70.0		dBc
P1dB	Output 1dB Compression Point				19.2		dBm
NF	Noise Figure	De-Embedded to Package			6.67		dB
Frequency = 1MHz							
S21	Power Gain	De-Embedded to Package			16.0		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		52.0 49.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–100 –94.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–73.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–81.0		dBc
P1dB	Output 1dB Compression Point				19.1		dBm
NF	Noise Figure	De-Embedded to Package			3.93		dB
Frequency = 10MHz							
S21	Power Gain	De-Embedded to Package			15.9		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 8MHz	A-Grade B-Grade		47.6 45.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 8MHz	A-Grade B-Grade		–91.2 –87.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–54.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–77.0		dBc
P1dB	Output 1dB Compression Point				19.3		dBm
NF	Noise Figure	De-Embedded to Package			3.65		dB

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C (Note 3), V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Frequency = 50MHz								
S21	Power Gain	De-Embedded to Package				15.9		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			48.0 46.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–92.0 –88.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–56.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–84.0		dBc
P1dB	Output 1dB Compression Point					19.3		dBm
NF	Noise Figure	De-Embedded to Package				2.92		dB
Frequency = 100MHz								
S21	Power Gain	De-Embedded to Package				15.9		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			47.5 45.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–91.0 –87.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–55.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–80.0		dBc
P1dB	Output 1dB Compression Point					19.2		dBm
NF	Noise Figure	De-Embedded to Package				3.10		dB
Frequency = 150MHz								
S21	Power Gain	De-Embedded to Package		 ●	14.5 14.25	15.9	16.5 16.75	dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		43.0	47.2 45.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–82.0	–90.4 –86.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–54.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–78.0		dBc
P1dB	Output 1dB Compression Point					19.2		dBm
NF	Noise Figure	De-Embedded to Package				3.22		dB
e_n	Noise Density	Input Referred				1		nV/√Hz
Frequency = 240MHz								
S21	Power Gain	De-Embedded to Package				15.9		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			43.1 42.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–82.2 –80.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–53.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–73.0		dBc
P1dB	Output 1dB Compression Point					19.1		dBm
NF	Noise Figure	De-Embedded to Package				3.44		dB

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C (Note 3), V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency = 300MHz							
S21	Power Gain	De-Embedded to Package			15.8		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		41.5 40.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–79.0 –76.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–51.9		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–72.0		dBc
P1dB	Output 1dB Compression Point				19.0		dBm
NF	Noise Figure	De-Embedded to Package			3.61		dB
Frequency = 500MHz							
S21	Power Gain	De-Embedded to Package			15.5		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		38.4 37.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–72.8 –70.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–51.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–70.0		dBc
P1dB	Output 1dB Compression Point				18.9		dBm
NF	Noise Figure	De-Embedded to Package			3.93		dB
Frequency = 800MHz							
S21	Power Gain	De-Embedded to Package			15.0		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		34.9 33.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–65.8 –63.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–47.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–59.5		dBc
P1dB	Output 1dB Compression Point				18.0		dBm
NF	Noise Figure	De-Embedded to Package			4.40		dB
Frequency = 1000MHz							
S21	Power Gain	De-Embedded to Package			14.5		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		33.3 32.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–62.6 –60.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–45.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–57.0		dBc
P1dB	Output 1dB Compression Point				17.3		dBm
NF	Noise Figure	De-Embedded to Package			4.83		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and characterization. This parameter is not tested.

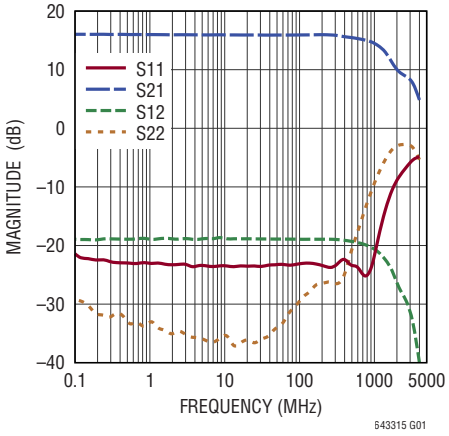
Note 3: The LTC6433-15 is guaranteed functional over the case operating temperature range of –40°C to 85°C.

Note 4: Small-signal parameters S and noise are de-embedded to the package pins, while large-signal parameters are measured directly from the circuit.

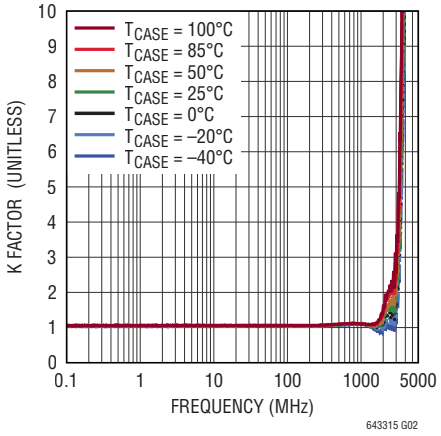
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. S parameter measurements are performed using 1µF feedback capacitor.

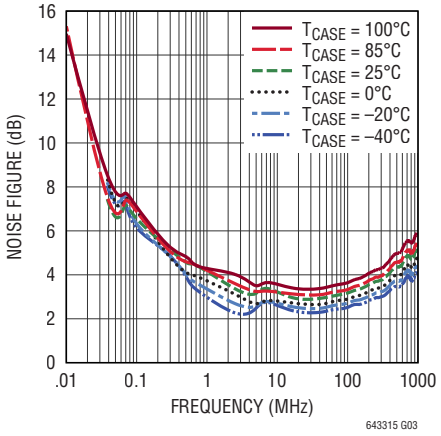
S Parameters vs Frequency



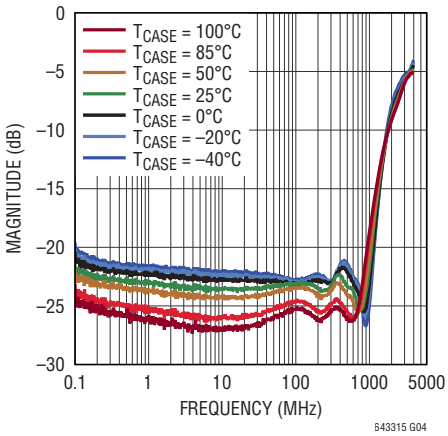
K Factor vs Frequency Over Temperature



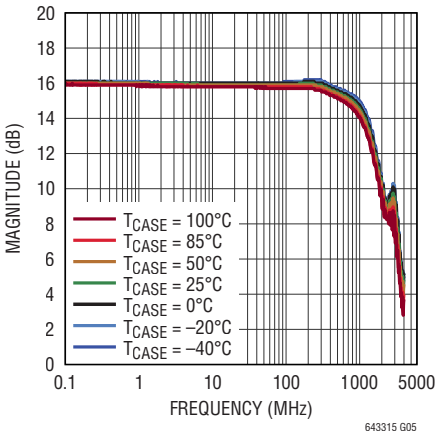
Noise Figure vs Frequency Over Temperature



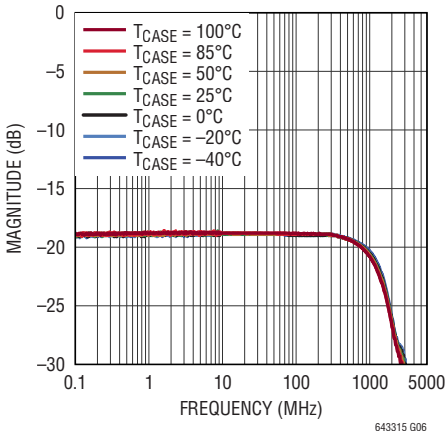
S11 vs Frequency Over Temperature



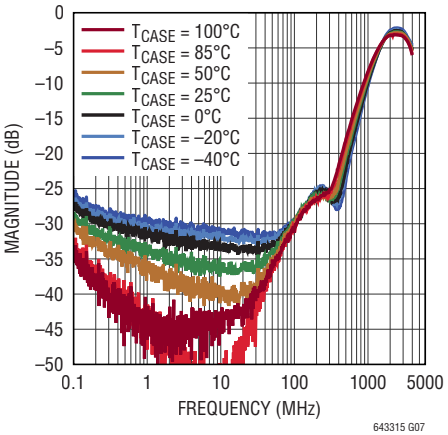
S21 vs Frequency Over Temperature



S12 vs Frequency Over Temperature



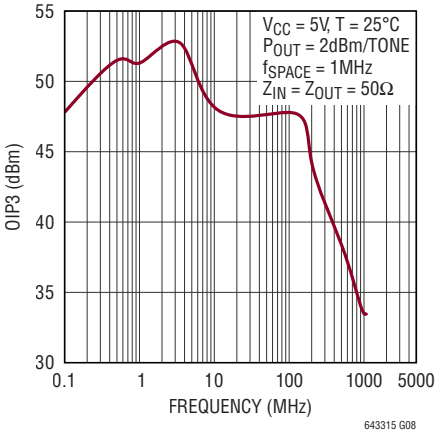
S22 vs Frequency Over Temperature



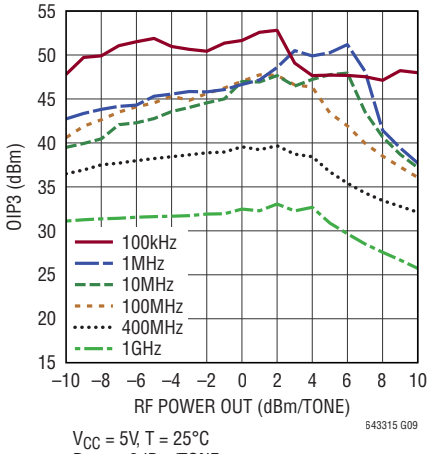
TYPICAL PERFORMANCE CHARACTERISTICS A-Grade

T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

OIP3 vs Frequency

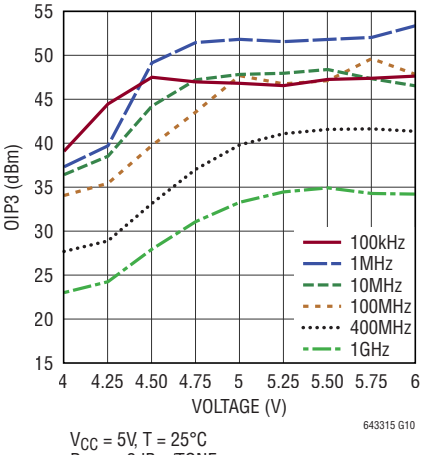


OIP3 vs RF Output Power Over Frequency



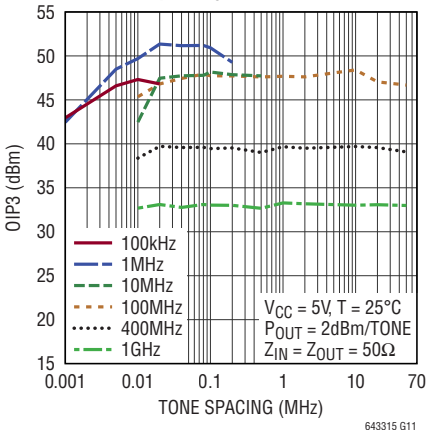
VCC = 5V, T = 25°C
POUT = 2dBm/TONE
fSPACE = 1MHz
ZIN = ZOUT = 50Ω

OIP3 vs Voltage Over Frequency

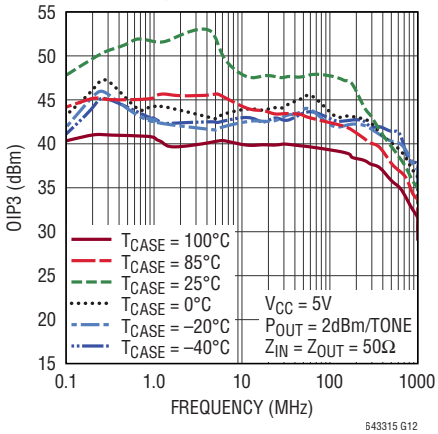


VCC = 5V, T = 25°C
POUT = 2dBm/TONE
fSPACE = 1MHz
ZIN = ZOUT = 50Ω

OIP3 vs Tone Spacing Over Frequency



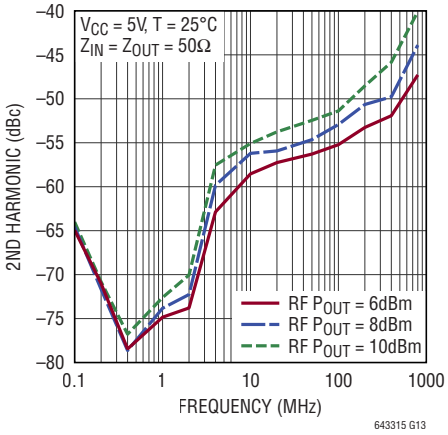
OIP3 vs Frequency Over Case Temperature



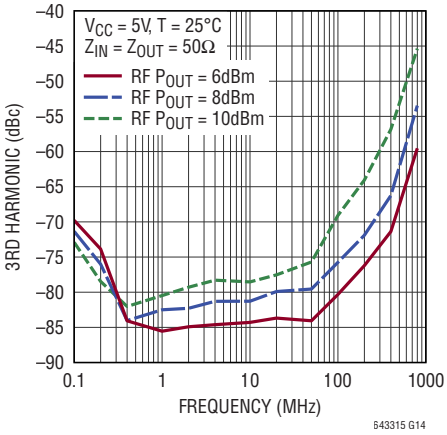
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

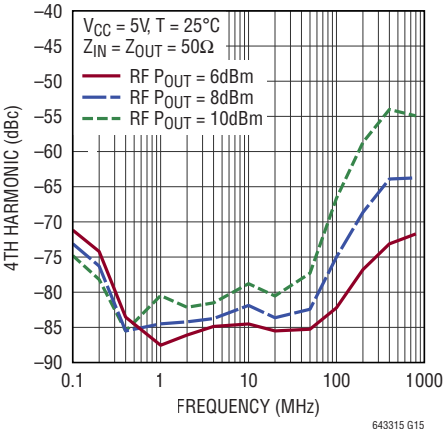
2nd Harmonic vs Frequency Over RF Power Out



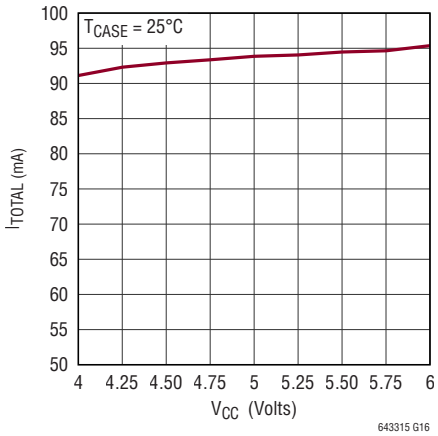
3rd Harmonic vs Frequency Over RF Power Out



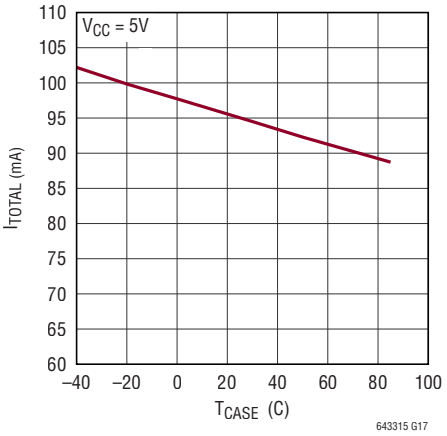
4th Harmonic vs Frequency Over RF Power Out



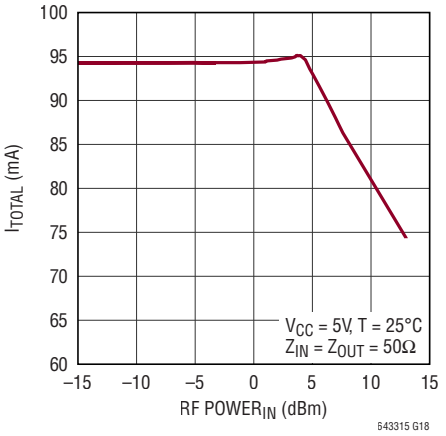
I_{TOTAL} vs V_{CC}



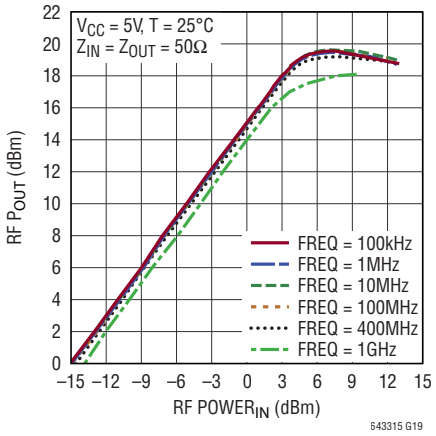
I_{TOTAL} vs T_{CASE}



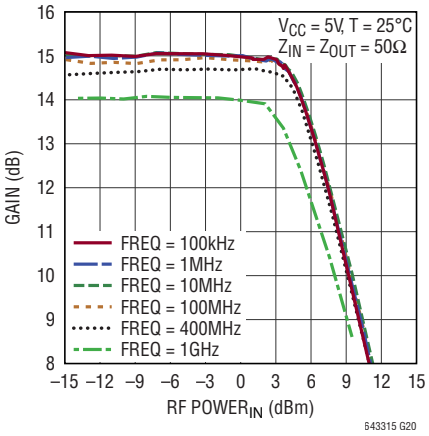
I_{TOTAL} vs Input Power



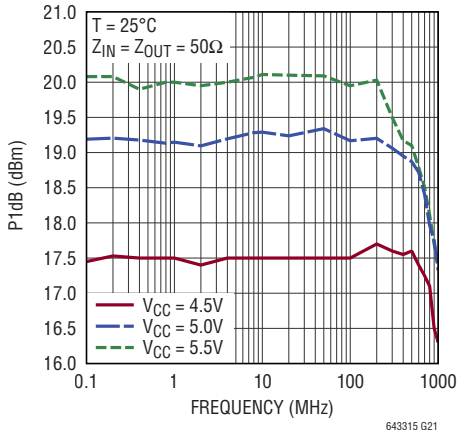
RF Power Out vs RF Power In Over Frequency



Gain vs RF Power In Over Frequency



P1dB vs Frequency



PIN FUNCTIONS

GND (Pins 8, 17, 23, Exposed Pad Pin 25): Ground. For best RF performance, all ground pins should be connected to the printed circuit board ground plane. The exposed pad should have multiple via holes to an underlying ground plane for low inductance and good thermal dissipation.

IN (Pin 24): Signal Input Pin. This pin has an internally generated 2V DC bias. A DC blocking capacitor is required. See the Applications Information section for specific recommendations.

V_{CC} (Pins 9, 22): Positive Power Supply. Either V_{CC} pin should be connected to the 5V supply. Bypass the V_{CC} pin with 1000pF and 0.1µF capacitors. The 1000pF capacitor should be physically close to the package. Pins 9 and 22 are internally connected within the package

N_{FILT} (Pins 6): Noise Filter Capacitor. A capacitor to GND is required to reduce low frequency noise.

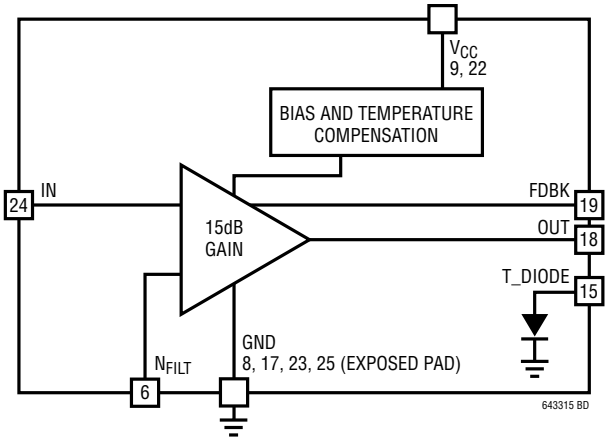
FDBK (Pin 19): A feedback capacitor is required between OUT (Pin 18) and the FDBK pin to ensure good matching and gain flatness at low frequencies.

OUT (Pin 18): Amplifier Output Pin. A choke inductor is necessary to provide power from the 5V supply and to provide RF isolation. For best performance select a choke with low DC loss and high self-resonant frequency (SRF). A DC blocking capacitor is also required. See the Applications Information section for specific recommendations.

DNC (Pins 1 to 5, 7, 10 to 14, 16, 20, 21): Do Not Connect. Do not connect these pins; allow them to **float. Failure to float these pins may impair operation of the LTC6433-15.**

T_DIODE (Pin 15): Optional Diode. The T_DIODE can be forward-biased to ground with 1mA of current. The measured voltage will be an indicator of chip temperature.

BLOCK DIAGRAM



TEST CIRCUIT A

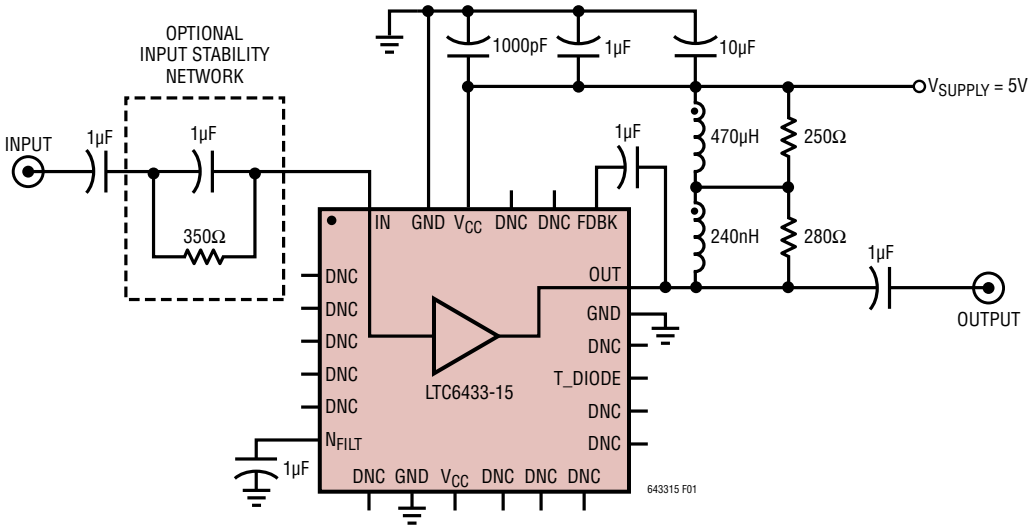


Figure 1. Test Circuit A Evaluation Circuit

OPERATION

The LTC6433-15 is a highly linear, fixed-gain amplifier that is configured to operate single ended. Its core signal path consists of a single amplifier stage minimizing stability issues. The input is a Darlington pair for high input impedance and high current gain. Additional circuit enhancements increase the output impedance and minimize the effects of internal Miller capacitance.

The LTC6433-15 starts with a classic RF gain-block topology but adds additional enhancements to achieve dramatically improved linearity. Shunt and series feedback are added to lower the input/output impedance and match them simultaneously to the 50Ω source and load. Meanwhile, an internal bias controller optimizes the internal operating point for peak linearity over environmental changes. This circuit architecture provides low noise, excellent RF power handling capability and wide bandwidth—characteristics that are desirable for IF signal chain applications.

APPLICATIONS INFORMATION

The LTC6433-15 is a highly linear fixed-gain amplifier designed for ease of use. Implementing an RF gain stage is often a multistep project. Typically an RF designer must choose a bias point and design a bias network. Next the designer needs to address impedance matching with input and output matching networks and, finally, add stability networks to ensure stable operation in and out of band. These tasks are handled internally within the LTC6433-15.

The LTC6433-15 has an internal self-biasing network which compensates for temperature variation and keeps the device biased for optimal linearity. Therefore, input and output DC blocking capacitors are required.

Both the input and output are internally impedance matched to 50Ω. An RF choke is required at the output to deliver DC current to the device. The RF choke acts as a high impedance (isolation) to the DC supply which is at RF ground. Thus, the internal LTC6433-15 impedance matching is unaffected by the biasing network. The open collector output topology can deliver much more power than an amplifier whose collector is biased through a resistor or active load.

Choosing the Right RF Choke

Not all choke inductors are created equal. Proper selection of a choke is critical to achieve high linearity and wide bandwidth. At frequencies below 100MHz, a large valued choke is required. It is always important to select an inductor with low R_{LOSS}, as this will drop the available voltage to the device. Also look for an inductor with high self-resonant frequency (SRF) as this will limit the upper frequency where the choke is useful. Above the SRF, its parasitic capacitance dominates and the choke impedance will drop. For these reasons, wire wound inductors are preferred, and multilayer ceramic chip inductors should be avoided for an RF choke. Choke inductors with magnetic cores should be used with caution as they can contribute distortion products themselves. We have successfully used power inductors as chokes but their evaluation at RF frequencies is normally left to the end user. Please see Table 1 for suggested RF chokes. Since the LTC6433-15 is capable of such wideband operation, a single choke value will not result in optimized performance across its full frequency band.

Table 1 lists target frequency bands and suggested corresponding inductor values.

Table 1. Target Frequency Bands and Suggested Inductor Values

FREQUENCY BAND	INDUCTOR VALUE	MODEL NUMBER	MANUFACTURER
100kHz to 500kHz	470µH	LPS5030	Coilcraft www.coilcraft.com
500kHz to 1MHz	220µH	LPS5030	
1MHz to 10MHz	120µH	LPS5030	
10MHz to 20MHz	12µH	LPS5030	
20MHz to 100MHz	1500nH	0805LS	
100MHz to 500MHz	560nH	0603LS	
500MHz to 1000MHz	100nH	0603LS	
1000MHz to 2000MHz	51nH	0603LS	

DC Blocking Capacitor

The role of a DC blocking capacitor is straightforward: block the path of DC current and allow a low series impedance path for the AC signal. Lower frequencies require a higher value of DC blocking capacitance. Generally, 1µF will suffice for operation down to 100kHz. Care must be taken when using high capacitance density materials. These high capacitance materials often have high voltage coefficients. At low frequencies this voltage dependence creates distortion products. Film caps and NPO caps get physically large and expensive at large capacitance values. High quality capacitors like the X8R series offer high capacitance density and good voltage coefficients. They are recommended for best linearity below 1 MHz.

RF Bypass Capacitor

RF bypass capacitors act to shunt AC signals to ground with a low impedance path. It is best to place them as close as possible to the DC power supply pins of the device. Any extra distance translates into additional series inductance which lowers the self-resonant frequency and useful bandwidth of the bypass capacitor. The suggested bypass capacitor network consists of multiple capacitors: a low value 1000pF capacitor to handle high frequencies in parallel with larger 0.1µF and 1µF capacitors to handle lower frequencies. Use ceramic capacitors of an appropriate physical size for each capacitance value (e.g., 0402 for the 1000pF, 0805 for the 0.1µF) to minimize the equivalent series resistance (ESR) of the capacitor.

APPLICATIONS INFORMATION

Low Frequency Stability

Most RF gain blocks suffer from low frequency instability. To avoid any stability issues, the LTC6433-15 has a feedback network that lowers the gain and matches the input and output impedances. This feedback network contains a series capacitor, so if at some low frequency the feedback fails, the gain increases and gross impedance mismatches occur—indeed a recipe for instability. Luckily, this situation is easily resolved with a parallel capacitor and resistor network on the input, as seen in Figure 1. This network provides resistive loss at low frequencies and is bypassed by the parallel capacitor within the desired band of operation. However, if the LTC6433-15 is preceded by a low frequency termination, such as a choke, the input stability network is NOT required.

Test Circuit

The test circuit shown in Figure 2 is designed to allow evaluation of the LTC6433-15 with standard single-ended 50Ω test equipment. The circuit requires a minimum of external components. Since the LTC6433-15 is a wideband part, the evaluation test circuit is optimized for wideband operation. Obviously, for narrowband applications, the circuit can be further optimized. As mentioned earlier, input and output DC blocking capacitors are required as this device is internally biased for optimal operation. A frequency appropriate choke and decoupling capacitors are required to provide DC bias to the RF out node. A 5V supply should also be applied to either of the V_{CC} pins on the device. A suggested parallel 1µF, 350Ω network has been added to the input to ensure low frequency stability. The 1µF capacitance can be increased to improve low frequency performance. However, the designer needs to be sure that the impedance presented at low frequency will not create instability.

A 1µF noise filter capacitor is required to reduce low frequency noise.

Please note that a number of DNC pins are connected on the demo board. These connections are not necessary for normal circuit operation.

Exposed Pad and Ground Plane Considerations

As with any RF device, minimizing ground inductance is critical. Care should be taken with board layouts using these exposed pad packages. The maximum allowable number of minimum diameter via holes should be placed underneath the exposed pad and connect to as many ground plane layers as possible. This will provide good RF ground and low thermal impedance. Maximizing the copper ground plane will also improve heat spreading and lower inductance. It is a good idea to cover the via holes with a solder mask on the backside of the PCB to prevent the solder from wicking away from the critical PCB to the exposed pad interface.

Wideband Output Network

The DC2168A demonstration circuit has flat gain, excellent linearity and low noise from 100kHz to 1GHz. A key to this wide bandwidth performance is the output network. A single RF choke is replaced with a network that gives good RF isolation from 100kHz to 1GHz. In this case, we use a 240nH (0603) inductor in series with a 470µH power inductor. The 240nH inductor provides isolation at high frequencies, while the 470µH inductor provides RF isolation at low frequencies. Resistors are shunted across each inductor to flatten the loss over the desired 100kHz to 1GHz band. Our resulting output network has minimal R_{LOSS} which allows operation with a single 5V supply.

APPLICATIONS INFORMATION

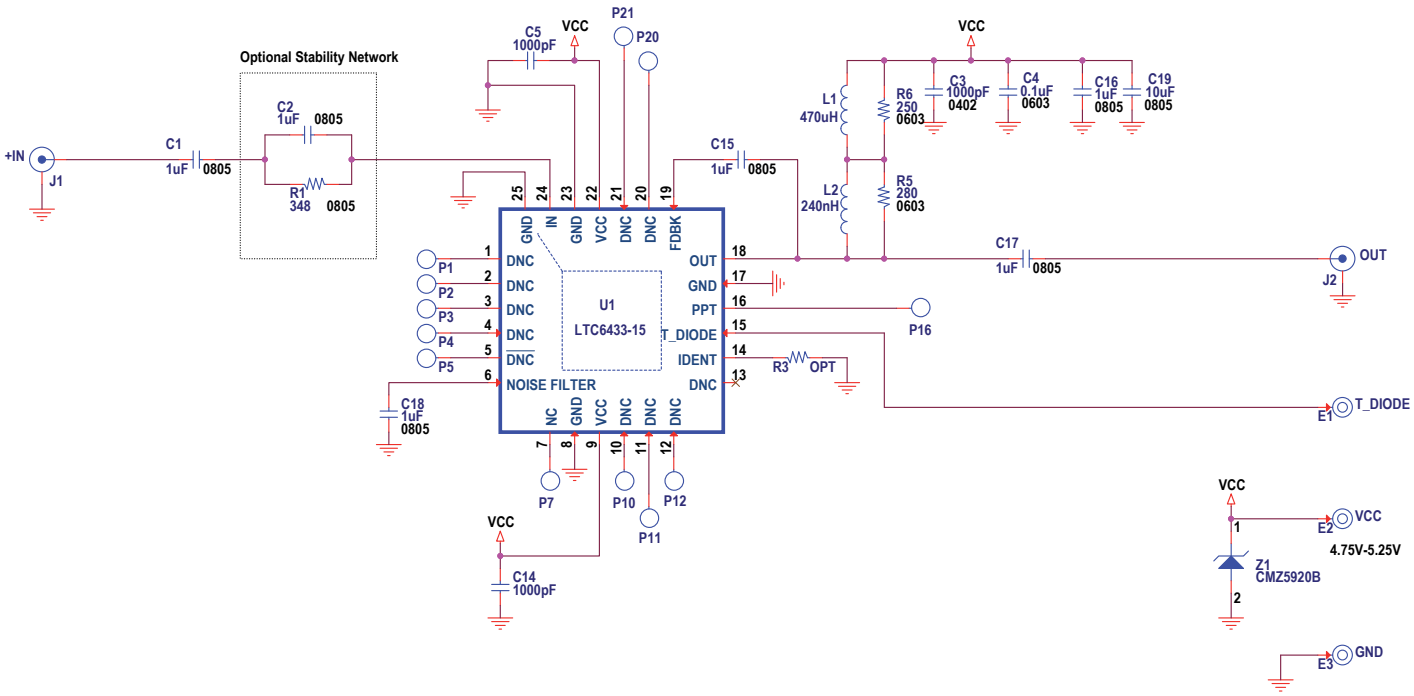


Figure 2. DC2168A Demo Board Schematic

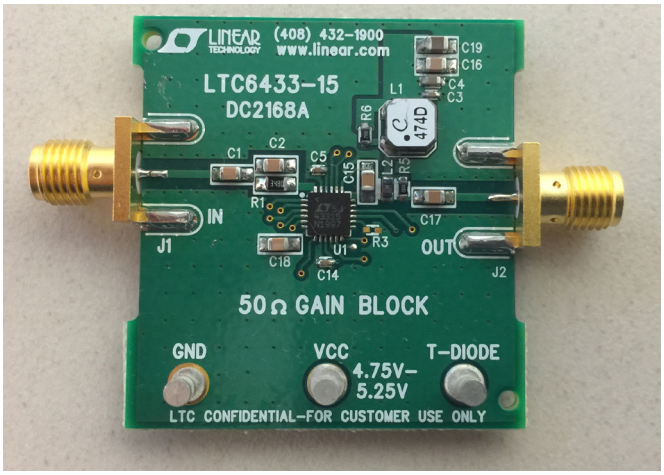


Figure 3. LTC6433-15 DC2168A Demo Board

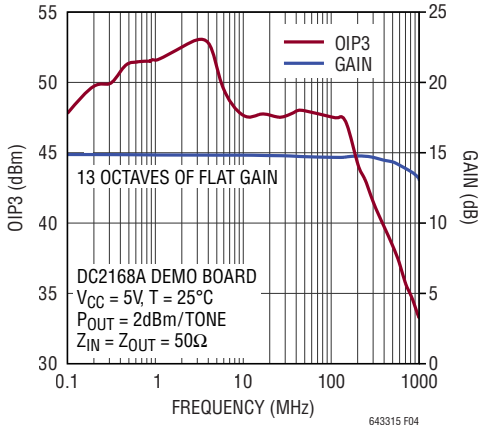


Figure 4. DC2168A Gain and OIP3 vs Frequency

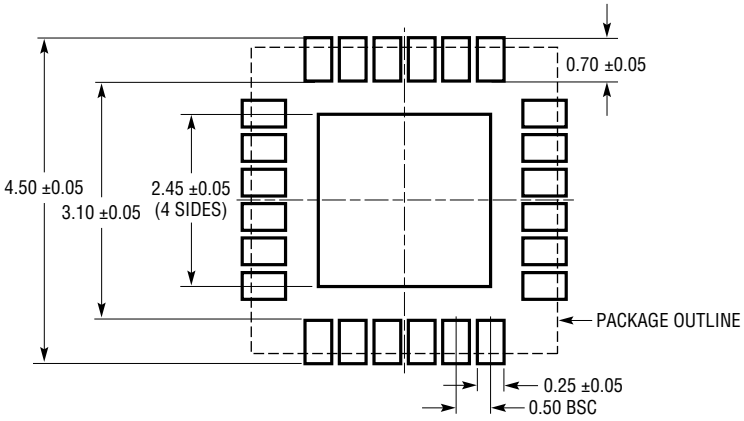
S PARAMETERS 5V, 95mA, Z = 50Ω, T = 25°C, De-Embedded to Package Pins with 1µF Capacitors for FDBK

FREQUENCY (MHz)	S11 (Mag)	S11 (Ph)	S21 (Mag)	S21 (Ph)	S12 (Mag)	S12 (Ph)	S22 (Mag)	S22 (Ph)	GTU (Max)	Stability (K)
0.10	–21.17	–154.55	16.03	–178.41	–18.94	2.35	–29.13	144.63	16.07	1.05
0.13	–21.99	–161.40	16.04	–178.87	–19.00	1.42	–29.78	144.70	16.07	1.05
0.17	–22.17	–164.29	16.04	–179.08	–18.96	1.50	–29.93	150.01	16.07	1.05
0.22	–22.53	–168.19	16.04	–179.35	–18.97	1.53	–31.07	150.94	16.07	1.05
0.28	–22.44	–170.32	16.03	–179.66	–19.00	0.55	–31.75	151.77	16.06	1.05
0.36	–22.76	–174.13	16.02	–179.71	–18.92	0.74	–31.05	156.67	16.05	1.05
0.46	–22.71	–175.92	16.01	–179.92	–18.88	0.95	–32.09	158.81	16.04	1.05
0.60	–22.83	–176.07	16.00	179.94	–18.87	0.19	–32.59	150.96	16.03	1.05
0.77	–22.90	–177.62	16.00	179.89	–18.88	0.35	–32.60	165.65	16.03	1.05
0.99	–22.85	–179.20	15.98	179.83	–18.96	0.45	–33.27	173.04	16.01	1.05
1.28	–22.81	59.69	15.99	179.84	–18.90	–0.15	–33.35	165.78	16.01	1.05
1.66	–22.98	179.51	15.98	179.62	–18.84	0.06	–33.19	163.84	16.00	1.05
2.14	–23.04	179.30	15.96	179.69	–18.90	0.10	–34.38	165.49	15.99	1.05
2.76	–23.14	59.39	15.96	179.56	–18.93	0.17	–34.22	166.41	15.98	1.05
3.53	–23.13	179.63	15.96	179.44	–18.86	0.17	–34.35	171.91	15.98	1.05
4.56	–23.23	177.95	15.95	179.46	–18.89	–0.58	–35.02	–59.59	15.97	1.05
5.91	–23.22	179.18	15.95	179.26	–18.89	0.05	–36.06	59.25	15.97	1.05
7.64	–23.39	59.83	15.94	179.16	–18.84	–0.59	–34.48	178.68	15.96	1.05
9.82	–23.30	179.10	15.93	178.95	–18.88	–0.77	–35.63	–176.60	15.95	1.05
12.6	–23.37	–59.79	15.93	178.71	–18.86	–1.01	–35.95	–174.44	15.95	1.05
16.3	–23.33	–179.27	15.92	178.34	–18.87	–1.39	–35.75	–169.41	15.94	1.05
21.1	–23.36	–59.87	15.92	177.89	–18.87	–1.77	–35.56	–166.88	15.94	1.05
27.2	–23.31	–178.86	15.91	177.37	–18.86	–2.25	–36.36	–156.65	15.93	1.05
35.0	–23.36	–178.71	15.91	176.71	–18.88	–2.96	–35.39	–150.36	15.93	1.05
44.7	–23.37	60.22	15.91	175.81	–18.89	–3.73	–34.47	–147.63	15.93	1.05
58.1	–23.14	–178.81	15.91	174.63	–18.91	–4.77	–33.34	–137.94	15.93	1.05
75.3	–23.16	60.12	15.92	173.12	–18.92	–6.20	–31.32	–132.08	15.94	1.05
97.1	–23.15	58.97	15.93	171.06	–18.93	–7.79	–29.78	–129.06	15.96	1.05
124.7	–23.06	176.54	15.94	168.50	–18.93	–10.00	–28.36	–131.68	15.97	1.05
159.8	–23.05	175.44	15.96	165.17	–18.93	–12.70	–27.35	–136.57	15.99	1.05
207.5	–23.11	174.45	15.97	160.31	–18.92	–16.52	–26.45	–138.23	16.00	1.05
268.5	–23.27	173.39	15.91	154.08	–18.95	–21.56	–26.24	–140.47	15.94	1.05
346.3	–22.28	171.00	15.76	146.33	–19.01	–28.30	–26.83	–130.53	15.79	1.06
443.5	–22.24	167.12	15.56	137.71	–19.18	–36.31	–24.05	–105.26	15.60	1.08
570.8	–23.19	160.37	15.35	126.33	–19.44	–46.52	–19.01	–99.82	15.42	1.09
740.7	–24.51	163.54	15.09	111.18	–19.83	–59.90	–14.36	–108.76	15.26	1.11
958.6	–22.68	–171.11	14.64	91.27	–20.47	–77.09	–10.35	–124.40	15.09	1.12
1232.8	–17.01	–172.86	13.82	65.84	–21.53	–98.71	–6.96	–146.60	14.88	1.09
1579.5	–12.08	158.84	12.10	37.27	–23.30	–124.44	–4.40	–175.70	14.34	1.07
2000.1	–9.02	119.72	9.99	6.13	–26.19	–151.27	–3.05	150.16	13.55	1.25

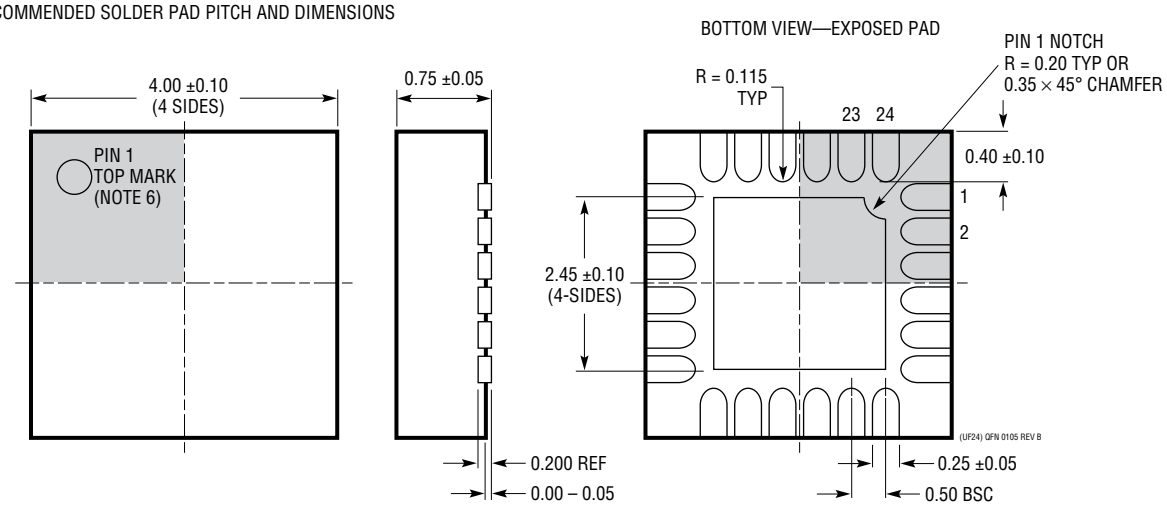
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6433-15#packaging for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE