Dual Matched, High Frequency Bandpass/Lowpass Filters

FEATURES

- **Matched Dual Filter/Driver, Ideal for RFID Readers**
- **Guaranteed Phase Matching to Within 2 Degrees**
- **Guaranteed Gain Matching to Within 0.2dB**
- **Configurable as Lowpass or Bandpass:**
  - **Programmable 5th Order Lowpass: 42kHz to 900kHz**
  - **Programmable 4th Order Highpass: 4.2kHz to 90kHz**
- **Programmable Gain: 1×, 4×, 16×, 32×**
- Simple Pin Programming or SPI Interface
- Low Noise: –145dBm/Hz (Input Referred)
- Low Distortion: –75dBc at 200kHz
- Differential, Rail-to-Rail Inputs and Outputs
- Input Range Extends from 0V to 5V
- Low Voltage Operation: 2.7V to 3.6V
- Shutdown Mode
- 4mm × 4mm QFN Package

APPLICATIONS

- Multiprotocol RFID Readers: EPC-GEN2, ISD and IPX
- IDEN, PHS, GSM Basestations
- Repeaters, Radio Links, and Modems
- Wireless Telemetry
- JTRS

DESCRIPTION

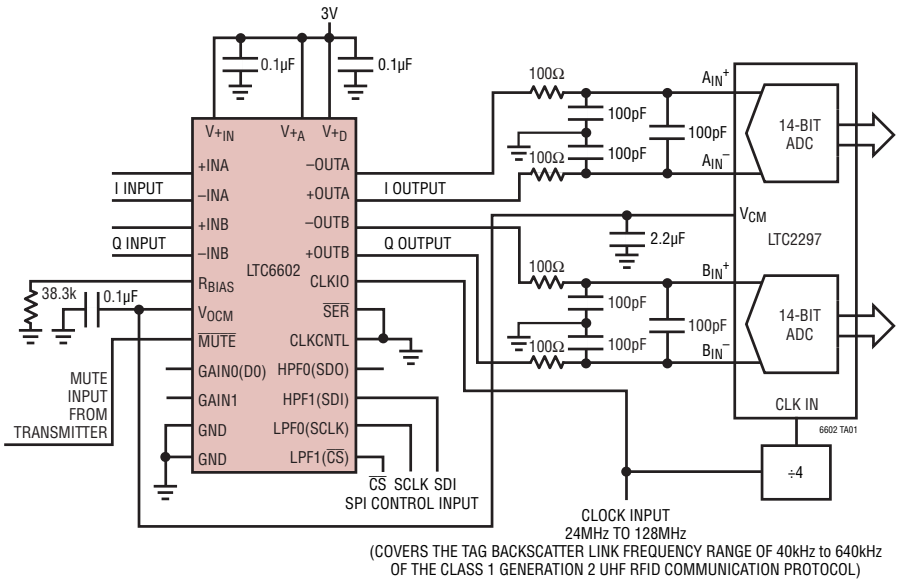
The LTC®6602 is a dual, matched, programmable bandpass or lowpass filter and differential driver. The selectivity of the LTC6602, combined with its phase matching and dynamic range, make it ideal for filtering in RFID systems. With two degree phase matching between channels, the LTC6602 can be used in applications requiring highly matched filters, such as transceiver I and Q channels. Gain programmability, and the fully differential inputs and outputs, simplify implementation in most systems.

Both channels of the LTC6602 consist of a programmable lowpass and highpass filter. For bandpass functionality, the lowpass filters are programmed for the upper cutoff frequency. For lowpass functionality, the highpass filters can be bypassed. The filter cutoff frequencies can be set with a guaranteed accuracy of 3% with the use of a single resistor. Alternatively, the filter cutoff frequencies can be controlled with an external clock.

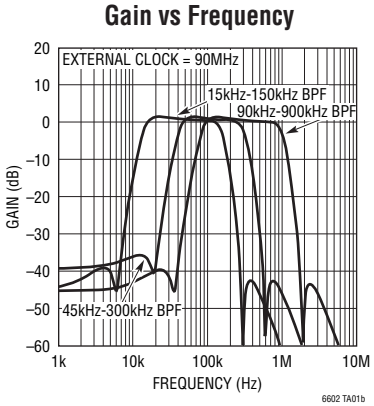
The LTC6602 operates on a single 2.7V to 3.6V supply and features a low power shutdown mode.

TYPICAL APPLICATION

UHF RFID Reader Dual Baseband Filter and Dual ADC



Gain vs Frequency

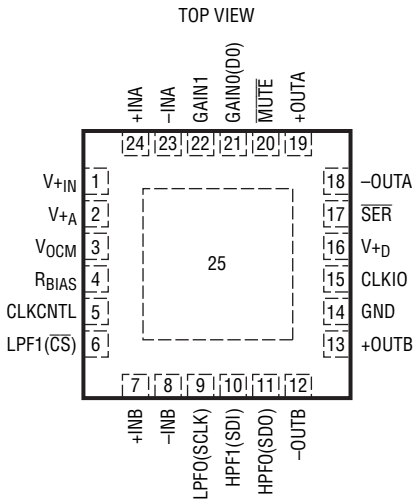


ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V+_{IN}$ to GND 6V
$V+_A$, $V+_D$ to GND 4V
Filter Inputs to GND ..... –0.3V to $V+_{IN}$ + 0.3V
All Other Pins to GND..... –0.3V to $V+_A$, $V+_D$ + 0.3V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2)
LTC6602CUF ..... –40°C to 85°C
LTC6602IUF ..... –40°C to 85°C
Specified Temperature Range (Note 3)
LTC6602CUF ..... 0°C to 70°C
LTC6602IUF ..... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO THE PCB.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6602CUF#PBF	LTC6602CUF#TRPBF	6602	24-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC6602IUF#PBF	LTC6602IUF#TRPBF	6602	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V+_A$ = $V+_D$ = $V+_{IN}$ = 3V, V_{ICM} = V_{OCM} = 1.5V, Gain = 0dB, lowpass cutoff = 300kHz, highpass cutoff = 45kHz, internal clocking with R_{BIAS} = 54.9k unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Gain Either Channel Gain = 0dB	External Clock = 90MHz, Highpass Filter Cutoff = 45kHz, Lowpass Filter Cutoff = 300kHz, V_{IN} = 3.6V_{P-P}					
	f_{IN} = 22.5kHz	●		–32	–30	dB
	f_{IN} = 45kHz	●	–1.8	–1.2	–0.8	dB
	f_{IN} = 150kHz	●	0.1	0.5	0.8	dB
	f_{IN} = 300kHz	●	–2.7	–2	–1.2	dB
	f_{IN} = 900kHz	●		–44	–43	dB
Matching of Filter Gain	External Clock = 90MHz, Highpass Filter Cutoff = 45kHz, Lowpass Filter Cutoff = 300kHz, V_{IN} = 3.6V_{P-P}					
	f_{IN} = 45kHz	●			±0.2	dB
	f_{IN} = 150kHz	●			±0.2	dB
	f_{IN} = 300kHz	●			±0.2	dB

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Phase Either Channel	External Clock = 90MHz, V_{IN} = 3.6V_{P-P}, Highpass Filter Cutoff = 45kHz, Lowpass Filter Cutoff = 300kHz					
	f_{IN} = 50kHz	●	125	130	134	deg
	f_{IN} = 250kHz	●	–134	–130	–126	deg
Matching of Filter Phase	External Clock = 90MHz, V_{IN} = 3.6V_{P-P} , Highpass Filter Cutoff = 45kHz, Lowpass Filter Cutoff = 300kHz					
	f_{IN} = 50kHz	●			±2	deg
	f_{IN} = 250kHz	●			±1.5	deg
Filter Gain Either Channel Gain = 0dB	External Clock = 90MHz, Highpass Filter Cutoff = 15kHz, Lowpass Filter Cutoff = 150kHz, V_{IN} = 3.6V_{P-P}					
	f_{IN} = 7.5kHz	●		–32	–30	dB
	f_{IN} = 15kHz	●	–1.6	–1.2	–0.8	dB
	f_{IN} = 50kHz	●	0.4	0.7	0.9	dB
	f_{IN} = 150kHz	●	–2.3	–1.9	–1.3	dB
	f_{IN} = 450kHz	●		–44	–43	dB
Matching of Filter Gain	External Clock = 90MHz, V_{IN} = 3.6V_{P-P} , Highpass Filter Cutoff = 15kHz, Lowpass Filter Cutoff = 150kHz					
	f_{IN} = 15kHz	●			±0.2	dB
	f_{IN} = 50kHz	●			±0.2	dB
	f_{IN} = 150kHz	●			±0.2	dB
Filter Phase Either Channel	External Clock = 90MHz, V_{IN} = 3.6V_{P-P} , Highpass Filter Cutoff = 15kHz, Lowpass Filter Cutoff = 150kHz					
	f_{IN} = 16.5kHz	●	137	142	146	deg
	f_{IN} = 125kHz	●	–143	–138	–134	deg
Matching of Filter Phase	External Clock = 90MHz, V_{IN} = 3.6V_{P-P} , Highpass Filter Cutoff = 15kHz, Lowpass Filter Cutoff = 150kHz					
	f_{IN} = 16.5kHz	●			±2	deg
	f_{IN} = 125kHz	●			±1	deg
Filter Gain Either Channel Gain = 0dB	External Clock = 90MHz, Highpass Filter Cutoff = 90kHz, Lowpass Filter Cutoff = 900kHz, V_{IN} = 3.6V_{P-P}					
	f_{IN} = 45kHz	●		–29	–27	dB
	f_{IN} = 90kHz	●	–1.8	–1.2	–0.7	dB
	f_{IN} = 300kHz	●	–0.1	0.6	1.2	dB
	f_{IN} = 900kHz	●	–2.1	–1.1	–0.5	dB
	f_{IN} = 2700kHz	●		–45	–44	dB
Matching of Filter Gain	External Clock = 90MHz, Highpass Filter Cutoff = 90kHz, Lowpass Filter Cutoff = 900kHz, V_{IN} = 3.6V_{P-P}					
	f_{IN} = 90kHz	●			±0.3	dB
	f_{IN} = 300kHz	●			±0.6	dB
	f_{IN} = 900kHz	●			±0.4	dB
Filter Phase Either Chanel	External Clock = 90MHz, V_{IN} = 3.6V_{P-P} , Highpass Filter Cutoff = 90kHz, Lowpass Filter Cutoff = 900kHz					
	f_{IN} = 100kHz	●	136	141	145	deg
	f_{IN} = 750kHz	●	–136	–131	–127	deg
Matching of Filter Phase	External Clock = 90MHz, V_{IN} = 3.6V_{P-P} , Highpass Filter Cutoff = 90kHz, Lowpass Filter Cutoff = 900kHz					
	f_{IN} = 100kHz	●			±2	deg
	f_{IN} = 750kHz	●			±1.5	deg
Filter Cutoff Accuracy when Self Clocked	CLKCNTL = 3V (Note 4)					
	R_{BIAS} = 200k, Output Clock = 24.705MHz	●			±3	%
	R_{BIAS} = 54.9k, Output Clock = 90MHz	●			±3	%

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGA Gain	Lowpass Cutoff = 150kHz, Highpass Filter Bypassed, Measured at DC, 0.6V to 2.4V Each Output					
	Gain Setting = 0dB	●	0.4	0.8	1.2	dB
	Gain Setting = 12dB	●	11.6	12	12.4	dB
	Gain Setting = 24dB	●	23.5	23.8	24.1	dB
	Gain Setting = 30dB	●	29.1	29.6	30.1	dB
PGA Gain Matching	Lowpass Cutoff = 150kHz, Highpass Filter Bypassed, Measured at DC, 0.6V to 2.4V Each Output					
	Gain Setting = 0dB	●			±0.2	dB
	Gain Setting = 12dB	●			±0.2	dB
	Gain Setting = 24dB	●			±0.3	dB
	Gain Setting = 30dB	●			±0.3	dB
Noise At 200kHz	Voltage Noise Referred to the Input					
	Gain = 0dB			–119		dBm/Hz
	Gain = 12dB			–131		dBm/Hz
	Gain = 24dB			–142		dBm/Hz
	Gain = 30dB			–146		dBm/Hz
Integrated Noise	Noise Bandwidth = 1.57MHz (Note 5), Referred to the Input					
	Gain = 0dB			–62		dBm
	Gain = 12dB			–74		dBm
	Gain = 24dB			–85		dBm
	Gain = 30dB			–89		dBm
THD	V_{IN} = 1.5V_{P-P}, f_{IN} = 100kHz			–75		dB
Input Impedance	Differential			16		kΩ
	Common Mode			20		kΩ
V_{OS} Differential	Differential Offset Voltage at Either Output	●		±7	±15	mV
	Differential Offset Voltage at Either Output HPF Bypassed, Lowest LPF Cutoff	●		±10	±30	mV
	Differential Offset Voltage at Either Output HPF Bypassed, Highest LPF Cutoff	●		±10	±30	mV
V_{OSCM}	Common Mode Offset Voltage V_{OCM} = 1.5V, Supplies = 3V V_{OSCM} = V_{OUT-CM} – V_{OCM}	●	–40	±20	70	mV
CMR Differential $\Delta V_{INCM}/\Delta V_{OUTDIFF}$	Common Mode Input from 0 to 3V					
	$V+_{IN}$ = 3V	●	75	95		dB
	Common Mode Input from 0 to 5V					
	$V+_{IN}$ = 5V	●	75	95		dB
V_{OCM} Pin Voltage	$V+_A$ = $V+_D$ = 3V, Pin 3 Open	●	1.2	1.4	1.6	V
V_{OCM} Pin Input Impedance	$V+_A$ = $V+_D$ = 3V, Pin 3 Open	●	300	400	700	Ω
Output Swing	Lowpass Cutoff = 150kHz, Highpass Filter Bypassed, Measured at DC					
	Source 1mA, V_{OUT} High, Relative to $V+_A$	●		200	500	mV
	Sink 1mA, V_{OUT} Low, Relative to GND	●		200	500	mV
Short-Circuit Current	Lowpass Cutoff = 150kHz, Highpass Filter Bypassed					
	Sourcing	●	4	15	25	mA
	Sinking	●	10	25	50	mA
Supply Current	Internal Clock (R_{BIAS} = 54.9k); Sum of the Currents into $V+_D$, $V+_A$, and $V+_{IN}$ All Supplies Set to 3V					
	HPF = 15k, LPF = 150k	●		65	88	mA
	HPF = 45k, LPF = 300k	●		100	133	mA
	HPF = 90k, LPF = 900k	●		105	138	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V+_A$ = $V+_D$ = $V+_{IN}$ = 3V, V_{ICM} = V_{OCM} = 1.5V, Gain = 0dB, lowpass cutoff = 300kHz, highpass cutoff = 45kHz, internal clocking with R_{BIAS} = 54.9k unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current, Shutdown Mode	Sum of the Currents into $V+_D$, $V+_A$, and $V+_{IN}$; All Supplies Set to 3V Shutdown Via Serial Interface, Control Bit D1 = 1.	 ●		 170	 235	 µA
Supply Voltage	$V+_D$, $V+_A$ Relative to GND $V+_{IN}$ Relative to GND	● ●	2.7 2.7		3.6 5.5	V V
PSR	$V+_D$ = $V+_A$ = $V+_{IN}$, All from 2.7V to 3.6V $V+_D$ = $V+_A$ = 3.0V, $V+_{IN}$ from 4.5V to 5.5V	● ●	50 80	60 95		dB dB
R_{BIAS} Resistor Range	Clock Frequency Error ≤ ±3%, CLKCNTL = 3V	●	54.9		200	kΩ
R_{BIAS} Pin Voltage	54.9k < R_{BIAS} < 200k			1.17		V
Clock Frequency Drift Over Temperature	R_{BIAS} = 54.9k, CLKCNTL Pin Open			40		ppm/°C
Clock Frequency Change Over Supply	$V+_A$, $V+_D$ from 2.7V to 3.6V, R_{BIAS} = 54.9k, CLKCNTL Pin Open	●	–0.6	0.1	0.6	%/V
Output Clock Duty Cycle	R_{BIAS} = 54.9k	●	25	50	75	%
CLKIO Pin High Level Input Voltage	CLKCNTL = 0V (Note 6)		V_{+D} – 0.3			V
CLKIO Pin Low Level Input Voltage	CLKCNTL = 0V (Note 6)				0.3	V
CLKIO Pin Input Current	CLKCNTL = 0V CLKIO = 0V (Note 7) CLKIO = $V+_D$	 ● ●	 –1	 	 10	 µA µA
CLKIO Pin High Level Output Voltage	$V+_A$ = $V+_D$ = 3V, CLKCNTL = 3V I_{OH} = –1mA I_{OH} = –4mA			 2.95 2.9		 V V
CLKIO Pin Low Level Output Voltage	$V+_A$ = $V+_D$ = 3V, CLKCNTL = 3V I_{OL} = 1mA I_{OL} = 4mA			 0.05 0.1		 V V
CLKIO Rise Time	$V+_A$ = $V+_D$ = CLKCNTL = 3V, 20%/80%, C_{LOAD} = 5pF			0.3		ns
CLKIO Fall Time	$V+_A$ = $V+_D$ = CLKCNTL = 3V, 20%/80%, C_{LOAD} = 5pF			0.3		ns
$\overline{SER}$, $\overline{MUTE}$ High Level Input Voltage	Pins 17, 20	●	V_{+D} – 0.3			V
$\overline{SER}$, $\overline{MUTE}$ Low Level Input Voltage	Pins 17, 20	●			0.3	V
$\overline{SER}$, $\overline{MUTE}$ Input Current	Pin 17 or Pin 20 = 0V (Note 7) Pin 17 or Pin 20 = $V+_D$	● ●	–10		 2	µA µA
CLKCNTL High Level Input Voltage	Pin 5	●	V_{+D} – 0.5			V
CLKCNTL Low Level Input Voltage	Pin 5				0.5	V
CLKCNTL Input Current	CLKCNTL = 0V (Note 7) CLKCNTL = $V+_D$	● ●	–25	–15 15	 25	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications apply to pins 6, 9-11, 21 and 22.

Pin Programmable Control Mode Specifications

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V+_D$ = 2.7V to 3.6V							
V_{IH}	Digital Input High Voltage	Pins 6, 9-11, 21, 22	●	2			V
V_{IL}	Digital Input Low Voltage	Pins 6, 9-11, 21, 22	●			0.8	V
I_{IN}	Digital Input Current	Pins 6, 9-11, 21, 22 (Note 7)	●	–1		1	µA

Serial Port DC and Timing Specifications

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V+_D$ = 2.7V to 3.6V							
V_{IH}	Digital Input High Voltage	Pins 6, 9, 10	●	2			V
V_{IL}	Digital Input Low Voltage	Pins 6, 9, 10	●			0.8	V
I_{IN}	Digital Input Current	Pins 6, 9, 10 (Note 7)	●	–1		1	µA
V_{OH}	Digital Output High Voltage	Pins 11, 21 Sourcing 500µA	●	V_{SUPPLY} – 0.3			V
V_{OL}	Digital Output Low Voltage	Pins 11, 21 Sinking 500µA	●			0.3	V
t_1	SDI Valid to SCLK Setup	(Note 6)	●	60			ns
t_2	SDI Valid to SCLK Hold	(Note 6)	●	0			ns
t_3	SCLK Low		●	100			ns
t_4	SCLK High		●	100			ns
t_5	$\overline{CS}$ Pulse Width		●	60			ns
t_6	LSB SCLK to $\overline{CS}$	(Note 6)	●	60			ns
t_7	$\overline{CS}$ Low to SCLK	(Note 6)	●	30			ns
t_8	SDO Output Delay	C_L = 15pF	●			125	ns
t_9	SCLK Low to $\overline{CS}$ Low	(Note 6)	●	0			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: LTC6602C and LTC6602I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: LTC6602C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6602C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6602I is guaranteed to meet the specified performance limits from –40°C to 85°C.

Note 4: This test measures the internal oscillator accuracy (deviation from the f_{CLK} equation). Variations in the internal oscillator frequency cause variations in the filter cutoff frequency. See the "Applications Information" section.

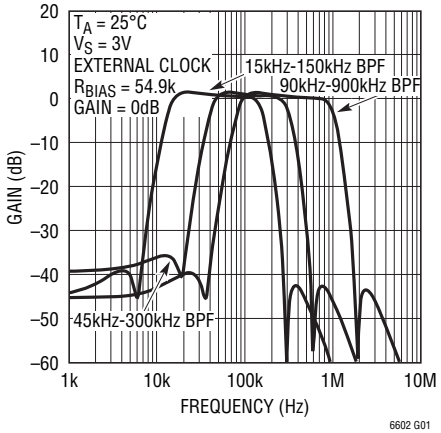
Note 5: 1.57MHz is the equivalent noise bandwidth of a 1MHz 1st order RC lowpass filter.

Note 6: Guaranteed by design, not subject to test.

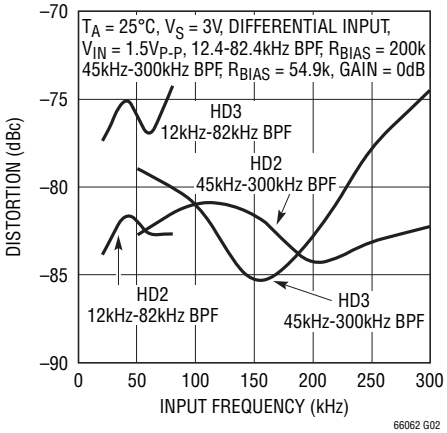
Note 7: To conform to the Logic IC standard, current out of a pin is arbitrarily given a negative value.

TYPICAL PERFORMANCE CHARACTERISTICS

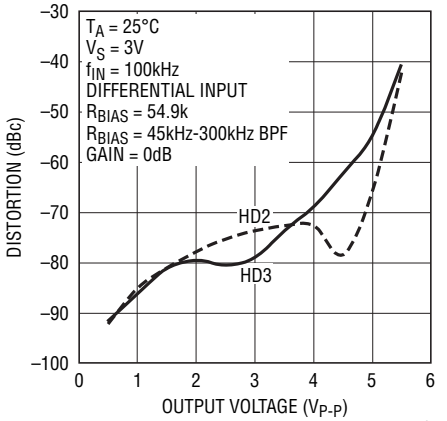
Gain vs Frequency



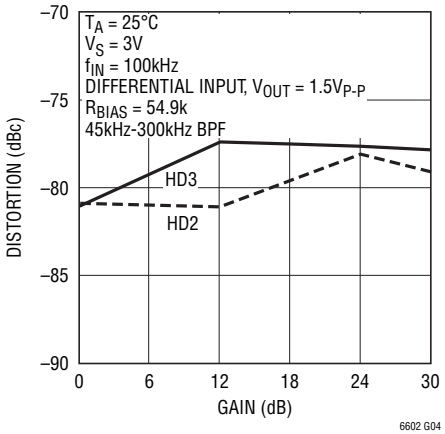
Distortion vs Input Frequency



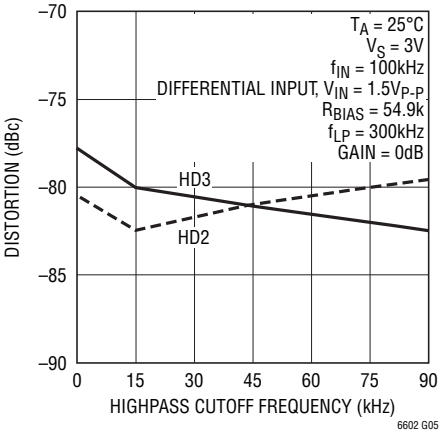
Distortion vs Output Voltage



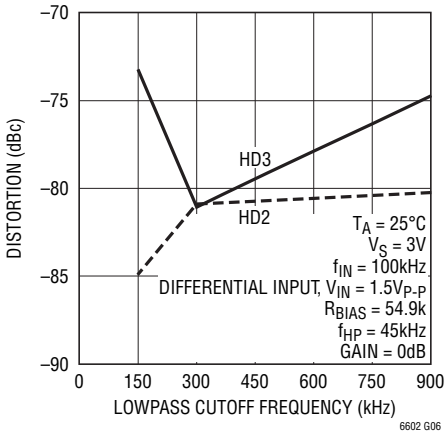
Distortion vs Gain



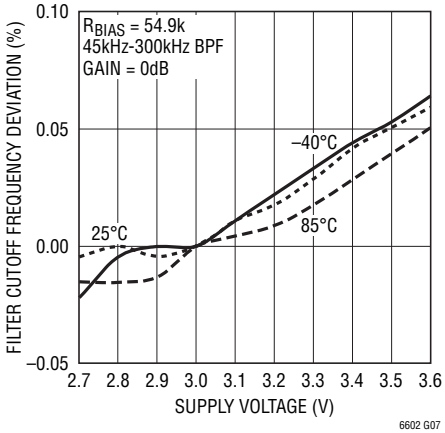
Distortion vs Highpass Cutoff Frequency



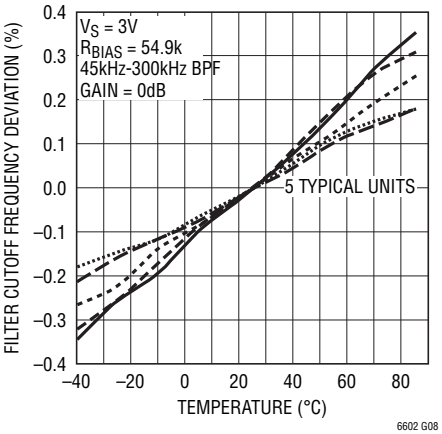
Distortion vs Lowpass Cutoff Frequency



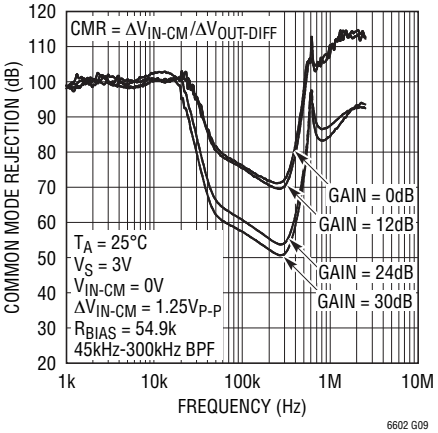
Filter Cutoff Accuracy vs Supply Voltage



Filter Cutoff Accuracy vs Temperature

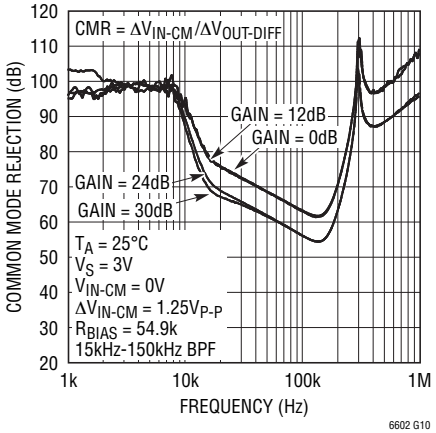


Common Mode Rejection

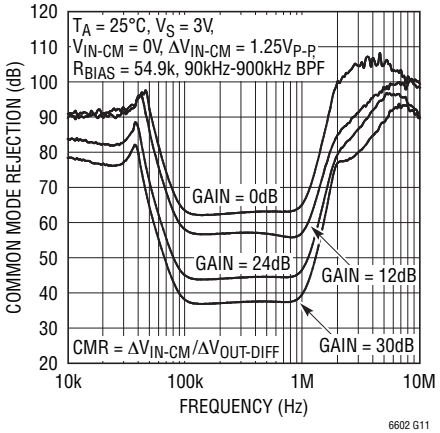


TYPICAL PERFORMANCE CHARACTERISTICS

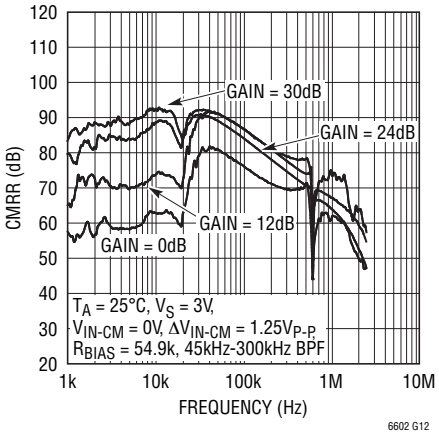
Common Mode Rejection



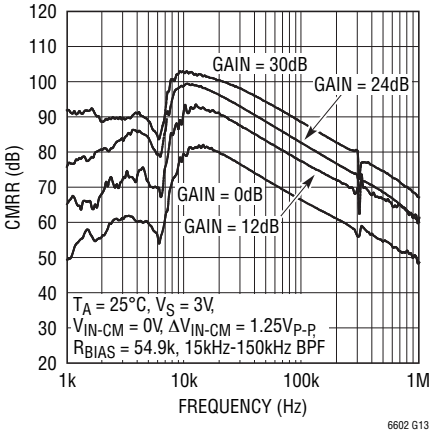
Common Mode Rejection



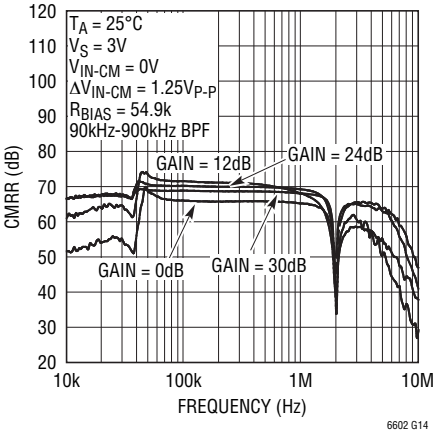
Common Mode Rejection Ratio



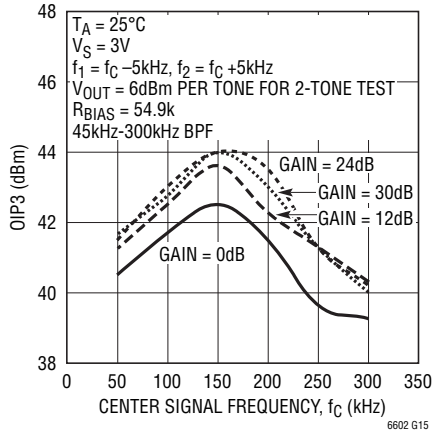
Common Mode Rejection Ratio



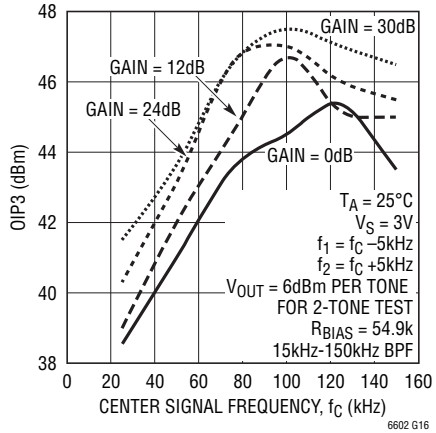
Common Mode Rejection Ratio



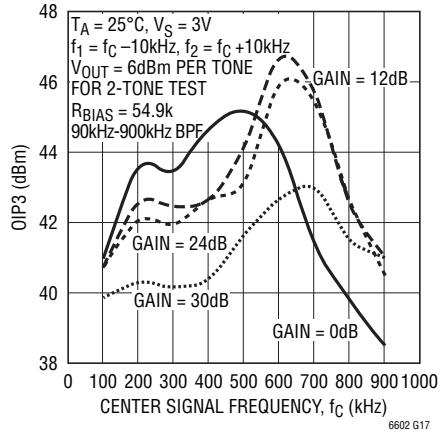
OIP3 vs Average Signal Frequency, f_C



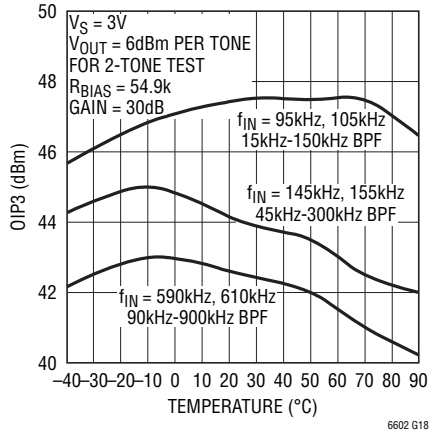
OIP3 vs Average Signal Frequency, f_C



OIP3 vs Average Signal Frequency, f_C

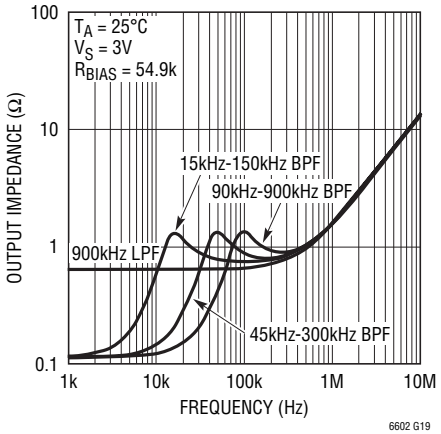


OIP3 vs Temperature

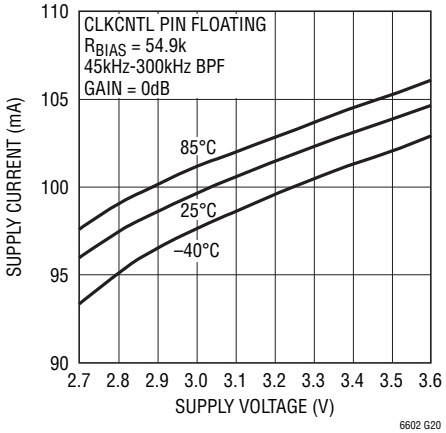


TYPICAL PERFORMANCE CHARACTERISTICS

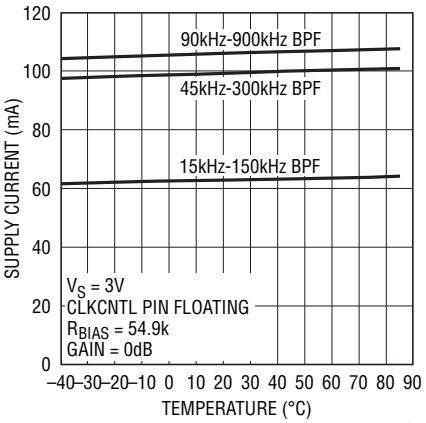
Output Impedance vs Frequency



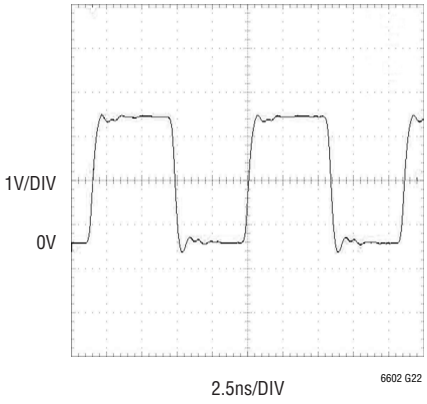
Supply Current vs Supply Voltage



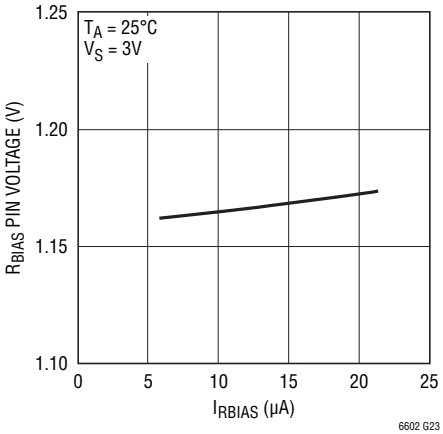
Supply Current vs Temperature



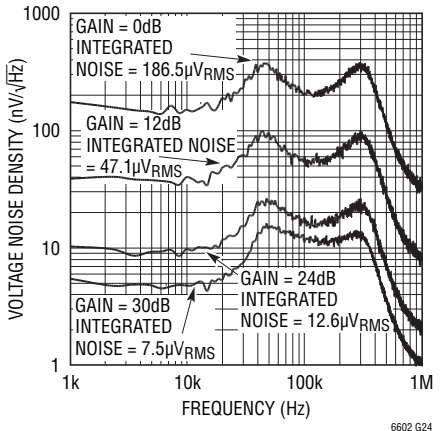
Clock Output Operating at 90MHz



R_{BIAS} Pin Voltage vs I_{RBIAS}

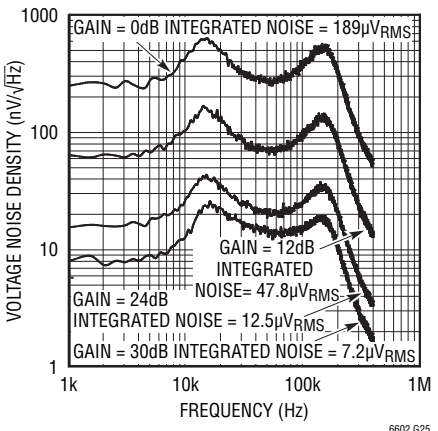


Input Referred Noise Density



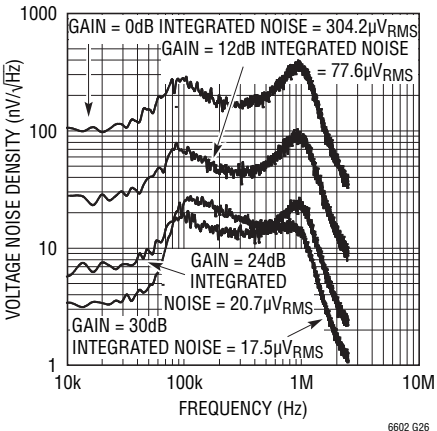
T_A = 25°C, V_S = 3V, EXTERNAL CLOCK
R_{BIAS} = 54.9k, 45kHz-300kHz BPF
INTEGRATED NOISE BW = 1.57MHz

Input Referred Noise Density



T_A = 25°C, V_S = 3V, EXTERNAL CLOCK
R_{BIAS} = 54.9k, 15kHz-150kHz BPF
INTERNAL NOISE BW = 400kHz

Input Referred Noise Density



T_A = 25°C, V_S = 3V, EXTERNAL CLOCK
R_{BIAS} = 54.9k, 90kHz-900kHz BPF
INTERNAL NOISE BW = 2.5MHz

PIN FUNCTIONS

$V+_{IN}$ (Pin 1): Input Voltage Supply (2.7V ≤ V ≤ 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1µF capacitor unless it is tied to $V+_A$ (Pin 2). The bypass should be as close as possible to the IC, but is not as critical as the bypassing of $V+_A$ and $V+_D$ (Pin16).

$V+_A$ (Pin 2): Analog Voltage Supply (2.7V ≤ V ≤ 3.6V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1µF capacitor. The bypass should be as close as possible to the IC.

V_{OCM} (Pin 3): Output common mode voltage reference. If floated, an internal resistive divider sets the voltage on this pin to half the supply voltage (typically 1.5V), maximizing the dynamic range of the filter. If this pin is floated, it must be bypassed with a quality 0.1µF capacitor to ground. This pin has a typical input impedance of 400Ω and may be overdriven. Driving this pin to a voltage other than the default value will reduce the signal range the filter can handle before clipping.

R_{BIAS} (Pin 4): Oscillator Frequency-Setting Resistor Input. The value of the resistor connected between this pin and ground determines the frequency of the master oscillator, and sets the bias currents for the filter networks. The voltage on this pin is held by the LTC6602 to approximately 1.17V. For best performance, use a precision metal film resistor with a value between 54.9k and 200k and limit the capacitance on this pin to less than 10pF. This resistor is necessary even if an external clock is used.

CLKCNTL (Pin 5): Clock Control Input. This three-state input selects the function of CLKIO (Pin 15). Tying the CLKCNTL pin to ground allows the CLKIO pin to be driven by an external clock (CLKIO is the master clock input). If the CLKCNTL pin is floated, the internal oscillator is enabled, but the master clock is not present at the CLKIO pin (CLKIO is a no-connect). If the CLKCNTL pin is tied to $V+_D$ (Pin 16), the internal oscillator is enabled and the master clock is present at the CLKIO pin (CLKIO is the master clock output). To detect a floating CLKCNTL pin, the LTC6602 attempts to pull the pin toward mid-supply. This is realized with two internal current sources, one tied to $V+_D$ and CLKCNTL and the other one tied to ground and CLKCNTL. Therefore, driving the CLKCNTL pin high requires sourcing approximately 15µA. Likewise, driving the CLKCNTL pin low requires sinking 15µA. When the CLKCNTL pin is floated, preferably it should be bypassed by a 1nF capacitor to ground or it should be surrounded by a ground shield to prevent excessive coupling from other PCB traces.

LPF1($\overline{CS}$) (Pin 6): Logic Input. When in pin programmable control mode, this pin is the MSB of the lowpass cutoff frequency control code; in serial control mode, this pin is the chip select input (active low).

+INB, –INB (Pins 7, 8): Channel B differential inputs. The input range and input resistance are described in the Applications Information section. Input voltages which exceed $V+_{IN}$ (Pin 1) should be avoided.

LPF0(SCLK) (Pin 9): Logic Input. When in pin programmable control mode, this pin is the LSB of the lowpass cutoff frequency control code; in serial control mode, this pin is the clock of the serial interface.

HPF1(SDI) (Pin 10): Logic Input. When in pin programmable control mode, this pin is the MSB of the highpass cutoff frequency control code; in serial control mode, this pin is the serial data input.

HPF0(SDO) (Pin 11): Logic Input. When in pin programmable control mode, this pin is the LSB of the highpass cutoff frequency control code; in serial control mode, this pin is the serial data output.

–OUTB, +OUTB (Pins 12, 13): Channel B differential filter outputs. These pins can drive 1k and/or 50pF loads. For larger capacitive loads, an external 100Ω series resistor is recommended for each output. The common mode voltage of the filter outputs is the same as the voltage at V_{OCM} (Pin 3).

GND (Pin 14): Ground. Connect to a ground plane for best performance.

PIN FUNCTIONS

CLKIO (Pin 15): When CLKCNTL (Pin 5) is tied to ground, CLKIO is the master clock input. When CLKCNTL is floated, CLKIO is pulled to ground by a weak, 5µA pulldown. When CLKCNTL is tied to $V+_D$ (Pin 16), CLKIO is the master clock output. When configured as a clock output, this pin can drive 1k and/or 5pF loads. Heavier loads may cause inaccuracies due to supply bounce at high frequencies.

$V+_D$ (Pin 16): Digital Voltage Supply ($2.7V \leq V \leq 3.6V$). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1µF capacitor. The bypass should be as close as possible to the IC.

$\overline{SER}$ (Pin 17): Interface Selection Input. When tied to V_{+D} (Pin 16), the interface is in pin programmable control mode, i.e. the filter gain and cutoff frequencies are programmed by the GAIN1, GAIN0, HPF1, HPF0, LPF1 and LPF0 pin connections. When $\overline{SER}$ is tied to ground, the filter gain, the filter cutoff frequencies and shutdown mode are programmed by the serial interface.

–OUTA, +OUTA (Pins 18, 19): Channel A differential filter outputs. These pins can drive 1k and/or 50pF loads. For larger capacitive loads, an external 100Ω series resistor is recommended for each output. The common mode voltage of the filter outputs is the same as the voltage at V_{OCM} (Pin 3).

$\overline{MUTE}$ (Pin 20): MUTEX input. Drive to ground to disconnect and mute the inputs. Float or drive to $V+_D$ (Pin 16) for normal operation.

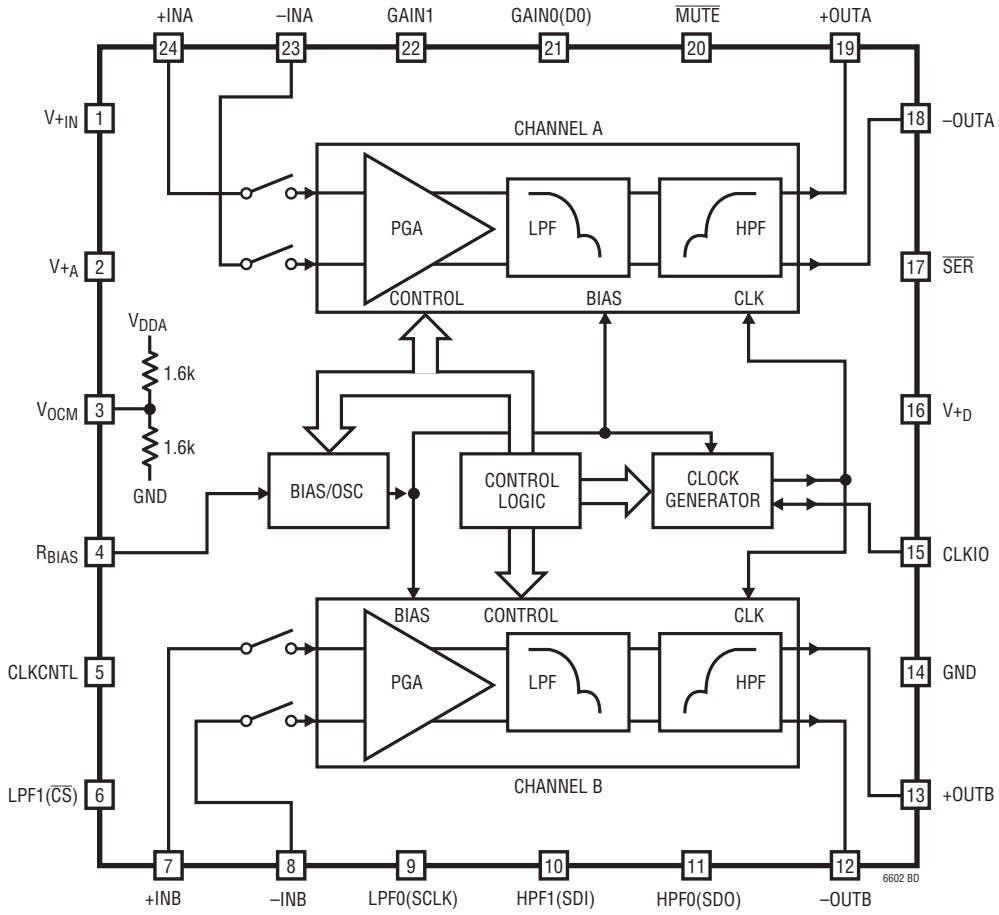
GAIN0(D0) (Pin 21): Logic Input. When in pin programmable control mode, this pin is the LSB of the gain control code; in serial control mode, this pin is the LSB of the serial control register, an output.

GAIN1 (Pin 22): Logic Input. When in pin programmable control mode, this pin is the MSB of the gain control code; in serial control mode, this pin is a no-connect.

–INA, +INA (Pins 23, 24): Channel A differential inputs. The input range and input resistance are described in the Applications Information section. Input voltage levels can range from GND to the $V+_{IN}$ supply rail.

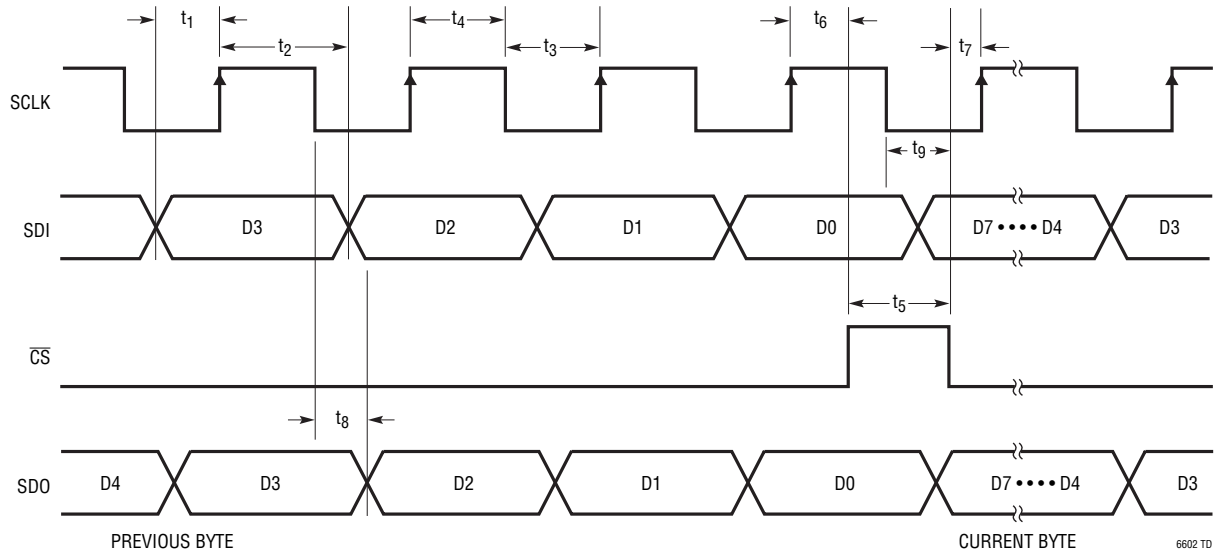
Exposed Pad (Pin 25): Ground. The Exposed Pad must be soldered to PCB.

BLOCK DIAGRAM



TIMING DIAGRAM

Timing Diagram of the Serial Interface



APPLICATIONS INFORMATION

Theory of Operation (Refer to Block Diagram)

The LTC6602 features two matched filter channels, each containing gain control, lowpass, and highpass networks that are controlled by a single control block and clocked by a single clock generator. The gain, lowpass and highpass sections can be independently programmed. The two channels are not independent, i.e. if the gain is set to 24dB, then both channels have a gain of 24dB. The filter can also be programmed to bypass the highpass filter networks, giving a lowpass response. The filter can be clocked with an external clock source, or using the internal oscillator. A resistor connected to the R_{BIAS} pin sets the bias currents for the filter networks and the internal oscillator frequency (unless driven by an external clock). Altering the clock frequency changes the filter bandwidths. This allows the filters to be "tuned" to many different bandwidths.

Pin Programmable Interface

As shown in Figure 1, connecting $\overline{SER}$ to $V+_D$ allows the filter to be directly controlled through the pin programmable control lines GAIN1, GAIN0, HPF1, HPF0, LPF1 and LPF0. The HPF0(SDO) and GAIN0(D0) pins are bidirectional (inputs in pin programmable control mode, outputs in serial mode). In pin programmable control mode, the voltages at HPF0(SDO) and GAIN0(D0) cannot exceed $V+_D$; otherwise, large currents can be injected to $V+_D$ through the internal diodes (see Figure 2). Connecting a 10k resistor at the HPF0(SDO) and GAIN0(D0) pins (see Figure 1) is recommended for current limiting, to less than 10mA. $\overline{SER}$ has an internal pull-up to V_{+D}. None of the logic inputs have an internal pull-up or pull-down.

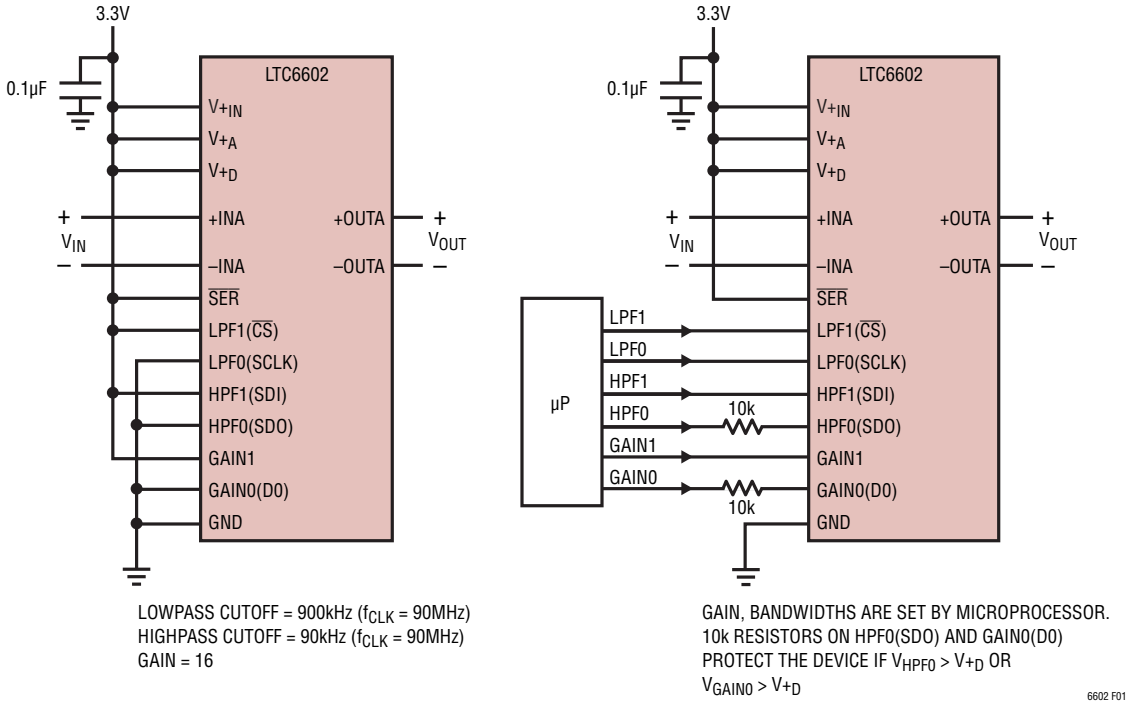


Figure 1. Filter in Pin Programmable Control Mode

APPLICATIONS INFORMATION

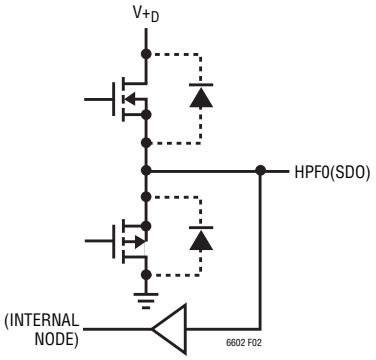


Figure 2. Bidirectional Design of HPF0(SDO) and GAIN0(D0) Pins

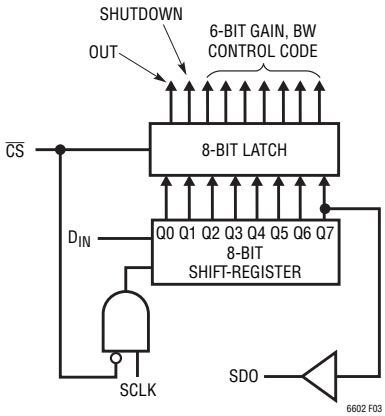


Figure 3. Diagram of Serial Interface (MSB First Out)

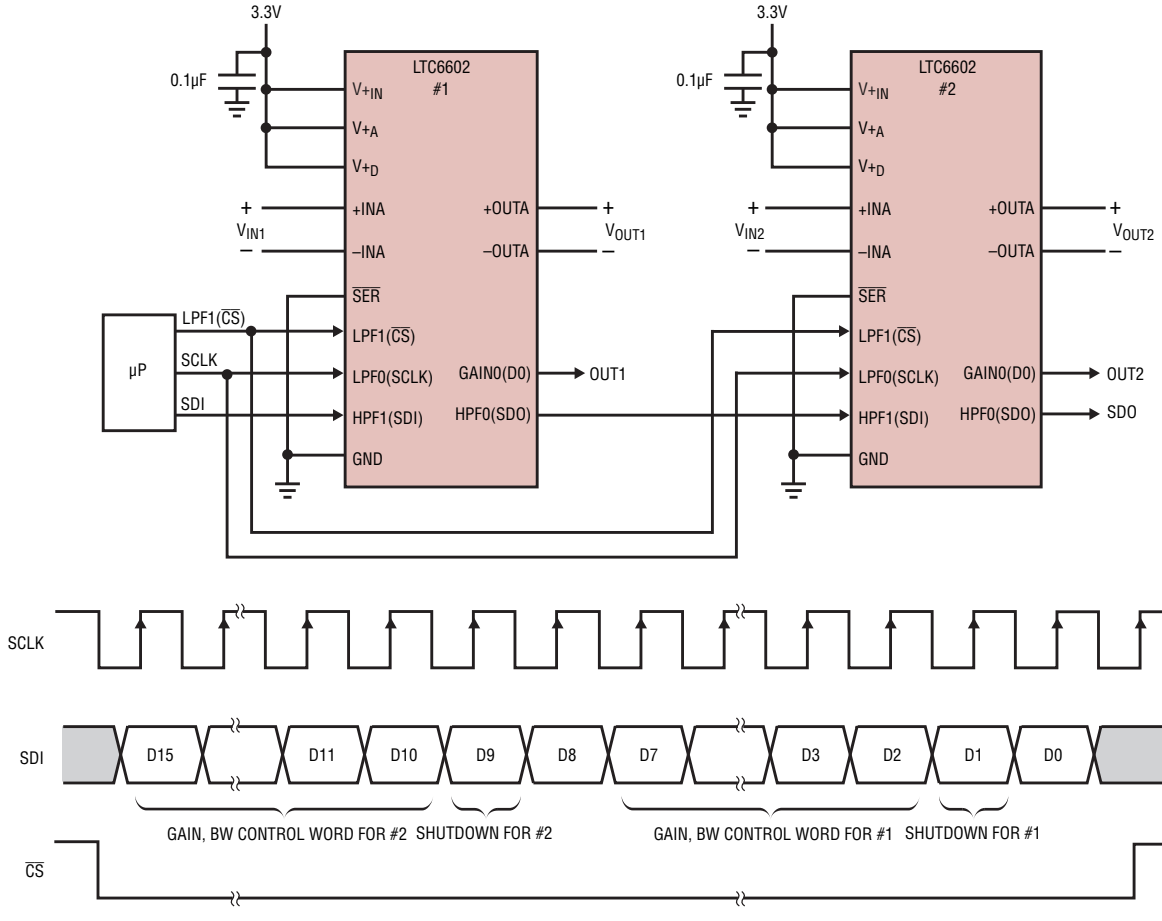


Figure 4. Two Filters in a Daisy Chain

Serial Control Register Definition

D7	D6	D5	D4	D3	D2	D1	D0
GAIN0	GAIN1	LPF0	LPF1	HPF0	HPF1	SHDN	OUT

APPLICATIONS INFORMATION

Serial Interface

Connecting $\overline{SER}$ to ground allows the filter to be controlled through the SPI serial interface. When $\overline{CS}$ is low, the serial data on SDI is shifted into an 8-bit shift-register on the rising edge of the clock (SCLK), with the MSB transferred first (see Figure 3). Serial data on SDO is shifted out on the clock's falling edge. A high $\overline{CS}$ will load the 8 bits of the shift-register into an 8-bit D-latch, which is the serial control register. The clock is disabled internally when $\overline{CS}$ is pulled high. Note: SCLK must be low before $\overline{CS}$ is pulled low to avoid an extra internal clock pulse. SDO is always active in serial mode (never tri-stated) and cannot be "wire-or'ed" to other SPI outputs. In addition, SDO is not forced to zero when $\overline{CS}$ is pulled high.

An LTC6602 may be daisy chained with other LTC6602s or other devices having serial interfaces. Daisy chaining is accomplished by connecting the SDO of the lead chip to the SDI of the next chip, while SCLK and $\overline{CS}$ remain common to all chips in the daisy chain. The serial data is clocked to all the chips then the $\overline{CS}$ signal is pulled high to update all of them simultaneously. Figure 4 shows an example of two LTC6602s in a daisy chained SPI configuration.

GAIN1 and GAIN0 are the gain control bits (register bits D6 and D7 when in serial mode). Their function is shown in Table 1. In serial mode, register bit D1 can be set to '1' to put the device into a low power shutdown mode. Register bit D0 is a general purpose output (Pin 21) when in serial mode.

Table 1. Gain Control

GAIN 1	GAIN 0	PASSBAND GAIN (dB)
0	0	0
0	1	12
1	0	24
1	1	30

Self-Clocking Operation

The LTC6602 features a unique internal oscillator which sets the filter cutoff frequency using a single external resistor connected to the R_{BIAS} pin. The clock frequency is determined by the following simple formula (see Figure 5):

$$f_{CLK} = 494.1MHz \bullet 10k/R_{BIAS}$$

Note: $R_{BIAS} \leq 200k$.

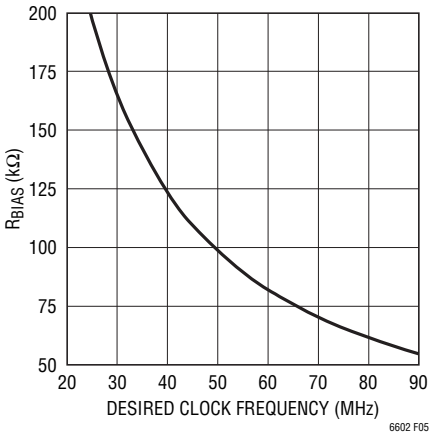


Figure 5. R_{BIAS} vs Desired Clock Frequency

The design is optimized for $V+_A$, $V+_D$ = 3V, f_{CLK} = 90MHz, where the filter cutoff frequency error is typically <3% when a 0.1% external 54.9k resistor is used. With different resistor values and cutoff frequency control settings (HPF1, HPF0, LPF1 and LPF0), the highpass and lowpass cutoff frequencies can be accurately varied from 4.1175kHz to 90kHz and from 41.175kHz to 900kHz, respectively. Table 2 summarizes the cutoff frequencies that can be obtained with an external resistor (R_{BIAS}) value of 54.9k. Note that the cutoff frequencies scale with the clock frequency. For example, if HPF1, HPF0, LPF1 and LPF0 are all equal to zero, and R_{BIAS} is increased from 54.9k to 200k, f_{CLK} will decrease from 90MHz to 24.705MHz, the lowpass cutoff frequency will be reduced from 150kHz to 41.175kHz, and the highpass cutoff frequency will be reduced from 15kHz to 4.1175Hz. The cutoff frequencies that can be obtained with an external resistor value of 200k

APPLICATIONS INFORMATION

are shown in Table 3. When the LTC6602 is programmed for the lowest lowpass cutoff frequency (LPF1, LPF0 = '0'), the power is automatically reduced by about 35%.

Table 2. Cutoff Frequency Control, R_{BIAS} = 54.9k, f_{CLK} = 90MHz

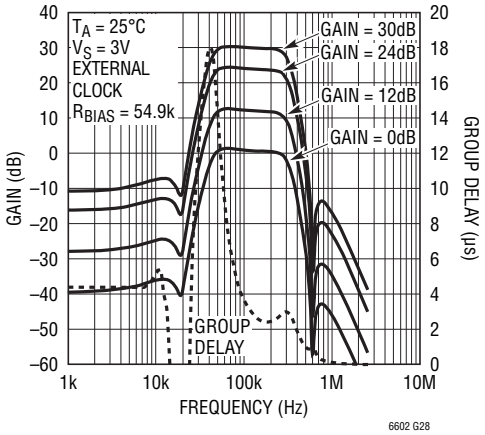
LPF1	LPF0	LOWPASS BW (kHz)	HPF1	HPF0	HIGHPASS BW (kHz)
0	0	150	0	0	15
0	1	300	0	1	45
1	0	900	1	0	90
1	1	900	1	1	Bypass HPF

Table 3. Cutoff Frequency Control, R_{BIAS} = 200k, f_{CLK} = 24.705MHz

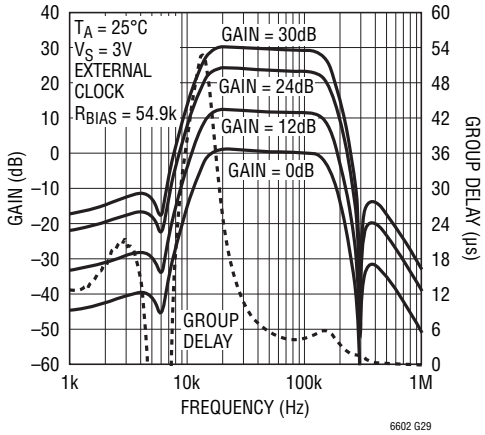
LPF1	LPF0	LOWPASS BW (kHz)	HPF1	HPF0	HIGHPASS BW (kHz)
0	0	41.175	0	0	4.1175
0	1	82.35	0	1	12.3525
1	0	247.05	1	0	24.705
1	1	247.05	1	1	Bypass HPF

The following graphs show a few of the possible combinations of highpass and lowpass filters.

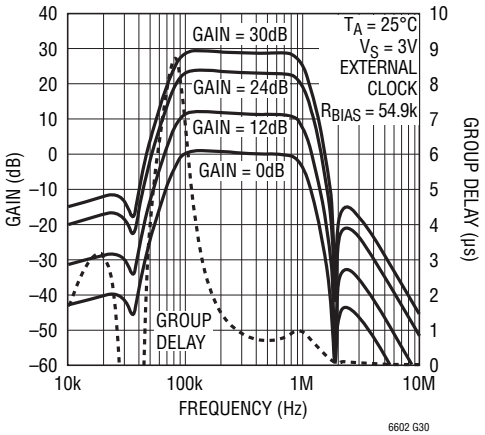
Gain and Group Delay vs Frequency (45kHz to 300kHz Bandpass Response)



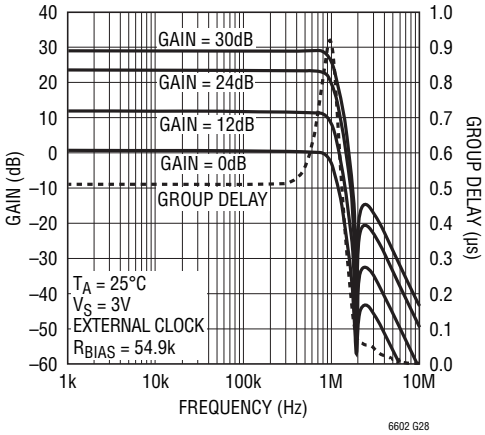
Gain and Group Delay vs Frequency (15kHz to 150kHz Bandpass Response)



Gain and Group Delay vs Frequency (90kHz to 900kHz Bandpass Response)



Gain and Group Delay vs Frequency (900kHz Lowpass Response)



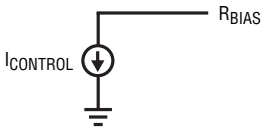
APPLICATIONS INFORMATION

Preserving Oscillator Accuracy

The oscillator is sensitive to transients on the positive supply. The IC should be soldered to the PC board and the PCB layout should include a 0.1µF ceramic capacitor between $V+_A$ (Pin 2) and ground, as close as possible to the IC to minimize inductance. The PCB layout should also include an additional 0.1µF ceramic capacitor between $V+_D$ (Pin 16) and ground. Avoid parasitic capacitance on R_{BIAS} (Pin 4) and avoid routing noisy signals near R_{BIAS}. Use a ground plane connected to Pin 14 and the Exposed Pad (Pin 25).

Alternative Methods of Setting the Clock Frequency of the LTC6602

The oscillator may be programmed by any method that sinks a current out of the R_{BIAS} pin. The circuit in Figure 6 sets the clock frequency by using a programmable current source and in the expression for f_{CLK}, the resistor R_{BIAS} is replaced by the ratio of $1.17V/I_{CONTROL}$. Because the voltage of the R_{BIAS} pin is approximately 1.17V ±5%, the Figure 6 circuit is less accurate than if a resistor controls the clock frequency.



$f_{CLK} = 10k \bullet (494.1MHz/1.17V) \bullet I_{CONTROL}(A)$

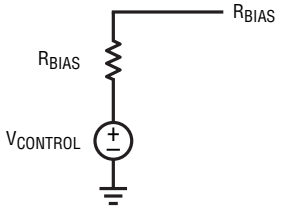
6602 F06

Figure 6. Current Controlled Clock Frequency

Figure 7 shows the LTC6602's oscillator configured as a VCO. A voltage source is connected in series with the R_{BIAS} resistor. The clock frequency, f_{CLK}, will vary with $V_{CONTROL}$. Again, this circuit decouples the relationship between the current out of the R_{BIAS} pin and the voltage of the R_{BIAS} pin; the frequency accuracy will be degraded. The clock frequency, however, will increase monotonically with decreasing $V_{CONTROL}$.

Operation Using an External Clock

The LTC6602 may be clocked by an external oscillator for tighter bandwidth control by pulling CLKCNTL (Pin 5) to ground and driving a clock into CLKIO (Pin 15). If an external clock is used, the R_{BIAS} resistor is still necessary. The value of R_{BIAS} must be no larger than the value that would be required for using the internal oscillator. For example, a 100k resistor would program the internal oscillator for 49.41MHz, so an external oscillator frequency of 49.41MHz would require an R_{BIAS} resistance of no more than 100k. If the value of R_{BIAS} is too large, the filters will not receive a large enough bias current, possibly causing errors due to insufficient settling.



$f_{CLK} = 494.1MHz \bullet (10k/R_{BIAS}) \bullet (1 - V_{CONTROL}/1.17V)$

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Figure 7. Voltage Controlled Clock Frequency

APPLICATIONS INFORMATION

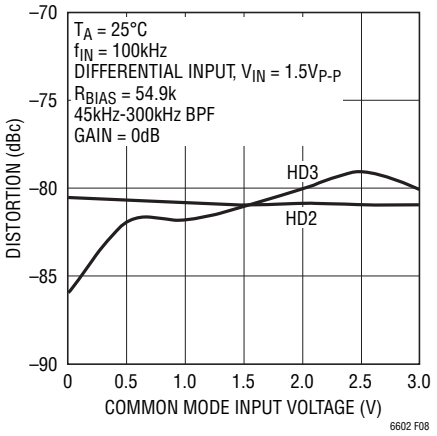


Figure 8. Distortion vs Common Mode Input Voltage (3V)

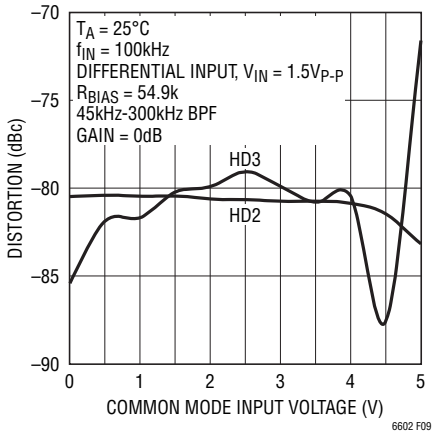


Figure 9. Distortion vs Common Mode Input Voltage (5V)

Input Common Mode and Differential Voltage Range

The input signal range extends from zero to the $V+_{IN}$ supply voltage. This input supply can be tied to $V+_A$ and $V+_D$, or driven up to 5.5V for increased input common mode voltage range. Figures 8 and 9 show the distortion of the filter versus common mode input voltage with a $1.5V_{P-P}$ differential input signal.

For best performance, the inputs should be driven differentially. For single ended signals, connect the unused input to V_{OCM} (Pin 3) or to a quiet DC reference voltage. To achieve the best distortion performance, the input signal should be centered around the DC voltage of the unused input.

Refer to the Typical Performance Characteristics section to estimate the distortion for a given input level.

Dynamic Input Impedance

The unique input sampling structure of the LTC6602 has a dynamic input impedance which depends on the configuration and the clock frequency. This dynamic input impedance has both a differential component and a common mode component. The common mode input impedance is a function of the clock frequency and the control bit LPF1. The differential input impedance is a function of the clock frequency and the control bits LPF1, GAIN1 and GAIN0. Table 4 shows the typical input impedances for a clock frequency of 90MHz. These input impedances are all proportional to $1/f_{CLK}$, so if the clock frequency were reduced by half to 45MHz, the impedances would be doubled. The typical part to part variation in dynamic input impedance for a given clock frequency is –20% to +35%.

Table 4. Differential, Common Mode Input Impedances, f_{CLK} = 90MHz

GAIN1	GAIN0	LPF1	DIFFERENTIAL INPUT IMPEDANCE (kΩ)	COMMON MODE INPUT IMPEDANCE (kΩ)
0	0	0	16	20
0	0	1	6	6.7
0	1	0	8	20
0	1	1	2.8	6.7
1	0	0	2.6	20
1	0	1	1.8	6.7
1	1	0	2.4	20
1	1	1	1.3	6.7

Output Common Mode and Differential Voltage Range

The output voltage is a fully differential signal with a common mode level equal to the voltage at V_{OCM}. Any of the filter outputs may be used as single-ended outputs, although this will degrade the performance. The output voltage range is typically 0.5V to $V+_A$ – 0.5V ($V+_A$ = 2.7V to 3.6V).

The common mode output voltage can be adjusted by overdriving the voltage present on V_{OCM}. To maximize the undistorted peak-to-peak signal swing of the filter, the V_{OCM} voltage should be set to $V+_A/2$. Note that the

APPLICATIONS INFORMATION

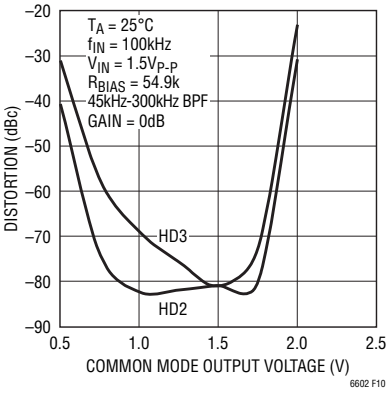


Figure 10. Distortion vs Common Mode Output Voltage

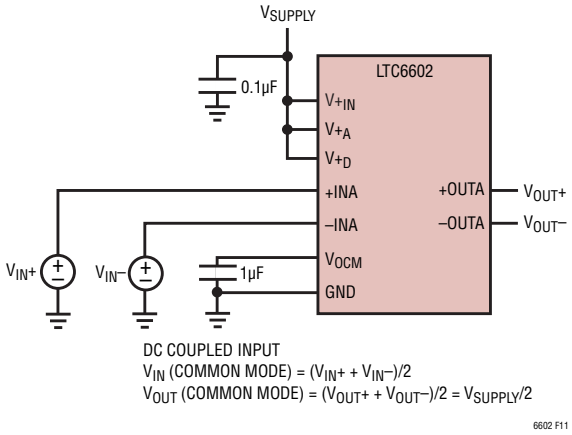
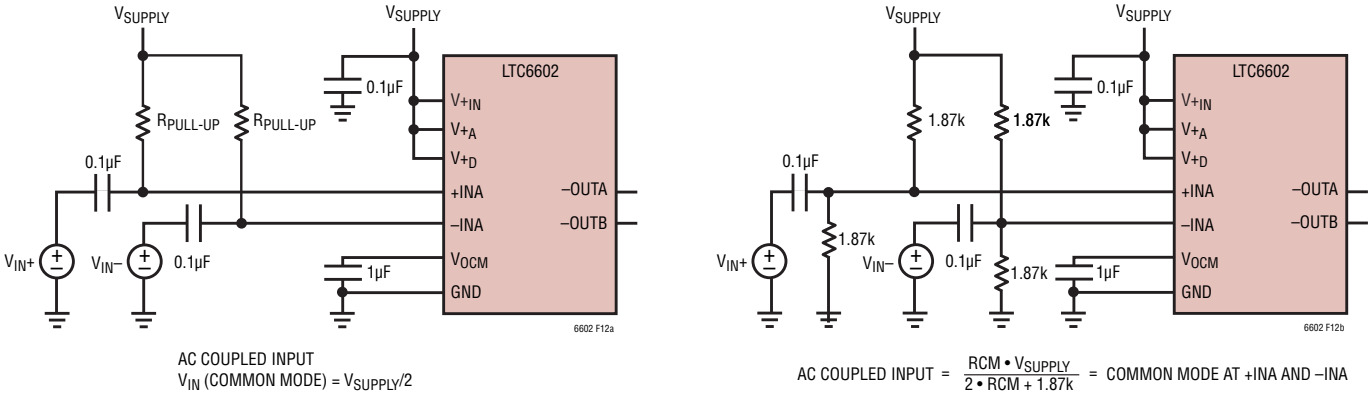


Figure 11. DC Coupled Inputs



(a) Fixed Lowpass Cutoff Frequency

(b) Variable Lowpass Cutoff Frequency

Figure 12. AC Coupled Inputs

output common mode voltages of the two channels are not independent as they are both set by the V_{OCM} pin. Figure 10 illustrates the distortion versus output common mode voltage for a $1.5V_{P-P}$ differential input voltage and a common mode input voltage that is equal to mid-supply.

Interfacing to the LTC6602

The input and output common mode voltages of the LTC6602 are independent. The input common mode voltage is set by the signal source if DC coupled, as shown in Figure 11. If the inputs are AC coupled, the input common mode voltage will pulled to ground by an equivalent resistance of R_{CM}, shown in Table 4. This does not affect the filter's performance as long as the input amplitude is less than $0.5V_{P-P}$. At low filter gain settings, a larger input voltage swing may be desired. Figure 12 shows two circuits with AC coupled inputs. In a fixed lowpass cutoff frequency, connecting resistors between each input and $V+_{IN}$ will pull the input common mode voltage up, increasing the input signal swing (Figure 12a). The resistance, $R_{PULL-UP}$, necessary to set the input common mode voltage, V_{ICM}, to any desired level can be calculated by

$$R_{PULL-UP} = R_{CM}\left(\frac{V_{SUPPLY}}{V_{ICM}} - 1\right)$$

where

$R_{CM} = 20k \bullet 90MHz/f_{CLK}$ for LPFI = 0

$R_{CM} = 6.7k \bullet 90MHz/f_{CLK}$ for LPFI = 1

For example, if the lowpass cutoff frequency is set to 300kHz, 20k resistors connected between each input and $V+_{IN}$ will set the input common mode voltage to mid-supply.

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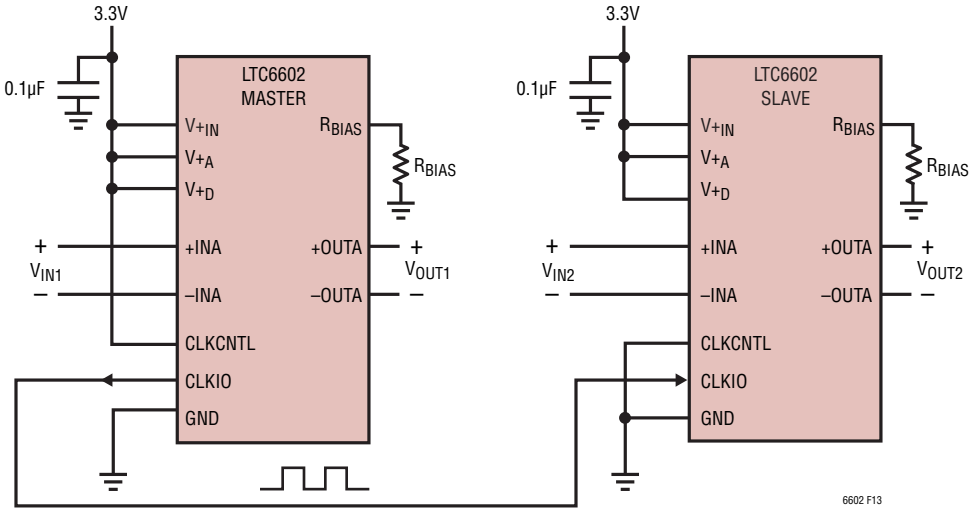


Figure 13. Two Filters in a Master/Slave Configuration

If the lowpass cutoff frequency varies then the Figure 12b circuit must be used.

The output common mode voltage is equal to the voltage of the V_{OCM} pin. The V_{OCM} pin is biased to one half of the supply voltage by an internal resistive divider (see Block Diagram). To alter the common mode output voltage, V_{OCM} can be driven with an external voltage source or resistor network. If external resistors are used, it is important to note that the internal 1.6k resistors can vary ±30% (their ratio varies only ±1%). The filter outputs can also be AC coupled.

The LTC6602 can be interfaced to an A/D converter by pulling CLKCNTL (Pin 5) to $V+_D$. This configures CLKIO (Pin 15) as a clock output, which can be used to drive the clock input of the A/D converter. This allows the A/D converter to be synchronized with the filter sampling clock, avoiding "beat frequencies" and simplifying the board layout. Any routing attached to the CLKIO pin should be as short as possible, in order to minimize ringing.

Similarly, two LTC6602s can be connected in a master/slave configuration as shown in Figure 13. This results in four matched filter channels, all synchronized to the same clock. The master has its CLKCNTL pin pulled to $V+_D$, configuring its CLKIO pin as an output, while the slave has its CLKCNTL pin pulled to ground, configuring its CLKIO pin as an input.

Output Drive

The filter outputs can drive 1k and/or 50pF loads connected to AC ground with a 0.5V to 2.5V signal (corresponding to a $4V_{P-P}$ differential signal). For differential loads (loads connected between +OUTA and –OUTA or +OUTB and –OUTB) the outputs can produce a $4V_{P-P}$ signal across 2k and/or 25pF. For smaller signal amplitudes, the outputs can drive correspondingly heavier loads. For larger capacitive loads, an external 50Ω series resistor is recommended for each output.

APPLICATIONS INFORMATION

Mute Function

The LTC6602 features a mute function which is asserted by pulling $\overline{\text{MUTE}}$ (Pin 20) to ground. This breaks the signal path that leads from the input pins to the filter networks, attenuating the input signal by at least 20dB. The mute function can be used to protect the filter inputs from large transients. The filter clock continues to run when the filter is muted, allowing for a fast recovery time when $\overline{\text{MUTE}}$ is deasserted. Typically, the recovery time is less than 5µs, as shown in Figure 14. When the mute function is asserted, the differential input impedance becomes very high, but the common mode input impedance to ground remains the same. This keeps the input common mode voltage stable when muted, even when the inputs are AC coupled. Connecting GAIN0(D0) to $\overline{\text{MUTE}}$ allows for serial control of the mute function. $\overline{\text{MUTE}}$ has an internal pull-up to $V+_D$.

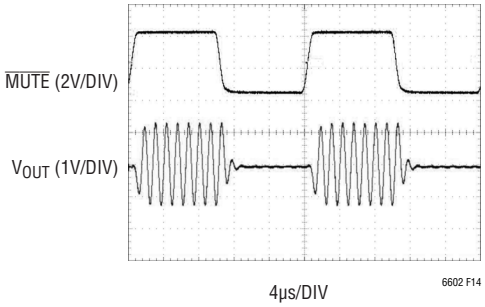


Figure 14. Mute Function Recovery Time

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output. The clock feedthrough is measured with +INA and –INA (or +INB, –INB) tied to V_{OCM} and depends on the PC board layout and the power supply decoupling. The clock feedthrough can be reduced with a simple RC post filter.

DC Offset

The output DC offset of the LTC6602 is less than ±15mV. To obtain optimum DC offset performance, appropriate PC board layout techniques should be used. The filter IC should be soldered to the PC board. The power supplies should be well decoupled including 0.1µF ceramic capacitors from $V+_D$ (Pin 16) and $V+_A$ (Pin 2) to ground. A ground plane should be used. Noisy signals should be isolated from the filter input pins.

The output DC offset typically changes less than ±2mV when the clock frequency varies from 24.705MHz to 90MHz. The offset is measured by connecting the inputs to V_{OCM} and measuring the differential voltage at the filter's output.

Aliasing

Aliasing is an inherent phenomenon of sampled data filters. Significant aliasing only occurs when the frequency of the input signal approaches the sampling frequency or multiples of the sampling frequency. The ratio of the LTC6602 input sampling frequency to the clock frequency, f_{CLK}, is determined by the state of control bit LPF1. If LPF1 is set to '0', the input sampling frequency is equal to $f_{CLK}/3$. If LPF1 is set to '1', the input sampling frequency is equal to f_{CLK}. Input signals with frequencies near the input sampling frequency will be aliased to the passband of the filter and appear at the output unattenuated.

A simple LC anti-aliasing filter is recommended at the filter inputs to attenuate frequencies near the input sampling frequency that will be aliased to the passband. For example, if the clock frequency is set to 90MHz and the lowpass cutoff frequency of the filter is set to it's maximum (LPF1 = '1'), the lowest frequency that would be aliased to the passband would be $f_{CLK} – f_{CUTOFF}$, i.e. 90MHz – 900kHz = 89.1MHz. In order to attenuate this frequency by 40dB, an LC filter with a cutoff frequency of 8.91MHz or lower would be required at the filter inputs. The capacitor connected between the LTC6602 filter inputs should be at least 150pF to provide sufficient charge to the input sampler. If there is no anti-aliasing filter, the LTC6602 filter inputs should be driven by a low impedance source (<100Ω).

Wideband Noise

The wideband noise of the filter is the RMS value of the device's output noise spectral density. The wideband noise voltage is used to determine the operating signal-to-noise ratio at a given distortion level. The wideband noise is nearly independent of the value of the clock frequency and excludes the clock feedthrough. Most of the wideband noise is concentrated in the filter passband and cannot be removed with post filtering.

APPLICATIONS INFORMATION

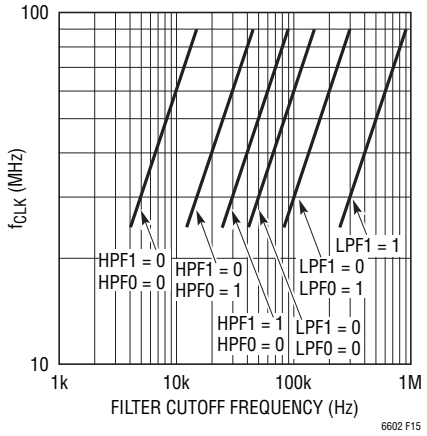


Figure 15. f_{CLK} vs Filter Cutoff Frequencies

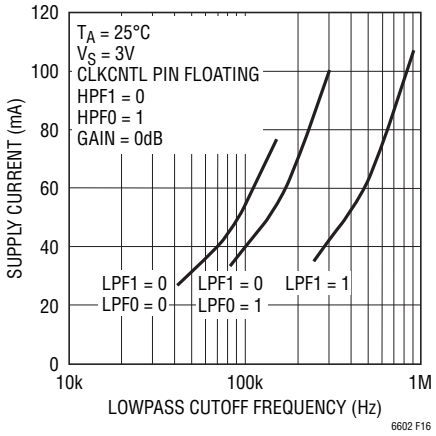


Figure 16. Supply Current vs Lowpass Cutoff Frequency

Table 5. Total Input Referred Integrated Noise Voltage (Passband Gain = 30dB)

LPF1	LPF0	HPF1	HPF0	Noise Voltage
0	0	0	0	–90dBm
0	1	0	1	–89dBm
1	X	1	0	–82dBm

Power Supply Current

The power supply current depends on the state of the lowpass cutoff frequency controls (LPF1, LPF0) and the value of R_{BIAS}. When the LTC6602 is programmed for the lowest lowpass cutoff frequency (LPF1 = LPF0 = '0'), the supply current is reduced by about 35% relative to the supply current for the higher bandwidth settings. Power supply current vs. cutoff frequency for various bandwidth settings is shown in the Typical Performance Characteristics section. The LTC6602 can be programmed through the serial interface to enter into a low power shutdown mode as described in the Serial Interface section. The power supply current during shutdown is less than 235µA.

Supply Current Versus Noise Tradeoff

The passband of the LTC6602 is determined by the master clock frequency (which is set by R_{BIAS} when the internal oscillator is used), HPF1, HPF0, LPF1 and LPF0. The LTC6602 is optimized for use with R_{BIAS} having a value between 200k and 54.9k to set the internal oscillation frequency from 24.705MHz to 90MHz. Both lowpass and highpass corner frequencies are proportional to the clock frequency (internal or external). To extend the filter's operational frequency range, the master clock is divided down before reaching the filter. LPF1 and LPF0 set the division ratio of the lowpass clock while HPF1 and HPF0 set the division ratio of the highpass clock. Figure 15 shows the possible cutoff frequencies versus f_{CLK}, HPF1, HPF0, LPF1 and LPF0. Overlapping frequency ranges allow more than one possible choice of bandwidth settings for some cutoff frequencies. Figure 16 shows supply current as a function of the lowpass cutoff frequency, LPF1 and LPF0. Note that the higher bandwidth setting always gives the minimum supply current for a given cutoff frequency. The total integrated noise voltage for a passband gain of 30dB is shown in Table 5. Note that the noise is higher for the higher bandwidth settings. This creates a tradeoff between supply current and noise. For a given cutoff frequency, using the highest possible bandwidth setting gives the minimum supply current at the expense of higher noise.

APPLICATIONS INFORMATION

The LTC6602, an Adaptable Baseband Filter for an RFID Reader

A radio-frequency identification (RFID) system is an auto-id technology that identifies any object that contains a coded tag. An RFID system consists of a reader (or interrogator) and a tag. An RFID system capable of identifying multiple tags at a maximum operating distance operates in the UHF frequency range. A UHF reader transmits information to a tag by modulating an RF signal in the 860MHz to 960MHz frequency range. Typically a tag is passive, meaning that it receives all of its operating energy from a reader that transmits a continuous wave (CW) RF signal to power a tag. A tag responds by modulating the reflection coefficient of its antenna, thereby backscattering an information signal to the reader. Reliable detection of a tag signal requires communication protocols that define the physical and operating interaction between readers and tags. The latest UHF RFID protocol, the Electronic Product Code™ (EPC) global class-1 generation 2 standard (C1G2), have been accepted worldwide and is also known as ISO 18000-6C. The C1G2 standard defines a reader to tag and a tag to reader communication using a flexible set of signal modulation, data encoding, data rates and command procedures. C1G2 specifies reader and tag data symbols using pulse-interval encoding. Tag signal detection requires measuring the time interval between signal transitions (a data "1" symbol has a longer interval than a data "0" symbol). The reader initiates a tag inventory by sending a signal that instructs a tag to set its backscatter data rate and encoding. C1G2 certified RFID readers can operate in an RF environment where many readers are in close proximity. The three operating modes of C1G2, single interrogator, multiple interrogator and dense interrogator, define the spectral limits of reader and tag signals for an optimum balance of reliable multitag detection and high data throughput (for more information on C1G2, consult the references at the end of this design note). The advantages of C1G2 complex protocols can be realized by using a reader whose receiver contains a high linearity direct conversion I and Q demodulator, a low noise amplifier, a dual baseband filter with variable gain and bandwidth and a dual analog to digital converter (ADC).

Certified C1G2 UHF RFID readers can adapt to a great variety of operating conditions. To achieve operating flexibility a reader's baseband circuits must include an adaptable bandwidth filter. Figure 17 shows an LTC6602 based filter circuit that uses SPI control to vary the filter's bandwidth to adjust for the C1G2 complex set of data rates, encoding and modulation. The filter's clock frequency is set by the SPI control of 8-bit LTC2630 DAC (digital to analog converter). The DAC voltage through a resistive divider sets the current into the LTC6602 R_{BIAS} pin. The resistive divider sets the clock frequency range for a DAC voltage range 0V to 3V. For the resistor values in Figure 17 (191k and 61.9k) the clock frequency range is 40MHz to 100MHz (234.4kHz per bit). The lowpass and highpass division ratio is set by the SPI control of the LTC6602. The cutoff range for the highpass filter is 6.7kHz to 100kHz and for the lowpass filter is 66.7kHz to 1MHz. The optimum filter bandwidth setting can be adjusted by a software algorithm and is a function of the reader's data clock, data rate, encoding and modulation. The filter bandwidth must be sufficiently narrow to maximize the dynamic range to the ADC input and wide enough to preserve signal transitions and pulse width. If the filter setting is optimum then a DSP algorithm can reliably detect tag data. Figure 18a shows the filter's time response to a typical tag symbol sequence (a "short" pulse interval followed by a "long" pulse interval). The lowpass cutoff frequency is set equal to the reciprocal of the shortest interval (f_{CUTOFF} = 1/10µs = 100kHz). If the lowpass cutoff frequency is lower the signal transition and time interval will be distorted beyond recognition by any tag signal detection algorithm. The setting of the highpass cutoff frequency is more qualitative than specific. The highpass cutoff frequency must be lower than the reciprocal of the longest interval (for Figure 18 example, highpass f_{CUTOFF} < 1/20µs < 50kHz) and as high as possible to decrease the receiver's low frequency noise (baseband amplifier and down-converted phase and amplitude noise). Figures 18a and 18b show the filter's total response (lowpass plus highpass filter). The filter's output is shown with 30kHz and a 10kHz highpass cutoff frequency setting. Comparing the filter outputs with a 10kHz and a 30kHz highpass setting, the signal transitions and time intervals of the 10kHz output are adequate for

APPLICATIONS INFORMATION

detecting the symbol sequence (in an RFID environment, noise will be superimposed on the output signal). In general, increasing the lowpass f_{CUTOFF} and/or decreasing the highpass f_{CUTOFF} "enhances" signal transitions and intervals and increases filter output noise.

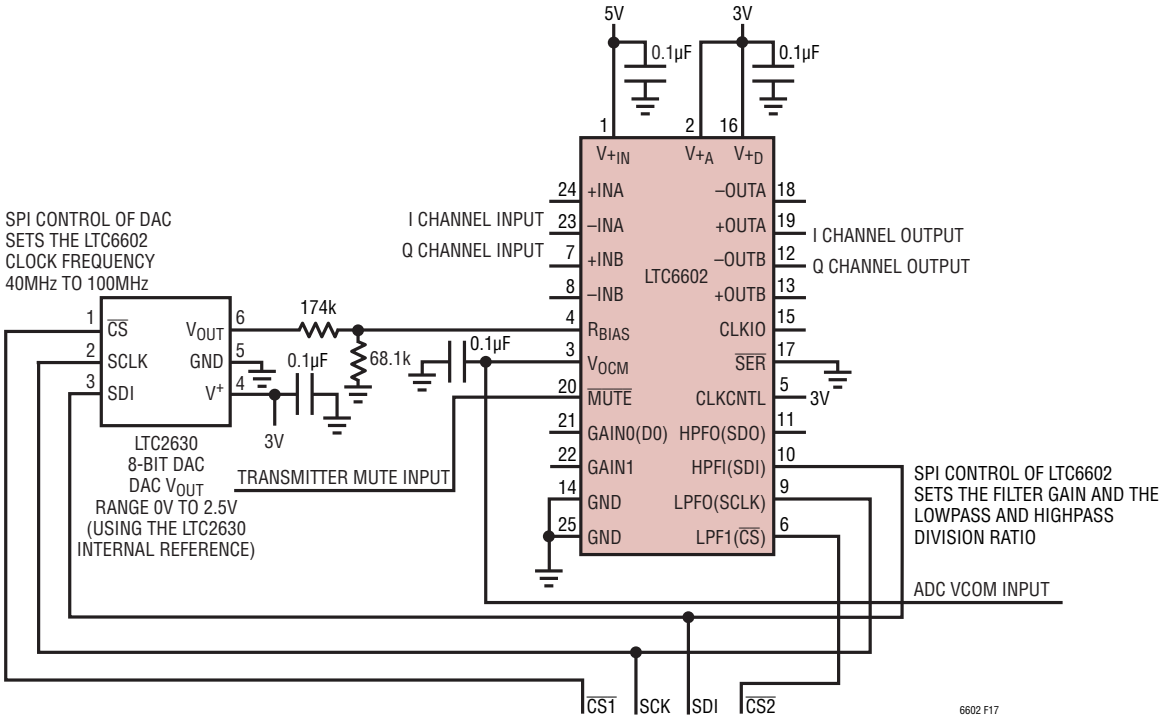


Figure 17. An Adaptable RFID Baseband Filter with SPI Control

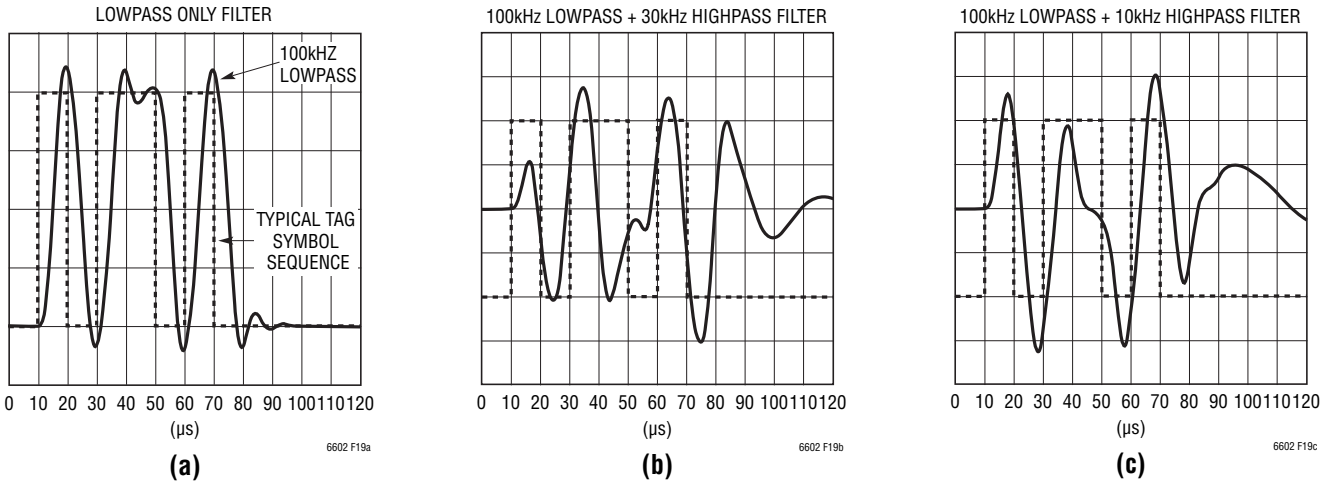
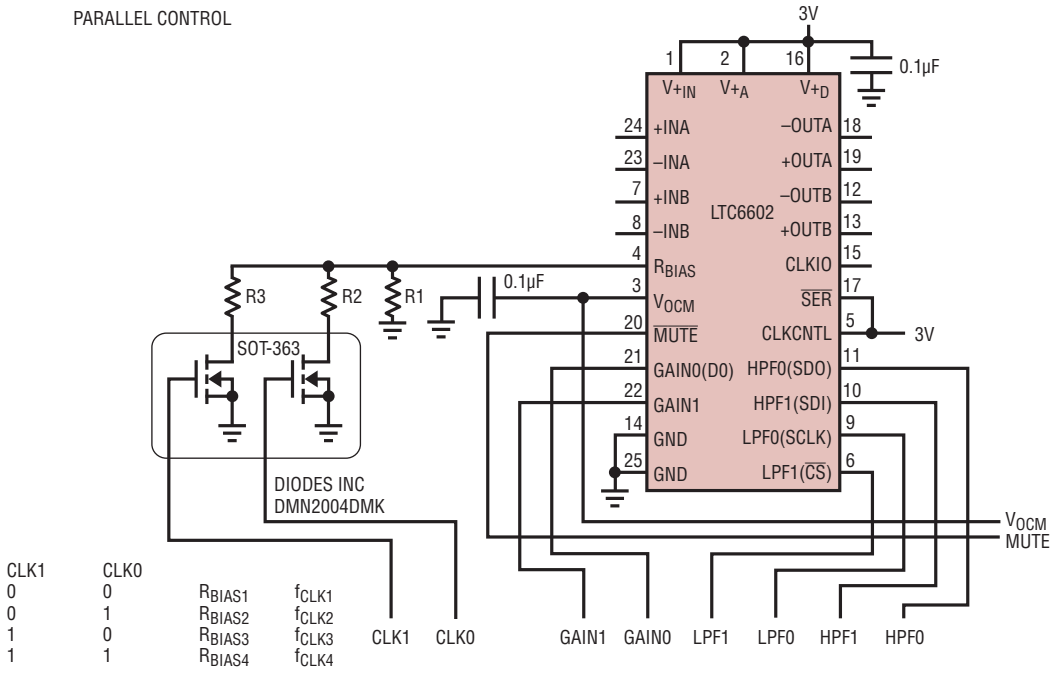


Figure 18. Filter Transient Response to a Tag Symbol Sequence

TYPICAL APPLICATIONS

Switching the R_{BIAS} Resistor

PARALLEL CONTROL



CLK1	CLK0		
0	0	R_{BIAS1}	f_{CLK1}
0	1	R_{BIAS2}	f_{CLK2}
1	0	R_{BIAS3}	f_{CLK3}
1	1	R_{BIAS4}	f_{CLK4}

$R_{BIAS1} > R_{BIAS2}$ OR R_{BIAS3}

$$R_{BIAS} = \frac{4941}{f_{CLK}}$$

R_{BIAS1} IN k
f_{CLK} IN MHz

DESIGN PROCEDURE
1. CHOOSE f_{CLK1}, f_{CLK2} AND f_{CLK3}
2. CALCULALTE R_{BIAS1}, R_{BIAS2} AND R_{BIAS3}
3. CALCULATE R2, R3 AND R_{BIAS4}

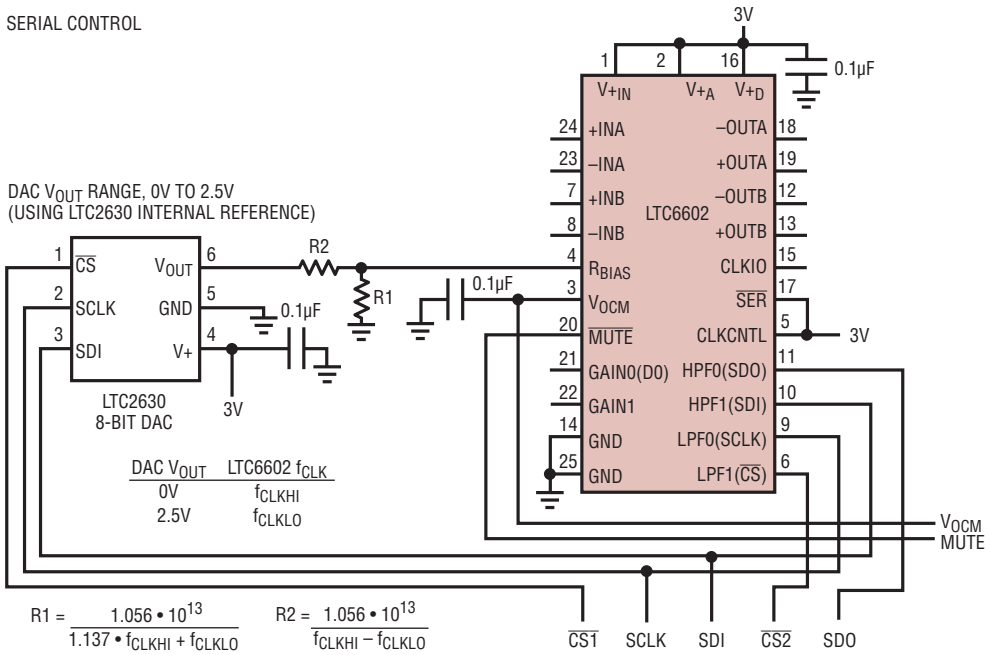
$R1 = R_{BIAS1}$

$$R2 = \frac{R_{BIAS1} \bullet R_{BIAS2}}{R_{BIAS1} - R_{BIAS2}}$$

$$R3 = \frac{R_{BIAS1} \bullet R_{BIAS3}}{R_{BIAS1} - R_{BIAS3}}$$

$$R_{BIAS4} = \frac{R1 \bullet R2 \bullet R3}{R1 \bullet (R2 + R3) + R2 \bullet R3}$$

SERIAL CONTROL



DAC V_{OUT}	LTC6602 f_{CLK}
0V	f_{CLKHI}
2.5V	f_{CLKLO}

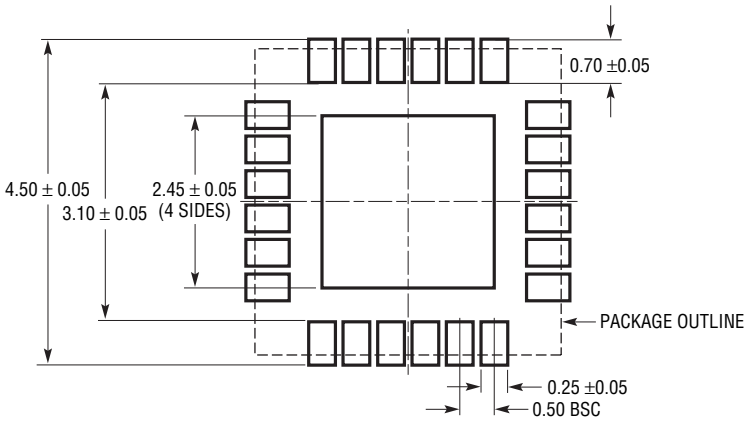
$$R1 = \frac{1.056 \bullet 10^{13}}{1.137 \bullet f_{CLKHI} + f_{CLKLO}}$$

$$R2 = \frac{1.056 \bullet 10^{13}}{f_{CLKHI} - f_{CLKLO}}$$

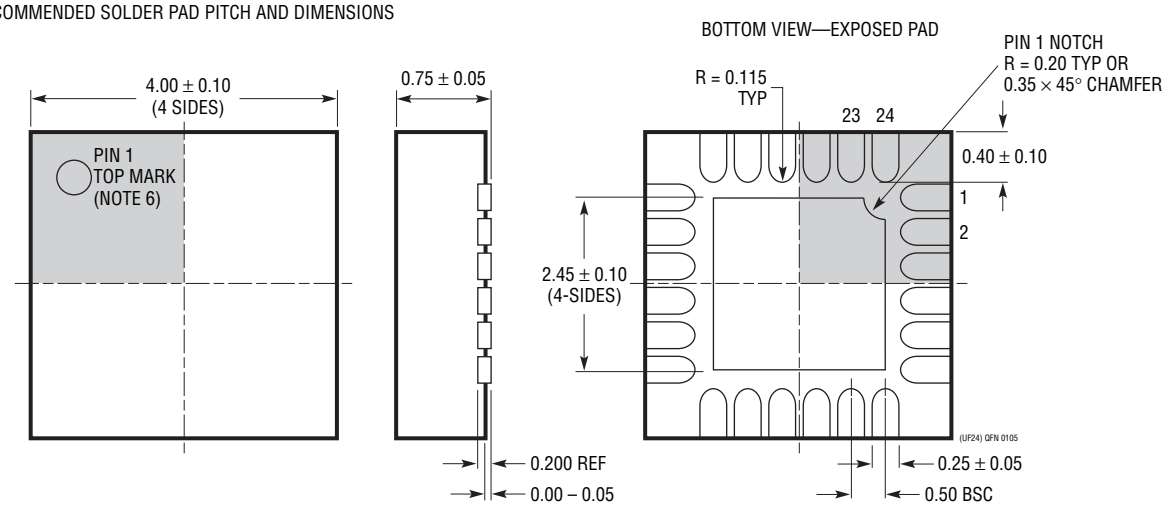
6602 TA02

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	10/10	Updated Filter Phase Either Channel Min value for f_{IN} = 125kHz to –143 in Electrical Characteristics section	3
		Updated all Max values for Supply Current in Electrical Characteristics section	4