Dual Matched 7MHz Filter with Low Noise, Low Distortion Differential Amplifier

FEATURES

- **Two Matched 7MHz 2nd Order Lowpass Filters with Differential Amplifiers**
  - **Gain Match: ±0.35dB Max, Passband**
  - **Phase Match: ±1.2° Max, Passband**
  - **Single-Ended or Differential Inputs**
- **< –90dBc Distortion in Passband**
- **2.1nV/√Hz Op Amp Noise Density**
- Pin-Selectable Gain (0dB/12dB/14dB)
- Pin-Selectable Power Consumption (0.35mA/16.2mA/33.1mA)
- Rail-to-Rail Output Swing
  - Adjustable Output Common Mode Voltage Control
  - Buffered, Low Impedance Outputs
- 2.7V to 5.25V Supply Voltage
- Small 22-Pin 6mm × 3mm × 0.75mm DFN Package

APPLICATIONS

- WCDMA ADC Driver/Filter
- Antialiasing Filter
- Single-Ended to Differential Conversion
- DAC Smoothing Filter
- Zero-IF Direct Conversion Receivers

DESCRIPTION

The LTC®6605-7 contains two independent, fully differential amplifiers configured as matched 2nd order lowpass filters. The f_{-3dB} of the filters is adjustable in the range of 6.5MHz to 10MHz.

The internal op amps are fully differential, feature very low noise and distortion, and are compatible with 16-bit dynamic range systems. The inputs can accept single-ended or differential signals. An input pin is provided for each amplifier to set the common mode level of the differential outputs.

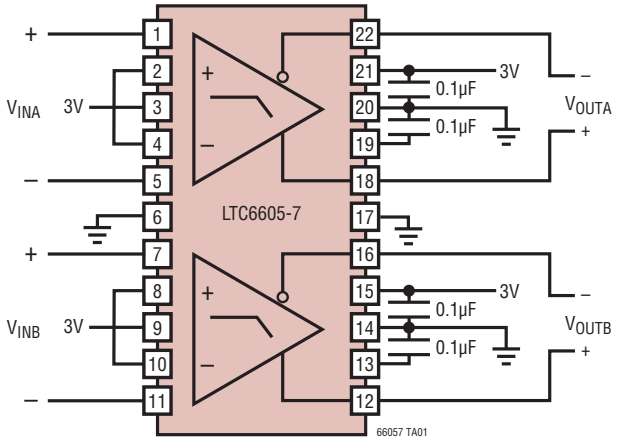
Internal laser-trimmed resistors and capacitors determine a precise, very well matched (in gain and phase) 7MHz 2nd order filter response. A single optional external resistor per channel can tailor the frequency response for each amplifier.

Three-state BIAS pins determine each amplifier's power consumption, allowing a choice between shutdown, medium power or full power.

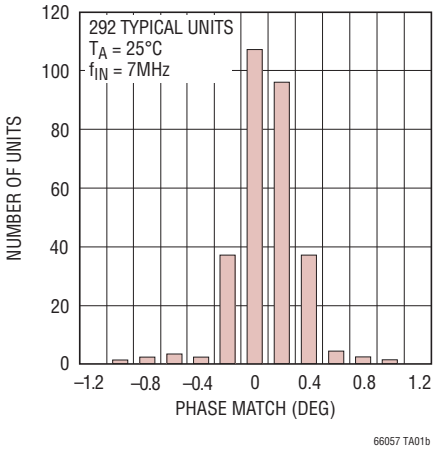
The LTC6605-7 is available in a compact 6mm × 3mm 22-pin leadless DFN package and operates over a –40°C to 85°C temperature range.

TYPICAL APPLICATION

Dual, Matched 6.5MHz Lowpass Filter



Channel to Channel Phase Matching

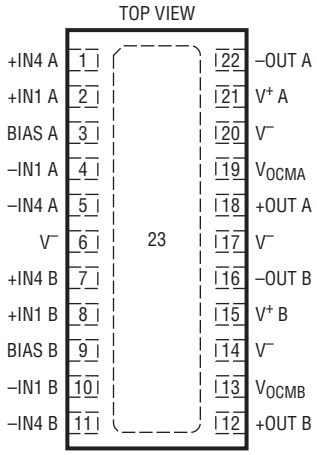


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 5.5V
Input Current (Note 2).....±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4).... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



DJC PACKAGE
22-LEAD (6mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 46.5°C/W
EXPOSED PAD (PIN 23) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6605CDJC-7#PBF	LTC6605CDJC-7#TRPBF	66057	22-Lead (6mm × 3mm) Plastic DFN	0°C to 70°C
LTC6605IDJC-7#PBF	LTC6605IDJC-7#TRPBF	66057	22-Lead (6mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{INCM} = V_{OCM} = mid-supply, BIAS tied to V^+, R_L = Open, R_{BAL} = 10k. The filter is configured for a gain of 1, unless otherwise noted. V_S is defined as (V^+ – V^-). V_{OUTCM} is defined as (V_{+OUT} + $V_{–OUT}$)/2. V_{INCM} is defined as (V_{INP} + V_{INM})/2. $V_{OUTDIFF}$ is defined as (V_{+OUT} – $V_{–OUT}$). V_{INDIFF} is defined as (V_{INP} – V_{INM}). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Differential Offset Voltage (at Op Amp Inputs) (Note 6)	V_S = 2.7V to 5V	●		±0.25	±1	mV
$\Delta V_{OS}/\Delta T$	Differential Offset Voltage Drift (at Op Amp Inputs)	BIAS = V^+ BIAS = Floating	● ●		±1 ±1		µV/°C µV/°C
I_B	Input Bias Current (at Op Amp Inputs) (Note 7)	BIAS = V^+ BIAS = Floating	● ●	–60 –30	–25 –12.5	0 0	µA µA
I_{OS}	Input Offset Current (at Op Amp Inputs) (Note 7)				±1		µA

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{INCM} = V_{OCM} = mid-supply, BIAS tied to V^+, R_L = Open, R_{BAL} = 10k. The filter is configured for a gain of 1, unless otherwise noted. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as (V_{+OUT} + $V_{–OUT}$)/2. V_{INCM} is defined as (V_{INP} + V_{INM})/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{–OUT}$). V_{INDIFF} is defined as ($V_{INP} - V_{INM}$). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{INCM}	Input Common Mode Voltage Range (Note 8)	V_S = 3V V_S = 5V	● ●	–0.2 –0.2		1.7 4.7	V V
CMRR	Common Mode Rejection Ratio ($\Delta V_{INCM}/\Delta V_{OS}$) (Note 9)	V_S = 3V; ΔV_{INCM} = 1.5V V_S = 5V; ΔV_{INCM} = 2.5V	● ●	46 46	74 74		dB dB
PSRR	Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OS}$) (Note 10)	V_S = 2.7V to 5V	●	66	95		dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} - V_{OCM}$)	V_S = 3V V_S = 5V	● ●		±10 ±10	±15 ±15	mV mV
V_{OCM}	Output Common Mode Range (Valid Range for V_{OCM} Pin) (Note 8)	V_S = 3V V_S = 5V	● ●	1.1 1.1		2 4	V V
V_{MID}	Self-Biased Voltage at the V_{OCM} Pin	V_S = 3V	●	1.475	1.5	1.525	V
R_{VOCM}	Input Resistance of V_{OCM} Pin		●	12.5	18	23.5	kΩ
V_{OUT}	Output Voltage Swing, High (Measured Relative to V^+)	V_S = 3V; I_L = 0mA V_S = 3V; I_L = 5mA V_S = 3V; I_L = 20mA	● ● ●		245 285 415	450 525 750	mV mV mV
		V_S = 5V; I_L = 0mA V_S = 5V; I_L = 5mA V_S = 5V; I_L = 20mA	● ● ●		350 390 550	625 700 1000	mV mV mV
	Output Voltage Swing, Low (Measured Relative to V^-)	V_S = 3V; I_L = 0mA V_S = 3V; I_L = –5mA V_S = 3V; I_L = –20mA	● ● ●		120 135 195	225 250 350	mV mV mV
		V_S = 5V; I_L = 0mA V_S = 5V; I_L = –5mA V_S = 5V; I_L = –20mA	● ● ●		175 200 270	325 360 475	mV mV mV
I_{SC}	Output Short-Circuit Current (Note 3)	V_S = 3V V_S = 5V	● ●	±40 ±50	±70 ±95		mA mA
V_S	Supply Voltage		●	2.7		5.25	V
I_S	Supply Current (per Channel)	V_S = 2.7V to 5V; BIAS = V^+ V_S = 2.7V to 5V; BIAS = Floating V_S = 2.7V to 5V; BIAS = V^-	● ● ●		33.1 16.2 0.35	45 26.5 1.6	mA mA mA
	BIAS Pin Range for Shutdown	Referenced to V^-	●	0		0.4	V
	BIAS Pin Range for Medium Power	Referenced to V^-	●	1		1.5	V
	BIAS Pin Range for Full Power	Referenced to V^-	●	2.3		V_S	V
	BIAS Pin Self-Biased Voltage (Floating)	Referenced to V^-	●	1.05	1.15	1.25	V
R_{BIAS}	BIAS Pin Input Resistance		●	100	150	200	kΩ
t_{ON}	Turn-On Time	V_S = 3V, V_{BIAS} = V^- to V^+			400		ns
t_{OFF}	Turn-Off Time	V_S = 3V, V_{BIAS} = V^+ to V^-			400		ns

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{INCM} = V_{OCM} = mid-supply, V_{BIAS} = V^+, unless otherwise noted. Filter configured as in Figure 2, unless otherwise noted. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{INCM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$). V_{INDIFF} is defined as ($V_{+IN} + V_{–IN}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain	Filter Gain	ΔV_{IN} = ±0.125V, DC	●	–0.25	±0.05	0.25	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 3.5MHz	●	–1.2	–0.84	–0.5	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 5.25MHz	●	–2.55	–2.08	–1.65	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 7MHz	●	–4.25	–3.71	–3.2	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 14MHz	●	–11.95	–11.3	–10.7	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 35MHz	●	–28	–25.9	–25	dB
Phase	Filter Phase	ΔV_{IN} = ±0.125V, DC			0		Deg
		V_{INDIFF} = 0.5V_{P-P}, f = 3.5MHz			–43.4		Deg
		V_{INDIFF} = 0.5V_{P-P}, f = 5.25MHz			–63.8		Deg
		V_{INDIFF} = 0.5V_{P-P}, f = 7MHz			–81.9		Deg
ΔGain	Gain Match (Channel-to-Channel)	ΔV_{IN} = ±0.125V, DC	●	–0.2	±0.05	0.2	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 3.5MHz	●	–0.2	±0.05	0.2	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 5.25MHz	●	–0.3	±0.05	0.3	dB
		V_{INDIFF} = 0.5V_{P-P}, f = 7MHz	●	–0.35	±0.05	0.35	dB
ΔPhase	Phase Match (Channel-to-Channel)	V_{INDIFF} = 0.5V_{P-P}, f = 3.5MHz	●	–1.0	±0.2	1.0	Deg
		V_{INDIFF} = 0.5V_{P-P}, f = 5.25MHz	●	–1.0	±0.2	1.0	Deg
		V_{INDIFF} = 0.5V_{P-P}, f = 7MHz	●	–1.2	±0.2	1.2	Deg
4V/V Gain	Filter Gain in 4V/V Configuration Inputs at ±IN1 Pins, ±IN4 Floating	ΔV_{IN} = ±0.125V, DC	●	11.85	12	12.25	dB
	Channel Separation	V_{INDIFF} = 1V_{P-P}, f = 3.5MHz			–100		dB
f_O TC	Filter Cut-Off Frequency Temperature Coefficient	BIAS = V^+			–55		ppm/°C
		BIAS = Floating			–180		ppm/°C
Noise	Integrated Output Noise (BW = 10kHz to 14MHz)				61		μV_{RMS}
	Input Referred Noise Density (f = 1MHz)	BIAS = V^+					
		Figure 4, Gain = 1			21		nV/√Hz
		Figure 4, Gain = 4			5.2		nV/√Hz
		Figure 4, Gain = 5			4.2		nV/√Hz
e_n	Voltage Noise Density Referred to Op Amp Inputs (f = 1MHz)	BIAS = V^+			2.1		nV/√Hz
		BIAS = Floating			2.6		nV/√Hz
i_n	Current Noise Density Referred to Op Amp Inputs (f = 1MHz)	BIAS = V^+			3		pA/√Hz
		BIAS = Floating			2.1		pA/√Hz
HD2	2nd Harmonic Distortion f_{IN} = 3MHz; V_{IN} = 2V_{P-P} Single-Ended	BIAS = V^+			–96		dBc
		BIAS = Floating, R_{LOAD} = 400Ω			–80		dBc
HD3	3rd Harmonic Distortion f_{IN} = 3MHz; V_{IN} = 2V_{P-P} Single-Ended	BIAS = V^+			–114		dBc
		BIAS = Floating, R_{LOAD} = 400Ω			–95		dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All pins are protected by steering diodes to either supply. If any pin is driven beyond the LTC6605-7's supply voltage, the excess input current (current in excess of what it takes to drive that pin to the supply rail) should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating when the output is shorted indefinitely. Long-term application of output currents in excess of the Absolute Maximum Ratings may impair the life of the device.

Note 4: Both the LTC6605C and the LTC6605I are guaranteed functional over the operating temperature range –40°C to 85°C.

Note 5: The LTC6605C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6605C is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. The LTC6605I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Output referred voltage offset is a function of gain. To determine output referred voltage offset, or output voltage offset drift, multiply V_{OS} by the noise gain (1 + GAIN). See Figure 3.

Note 7: Input bias current is defined as the average of the currents flowing into the noninverting and inverting inputs of the internal amplifier and is calculated from measurements made at the pins of the IC. Input offset current is defined as the difference of the currents flowing into the noninverting and inverting inputs of the internal amplifier and is calculated from measurements made at the pins of the IC.

ELECTRICAL CHARACTERISTICS

Note 8: See the Applications Information section for a detailed discussion of input and output common mode range. Input common mode range is tested by measuring the differential DC gain with V_{INCM} = mid-supply, and again with V_{INCM} at the input common mode range limits listed in the Electrical Characteristics table, with ΔV_{IN} = ±0.25V, verifying that the differential gain has not deviated from the mid-supply common mode input case by more than 0.5%, and that the common mode offset (V_{OSCM}) has not deviated by more than ±10mV from the mid-supply case.

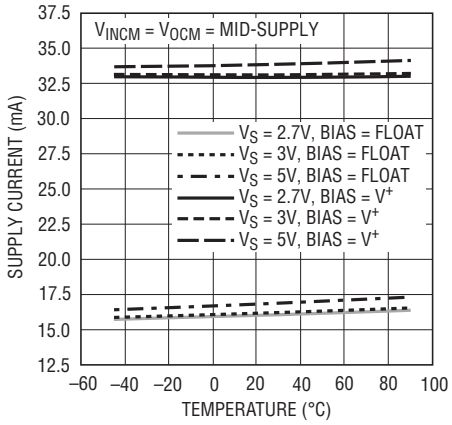
Output common mode range is tested by measuring the differential DC gain with V_{OCM} = mid-supply, and again with voltage set on the V_{OCM} pin at the output common range limits listed in the Electrical Characteristics table, verifying that the differential gain has not deviated from the mid-supply common mode input case by more than 0.5%, and that the common mode offset (V_{OSCM}) has not deviated by more than ±10mV from the mid-supply case.

Note 9: CMRR is defined as the ratio of the change in the input common mode voltage at the internal amplifier inputs to the change in differential input referred voltage offset (V_{OS}).

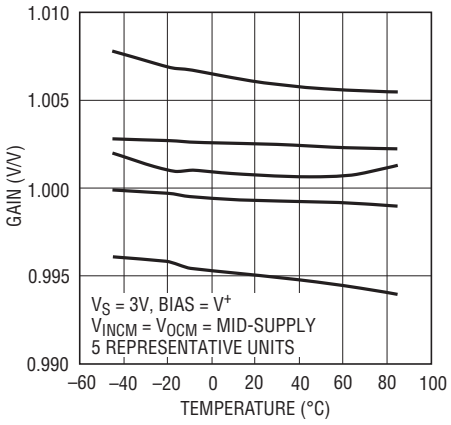
Note 10: Power supply rejection ratio (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred voltage offset (V_{OS}).

TYPICAL PERFORMANCE CHARACTERISTICS

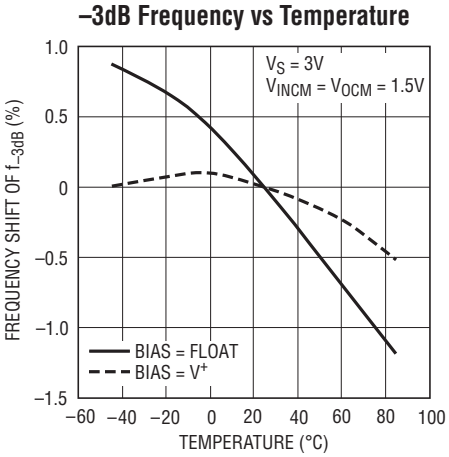
Supply Current vs Temperature



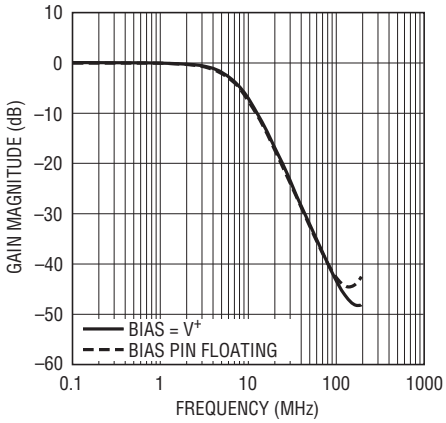
Filter Gain vs Temperature



–3dB Frequency vs Temperature

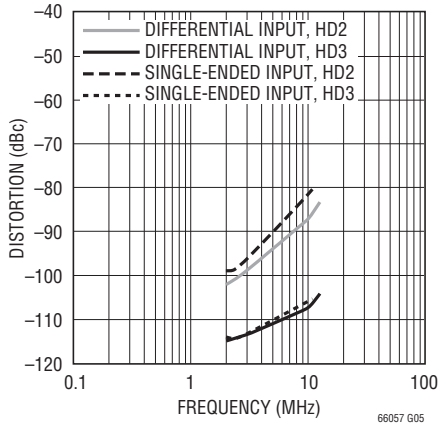


Filter Frequency Response



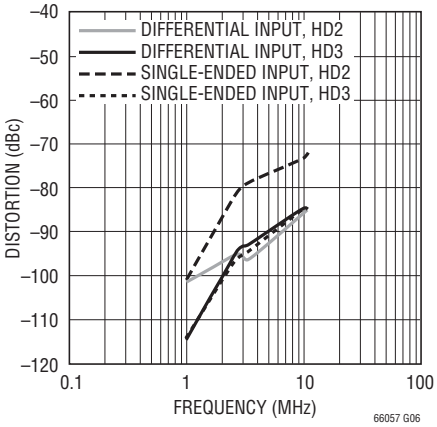
TYPICAL PERFORMANCE CHARACTERISTICS

Harmonic Distortion vs Frequency, BIAS High



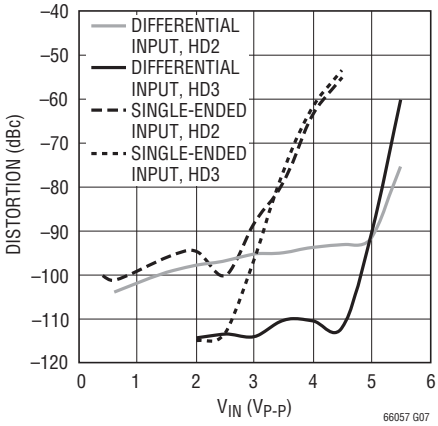
V_{IN} = 2V_{P-P}, V_S = 3V
R_L = 400Ω DIFFERENTIAL, GAIN = 1V/V

Harmonic Distortion vs Frequency, BIAS Floating



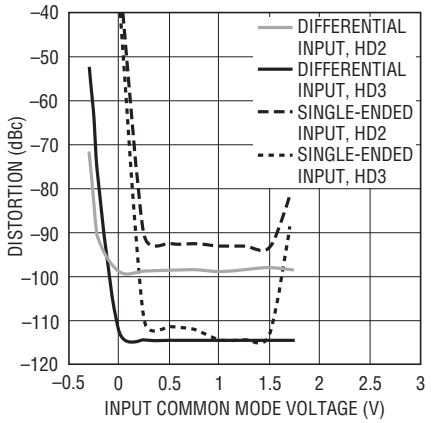
V_{IN} = 2V_{P-P}, V_S = 3V
R_L = 400Ω DIFFERENTIAL, GAIN = 1V/V

Harmonic Distortion vs Input Amplitude



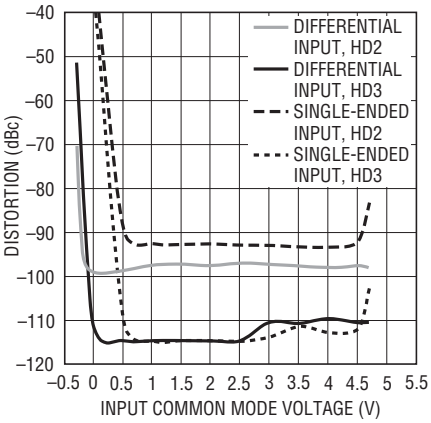
V_S = 3V, BIAS TIED TO V^+, V_{INCM} = V_{OCM} = 1.5V
R_{LOAD} = 400Ω, f_{IN} = 3MHz, GAIN = 1V/V

Harmonic Distortion vs Input Common Mode Voltage (V_S = 3V)



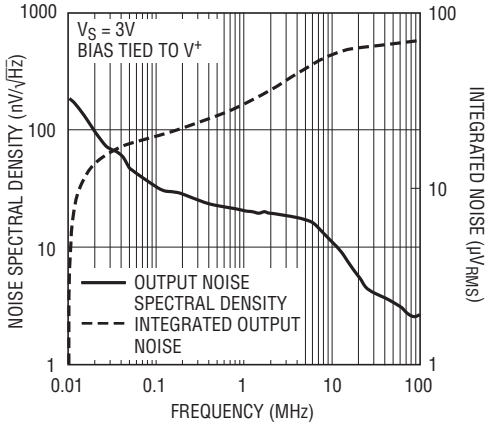
V_{IN} = 2V_{P-P}, V_{OCM} = 1.5V
BIAS = 3V, f = 3MHz
R_L = 400Ω DIFFERENTIAL, GAIN = 1V/V

Harmonic Distortion vs Input Common Mode Voltage (V_S = 5V)

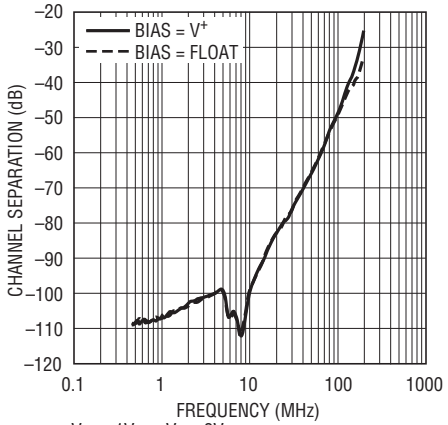


V_{IN} = 2V_{P-P}, V_{OCM} = 2.5V
BIAS = 5V, f = 3MHz
R_L = 400Ω DIFFERENTIAL, GAIN = 1V/V

Differential Output Noise vs Frequency

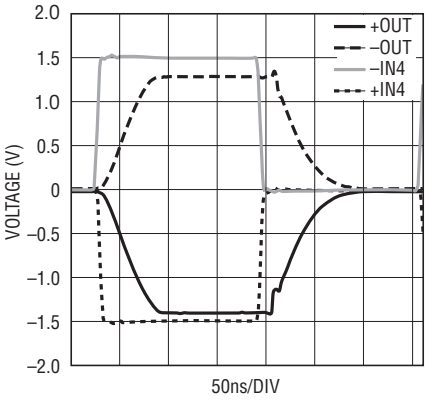


Channel Separation vs Frequency



V_{IN} = 1V_{P-P}, V_S = 3V
R_L = 400Ω DIFFERENTIAL

Overdrive Transient Response



V_S = 3V, V_{OCM} = 1.5V
BIAS = 3V, R_{LOAD} = 400Ω

TEST CIRCUITS

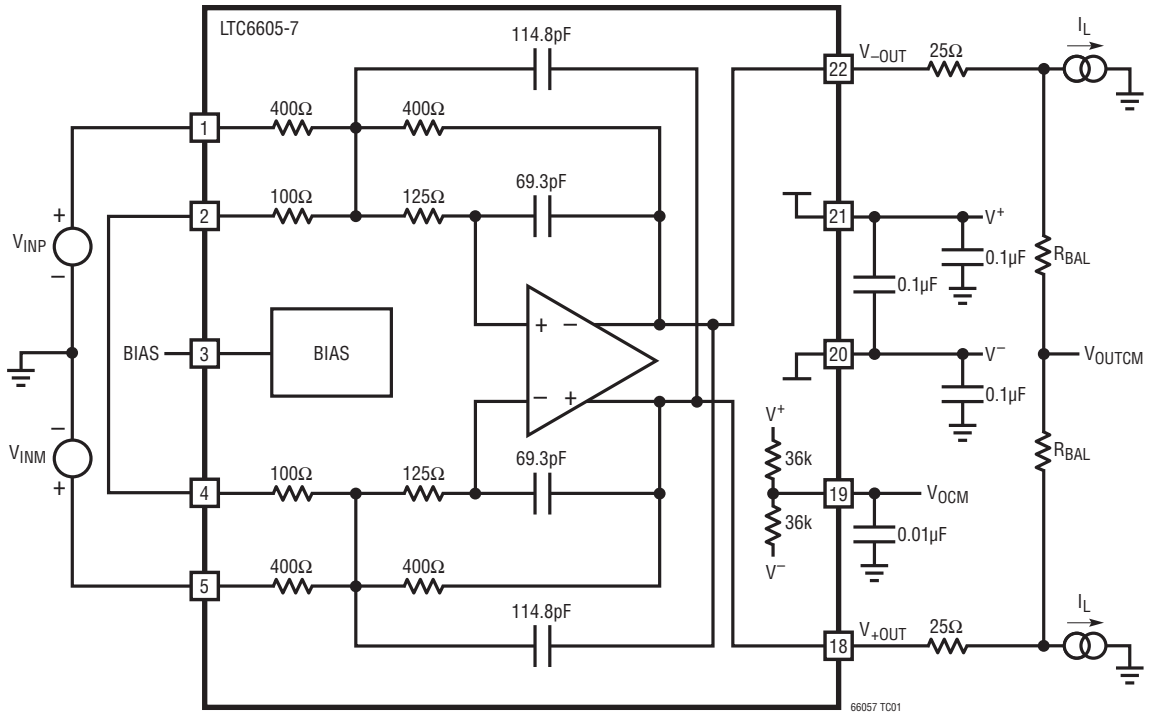


Figure 1. DC Test Circuit (Channel A Shown)

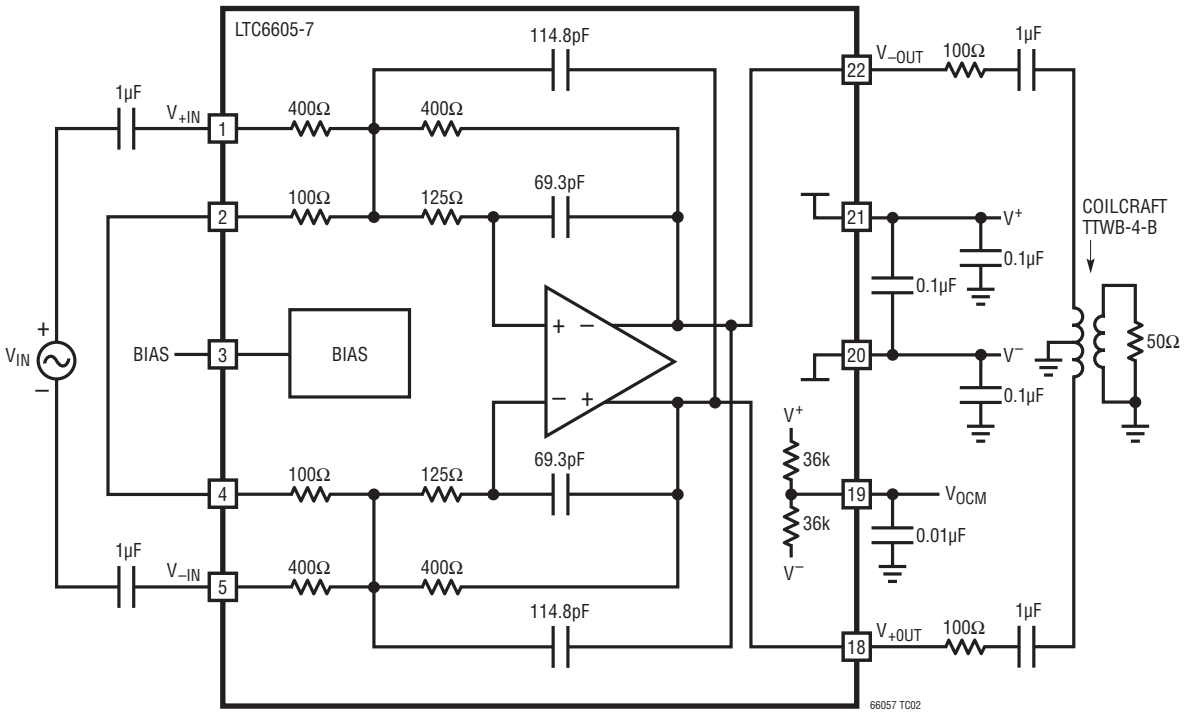


Figure 2. AC Test Circuit (Channel A Shown)

PIN FUNCTIONS

+IN4 A, –IN4 A, +IN4 B, –IN4 B (Pins 1, 5, 7, 11): Inputs to Trimmed 400Ω Resistors. Can accept an input signal, be floated, tied to an output pin, or connected to external components.

+IN1 A, –IN1 A, +IN1 B, –IN1 B (Pins 2, 4, 8, 10): Inputs to Trimmed 100Ω Resistors. Can accept an input signal, be floated, tied to an output pin, or connected to external components.

BIAS A, BIAS B (Pins 3, 9): Three-State Input to Select Amplifier Power Consumption. Drive low for shutdown, drive high for full power, leave floating for medium power. BIAS presents an input resistance of approximately 150k to a voltage 1.15V above V^-.

V^- (Pins 6, 14, 17, 20): Negative Supply. All V^- pins should be connected to the same voltage, either a ground plane or a negative supply rail.

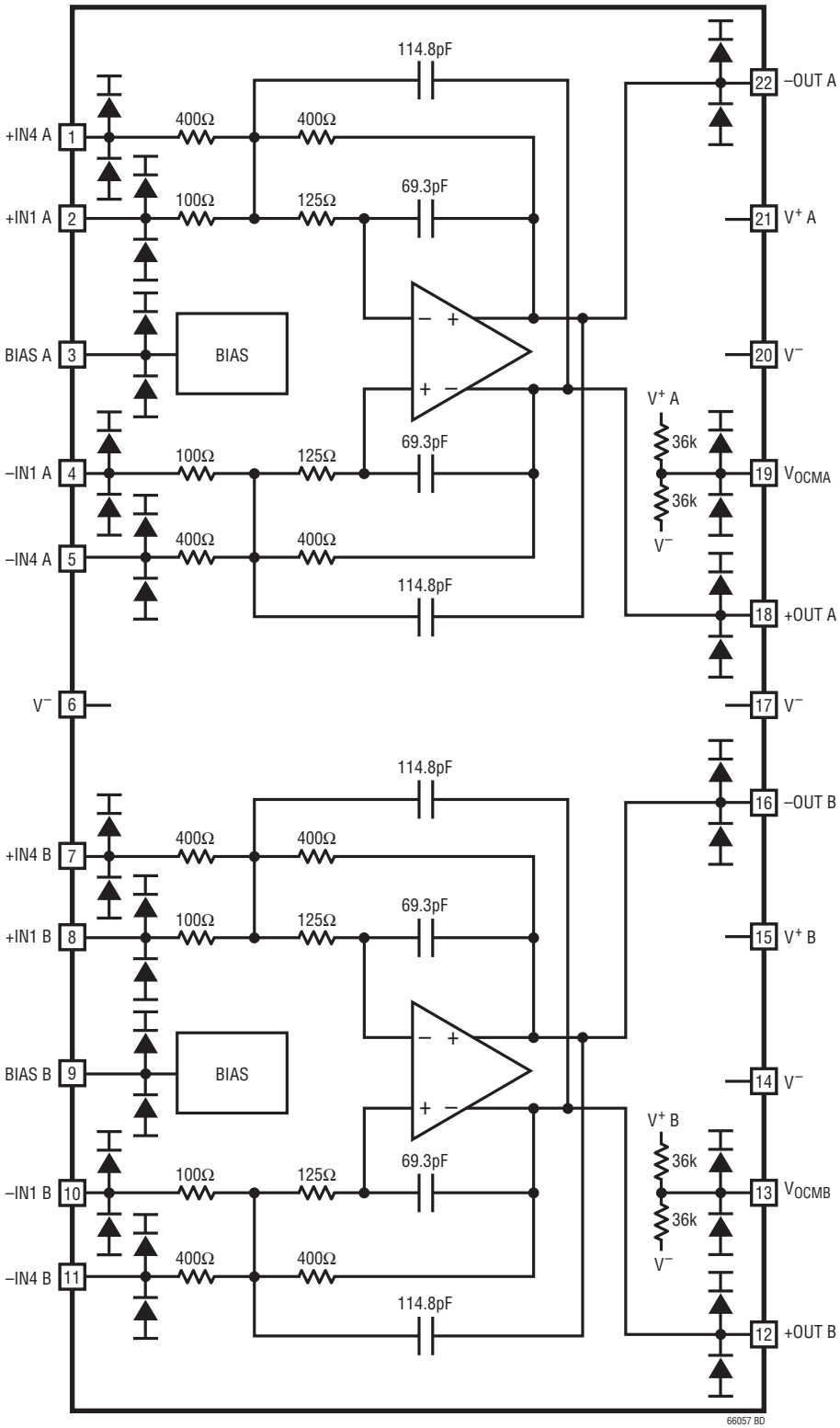
V_{OCMA}, V_{OCMB} (Pins 19, 13): The voltage applied to these pins sets the output common mode voltage of each filter channel. If left floating, V_{OCM} self-biases to a voltage midway between V^+ and V^-.

V^+ A, V^+ B (Pins 21, 15): Positive Supply for Filter Channel A and B, Respectively. These are not connected to each other internally.

–OUT A, +OUT A, –OUT B, +OUT B (Pins 22, 18, 16, 12): Differential Output Pins.

Exposed Pad (Pin 23): Always tie the underlying Exposed Pad to V^-. **If split supplies are used, do not tie the pad to ground.**

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Functional Description

The LTC6605-7 is designed to make the implementation of high frequency fully differential filtering functions very easy. Two very low noise amplifiers are surrounded by precision matched resistors and precision matched capacitors enabling various filter functions to be implemented by hard wiring pins. The amplifiers are wide band, low noise and low distortion fully differential amplifiers with accurate output phase balancing. They are optimized for driving low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LTC6605-7 operates with a supply voltage as low as 2.7V and accepts inputs up to 325mV below the V^- power rail, which makes it ideal for converting ground referenced, single-ended signals into differential signals that are referenced to the user-supplied common mode voltage. This is ideal for driving low voltage, single-supply, differential input ADCs. The balanced differential nature of the amplifier and matched surrounding components provide even-order harmonic distortion cancellation, and low susceptibility to common mode noise (like power supply noise). The LTC6605-7 can be operated with a single-ended input and differential output, or with a differential input and differential output.

The outputs of the LTC6605-7 can swing rail-to-rail. They can source or sink a transient 70mA of current. Load capacitances should be decoupled with at least 25Ω of series resistance from each output.

Filter Frequency Response and Gain Adjustment

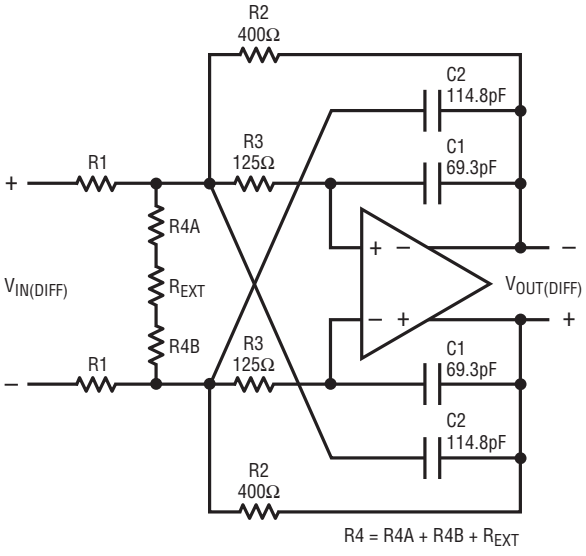
Figure 3 shows the filter architecture. The Laplace transfer function can be expressed in the form of the following generalized equation for a 2nd order lowpass filter:

$$\frac{V_{OUT(DIFF)}}{V_{IN(DIFF)}} = \frac{GAIN}{1+\frac{s}{2\pi f_0 \bullet Q}+\frac{s^2}{(2\pi f_0)^2}},$$

with GAIN, f_0 and Q as given in Figure 3.

Note that GAIN and Q of the filter are based on component ratios, which both match and track extremely well over temperature. The corner frequency f_0 of the filter is a function of an RC product. This RC product is trimmed to ±1% and is not expected to drift by more than ±1% from nominal over the entire temperature range –40°C to 85°C. As a result, fully differential filters with tight magnitude, phase tolerance and repeatability are achieved.

Various values for resistors R1 and R4 can be formed by pin-strapping the internal 100Ω and 400Ω resistors, and optionally by including one or more external resistors. Note that non-zero source resistance should be combined with, and included in, R1.



$$GAIN = \frac{V_{OUT(DIFF)}}{V_{IN(DIFF)}} = \frac{R2}{R1}$$

$$f_0 = \frac{1}{2 \bullet \pi \bullet \sqrt{R2 \bullet R3 \bullet C1 \bullet C2}}$$

$$Q = \frac{\sqrt{\frac{R3}{R2} \bullet \frac{C2}{C1}}}{1+\left(1+|GAIN|+2 \bullet \frac{R2}{R4}\right) \bullet \frac{R3}{R2} - \frac{C2}{C1}}$$

$$\frac{V_{OUT(DIFF)}}{V_{IN(DIFF)}} = \frac{\frac{GAIN}{R2 \bullet R3 \bullet C1 \bullet C2}}{S^2 + \frac{R1 \bullet (R2 \bullet (2 \bullet R3 + R4) + R3 \bullet R4) + R2 \bullet R3 \bullet R4}{R1 \bullet R2 \bullet R3 \bullet R4 \bullet C2} \bullet S + \frac{1}{R2 \bullet R3 \bullet C1 \bullet C2}}$$

66057 F03

Figure 3. Filter Architecture and Equations

APPLICATIONS INFORMATION

Setting the passband gain (GAIN = R2/R1) only requires choosing a value for R1, since R2 is a fixed internal 400Ω. Therefore, the following three gains can be easily configured without external components:

Table 1. Configuring the Passband Gain Without External Components

GAIN (V/V)	GAIN (dB)	R1 (Ω)	INPUT PINS TO USE
1	0	400	Drive the 400Ω Resistors. Tie the 100Ω Resistors Together.
4	12	100	Drive the 100Ω Resistors.
5	14	80	Drive the 400Ω and 100Ω Resistors in Parallel.

The resonant frequency, f_O, is independent of R1, and therefore independent of the gain. For any LTC6605-7 filter configuration that conforms to Figure 3, the f_O is fixed at 7.98MHz. The f_{-3dB} frequency depends on the combination of f_O and Q. For any specific gain, Q is adjusted by the selection of R4.

Setting the f_{-3dB} Frequency

Using an external resistor (R_{EXT}), the f_{-3dB} frequency is adjustable in the range of 6.5MHz to 10.0MHz (see Figure 3). The minimum f_{-3dB} is set for R_{EXT} equal to 0Ω and the maximum f_{-3dB} is arbitrarily set for a maximum passband gain less than 1dB.

Table 2. R_{EXT} Selection GAIN = 1, R1 = 400Ω, R4A = R4B = 100Ω

f_{-3dB} (MHz)	R_{EXT} Ω
6.5	0
7	12.7
7.5	24.9
8	39.2
8.5	54.9
9	73.2
9.5	95.3
10	124

Figure 4 shows three filter configurations with an f_{-3dB} = 6.5MHz, without any external components. These filters have a Q = 0.59, which is an almost ideal Bessel characteristic with linear phase.

Figure 5 shows three filter configurations that use some external resistors, and are tailored for a very flat ±0.4dB 6.7MHz passband.

Many other configurations are possible by using the equations in Figure 3. For example, external resistors can be added to modify the value of R1 to configure GAIN ≠ 1. For an even more flexible filter IC with similar performance, consider the LTC6601.

BIAS Pin

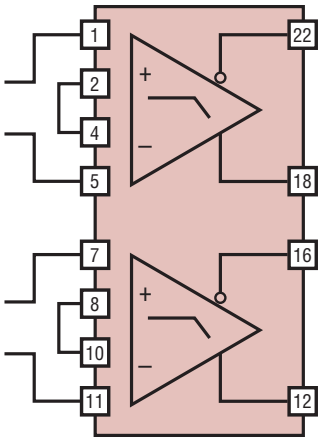
Each channel of the LTC6605-7 has a BIAS pin whose function is to tailor both performance and power. The BIAS pin can be modeled as a voltage source whose potential is 1.15V above the V^- supply and that has a Thevenin equivalent resistance of 150k. This three-state pin has fixed logic levels relative to V^- (see the Electrical Characteristics table), and can be driven by any external source that can drive the BIAS pin's equivalent input impedance.

If the BIAS pin is tied to the positive supply, the part is in a fully active state configured for highest performance (lowest noise and lowest distortion).

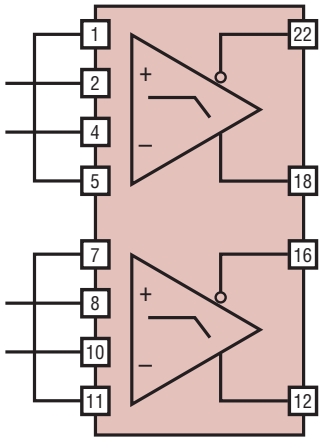
If the BIAS pin is floated (left unconnected), the part is in a fully active state, but with amplifier currents reduced and performance scaled back to preserve power consumption. Care should be taken to limit external leakage currents to this pin to under 1µA to avoid putting the part in an unexpected state.

If the BIAS pin is tied to the most negative supply (V^-), the part is in a low power shutdown mode with amplifier outputs disabled. In shutdown, all internal biasing current sources are shut off, and the output pins each appear as open collectors with a non-linear capacitor in parallel and steering diodes to either supply. Because of the non-linear capacitance, the outputs can still sink and source small amounts of transient current if exposed to significant voltage transients. Using this function to wire-OR outputs together is not recommended.

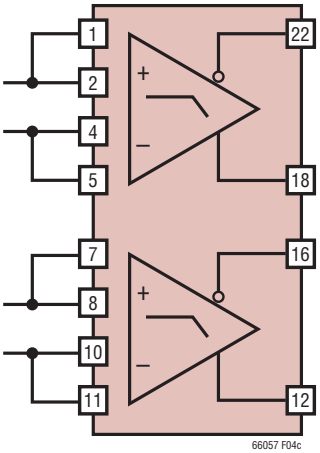
APPLICATIONS INFORMATION



f_{-3dB} = 6.5MHz
GAIN = 1V/V (0dB)
Z_{IN} = 800Ω

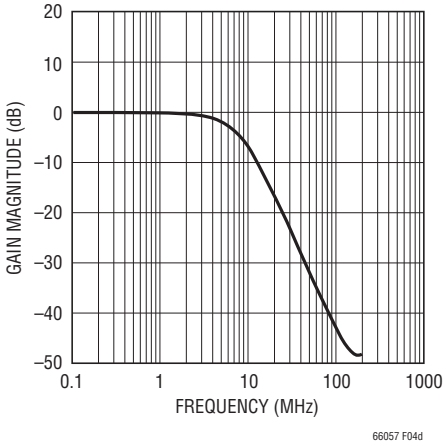


f_{-3dB} = 6.5MHz
GAIN = 4V/V (12dB)
Z_{IN} = 200Ω

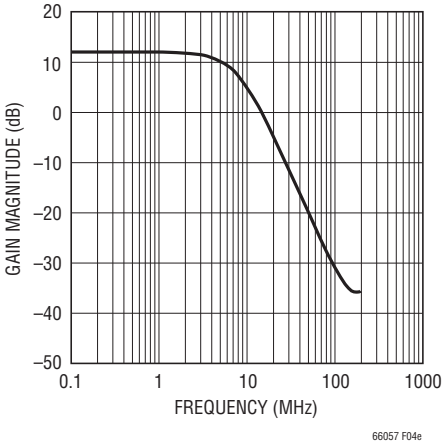


f_{-3dB} = 6.5MHz
GAIN = 5V/V (14dB)
Z_{IN} = 160Ω

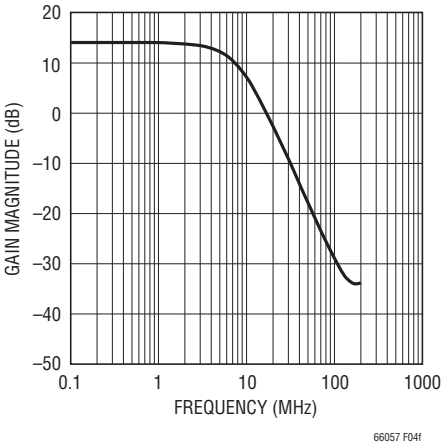
Gain Response



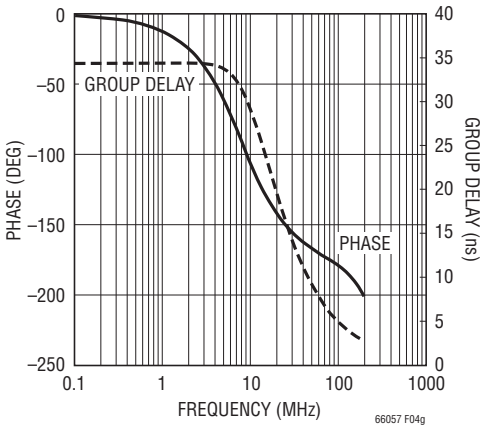
Gain Response



Gain Response



Phase and Group Delay Response



Small Signal Step Response

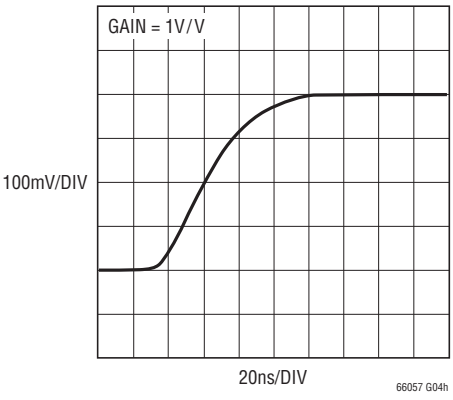
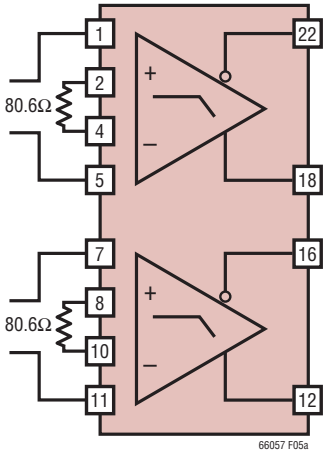
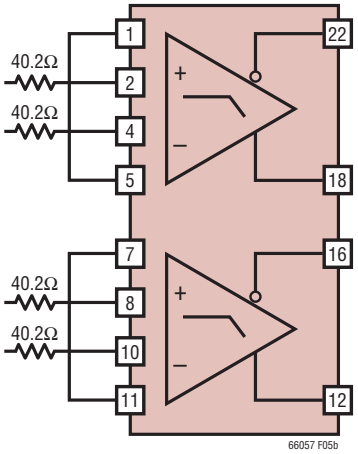


Figure 4. f_{-3dB} = 6.5MHz Filter Configurations without External Components

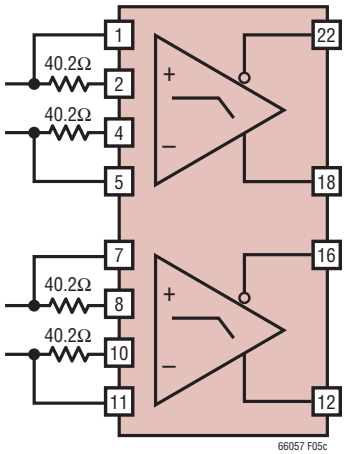
APPLICATIONS INFORMATION



±0.4dB 6.7MHz PASSBAND
GAIN = 1V/V (0dB)
Z_{IN} = 800Ω

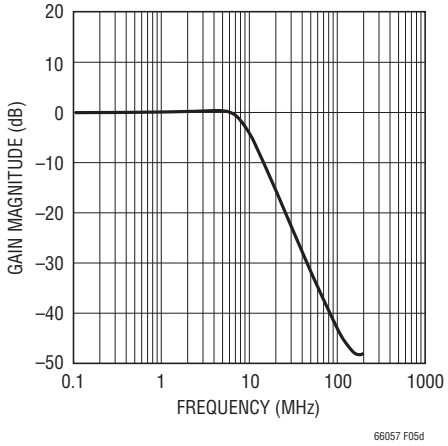


±0.4dB 6.7MHz PASSBAND
GAIN = 2.85V/V (9.1dB)
Z_{IN} = 280Ω

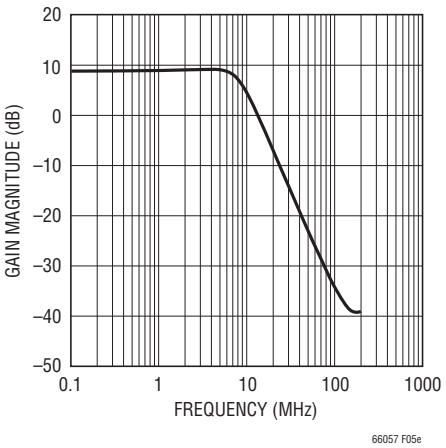


±0.4dB 6.7MHz PASSBAND
GAIN = 3.85V/V (11.7dB)
Z_{IN} = 208Ω

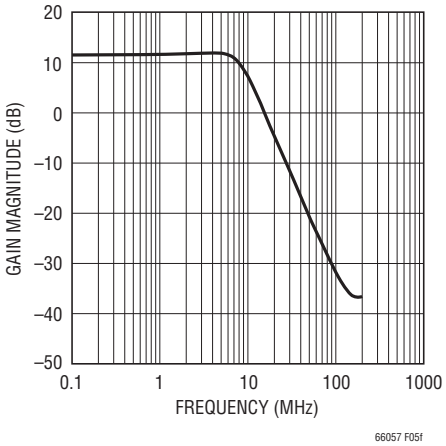
Gain Response



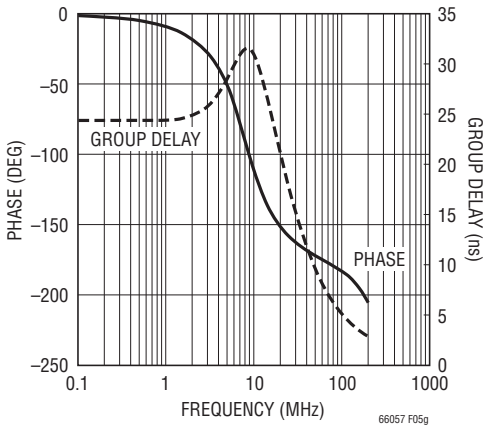
Gain Response



Gain Response



Phase and Group Delay Response



Small Signal Step Response

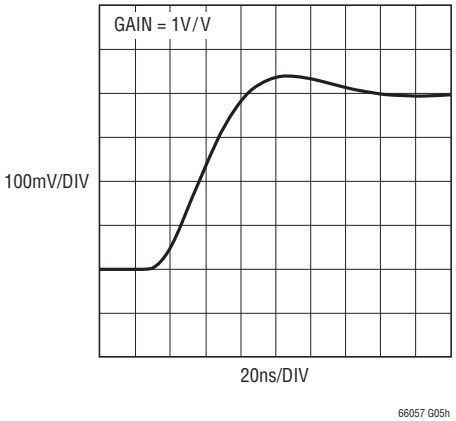


Figure 5. Flat Passband 6.7MHz Filter Configurations with Some External Resistors

APPLICATIONS INFORMATION

Input Impedance

Calculating the low frequency input impedance depends on how the inputs are driven.

Figure 6 shows a simplified low frequency equivalent circuit. For balanced input sources ($V_{INP} = -V_{INM}$), the low frequency input impedance is given by the equation:

$$R_{INP} = R_{INM} = R1$$

Therefore, the differential input impedance is simply:

$$R_{IN(DIFF)} = 2 \bullet R1$$

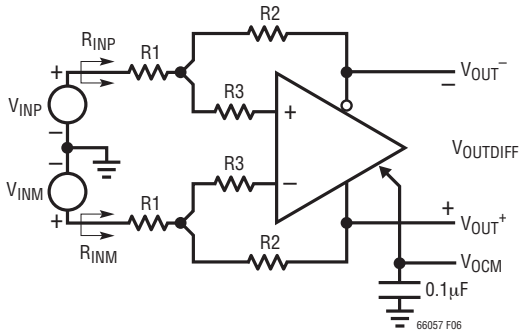


Figure 6. Input Impedance

For single-ended inputs ($V_{INM} = 0$), the input impedance increases over the balanced differential case due to the fact that the summing node (at the junction of R1, R2 and R3) moves in phase with V_{INP} to bootstrap the input impedance. Referring to Figure 6 with $V_{INM} = 0$, the input impedance looking into either input is:

$$R_{INP} = R_{INM} \quad \frac{R1}{\left[1 - \frac{1}{2} \bullet \left(\frac{R2}{R1 + R2}\right)\right]}$$

Input Common Mode Voltage Range

The input common mode voltage is defined as the average of the two inputs into resistor R1:

$$V_{INCM} = \frac{V_{INP} + V_{INM}}{2}$$

The input common mode range is a function of the filter configuration (GAIN), V_{INDIFF} and the V_{OCM} potential. Referring to Figure 6, the summing junction where R1, R2 and R3 merge together should not swing within 1.4V of the V^+ power supply. Additionally, to avoid forward biasing the ESD protection diodes on the input pins, neither input should swing further than 325mV below the V^- power rail. Therefore, the input common mode voltage should be constrained to:

$$V^- - 325mV + \frac{V_{INDIFF}}{2} \le V_{INCM} \le \left(1 + \frac{R1}{R2}\right) \bullet \left(V^+ - 1.4V\right) - \left(\frac{R1}{R2}\right) V_{OCM}$$

The specifications in the Electrical Characteristics table are a special case of the general equation above. For a single 3V power supply, ($V^+ = 3V$, $V^- = 0V$) with $V_{OCM} = 1.5V$, $\Delta V_{INDIFF} = \pm 0.25V$ and R1 = R2, the valid input common mode range is:

$$-200mV \le V_{INCM} \le 1.7V$$

Likewise, for a single 5V power supply, ($V^+ = 5V$, $V^- = 0V$) with $V_{OCM} = 2.5V$, $\Delta V_{INDIFF} = \pm 0.25V$ and R1 = R2, the valid input common mode range is:

$$-200mV \le V_{INCM} \le 4.7V$$

Output Common Mode and V_{OCM} Pin

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^+ + V_{OUT}^-}{2}$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the V_{OCM} pin, by means of an internal feedback loop.

If the V_{OCM} pin is left open, an internal resistor divider develops a potential halfway between the V^+ and V^- voltages. The V_{OCM} pin can be overdriven to another voltage if desired. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the V_{OCM} pin, as long as the ADC is capable of driving the input impedance presented by the V_{OCM} pin as listed in the Electrical Characteristics table (R_{VOCM}). The Electrical Characteristics table also specifies the valid range that can be applied to the V_{OCM} pin.

APPLICATIONS INFORMATION

Noise

When comparing the LTC6605-7's noise to that of other amplifiers, be sure to compare similar specifications. Standalone op amps often specify noise referred to the inputs of the op amp. The LTC6605-7's internal op amp has input referred voltage noise of only 2.1nV/$\sqrt{Hz}$. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A noise model is shown in Figure 7a. The output spot noise generated by both the amplifier and the feedback components is given in Figure 7b. Substituting the equation for Johnson noise of a resistor (e^2_{nR} = 4kTR) into the equation in Figure 7b and simplifying gives the result shown in Figure 7c.

Board Layout and Bypass Capacitors

For single-supply applications it is recommended that a high quality X5R or X7R, 0.1µF bypass capacitor be placed directly between V^+ and the adjacent V^- pin. The V^- pins, including the Exposed Pad, should be tied directly to a low impedance ground plane with minimal routing.

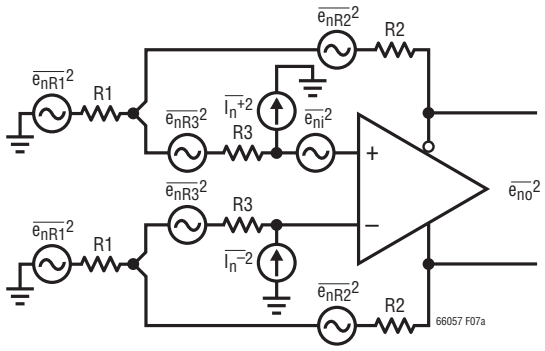


Figure 7a. Differential Noise Model

$$e_{no} = \sqrt{\left[e_{ni} \bullet \left(1+\frac{R2}{R1}\right)\right]^2 + 2 \bullet \left[I_n \bullet \left(R2 + R3 \bullet \left[1+\frac{R2}{R1}\right]\right)\right]^2 + 2 \bullet \left[e_{nR1} \bullet \left(\frac{R2}{R1}\right)\right]^2 + 2 \bullet \left[e_{nR3} \bullet \left(1+\frac{R2}{R1}\right)\right]^2 + 2 \bullet {e_{nR2}}^2}$$

Figure 7b

$$e_{no} = \sqrt{\left[e_{ni} \bullet \left(1+\frac{R2}{R1}\right)\right]^2 + 2 \bullet \left[I_n \bullet \left(R2 + R3 \bullet \left[1+\frac{R2}{R1}\right]\right)\right]^2 + 8 \bullet k \bullet T \bullet \left[R2 \bullet \left(1+\frac{R2}{R1}\right) + R3 \bullet \left(1+\frac{R2}{R1}\right)^2\right]}$$

Figure 7c

APPLICATIONS INFORMATION

For split power supplies, it is recommended that additional high quality X5R or X7R, 0.1µF capacitors be used to bypass pin V^+ to ground and V^- to ground, again with minimal routing.

For driving heavy differential loads (< 200Ω), additional bypass capacitance may be needed between V^+ and V^- for optimal performance. Keep in mind that small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than do leaded capacitors, and perform best in high speed applications.

The V_{OCM} pins should be bypassed to ground with a high quality ceramic capacitor (at least 0.01µF). In split-supply applications, the V_{OCM} pin can be either bypassed to ground or directly hard wired to ground.

Stray parasitic capacitances to any unused input pins should be kept to a minimum to prevent deviations from the ideal frequency response. The best approach is to remove the solder pads for the unused component pins and strip away any ground plane underneath. Floating unused pins does not reduce the reliability of the part.

At the output, always keep in mind the differential nature of the LTC6605-7, because it is important that the load impedances seen by both outputs (stray or intended) be as balanced and symmetric as possible. This will help preserve the balanced operation that minimizes the generation of even-order harmonics and maximizes the rejection of common mode signals and noise.

Driving ADCs

The LTC6605-7's rail-to-rail differential output and adjustable output common mode voltage make it ideal for interfacing to differential input ADCs. These ADCs are typically supplied from a single-supply voltage which can be as low as 3V (2.7V minimum), and have an optimal common mode input range near mid-supply. The LTC6605-7 makes interfacing to these ADCs easy, by providing antialiasing, single-ended to differential conversion and common mode level shifting.

The sampling process of ADCs creates a transient that is caused by the switching in of the ADC sampling capacitor. This momentarily "shorts" the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before the acquisition period has ended, for a valid representation of the input signal. The LTC6605-7 will settle quickly from these periodic load impulses. The RC network between the outputs of the driver decouples

APPLICATIONS INFORMATION

the sampling transient of the ADC (see Figure 8). The capacitance serves to provide the bulk of the charge during the sampling process, while the two resistors at the outputs of the LTC6605-7 are used to dampen and attenuate any charge injected by the ADC. The RC filter gives the additional benefit of band limiting broadband output noise. The selection of the RC time constant is trial and error for a given ADC, but the following guidelines are recommended. Choose an RC time constant that is smaller than the reciprocal of the filter cutoff frequency configured by the LTC6605-7. Time constants on the order of 2ns do a good job of filtering broadband noise. Longer time constants improve SNR at the expense of settling time. The resistors in the decoupling network should be at least 25Ω. Too large of a resistor will leave insufficient settling time. Too small of a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling. In 16-bit applications, this will typically require a minimum of eleven RC time constants. The 10Ω resistors at the inputs to the ADC minimize the sampling transients that charge the RC filter capacitors. For lowest distortion, choose capacitors with low dielectric absorption, such as a C0G multilayer ceramic capacitor.

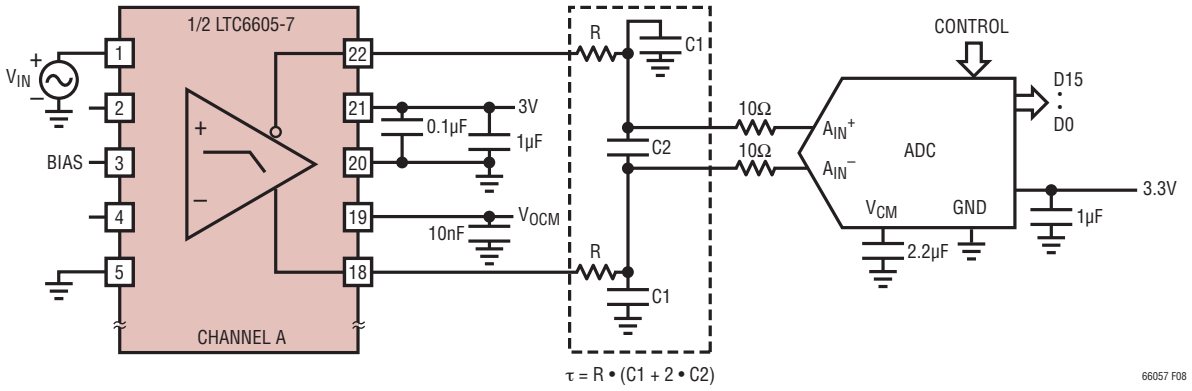
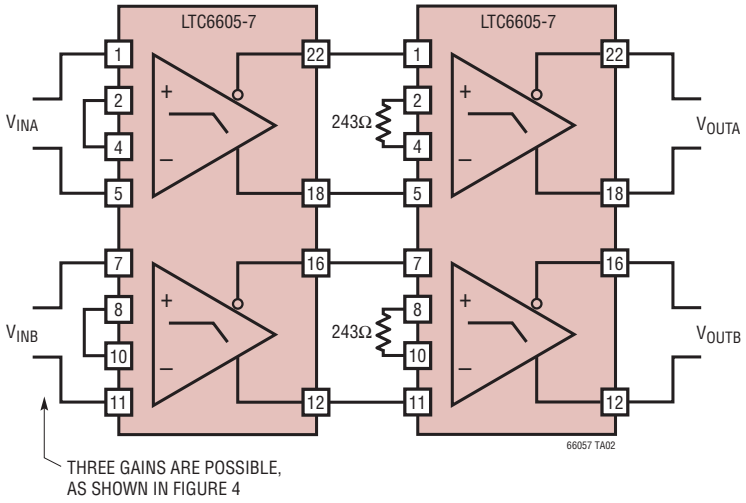


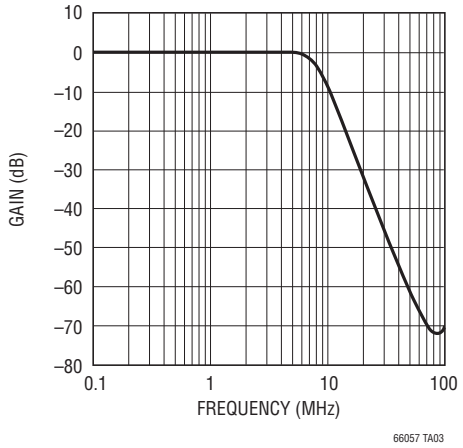
Figure 8. Driving an ADC

TYPICAL APPLICATIONS

Dual, Matched, 4th Order 7MHz Lowpass Filter

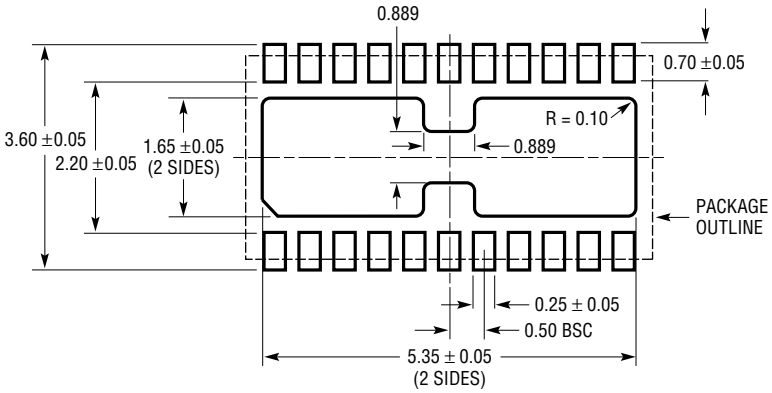


Gain Magnitude vs Frequency



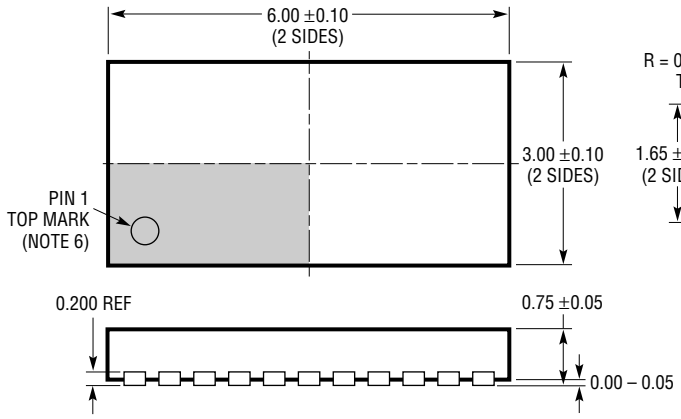
PACKAGE DESCRIPTION

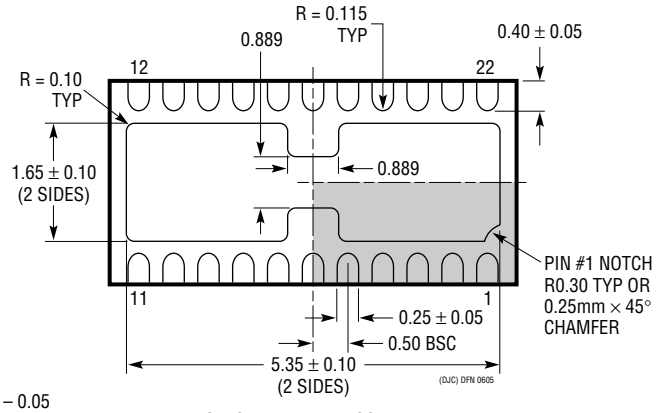
DJC Package
22-Lead Plastic DFN (6mm × 3mm)
(Reference LTC DWG # 05-08-1714)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED
3. DRAWING IS NOT TO SCALE





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE