

# Tiny Micropower, Low Voltage Dual Comparators

## FEATURES

- **Low Supply Operation: 1.7V Minimum**
- **Low Supply Current: 30 $\mu$ A/Comparator Maximum**
- **Propagation Delay: 500ns Maximum ( $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ )**
- 3.2MHz Toggle Frequency
- Input Voltage Range Extends 100mV Below Ground
- Internal Hysteresis: 4mV
- High Output Drive: TTL and CMOS Compatible  
Specified at  $\pm 15\text{mA}$  ( $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  
Capacitive Load Handling to 10,000pF
- Specified for  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Temperature Range
- Available in Low Profile (1mm) ThinSOT™ and  
2mm  $\times$  2mm DFN Packages

## APPLICATIONS

- Battery Powered Systems
- Window Comparators
- Threshold Detectors/Discriminators
- Clock Regeneration
- Automotive Sensing and Controls

## DESCRIPTION

The LTC®6702 is an extremely small dual comparator designed to maximize battery life while providing both speed and low voltage operation in applications where board space is a premium.

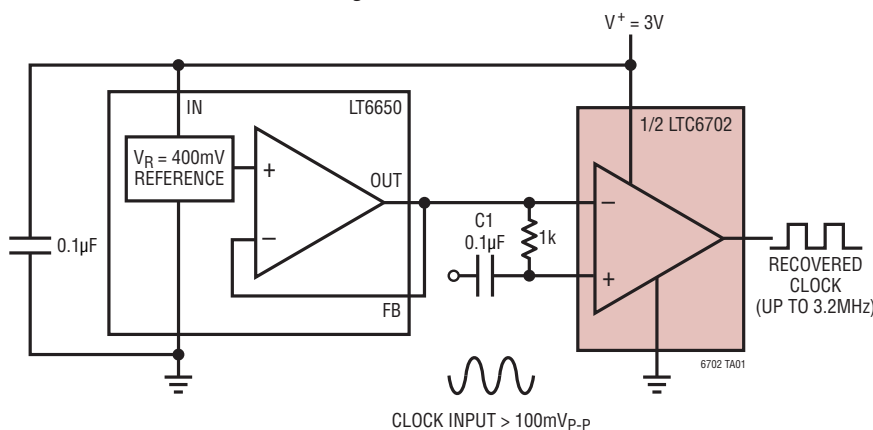
These comparators operate on supplies between 1.7V and 5.5V, and have a maximum guaranteed propagation delay of 500ns while drawing only 30 $\mu$ A maximum quiescent current. Internal hysteresis desensitizes the LTC6702 to input noise and makes it easy to use, even with slow moving signals. CMOS inputs allow the use of large source impedances.

The LTC6702 is available in the 8-pin SOT-23 and the tiny 2mm  $\times$  2mm DFN package.

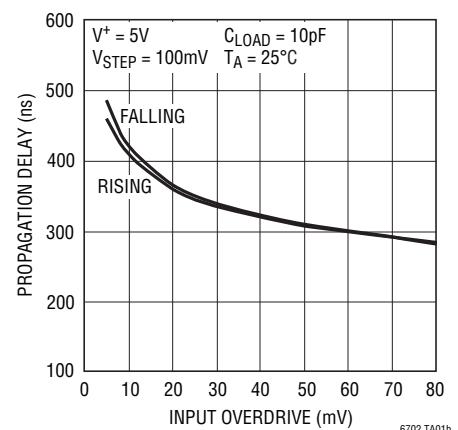
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## TYPICAL APPLICATION

**Clock Regeneration Circuit**



**Propagation Delay vs Input Overdrive**

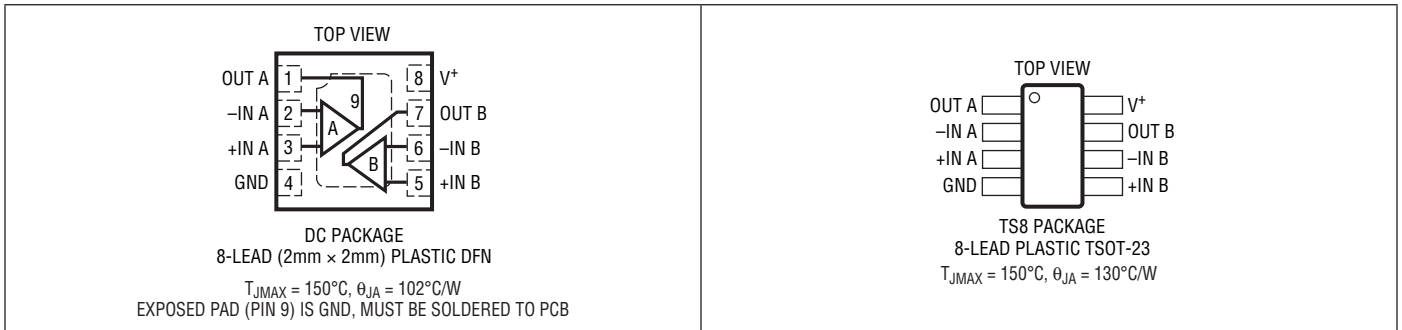


# LTC6702

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ( $V^+$ to GND) .....	6V	Specified Temperature Range (Note 4)	
Input Voltage.....	6V	LTC6702C .....	0°C to 70°C
Input Current.....	-10mA	LTC6702I .....	-40°C to 85°C
Output Short-Circuit Duration (Note 2) .....	Indefinite	LTC6702H .....	-40°C to 125°C
Operating Temperature Range (Note 3)		Junction Temperature .....	150°C
LTC6702C .....	-40°C to 85°C	Storage Temperature Range.....	-65°C to 150°C
LTC6702I .....	-40°C to 85°C	Lead Temperature (Soldering, 10 sec)	
LTC6702H .....	-40°C to 125°C	TSOT Packages.....	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

### Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6702CDC#TRMPBF	LTC6702CDC#TRPBF	LCZJ	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC6702IDC#TRMPBF	LTC6702IDC#TRPBF	LCZJ	8-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LTC6702HDC#TRMPBF	LTC6702HDC#TRPBF	LCZJ	8-Lead (2mm × 2mm) Plastic DFN	-40°C to 125°C
LTC6702CTS8#TRMPBF	LTC6702CTS8#TRPBF	LTCZK	8-Lead Plastic TSOT-23	0°C to 70°C
LTC6702ITS8#TRMPBF	LTC6702ITS8#TRPBF	LTCZK	8-Lead Plastic TSOT-23	-40°C to 85°C
LTC6702HTS8#TRMPBF	LTC6702HTS8#TRPBF	LTCZK	8-Lead Plastic TSOT-23	-40°C to 125°C

TRM = 500 pieces. \*Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = 3\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $C_{\text{OUT}} = 20\text{pF}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V^+$	Supply Voltage	Guaranteed by PSRR	● 1.7		5.5	V	
$I_+$	Supply Current per Comparator	$V^+ = 3\text{V}$	●	24	30 40	$\mu\text{A}$ $\mu\text{A}$	
		$V^+ = 5\text{V}$	●	25	32 42	$\mu\text{A}$ $\mu\text{A}$	
$V_{\text{OS}}$	Input Offset Voltage	(Note 5)	●	1	3.5	mV	
		LTC6702C/LTC6702I	●		5	mV	
		LTC6702H	●		6	mV	
$V_{\text{HYST}}$	Input Hysteresis Voltage	(Note 5)	●	2.5	4.3	6.2	mV
		LTC6702C/LTC6702I	●	1.6	7.2	mV	
		LTC6702H	●	1.6	8.2	mV	
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	6		$\mu\text{V}/^\circ\text{C}$	
$I_{\text{IN}}$	Input Leakage Current	LTC6702C/LTC6702I	●	0.001	1	nA	
		LTC6702H	●		10	nA	
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -0.1\text{V}$ to $V_{\text{DD}} - 1.2\text{V}$	●	58	70	dB	
			●	56		dB	
	Input Voltage Range	Guaranteed by CMRR	●	-0.1	$V_{\text{DD}} - 1.2$	V	
PSRR	Power Supply Rejection Ratio	$V^+ = 1.7\text{V}$ to $5.5\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	●	56	65	dB	
			●	54		dB	
$V_{\text{OL}}$	Output Swing Low	Overdrive = 20mV (Note 6)	●		10	mV	
		$I_{\text{SINK}} = 100\mu\text{A}$	●		250	mV	
		$I_{\text{SINK}} = 15\text{mA}$	●				
$V_{\text{OH}}$	Output Swing High	Overdrive = 20mV (Note 6)	●		10	mV	
		$I_{\text{SOURCE}} = 100\mu\text{A}$	●		350	mV	
		$I_{\text{SOURCE}} = 15\text{mA}$	●				
$t_{\text{PD}}$	Propagation Delay	(Note 7)	●	320	450 500	ns	
						ns	
$\Delta t_{\text{PD}}$	Differential Propagation Delay	Between Channels		4		ns	
$t_{\text{SKEW}}$	Propagation Delay Skew	Between $t_{\text{PDHL}}/t_{\text{PDHL}}$		4		ns	
$t_r$	Output Rise Time			11		ns	
$t_f$	Output Fall Time			15		ns	
$f_{\text{MAX}}$	Maximum Toggle Frequency			3.2		MHz	
$I_{\text{SC}}$	Short-Circuit Current	$V^+ = 5\text{V}$		$\pm 250$		mA	

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply voltage and how many comparators are shorted. The  $\theta_{\text{JA}}$  specified for the DC and TS packages is with minimal PCB heat spreading metal. Using expanded metal area on all layers of a board reduces this value.

**Note 3:** The LTC6702C and LTC6702I are guaranteed functional over the temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6702H is guaranteed functional over the operating temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 4:** The LTC6702C is guaranteed to meet specified performance from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . The LTC6702C is designed, characterized and expected to

meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  but is not tested or QA sampled at these temperatures. The LTC6702I is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6702H is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

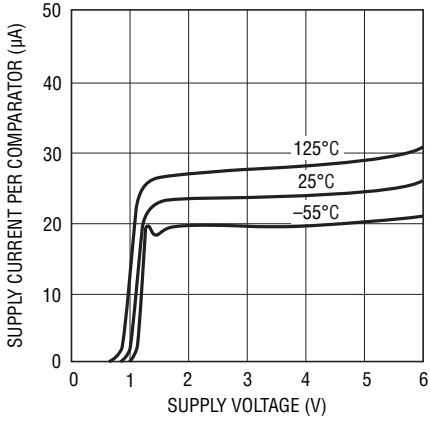
**Note 5:** The LTC6702 comparators include internal hysteresis. The offset voltage is defined as the average of the input voltages (trip points) required to change the output in each direction minus  $V_{\text{CM}}$ , while the hysteresis voltage is the difference of these trip points.

**Note 6:** Output voltage swings are measured between the output and power supply rails.

**Note 7:** Propagation delay is for 200mV steps, and 50mV of overdrive. Overdrive is measured relative to the positive and negative trip points.

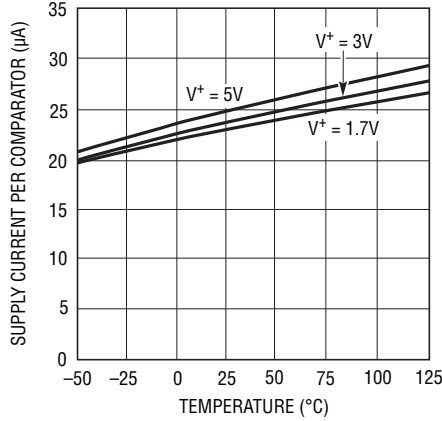
## TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current vs Supply Voltage**



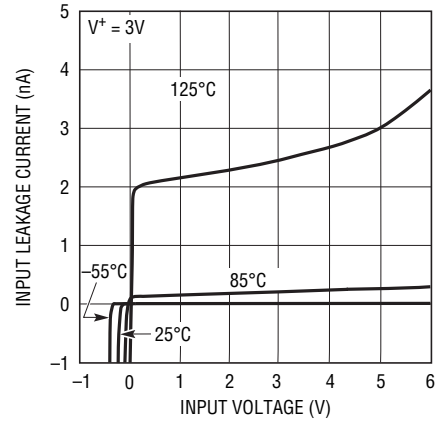
6702 G01

**Supply Current vs Temperature**



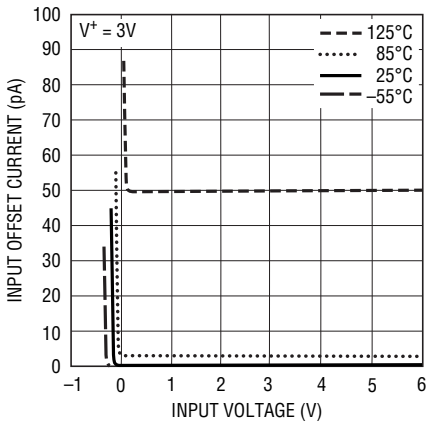
6702 G02

**Input Leakage Current vs Input Voltage**



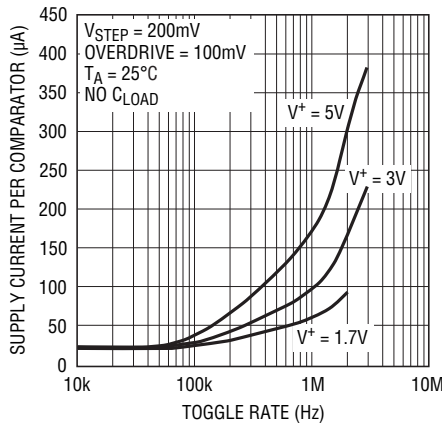
6702 G03

**Input Offset Current vs Input Voltage**



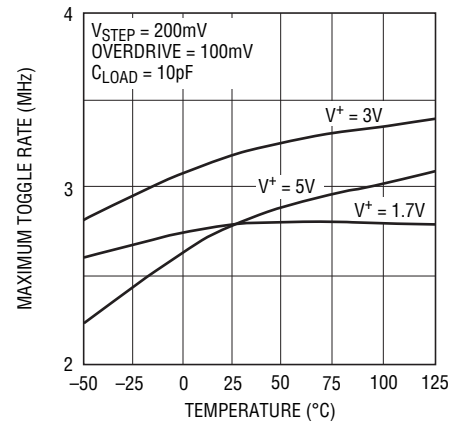
6702 G04

**Supply Current vs Toggle Rate**



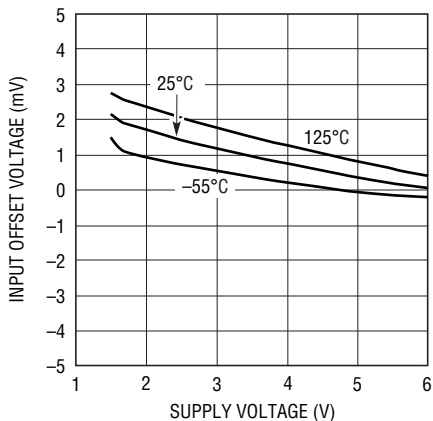
6702 G05

**Maximum Toggle Rate vs Temperature**



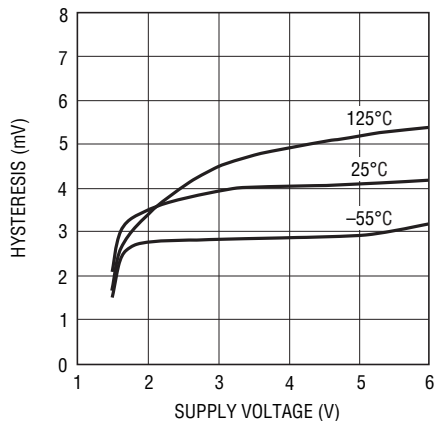
6702 G06

**Input Offset Voltage vs Supply Voltage**



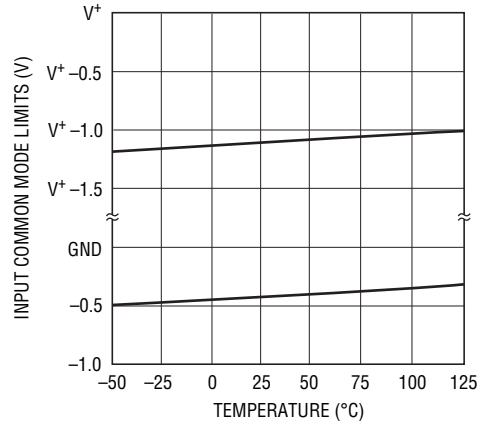
6702 G07

**Hysteresis vs Supply Voltage**



6702 G08

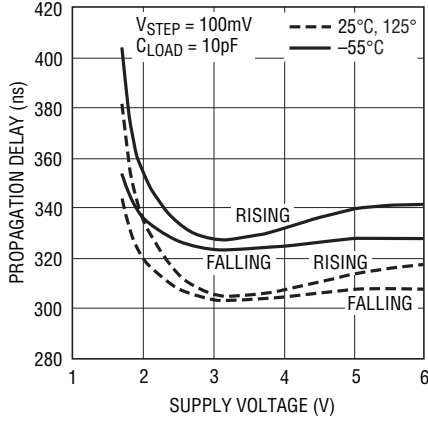
**Input Common Mode Limits vs Temperature**



6702 G09

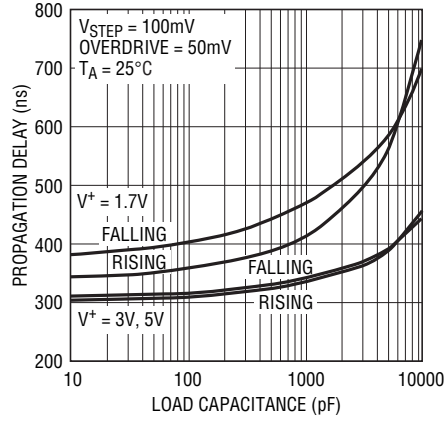
# TYPICAL PERFORMANCE CHARACTERISTICS

**Propagation Delay vs Supply Voltage**



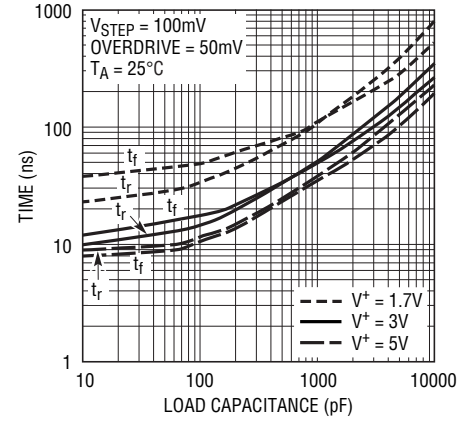
6702 G10

**Propagation Delay vs Load Capacitance**



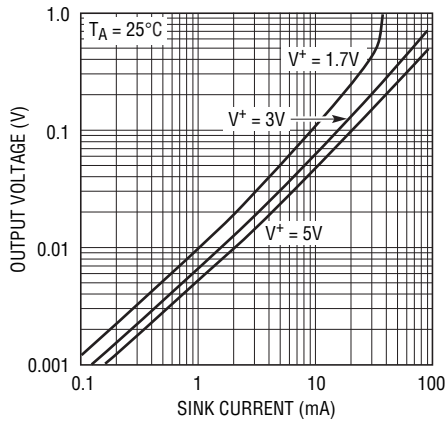
6702 011

**Output Rise and Fall Times vs Load Capacitance**



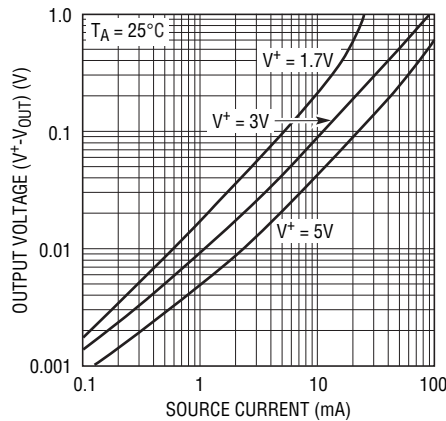
6702 G12

**Output Low Voltage vs Load Current**



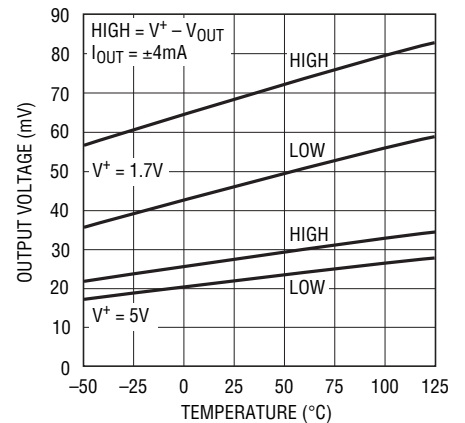
6702 G13

**Output High Voltage vs Load Current**



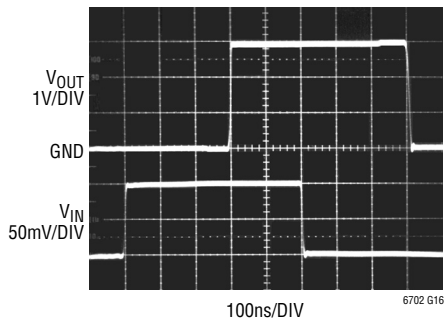
6702 G14

**Output Voltage vs Temperature**



6702 G15

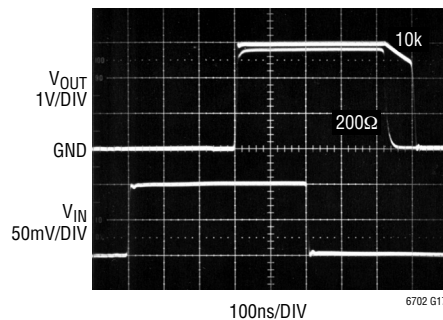
**Propagation Delay**



6702 G16

V+ = 3V  
CL = 20pF  
VCM = 500mV

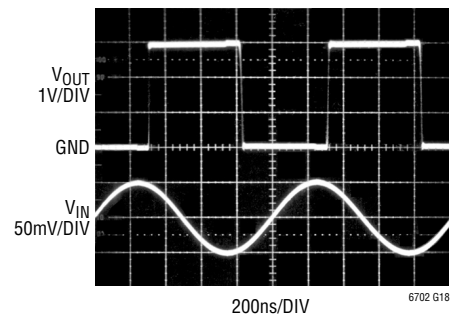
**Propagation Delay with Load**



6702 G17

V+ = 3V VCM = 500mV  
CL = 20pF RL = 10k, 200Ω

**1MHz Sinusoid Response**



6702 G18

V+ = 3V  
CL = 20pF  
VCM = 500mV

## PIN FUNCTIONS

**OUT A (Pin 1):** Output of Comparator A.

**-IN A (Pin 2):** Inverting Input of Comparator A.

**+IN A (Pin 3):** Noninverting Input of Comparator A.

**GND (Pin 4):** Ground.

**+IN B (Pin 5):** Noninverting Input of Comparator B.

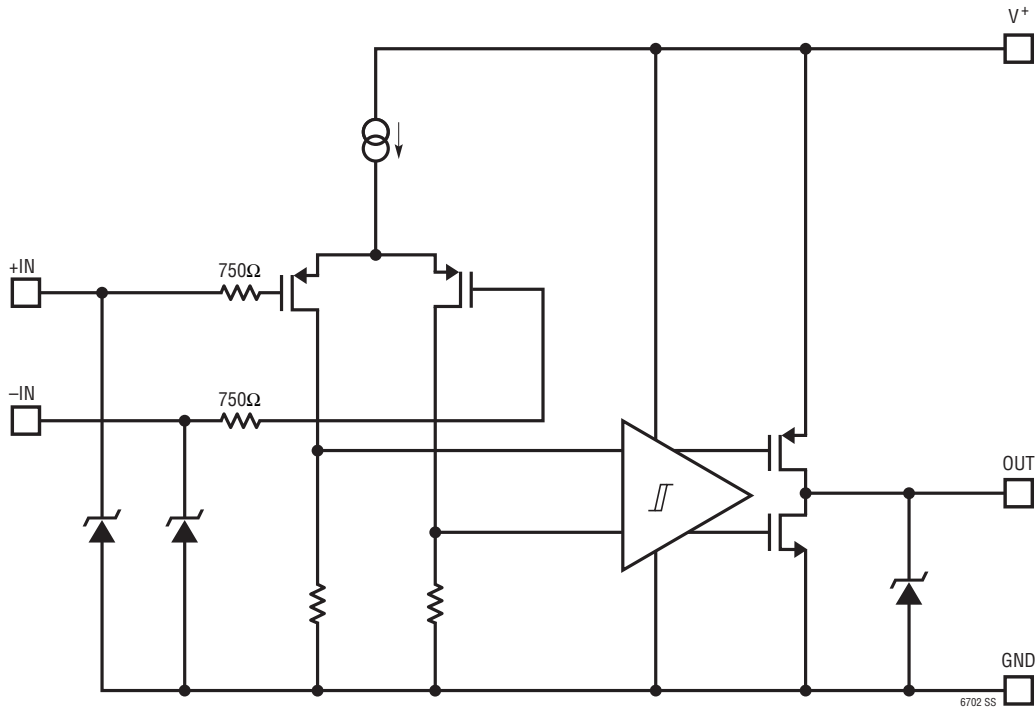
**-IN B (Pin 6):** Inverting Input of Comparator B.

**OUT B (Pin 7):** Output of Comparator B.

**V<sup>+</sup> (Pin 8):** Positive Supply Voltage

**Exposed Pad (Pin 9, DC Package Only):** Ground. The Exposed Pad must be soldered to PCB.

## SIMPLIFIED SCHEMATIC



## APPLICATIONS INFORMATION

The LTC6702 device is a fast (500ns delay), low power, low voltage (1.7V to 5.5V supply) general purpose dual comparator. It provides rail-to-rail outputs able to interface to TTL/CMOS, draws low supply currents (30 $\mu$ A/comparator), and has internal hysteresis (approximately 4mV).

### Hysteresis

Each comparator has built-in hysteresis to simplify designs, to insure stable operation in the presence of noise at the inputs, and to reject supply rail noise. The reference voltage applied to the input is not the exact switching threshold value due to the built-in hysteresis. Actual output switching typically occurs within  $\pm 2.2$ mV of the reference voltage, plus or minus the input offset voltage. External positive feedback circuitry can be employed to increase effective hysteresis if desired, as shown in Figure 1. This circuitry will provide an apparent effect on both the rising and falling input thresholds (the actual internal trip points remain unaffected). If an inverting configuration with hysteresis is needed, simply swap the  $V_{IN}$  and  $V_{REF}$  connections.

### Unused Inputs

Any unused inputs should be connected in a way that fixes the output logic state high or low. One easy way to do this is to tie +IN to  $V^+$  and -IN to GND.

### Input Protection

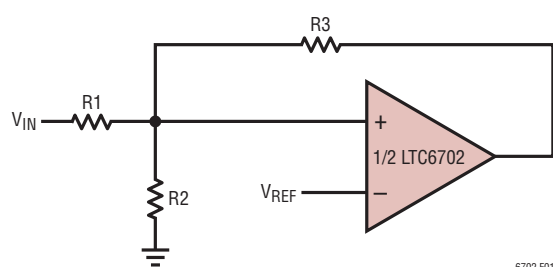
External input protection circuitry is only needed if currents would otherwise exceed the absolute maximum rating. Inputs driven further negative than 100mV below ground will not cause damage provided the current is limited to 10mA. ESD protection diodes are provided to prevent damage during handling.

### Comparator Input

The allowable input voltage ranges from 100mV below GND to within 1.2V of the positive supply. The input may be forced below ground without causing an improper output, though some additional input current will begin to flow from the ESD input protection diode. The inputs can reach up to 6V independent of the  $V^+$  supply voltage without causing additional input current or damage to the part. As long as one input is within the allowable input voltage range, the LTC6702 will continue to function normally.

### Comparator Output

The comparator output is a push-pull CMOS stage guaranteed to swing to within 350mV of  $V^+$  and 250mV of ground, over temperature when sourcing or sinking 15mA. No external pull-up/down resistor is required. To



$$\text{Additional Hysteresis} = \frac{R1}{R3} \cdot V^+$$

Trip Voltages:

$$V_{IN(L \rightarrow H)} = V_{REF} \cdot R1 \cdot \left( \frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3} \right)$$

$$V_{IN(H \rightarrow L)} = V_{REF} \cdot R1 \cdot \left( \frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3} \right) - \left( \frac{R1}{R3} \right) \cdot V^+$$

Example: Additional Hysteresis = 50mV,  $V^+ = 5V$

$R1 = 10k$

$R2 = 249k$

$R3 = 1M$

FOR  $V_{REF} = 0.5V$ :  $V_{IN(L \rightarrow H)} = 0.525V$

$V_{IN(H \rightarrow L)} = 0.475V$

Figure 1. Additional Hysteresis Circuit for Noninverting Configuration

## APPLICATIONS INFORMATION

maintain micropower operation, the output stage uses a break-before-make circuit. The break interval of this circuit turns off both the pull-up and pull-down devices for tens of nanoseconds before activating the appropriate output transistor (depends on the output transition direction). Any load connected to the output will charge or discharge internal capacitance during this interval. This can create a soft corner during output transitions and also decrease the propagation delay. The Typical Performance Characteristics section shows this behavior under three load conditions: unloaded, 10k to ground and 200Ω to ground. Loads to V<sup>+</sup> have a similar affect when the output is transitioning from low to high.

### Power Supplies

The comparator circuitry operates from a single 1.7V to 5.5V. A 0.1μF minimum bypass capacitor is required between the V<sup>+</sup> pin and GND. When the output is sinking

at least 1mA, a 1μF bypass capacitor is recommended. Pulsing the V<sup>+</sup> supply to the comparators on and off may engage the ESD protection circuitry at the V<sup>+</sup> pin. If this occurs, current is pulled from the V<sup>+</sup> pin through the output stage. Using the recommended supply bypass capacitors with some series resistance in the V<sup>+</sup> supply line will help to prevent this action in pulsed supply applications.

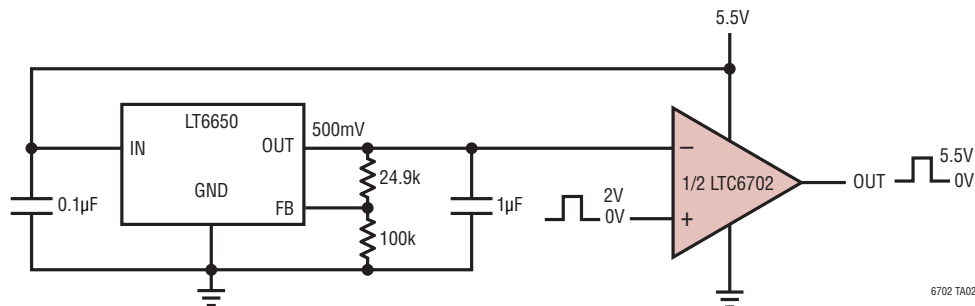
### Level Translators

The level translators in the Typical Applications section show an adjustable high-precision voltage reference enabling the user to vary the threshold voltage. Simply adjusting the ratio of the two resistors changes the threshold voltage according to the following equation:

$$V_{\text{THR}} = 0.4 \left( 1 + \frac{R_F}{R_G} \right)$$

## TYPICAL APPLICATIONS

Low to High Level Translator

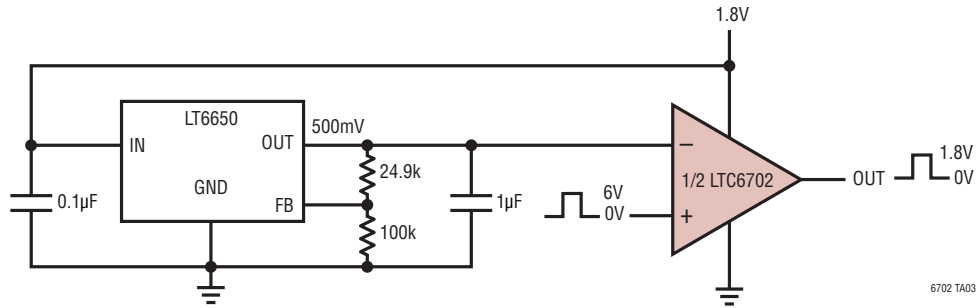


6702 TA02

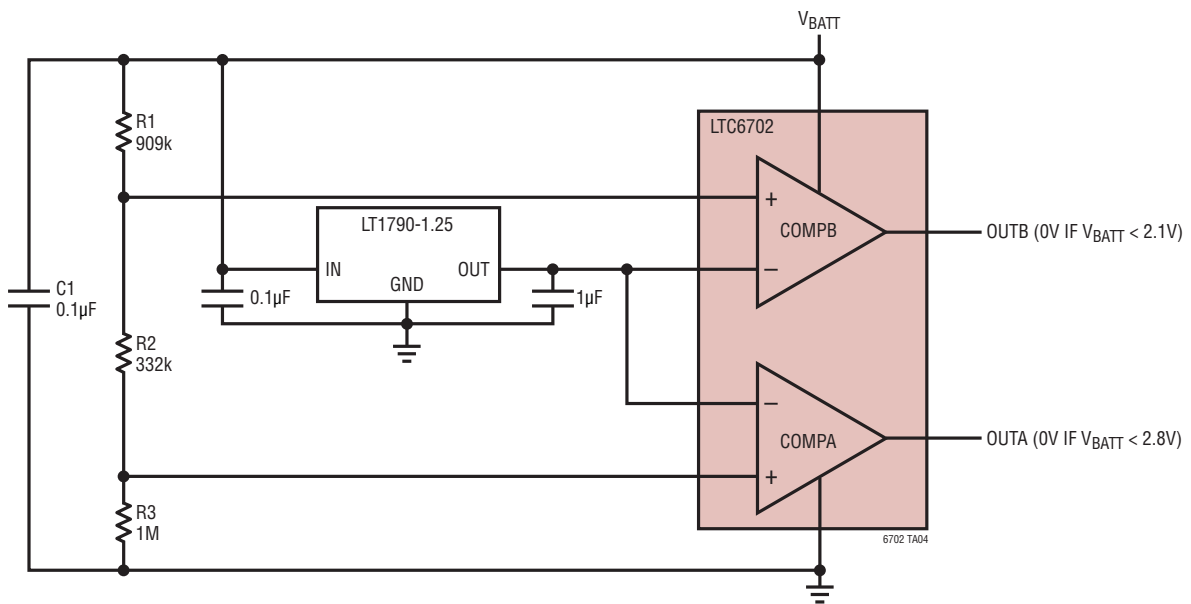


TYPICAL APPLICATIONS

High to Low Level Translator

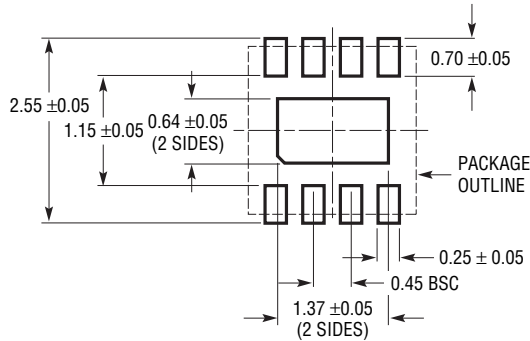


Micropower Battery Monitor with Fast Response

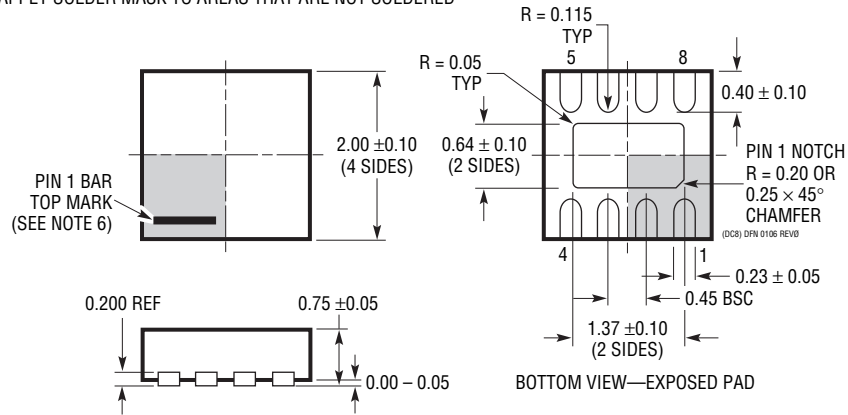


# PACKAGE DESCRIPTION

**DC Package**  
**8-Lead Plastic DFN (2mm × 2mm)**  
 (Reference LTC DWG # 05-08-1719 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

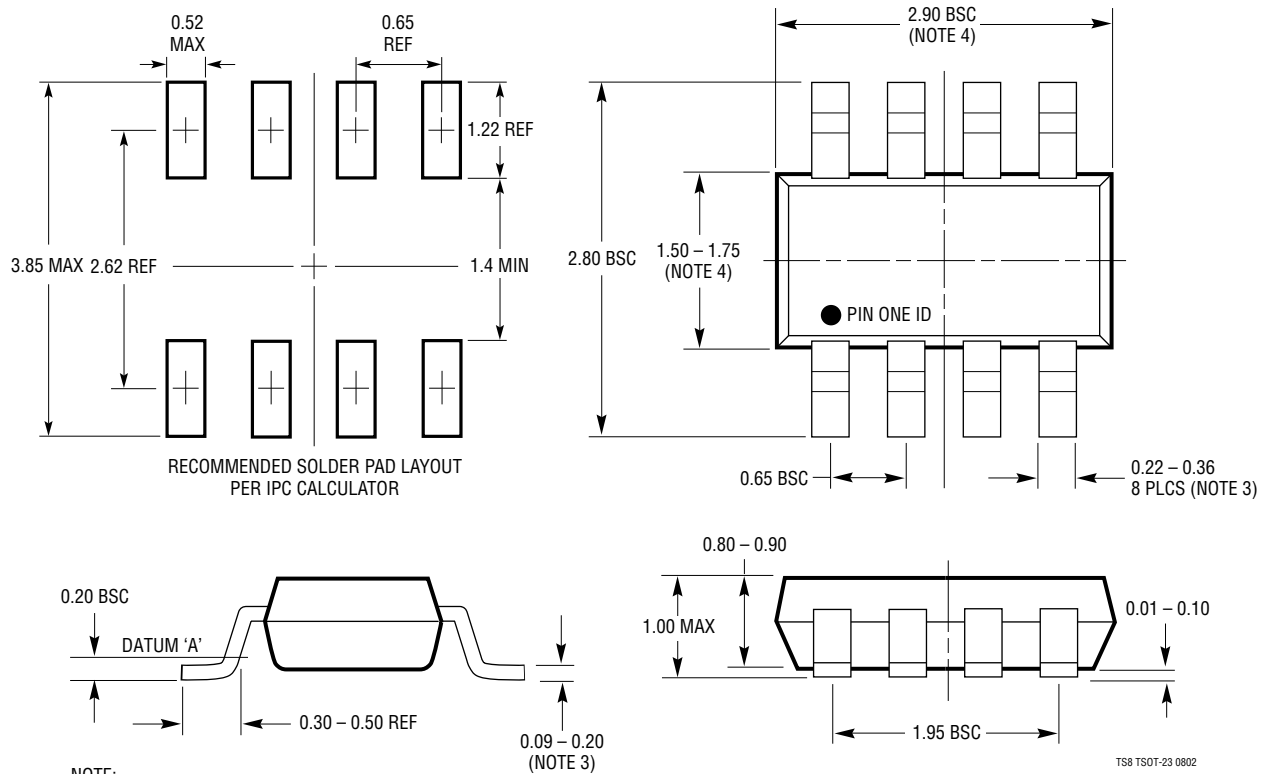


**NOTE:**

1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**TS8 Package**  
**8-Lead Plastic TSOT-23**  
 (Reference LTC DWG # 05-08-1637)



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS ARE INCLUSIVE OF PLATING
  4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
  5. MOLD FLASH SHALL NOT EXCEED 0.254mm
  6. JEDEC PACKAGE REFERENCE IS MO-193

TS8 TSOT-23 0802