Zero Drift, Precision Instrumentation Amplifier with Digitally Programmable Gain

FEATURES

- **14 Levels of Programmable Gain**
- **125dB CMRR Independent of Gain**
- **Gain Accuracy 0.1% (Typ)**
- **Maximum Offset Voltage of 10µV**
- **Maximum Offset Voltage Drift: 50nV/°C**
- **Rail-to-Rail Input and Output**
- **Parallel or Serial (SPI) Interface for Gain Setting**
- Supply Operation: 2.7V to ±5.5V
- Typical Noise: 2.5µV$_{P-P}$ (0.01Hz to 10Hz)
- 16-Lead SSOP and 12-Lead DFN Packages

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifier
- High Resolution Data Acquisition

DESCRIPTION

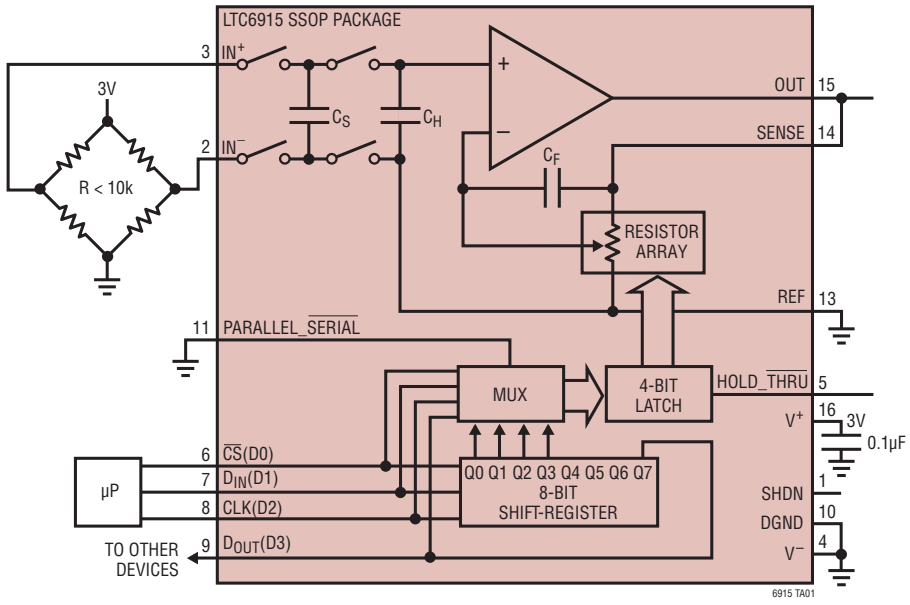
The LTC®6915 is a precision programmable gain instrumentation amplifier. The gain can be programmed to 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, or 4096 through a parallel or serial interface. The CMRR is typically 125dB with a single 5V supply with any programmed gain. The offset is below 10µV with a temperature drift of less than 50nV/°C.

The LTC6915 uses charge balanced sampled data techniques to convert a differential input voltage into a single ended signal that is in turn amplified by a zero-drift operational amplifier.

The differential inputs operate from rail-to-rail and the single-ended output swings from rail-to-rail. The LTC6915 can be used in single power supply applications as low as 2.7V, or with dual ±5V supplies. The LTC6915 is available in a 16-lead SSOP package and a 12-lead DFN surface mount package.

TYPICAL APPLICATION

Differential Bridge Amplifier with Gain Programmed through the Serial Interface

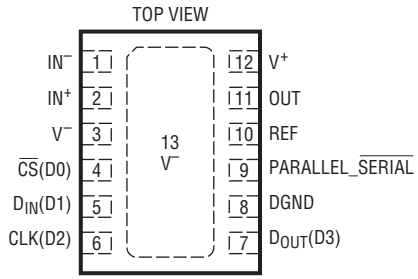


ABSOLUTE MAXIMUM RATINGS

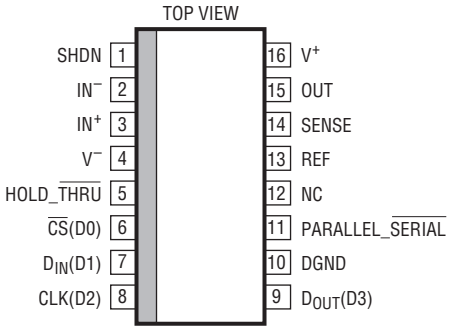
(Note 1)

Total Supply Voltage (V^+ to V^-) 11V
Input Current..... ±10mA
$|V_{IN}^+ - V_{REF}|$ 5.5V
$|V_{IN}^- - V_{REF}|$ 5.5V
$|V^+ - V_{DGND}|$ 5.5V
$|V_{DGND} - V^-|$ 5.5V
Digital Input Voltage..... V^- to V^+
Operating Temperature Range
LTC6915C ..... –0°C to 70°C
LTC6915I ..... –40°C to 85°C
LTC6915H ..... –40°C to 125°C
Junction Temperature
(GN Package) ..... 150°C
(DFN Package) ..... 125°C
Storage Temperature
(GN Package) ..... –65°C to 150°C
(DFN Package) ..... –65°C to 125°C
Lead Temperature (Soldering 10 sec)..... 300°C

PIN CONFIGURATION



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W
EXPOSED PAD (PIN 13) IS V^-, MUST BE SOLDERED TO PCB



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6915CDE#PBF	LTC6915CDE#TRPBF	6915	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC6915IDE#PBF	LTC6915IDE#TRPBF	6915I	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6915CGN#PBF	LTC6915CGN#TRPBF	6915	16-Lead Narrow Plastic SSOP	0°C to 70°C
LTC6915IGN#PBF	LTC6915IGN#TRPBF	6915I	16-Lead Narrow Plastic SSOP	–40°C to 85°C
LTC6915HGN#PBF	LTC6915HGN#TRPBF	6915H	16-Lead Narrow Plastic SSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC6915CDE	LTC6915CDE#TR	6915	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC6915IDE	LTC6915IDE#TR	6915I	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6915CGN	LTC6915CGN#TR	6915	16-Lead Narrow Plastic SSOP	0°C to 70°C
LTC6915IGN	LTC6915IGN#TR	6915I	16-Lead Narrow Plastic SSOP	–40°C to 85°C
LTC6915HGN	LTC6915HGN#TR	6915H	16-Lead Narrow Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+ = 3V, V^- = 0V, V_{REF} = 200mV							
	Gain Error (Note 2)	A_V = 1 (R_L =10k)	●	–0.075	0	0.075	%
	Gain Error (Note 2)	A_V = 2 to 32 (R_L = 10k)	●	–0.5	0	0.5	%
	Gain Error (Note 2)	A_V = 64 to 1024 (R_L = 10k)	●	–0.6	–0.1	0.6	%
	Gain Error (Note 2)	A_V = 2048, 4096 (R_L = 10k)	●	–1	–0.2	1.0	%
	Gain Nonlinearity	A_V = 1	●		3	15	ppm
V_{OS}	Input Offset Voltage (Note 3)	V_{CM} = 200mV			–3	±10	µV
	Average Input Offset Drift (Note 3)	T_A = –40°C to 85°C T_A = 85°C to 125°C	● ●			±50 ±100	nV/°C nV/°C
I_B	Average Input Bias Current (Note 4)	V_{CM} = 1.2V	●		5	10	nA
I_{OS}	Average Input Offset Current (Note 4)	V_{CM} = 1.2V	●		1.5	3	nA
en	Input Noise Voltage	DC to 10Hz			2.5		μV_{P-P}
V^+ = 3V, V^- = 0V, V_{REF} = 200mV							
CMRR	Common Mode Rejection Ratio	A_V = 1024, V_{CM} = 0V to 3V, LTC6915C A_V = 1024, V_{CM} = 0.1V to 2.9V, LTC6915I A_V = 1024, V_{CM} = 0V to 3V, LTC6915I A_V = 1024, V_{CM} = 0.1V to 2.9V, LTC6915H A_V = 1024, V_{CM} = 0V to 2.97V, LTC6915H	● ● ● ● ●	100 100 95 100 85	119 119 119		dB dB dB dB dB
PSRR	Power Supply Rejection Ratio (Note 5)	V_S = 2.7V to 6V	●	110	116		dB
	Output Voltage Swing High (Referenced to V^-)	Sourcing 200µA Sourcing 2mA	● ●	2.95 2.75	2.98 2.87		V V
	Output Voltage Swing Low (Referenced to V^-)	Sinking 200µA Sinking 2mA	● ●		18 130	50 300	mV mV
	Supply Current, Parallel Mode	No Load at OUT, V_{CM} = 200mV	●		0.88	1.3	mA
	Supply Current, Serial Mode (Note 6)	No Load at OUT, Capacitive Load at D_{OUT} (C_L) = 15pF, Continuous CLK Frequency = 4MHz, $\overline{CS}$ = LOW, Gain Control Code = 0001	●		1.1	1.65	mA
	Supply Current Shutdown	V_{SHDN} = 2.7V (Hardware Shutdown) V_{SHDN} = 1V, Gain Control Code = 0000 (Software Shutdown)	● ●		1 125	4 180	µA µA
	SHDN Input High		●	2.7			V
	SHDN Input Low		●			1	V
	SHDN and HOLD_THRU Input Current (Note 2)		●			5	µA
	Internal Op Amp Gain Bandwidth				200		kHz
	Slew Rate				0.2		V/µs
	Internal Sampling Frequency				3		kHz
V^+ = 5V, V^- = 0V, V_{REF} = 200mV							
	Gain Error (Note 2)	A_V = 1 (R_L = 10k)	●	–0.075	0	0.075	%
	Gain Error (Note 2)	A_V = 2 to 32 (R_L= 10k)	●	–0.5	0	0.5	%
	Gain Error (Note 2)	A_V = 64 to 1024 (R_L = 10k)	●	–0.6	–0.1	0.6	%
	Gain Error (Note 2)	A_V = 2048, 4096 (R_L = 10k)	●	–1	–0.2	1	%
	Gain Nonlinearity	A_V = 1	●		3	15	ppm

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

V_{OS}	Input Offset Voltage (Note 3)	V_{CM} = 200mV			–3	±10	µV
	Average Input Offset Drift (Note 3)	T_A = –40°C to 85°C T_A = 85°C to 125°C	● ●			±50 ±100	nV/°C nV/°C
	Average Input Bias Current (Note 4)	V_{CM} = 1.2V	●		5	10	nA
I_{OS}	Average Input Offset Current (Note 4)	V_{CM} = 1.2V	●		1.5	3	nA
CMRR	Common Mode Rejection Ratio	A_V = 1024, V_{CM} = 0V to 5V, LTC6915C A_V = 1024, V_{CM} = 0.1V to 4.9V, LTC6915I A_V = 1024, V_{CM} = 0V to 5V, LTC6915I A_V = 1024, V_{CM} = 0.1V to 4.9V, LTC6915H A_V = 1024, V_{CM} = 0V to 4.97V, LTC6915H	● ● ● ● ●	105 105 95 100 85	125 125 125		dB dB dB dB dB
PSRR	Power Supply Rejection Ratio (Note 5)	V_S = 2.7V to 6V	●	110	116		dB
	Output Voltage Swing High	Sourcing 200µA Sourcing 2mA	● ●	4.95 4.80	4.99 4.93		V V
	Output Voltage Swing Low	Sinking 200µA Sinking 2mA	● ●		17 120	50 300	mV mV
V^+ = 5V, V^- = 0V, V_{REF} = 200mV							
	Supply Current, Parallel Mode	No Load at OUT, V_{CM} = 200mV	●		0.95	1.48	mA
	Supply Current, Serial Mode (Note 6)	No Load at OUT, Capacitive Load at D_{OUT} (C_L) = 15pF, Continuous CLK Frequency = 4MHz, $\overline{CS}$ = LOW, Gain Control Code = 0001	●		1.4	2	mA
	Supply Current, Shutdown	V_{SHDN} = 4.5V (Hardware Shutdown) V_{SHDN} = 1V, Gain Control Code = 0000 (Software Shutdown)	● ●		2 135	10 200	µA µA
	SHDN Input High		●	4.5			V
	SHDN Input Low		●			1	V
	SHDN and HOLD_THRU Input Current (Note 2)		●			5	µA
	Internal Op Amp Gain Bandwidth				200		kHz
	Slew Rate				0.2		V/µs
	Internal Sampling Frequency				3		kHz
V^+ = 5V, V^- = –5V, V_{REF} = 0V							
	Gain Error (Note 2)	A_V = 1 (R_L = 10k)	●	–0.075	0	0.075	%
	Gain Error (Note 2)	A_V = 2 to 32 (R_L = 10k)	●	–0.5	0	0.5	%
	Gain Error (Note 2)	A_V = 64 to 1024 (R_L = 10k)	●	–0.6	–0.1	0.6	%
	Gain Error (Note 2)	A_V = 2048, 4096 (R_L = 10k)	●	–1	–0.2	1	%
	Gain Nonlinearity	A_V = 1	●		3	15	ppm
V_{OS}	Input Offset Voltage (Note 3)	V_{CM} = 0mV			5	±20	µV
	Average Input Offset Drift (Note 3)	T_A = –40°C to 85°C T_A = 85°C to 125°C	● ●			±50 ±100	nV/°C nV/°C
I_{OS}	Average Input Bias Current (Note 4)	V_{CM} = 1V	●		4	10	nA
	Average Input Offset Current (Note 4)	V_{CM} = 1V	●		1.5	3	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

CMRR	Common Mode Rejection Ratio	A_V = 1024, V_{CM} = –5V to 5V, LTC6915C A_V = 1024, V_{CM} = –4.9V to 4.9V, LTC6915I A_V = 1024, V_{CM} = –5V to 5V, LTC6915I A_V = 1024, V_{CM} = –4.9V to 4.9V, LTC6915H A_V = 1024, V_{CM} = –5V to 4.97V, LTC6915H	● ● ● ● ●	105 105 100 100 90	123 123 123		dB dB dB dB dB
PSRR	Power Supply Rejection Ratio (Note 5)	V_S = 2.7V to 11V	●	110	116		dB
	Output Voltage Swing High	Sourcing 200µA Sourcing 2mA	● ●	4.97 4.90	4.99 4.96		V V
	Output Voltage Swing Low	Sinking 200µA Sinking 2mA	● ●		–4.98 –4.90	–4.92 –4.70	V V
	Supply Current, Parallel Mode	No Load, V_{CM} = 0mV	●		1.1	1.6	mA
	Supply Current, Serial Mode (Note 6)	No Load at OUT, Capacitive Load at D_{OUT} (C_L) = 15pF, Continuous CLK Frequency = 4MHz, $\overline{CS}$ = LOW, Gain Control Code = 0001	●		1.73	2.48	mA
	Supply Current, Shutdown	V_{SHDN} = 4V (Hardware Shutdown) V_{SHDN} = 1V, Gain Control Code = 0000 (Software Shutdown)	● ●		 160	25 240	µA µA
	SHDN Input High		●	4			V
	SHDN Input Low		●			1	V
V^+ = 5V, $V^–$ = –5V, V_{REF} = 0V							
	SHDN and HOLD_THRU Input Current (Note 2)		●			5	µA
	Internal Op Amp Gain Bandwidth				200		kHz
	Slew Rate				0.2		V/µs
	Internal Sampling Frequency				3		kHz
Digital I/O, All Digital I/O Voltage Referenced to DGND							
V_{IH}	Digital Input High Voltage		●	2.0			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
V_{OH}	Digital Output High Voltage	Sourcing 500µA	●	V^+ – 0.3			V
V_{OL}	Digital Output Low Voltage	Sinking 500µA	●			0.3	V
	Digital Input Leakage	V^+ = 5V, $V^–$ = –5V, V_{IN} = 0V to 5V	●			±2	µA
Timing, V^+ = 2.7V to 4.5V, $V^–$ = 0V (Note 7)							
t_1	D_{IN} Valid to CLK Setup		●	60			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK Low		●	100			ns
t_4	CLK High		●	100			ns
t_5	$\overline{CS}$/LD Pulse Width		●	60			ns
t_6	LSB CLK to $\overline{CS}$/LD		●	60			ns
t_7	$\overline{CS}$/LD Low to CLK		●	30			ns
t_8	D_{OUT} Output Delay	C_L = 15pF	●			125	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	0			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

Timing, V^+ = 4.5V to 5.5V, V^- = 0V (Note 7)					
t_1	D_{IN} Valid to CLK Setup		●	30	ns
t_2	D_{IN} Valid to CLK Hold		●	0	ns
t_3	CLK Low		●	50	ns
t_4	CLK High		●	50	ns
t_5	$\overline{CS}$/LD Pulse Width		●	40	ns
t_6	LSB CLK to $\overline{CS}$/LD		●	40	ns
t_7	$\overline{CS}$/LD Low to CLK		●	20	ns
t_8	D_{OUT} Output Delay	C_L = 15pF	●	85	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	0	ns
Timing, Dual ±4.5V to ±5.5V Supplies (Note 7)					
t_1	D_{IN} Valid to CLK Setup		●	30	ns
t_2	D_{IN} Valid to CLK Hold		●	0	ns
t_3	CLK High		●	50	ns
t_4	CLK Low		●	50	ns
t_5	$\overline{CS}$/LD Pulse Width		●	40	ns
t_6	LSB CLK to $\overline{CS}$/LD		●	40	ns
t_7	$\overline{CS}$/LD Low to CLK		●	20	ns
t_8	D_{OUT} Output Delay	C_L = 15pF	●	85	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	0	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: These parameters are tested at ±5V supply; at 3V and 5V supplies they are guaranteed by design.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit set by test equipment capability.

Note 4: If the total source resistance is less than 10k, no DC errors result from the input bias current or mismatch of the input bias currents or the mismatch of the resistances connected to IN^- and IN^+.

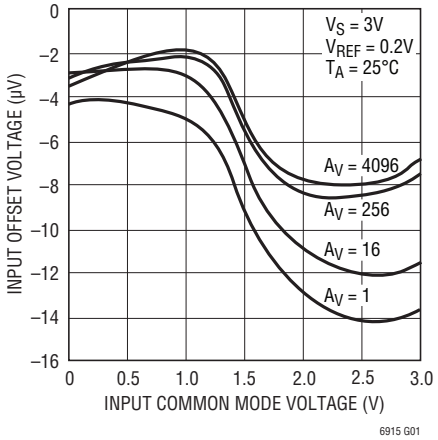
Note 5: The PSRR measurement accuracy depends on the proximity of the power supply bypass capacitor to the device under test. Because of this, the PSRR is 100% tested to relaxed limits at final test. However, their values are guaranteed by design to meet the data sheet limits.

Note 6: Supply current is dependent on the clock frequency. A higher clock frequency results in higher supply current.

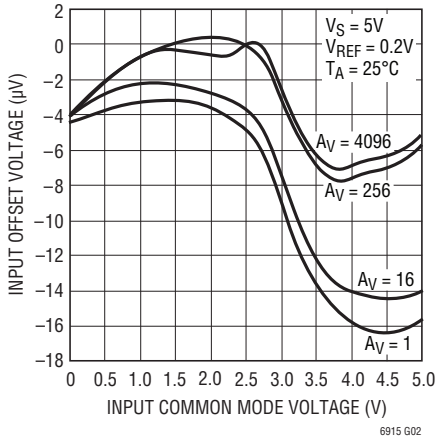
Note 7: Guaranteed by design, not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

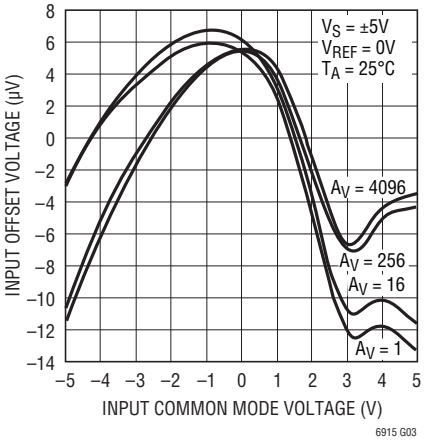
Input Offset Voltage vs Input Common Mode



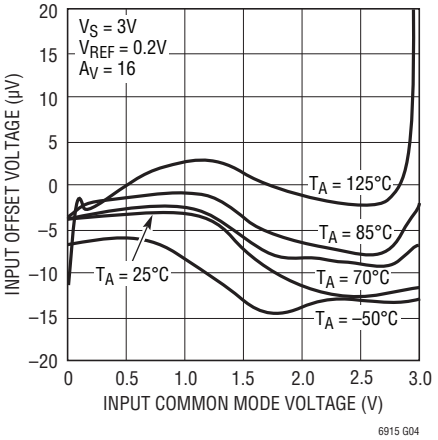
Input Offset Voltage vs Input Common Mode



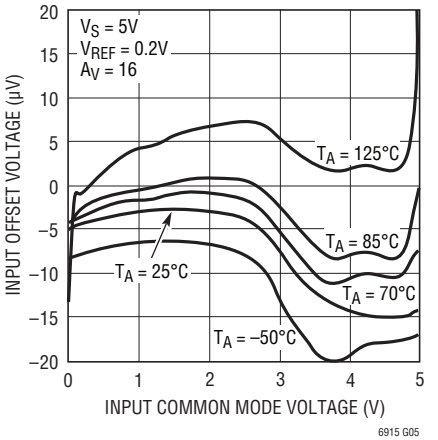
Input Offset Voltage vs Input Common Mode



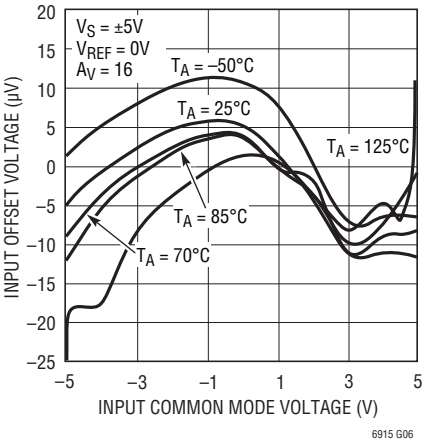
Input Offset Voltage vs Input Common Mode



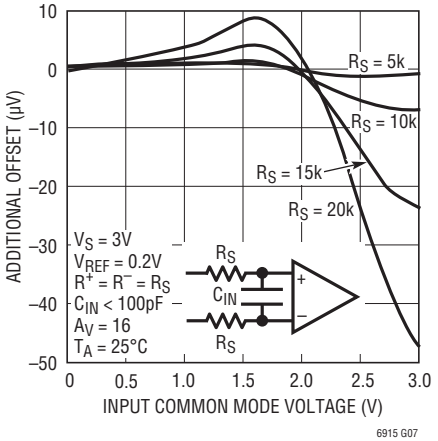
Input Offset Voltage vs Input Common Mode



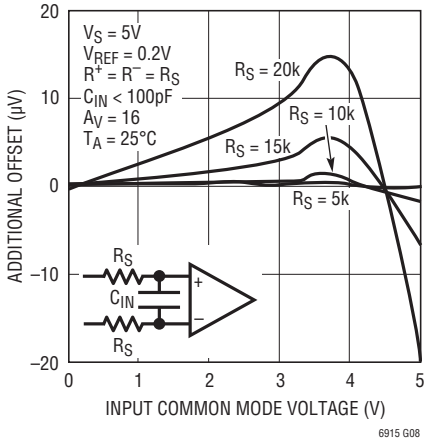
Input Offset Voltage vs Input Common Mode



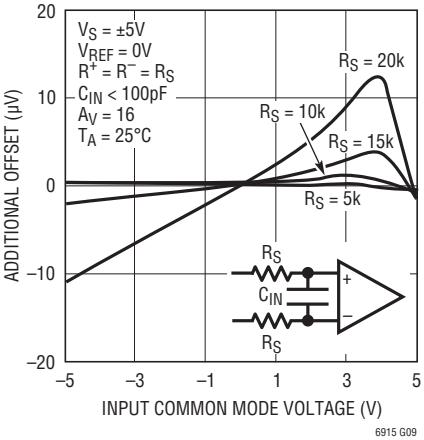
Error Due to Input R_S vs Input Common Mode



Error Due to Input R_S vs Input Common Mode

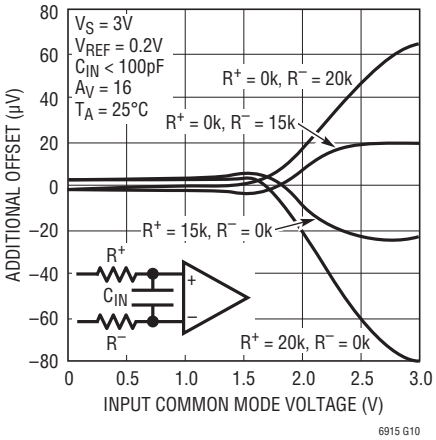


Error Due to Input R_S vs Input Common Mode

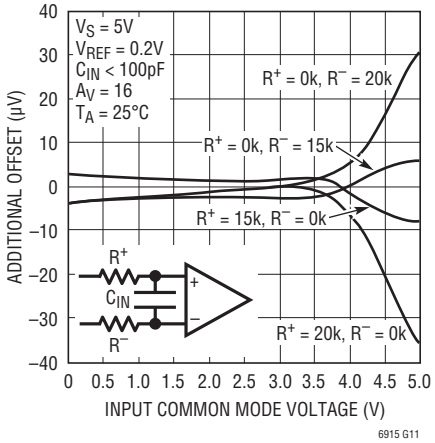


TYPICAL PERFORMANCE CHARACTERISTICS

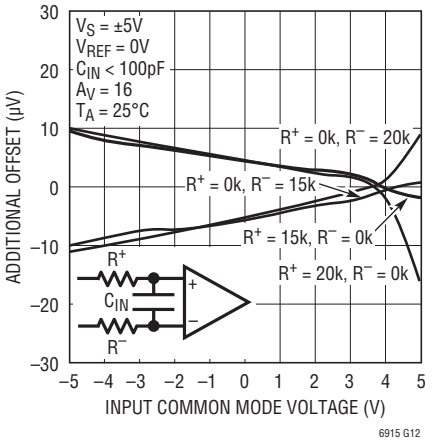
Error Due to Input R_S Mismatch vs Input Common Mode



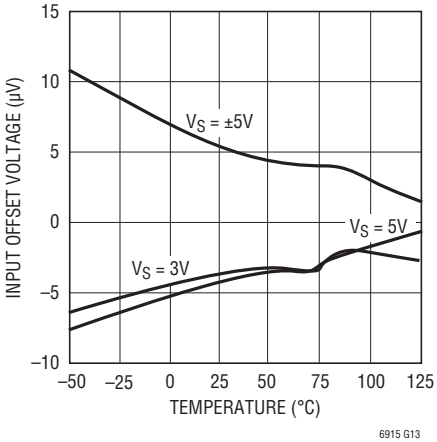
Error Due to Input R_S Mismatch vs Input Common Mode



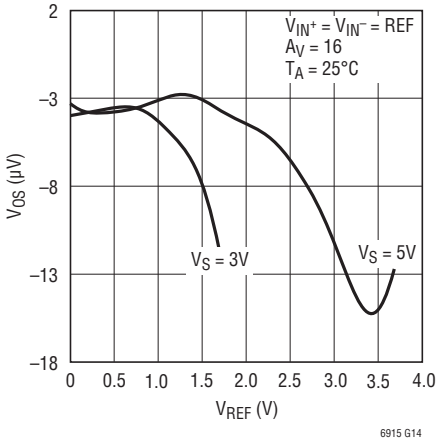
Error Due to Input R_S Mismatch vs Input Common Mode



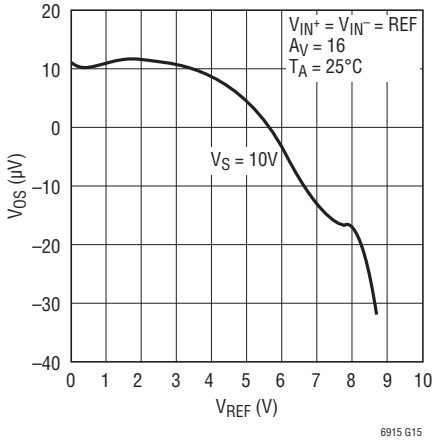
Offset Voltage vs Temperature



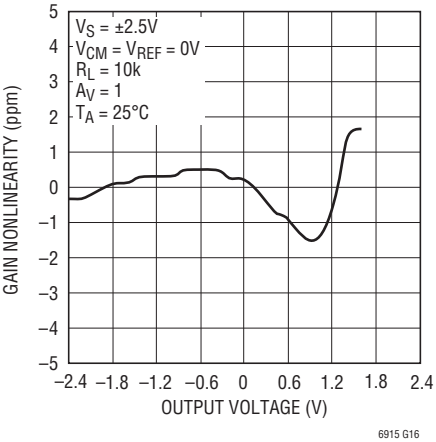
V_{OS} vs REF (Pin 13)



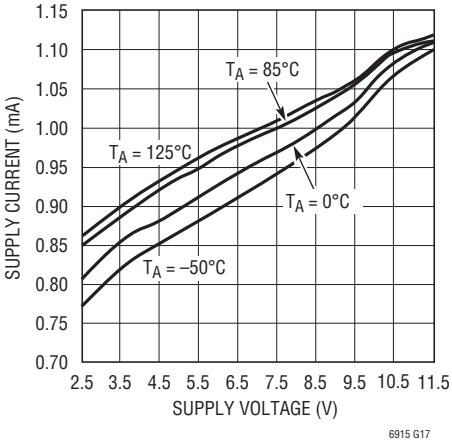
V_{OS} vs REF (Pin 13)



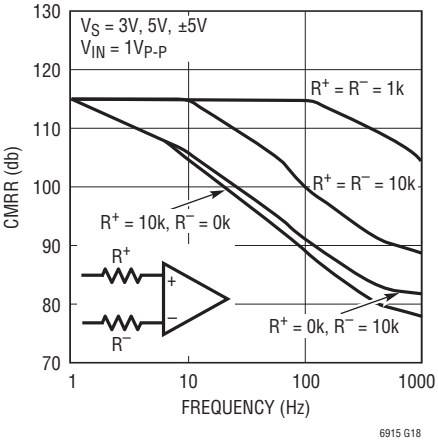
Gain Nonlinearity at Gain = 1 (Gain Nonlinearity Decreases for Gain > 1)



Supply Current vs Supply Voltage

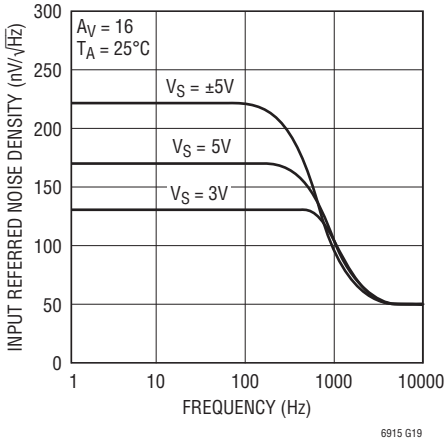


CMRR vs Frequency

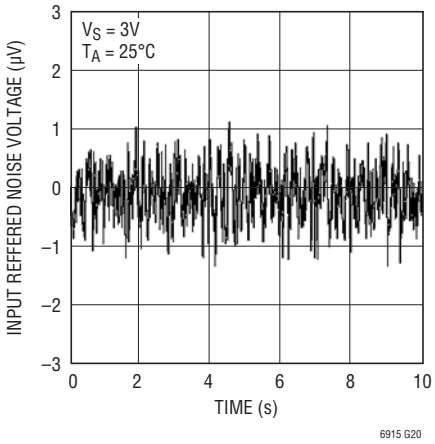


TYPICAL PERFORMANCE CHARACTERISTICS

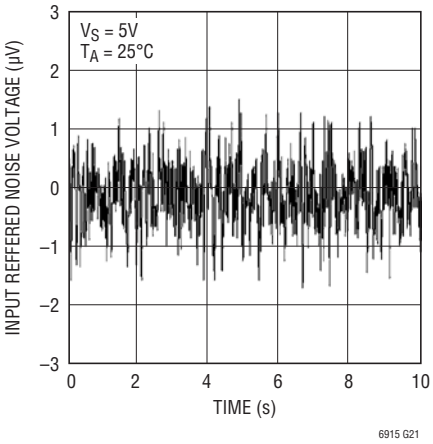
Input Voltage Noise Density vs Frequency



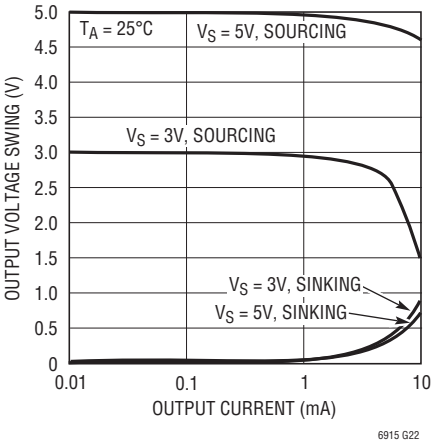
Input Referred Noise in 10Hz Bandwidth



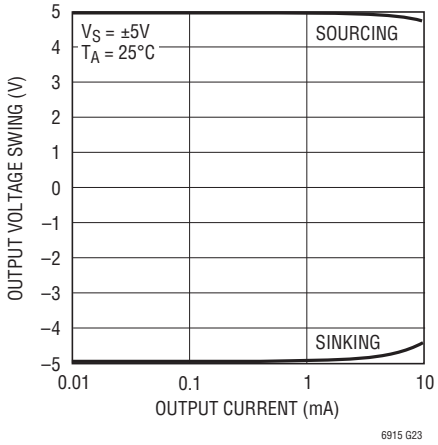
Input Referred Noise in 10Hz Bandwidth



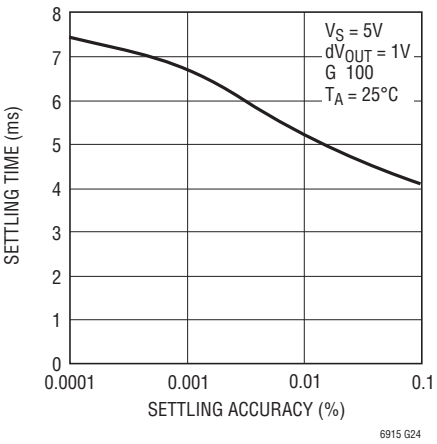
Output Voltage Swing vs Output Current



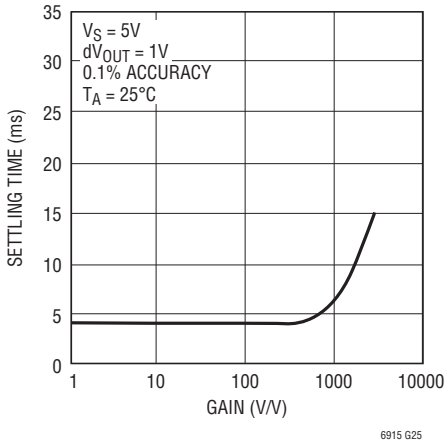
Output Voltage Swing vs Output Current



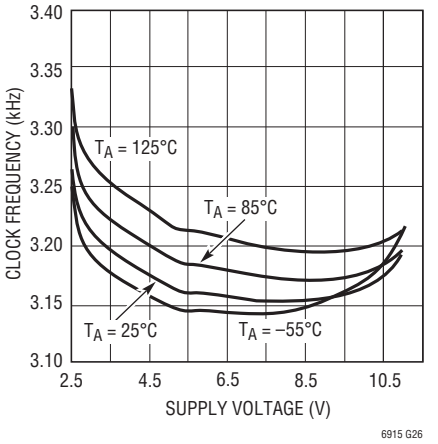
Low Gain Settling Time vs Settling Accuracy



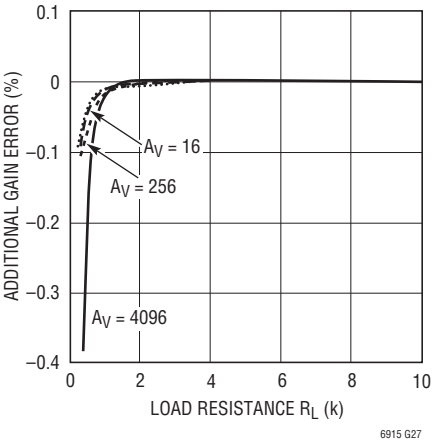
Settling Time vs Gain



Internal Clock Frequency vs Supply Voltage



Additional Gain Error vs Load Resistance



PIN FUNCTIONS (DFN/GN)

IN^- (Pin 1/Pin 2): Inverting Analog Input.

SHDN (Pin 1 GN Package Only): Shutdown Pin. The IC is shut down when SHDN is tied to V^+. An internal current source pulls this pin to V^- when floating.

IN^+ (Pin 2/Pin 3): Noninverting Analog Input.

V^- (Pin 3/Pin 4): Negative Supply.

$\overline{CS}$(D0) (Pin 4/Pin 6): TTL Level Input. When in serial control mode, this pin is the chip select input (active low); in parallel control mode, this pin is the LSB of the parallel gain control code.

D_{IN}(D1) (Pin 5/Pin 7): TTL Level Input. When in serial control mode, this pin is the serial input data; in parallel mode, this pin is the second LSB of the parallel gain control code.

HOLD_$\overline{THRU}$ (Pin 5 GN Package Only): TTL Level Input for Parallel Control Mode. When HOLD_$\overline{THRU}$ is high, the parallel data is latched in an internal D-latch.

CLK(D2) (Pin 6/Pin 8): TTL Level Input. When in serial control mode, this pin is the clock of the serial interface; in parallel mode, this pin is the third LSB of the parallel gain control code.

D_{OUT}(D3) (Pin 7/Pin 9): TTL Level Input. When in serial control mode, this pin is the output of the serial data; in parallel mode, this pin is the MSB of the 4-bit parallel gain control code. In parallel mode operation, if the data in to D_{OUT} (Pin 9) is from a voltage source greater than V^+ (Pin 12), then connect a resistor between the voltage source and D_{OUT} to limit the current into Pin 9 to 5mA or less.

DGND (Pin 8/Pin 10): Digital Ground.

PARALLEL_$\overline{SERIAL}$ (Pin 9/Pin 11): Interface Selection Input. When tied to V^+, the interface is in parallel mode, i.e., the PGA gain is defined by the parallel codes (D3 ~ D0), i.e., $\overline{CS}$(D0), DATA(D1), CLK(D2), and D_{OUT}(D3). When PARALLEL_$\overline{SERIAL}$ pin is tied to V^-, the PGA gain is set by the serial interface.

REF (Pin 10/Pin 13): Voltage Reference for PGA output.

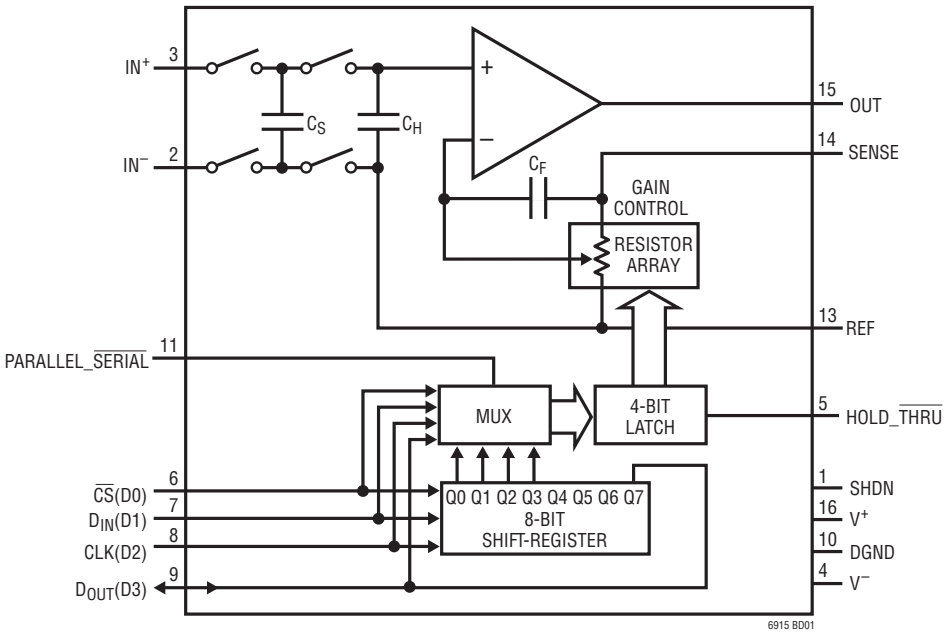
OUT (Pin 11/Pin 15): Amplifier Output. The typical current sourcing/sinking of the OUT pin is 1mA. For minimum gain error, the load resistance should be 1k or greater (refer to the Output Voltage Swing vs Output Current and Gain Error vs Load Resistance in the Typical Performance Characteristics section).

V^+ (Pin 12/Pin 16): Positive Supply.

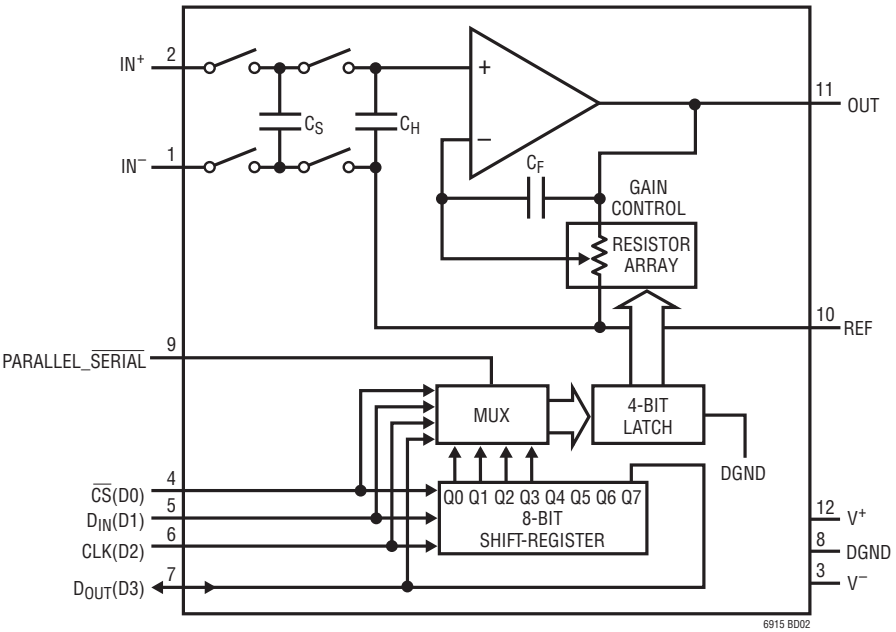
SENSE (Pin 14 GN Package Only): Sense Pin. When the PGA drives a low resistance load and the interconnect resistance between the OUT pin and the load is not negligible, tying the SENSE pin as close as possible to the load can improve the gain accuracy.

BLOCK DIAGRAMS

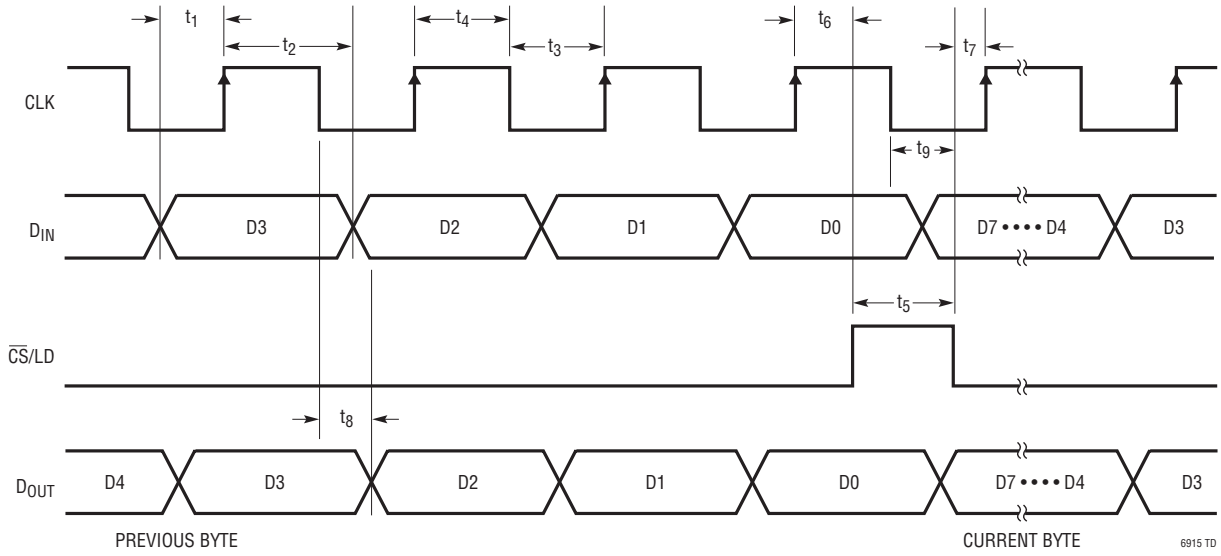
(GN Package Only)



(DFN Package Only)



TIMING DIAGRAM



OPERATION

Theory of Operation (Refer to Block Diagrams)

The LTC6915 uses an internal capacitor (C_S) to sample a differential input signal riding on a DC common mode voltage (the sampling rate is 3kHz and the input switch-on resistance is 1k to 2k, depending on the power supply voltage). This capacitor's charge is transferred to a second internal hold capacitor (C_H) translating the common mode voltage of the input differential signal to that of REF pin. The resulting signal is amplified by a zero-drift op amp in the noninverting configuration. Gain control within the amplifier occurs by switching resistors from a matched resistor array. The LTC6915 has 14 levels of gain, controlled by the parallel or serial interface. A feedback capacitor C_F helps to reduce the switching noise. Due to the input sampling, an LTC6915 may produce aliasing errors for input signals greater than 1.5kHz (one half the 3kHz sampling frequency). However, if the input signal is bandlimited to less than 1.5kHz then an LTC6915 is useful as instrumentation or as a differential to single-ended AC amplifier with programmable gain.

Parallel Interface

As shown in Figure 1, connecting PARALLEL_$\overline{\text{SERIAL}}$ to V^+ allows the gain control code to be set through the parallel lines (D3, D2, D1, D0). When HOLD_$\overline{\text{THRU}}$ is low (referenced to DGND) or floating, the parallel gain control bits (D3 ~ D0) directly control the PGA gain. When HOLD_$\overline{\text{THRU}}$ is high, the parallel gain control bits are read into and held by a 4-bit latch. Any change at D3 ~ D0 will not affect the PGA gain when HOLD_$\overline{\text{THRU}}$ is high. Note that the DFN12 package does not have the HOLD_$\overline{\text{THRU}}$ pin. Instead, it is tied to DGND internally. The D_{OUT}(D3) pin is bidirectional (output in serial mode, input in parallel mode). In parallel mode, the voltage at D_{OUT}(D3) cannot exceed V^+; otherwise, large currents can be injected to V^+ through the parasitic diode (see Figure 2). Connecting a 10k resistor at the D_{OUT}(D3) pin if parallel mode is selected (see Figure 1) is recommended for current limiting.

Serial Interface

Connecting PARALLEL_$\overline{\text{SERIAL}}$ to V^- allows the gain control code to be set through the serial interface. When $\overline{\text{CS}}$ is low, the serial data on D_{IN} is shifted into an 8-bit shift-register on the rising edge of the clock, with the MSB transferred first (see Figure 3). Serial data on D_{OUT} is shifted out on the clock's falling edge. A high $\overline{\text{CS}}$ will load the 4 LSBs of the shift-register into a 4-bit D-latch, which are the gain control bits. The clock is disabled internally when $\overline{\text{CS}}$ is pulled high. Note: CLK must be low before $\overline{\text{CS}}$ is pulled low to avoid an extra internal clock pulse.

OPERATION

D_{OUT} is always active in serial mode (never tri-stated). This simplifies the daisy chaining of the multiple devices. D_{OUT} cannot be "wire-or" to other SPI outputs. In addition, D_{OUT} does not return to zero at the end of transmission, i.e. when $\overline{CS}$ is pulled high.

A LTC6915 may be daisy-chained with other LTC6915s or other devices having serial interfaces by connecting the D_{OUT} to the D_{IN} of the next chip while CLK and $\overline{CS}$ remain common to all chips in the daisy chain. The serial data is clocked to all the chips then the $\overline{CS}$ signal is pulled high to update all of them simultaneously. Figure 4 shows an example of two LTC6915s in a daisy chained SPI configuration.

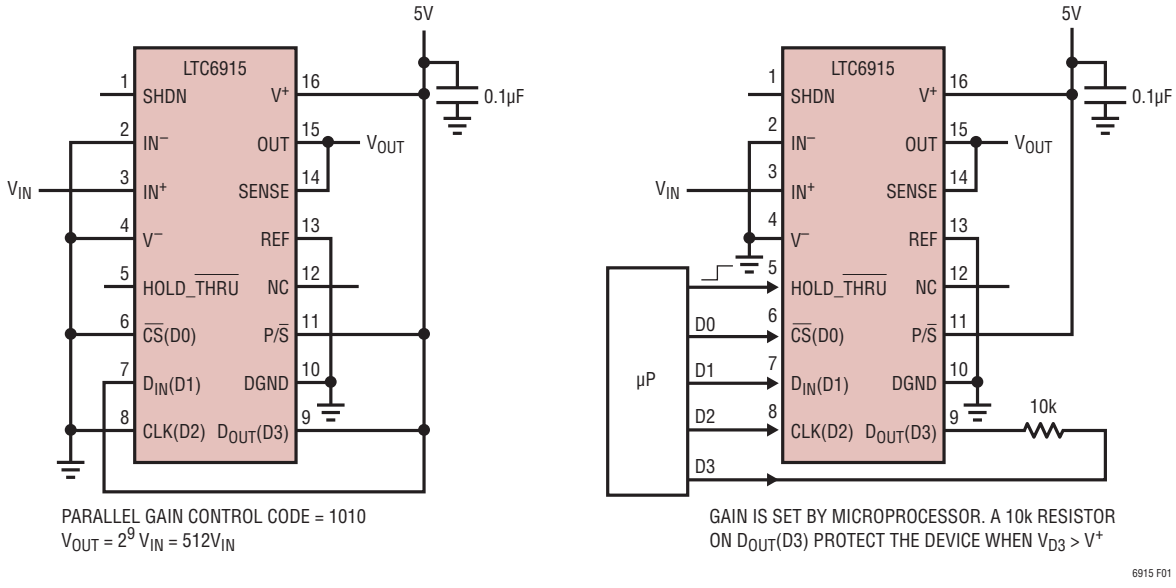


Figure 1. PGA in the Parallel Control Mode

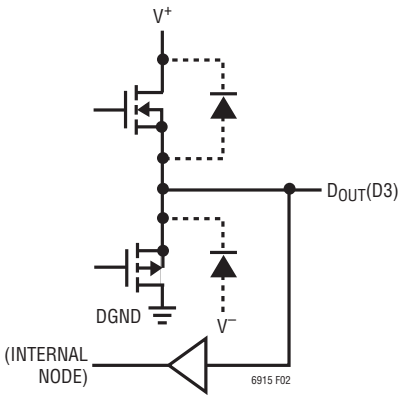


Figure 2. Bidirectional Nature of D_{OUT}/D3 Pin

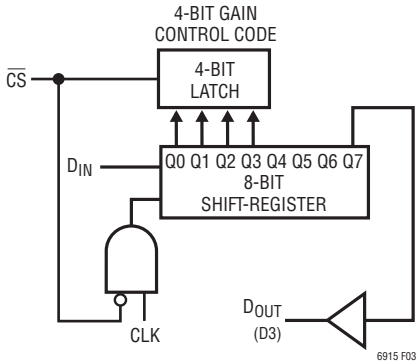


Figure 3. Diagram of Serial Interface (MSB First Out)

OPERATION

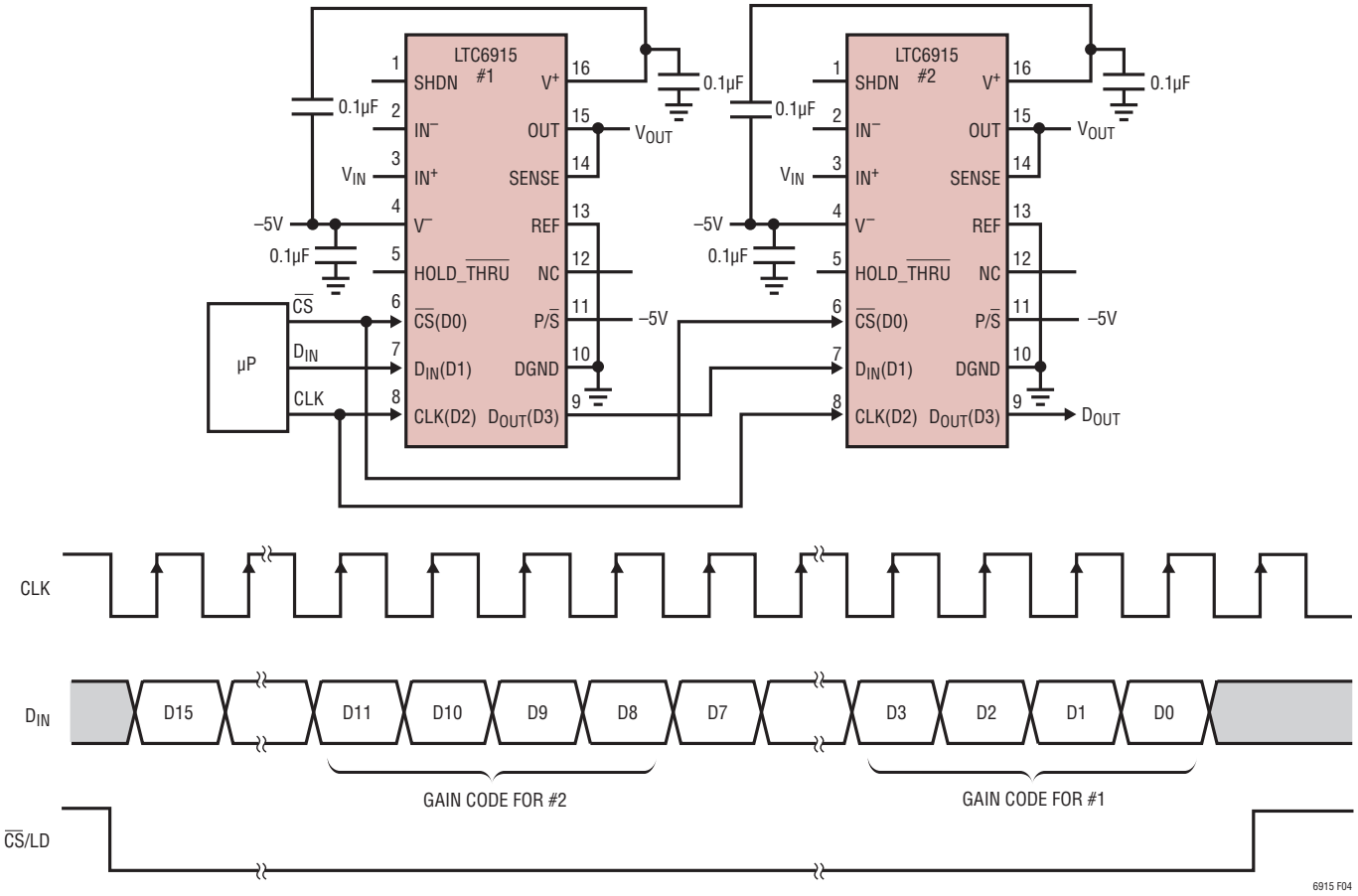


Figure 4. 2 PGAs in a Daisy Chain

The amplifier's gain is set as follows:

D3, D2, D1, D0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101~ 1111
Gain	0	1	2	4	8	16	32	64	128	256	512	1024	2048	4096

Input Voltage Range

The input common mode voltage range of the LTC6915 is rail-to-rail. However, the following equation limits the size of the differential input voltage:

$$V^- \le (V_{IN}^+ - V_{IN}^-) + V_{REF} \le V^+ - 1.3$$

Where V_{IN}^+ and V_{IN}^- are the voltage of the differential input pins, V^+ and V^- are the positive and negative supply voltages respectively and V_{REF} is the voltage of REF pin. In addition, V_{IN}^+ and V_{IN}^- must not exceed the power supply voltages, i.e.,

$$V^- < V_{IN}^+ < V^+ \text{ and } V^- < V_{IN}^- < V^+$$

±5 Volt Operation

When using the LTC6915 with supplies over 5.5V, care must be taken to limit the maximum difference between any of the input pins (IN^+ or IN^-) and the REF pin to 5.5V, i.e.,

$$|V_{IN}^+ - V_{REF}| < 5.5 \text{ and } |V_{IN}^- - V_{REF}| < 5.5$$

If not, the device will be damaged. For example, if rail-to-rail input operation is desired when the supplies are at ±5V, the REF pin should be 0, ±0.5V. As a second example, if the V^+ pin is 10V, and the V^- and REF pins are at 0, the inputs should not exceed 5.5V.

OPERATION

Settling Time

The sampling rate is 3kHz and the input sampling period during which C_S is charged to the input differential voltage, V_{IN}, is approximately 150µs. First assume that on each input sampling period, C_S is charged fully to V_{IN}. Since $C_S = C_H$ (= 1000pF), a change in the input will settle to N bits of accuracy at the op amp noninverting input after N clock cycles or 333µs(N). The settling time at the OUT pin is also affected by the internal op amp. Since the gain bandwidth of the internal op amp is typically 200kHz, the settling time is dominated by the switched-capacitor front end for gains below 100 (see the Low Gain Settling Time vs Settling Accuracy and the Settling Time vs Gain graphs in the Typical Performance Characteristics section). In addition, the worst case settling time after a device-enable (active low on Pin 1 of a GN package) is equal to the settling due to the gain plus the input settling time (333µs • N). For example, if an LTC6915 is enabled with a logic high on Pin 1 then, the maximum settling time to 10 bits of accuracy (0.1%) and a gain equal to 100 is 8.33ms ([333µs • 1024] + 5ms).

Input Current

Whenever the differential input V_{IN} changes, C_H must be charged up to the new input voltage via C_S. This results in an input charging current during each input sampling period. Eventually, C_H and C_S will reach V_{IN} and ideally, the input current would go to zero for DC inputs.

In reality, there are additional parasitic capacitors which disturb the charge on C_S every cycle even if V_{IN} is a DC voltage. For example, the parasitic bottom plate capacitor on C_S must be charged from the voltage on the REF pin to the voltage on the IN^- pin every cycle. The resulting input charging current decays exponentially during each input sampling period with a time constant equal to R_SC_S. If the voltage disturbance due to these currents settles before the end of the sampling period, there will be no errors due to source resistance or the source resistance mismatch between IN^+ and IN^-. With R_S less than 10k, no DC errors occur due to input current mismatch.

In the Typical Performance Characteristics section of this data sheet, there are curves showing the additional error from non-zero source resistance in the inputs. If there are no large capacitors across the inputs, the amplifier is less sensitive to source resistance and source resistance mismatch. When large capacitors are placed across the inputs, the input charging currents are placed across the inputs. The input charging currents described above result in larger DC errors, especially with source resistor mismatches.

Power Supply Bypassing

In a dual supply operation, connect a 0.1µF bypass capacitor from each power supply pin (V^+ and V^-) to an analog round plance surrounding an LTC6915. The bypass capacitor trace to the supply pins must be less than 0.2 inches (an X7R or X5R capacitor type is recommended). In single supply operation, connect the V^- pin to the analog ground plane and bypass the V^+ pin.

Shutdown Modes

The IC has two shutdown modes, hardware shutdown and software shutdown. When SHDN is tied to V^+, the IC is in hardware shutdown mode. During this shutdown mode, the gain setting digital interface (serial or parallel) and the main op amp are both disabled, thus the PGA dissipates very small supply current (see the Electrical Characteristic table). When SHDN is floating, an internal current source will pull it down to V^-. The digital interface is turned on to read the gain setting codes. The IC is in normal amplification mode as long as the gain control code is other than 0000. If the gain control code is 0000, the IC operates in software shutdown mode, i.e., the main op amp is turned off so that the PGA dissipates less power. The DFN package does not have hardware shutdown.

Setting the Voltage at the REF Pin

The current coming out of the REF pin may affect the reference voltage at the REF pin (V_{REF}). If V_{REF} is set by a resistive divider then the V_{REF} voltage is a function of the V_{OUT} voltage (see Figure 5). In order to minimize the V_{REF} variations, the total resistance of R1 plus R2 should be much less than 32k (5k or less) or use a voltage reference to set V_{REF}.

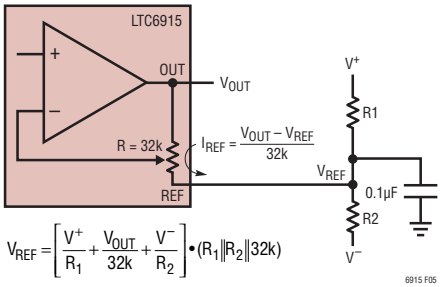


Figure 5

TYPICAL APPLICATION

Multiplexing Two LTC6915's

Send a gain code of 0000 to one IC to set its output to a high impedance state and send a gain code other than 0000 to the second IC to set it for normal amplification. If both devices are ON, the 200Ω resistors protect the outputs. The sense pin connection maintains gain accuracy for loads 1k or greater.

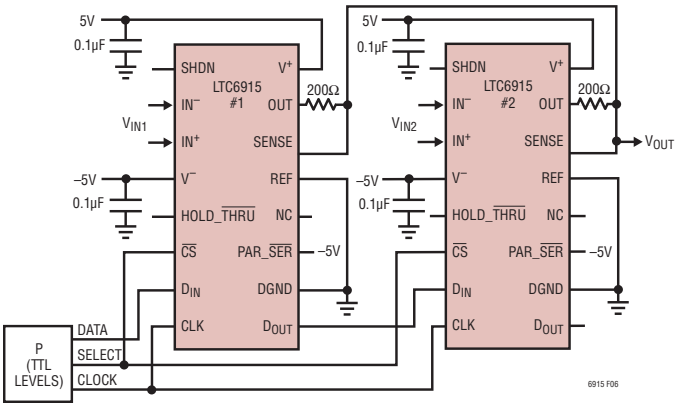
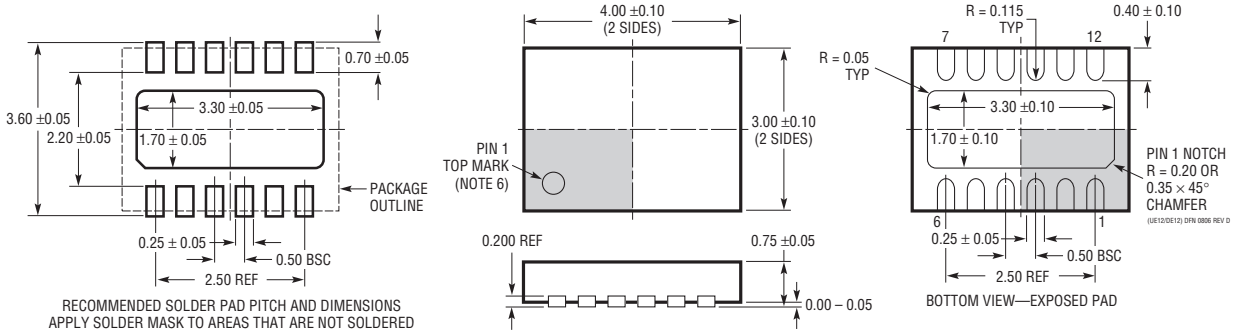


Figure 6. A 2:1 Multiplexing Two LTC6915's with Daisy Chained Gain Control

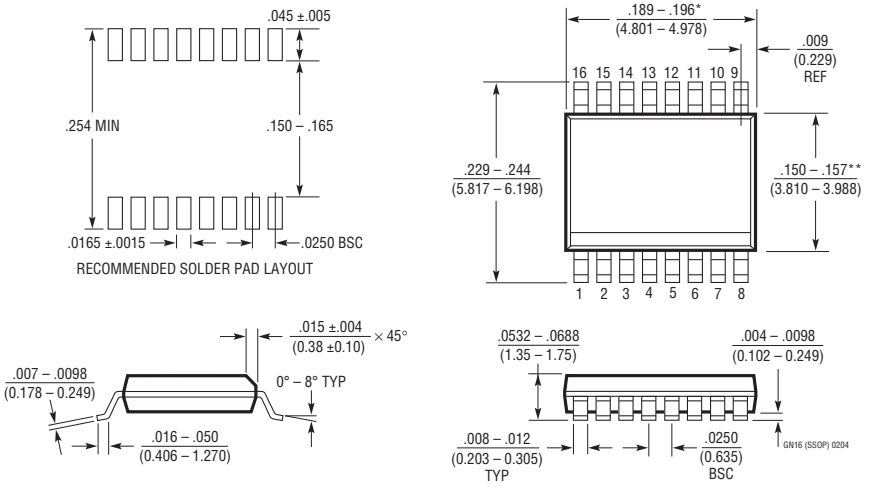
PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	6/11	Revised units for PSRR in Electrical Characteristics	5